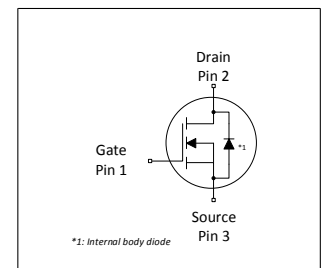


# MOSFET

## 600V CoolMOS™ CFD7 Power Device

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge ( $Q_g$ ), best-in-class reverse recovery charge ( $Q_{rr}$ ) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.



### Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge ( $Q_{rr}$ )
- Improved MOSFET reverse diode  $dv/dt$  and  $di_f/dt$  ruggedness
- Lowest FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- Best-in-class  $R_{DS(on)}$  in SMD and THD packages

### Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

### Potential applications

Suitable for Soft Switching topologies  
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

### Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	360	m $\Omega$
$Q_{g,typ}$	14	nC
$I_{D,pulse}$	24	A
$E_{oss} @ 400V$	1.6	$\mu$ J
Body diode $di_f/dt$	1300	A/ $\mu$ s

Type / Ordering Code	Package	Marking	Related Links
IPA60R360CFD7	PG-TO 220 FullPAK	60R360F7	see Appendix A

## Table of Contents

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	5 3	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	24	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	29	mJ	$I_D=2.0\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.14	mJ	$I_D=2.0\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	2.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	23	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 and M3 screws
Continuous diode forward current	$I_S$	-	-	5	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	24	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 5\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>F</sub> /dt	-	-	1300	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 5\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	5.54	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$ , $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}$ , $I_D=0.14\text{mA}$
Zero gate voltage drain current <sup>1)</sup>	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=600\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $V_{DS}=600\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=125^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.295 0.674	0.36	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=2.9\text{A}$ , $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$ , $I_D=2.9\text{A}$ , $T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	11.6	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	679	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	11	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Effective output capacitance, energy related <sup>2)</sup>	$C_{o(er)}$	-	20	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related <sup>3)</sup>	$C_{o(tr)}$	-	198	-	pF	$I_D=\text{constant}$ , $V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	15.5	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=4.0\text{A}$ , $R_G=10.2\Omega$ ; see table 9
Rise time	$t_r$	-	12	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=4.0\text{A}$ , $R_G=10.2\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	41.5	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=4.0\text{A}$ , $R_G=10.2\Omega$ ; see table 9
Fall time	$t_f$	-	8.5	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=4.0\text{A}$ , $R_G=10.2\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	4	-	nC	$V_{DD}=400\text{V}$ , $I_D=4.0\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	4	-	nC	$V_{DD}=400\text{V}$ , $I_D=4.0\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	14	-	nC	$V_{DD}=400\text{V}$ , $I_D=4.0\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	5.8	-	V	$V_{DD}=400\text{V}$ , $I_D=4.0\text{A}$ , $V_{GS}=0$ to $10\text{V}$

<sup>1)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

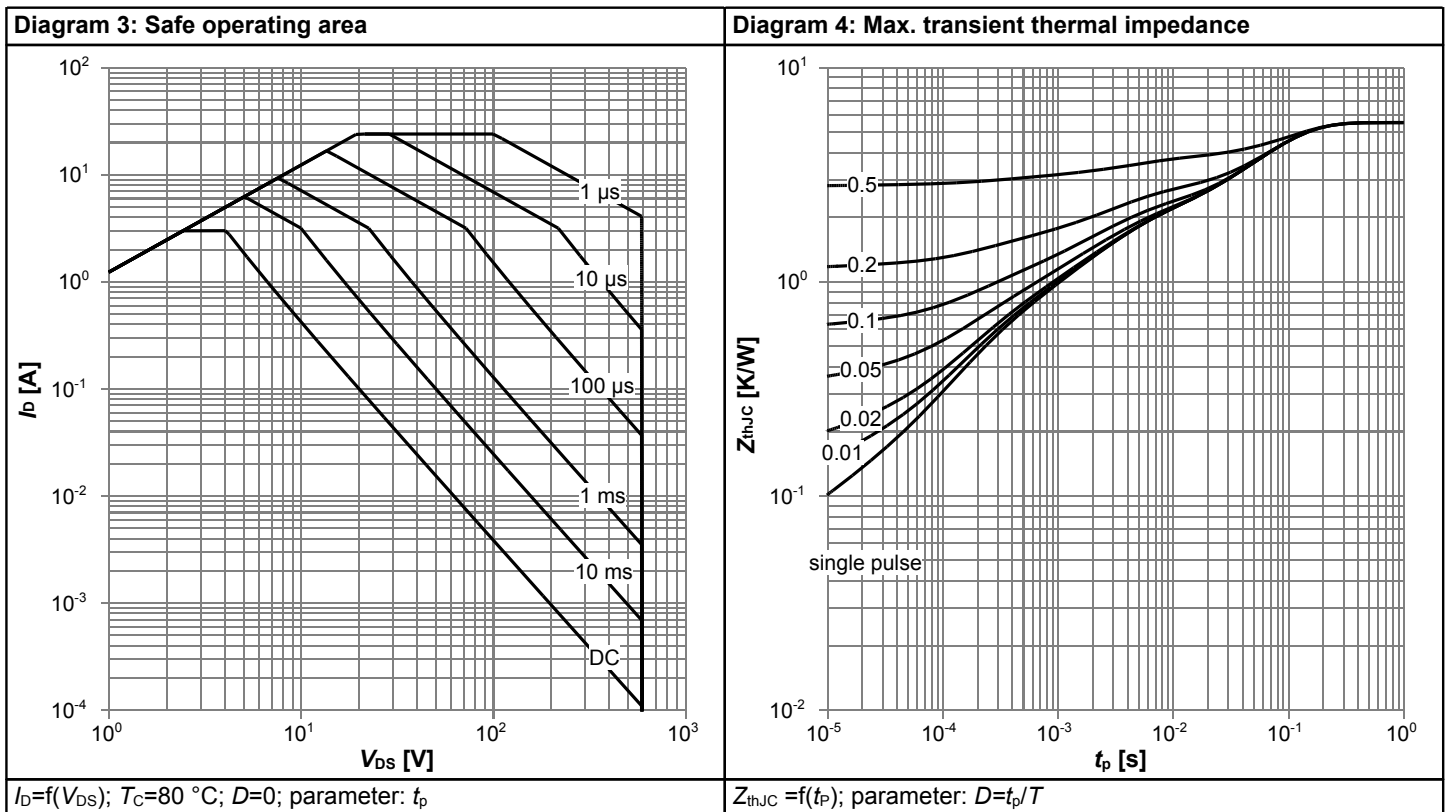
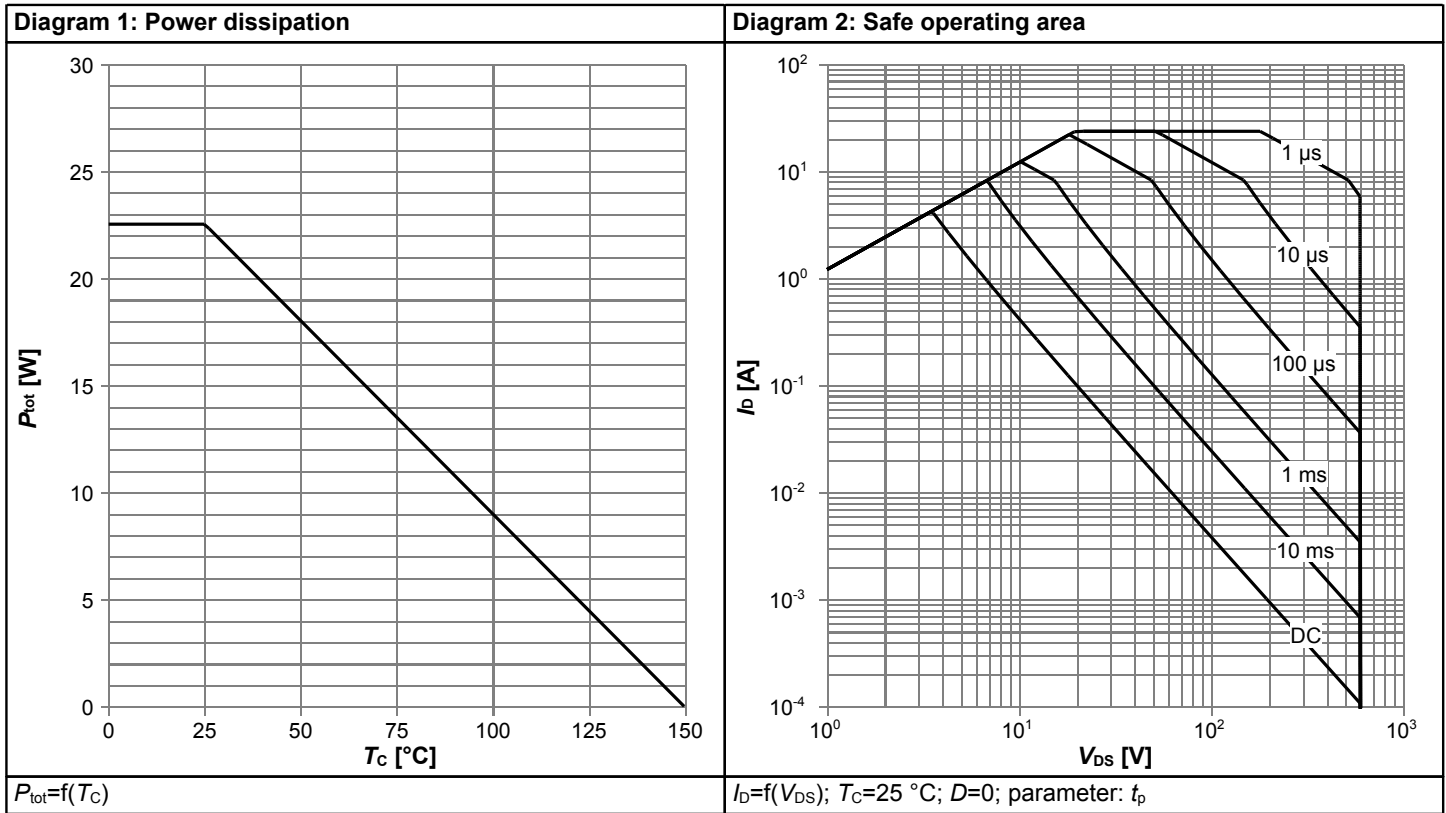
<sup>2)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>3)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

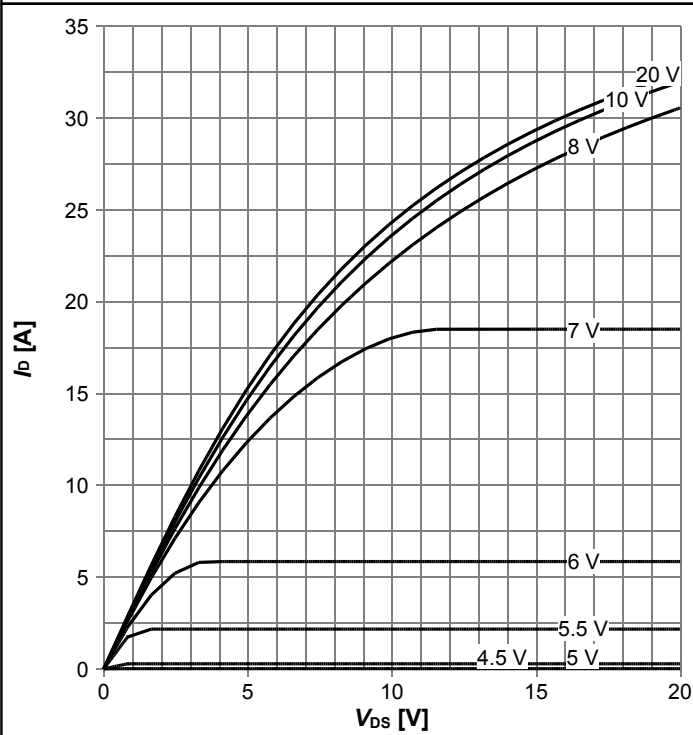
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.0	-	V	$V_{GS}=0V, I_F=2.9A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	81	122	ns	$V_R=400V, I_F=4.0A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	0.28	0.56	$\mu C$	$V_R=400V, I_F=4.0A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	6.4	-	A	$V_R=400V, I_F=4.0A, di_F/dt=100A/\mu s$ ; see table 8

## 4 Electrical characteristics diagrams

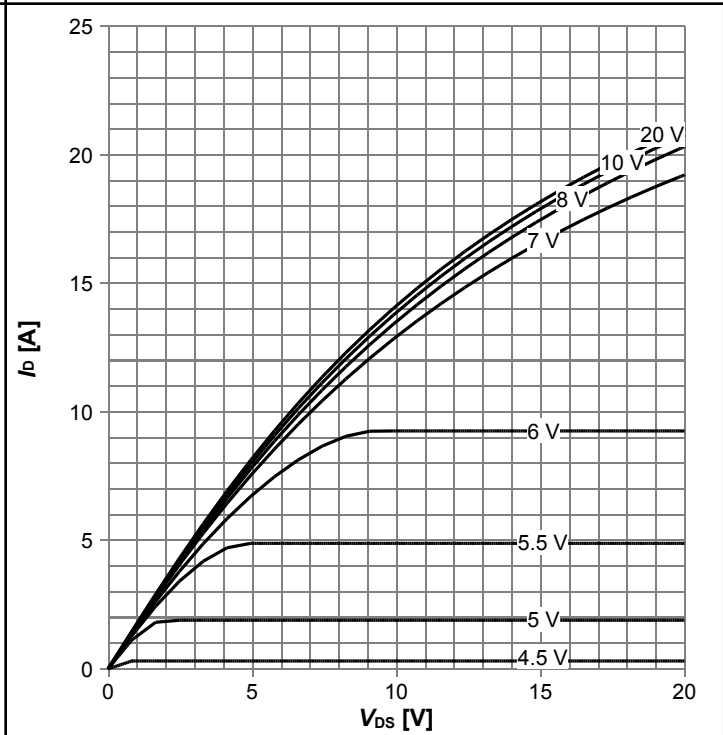


**Diagram 5: Typ. output characteristics**



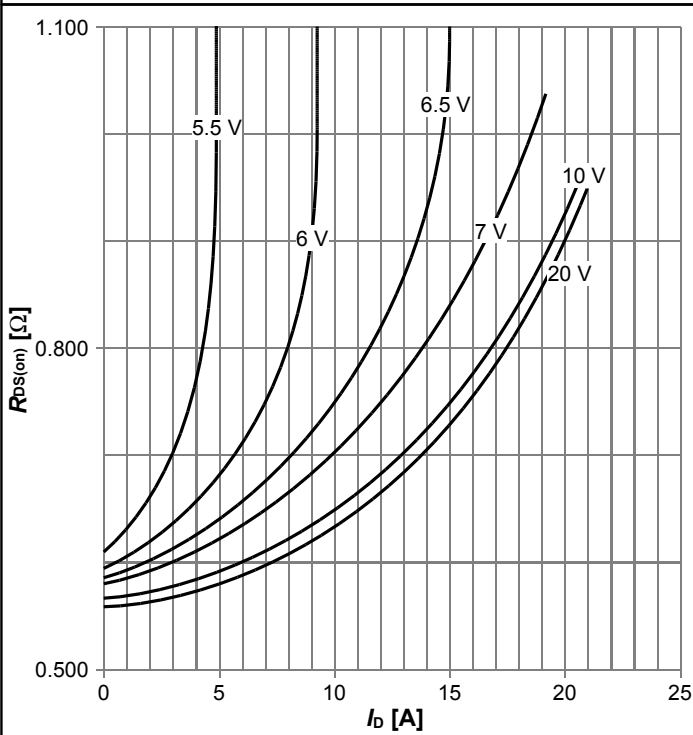
$I_D=f(V_{DS}); T_j=25\text{ °C}; \text{parameter: } V_{GS}$

**Diagram 6: Typ. output characteristics**



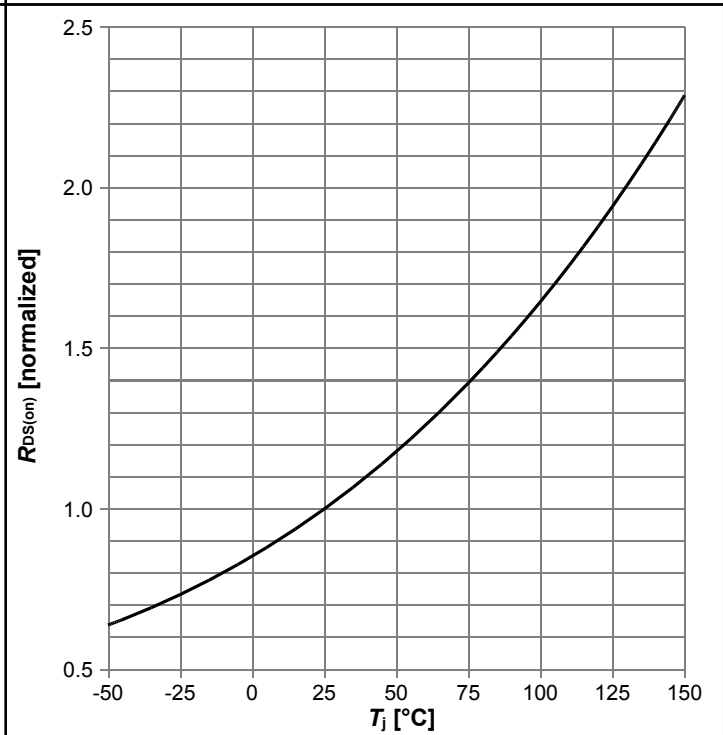
$I_D=f(V_{DS}); T_j=125\text{ °C}; \text{parameter: } V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)}=f(I_D); T_j=125\text{ °C}; \text{parameter: } V_{GS}$

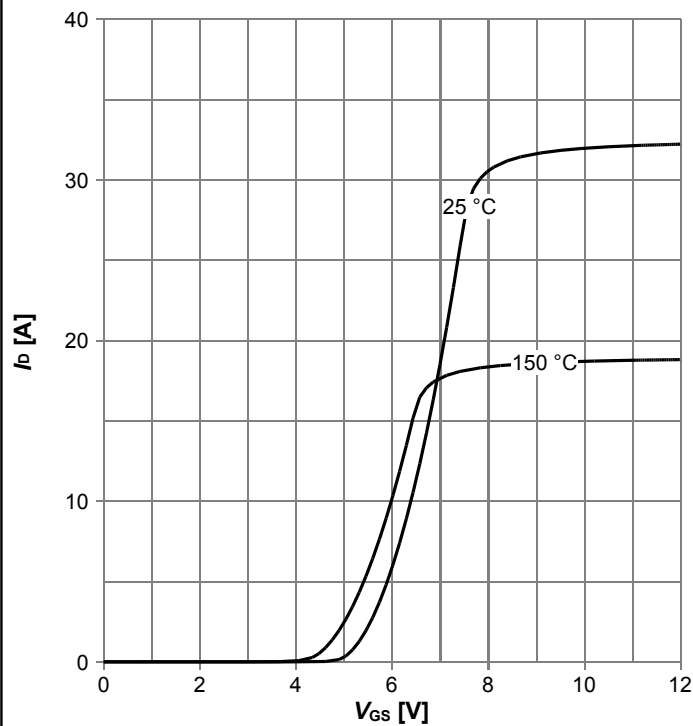
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)}=f(T_j); I_D=2.9\text{ A}; V_{GS}=10\text{ V}$

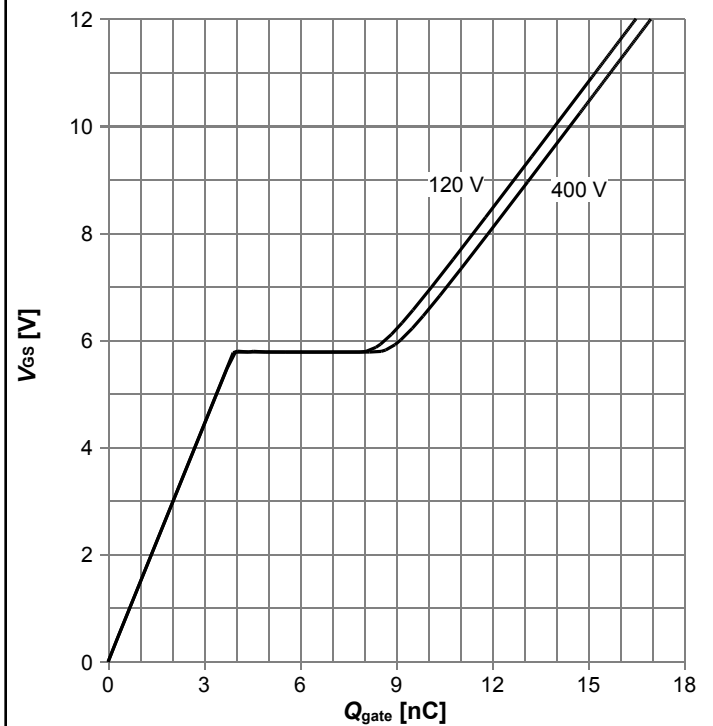


**Diagram 9: Typ. transfer characteristics**



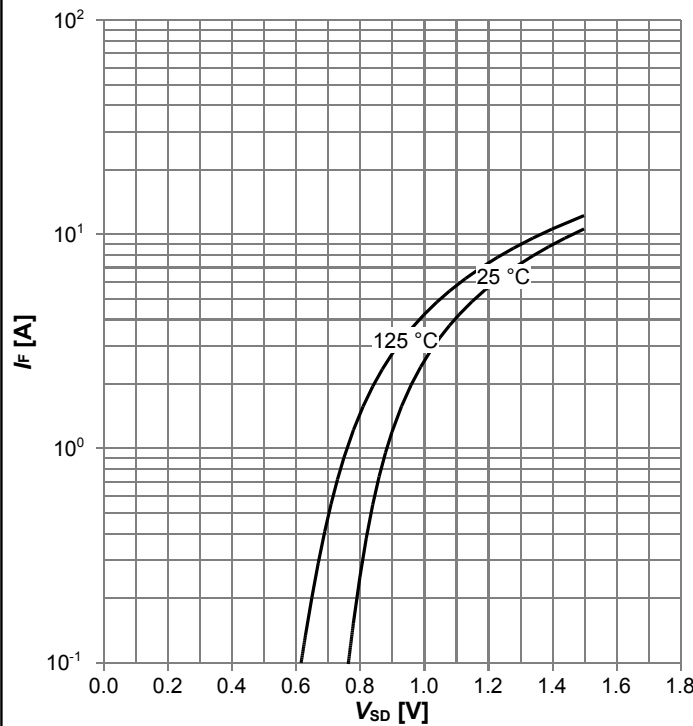
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

**Diagram 10: Typ. gate charge**



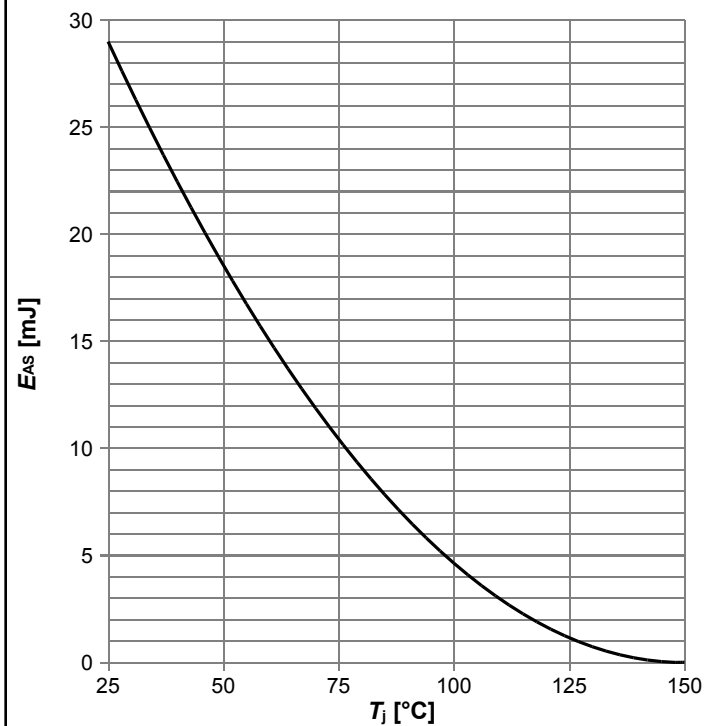
$V_{GS} = f(Q_{gate}); I_D = 4.0 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



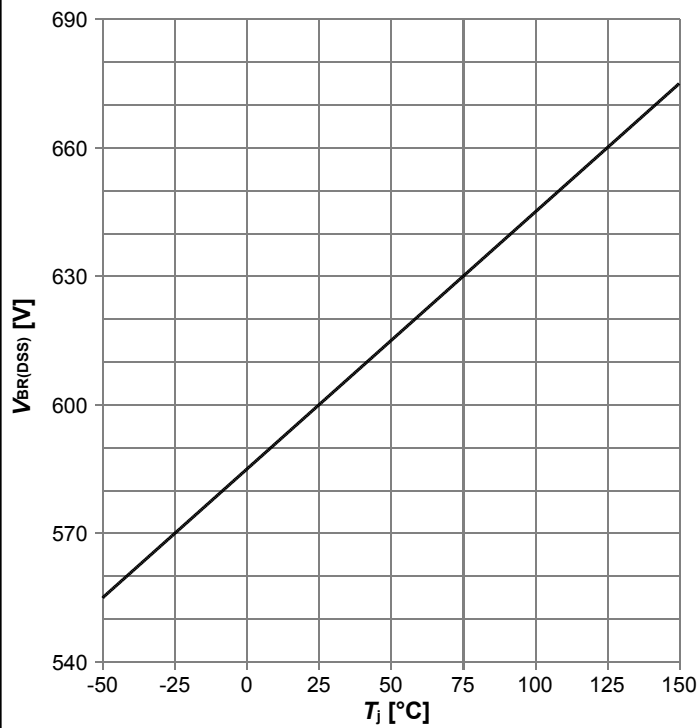
$I_F = f(V_{SD}); \text{parameter: } T_j$

**Diagram 12: Avalanche energy**



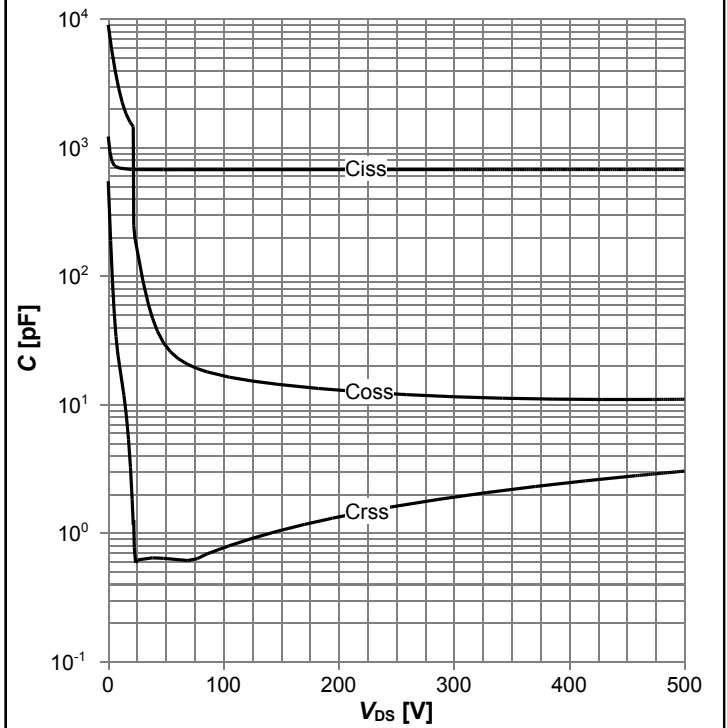
$E_{AS} = f(T_j); I_D = 2.0 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



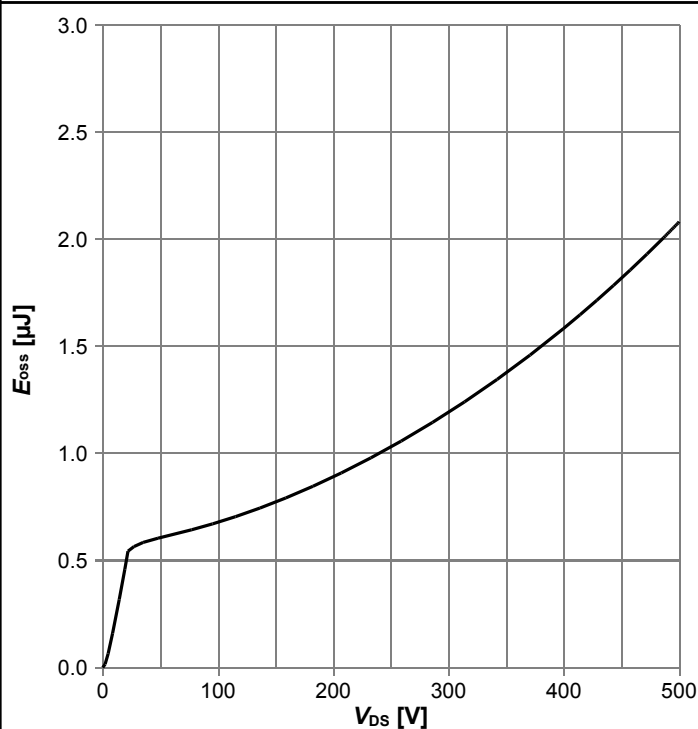
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



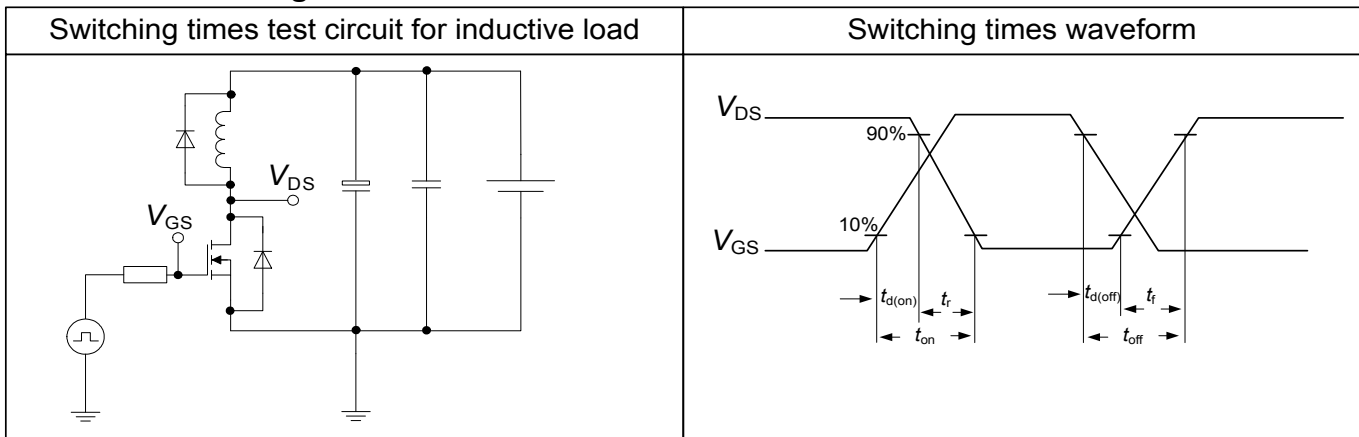
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

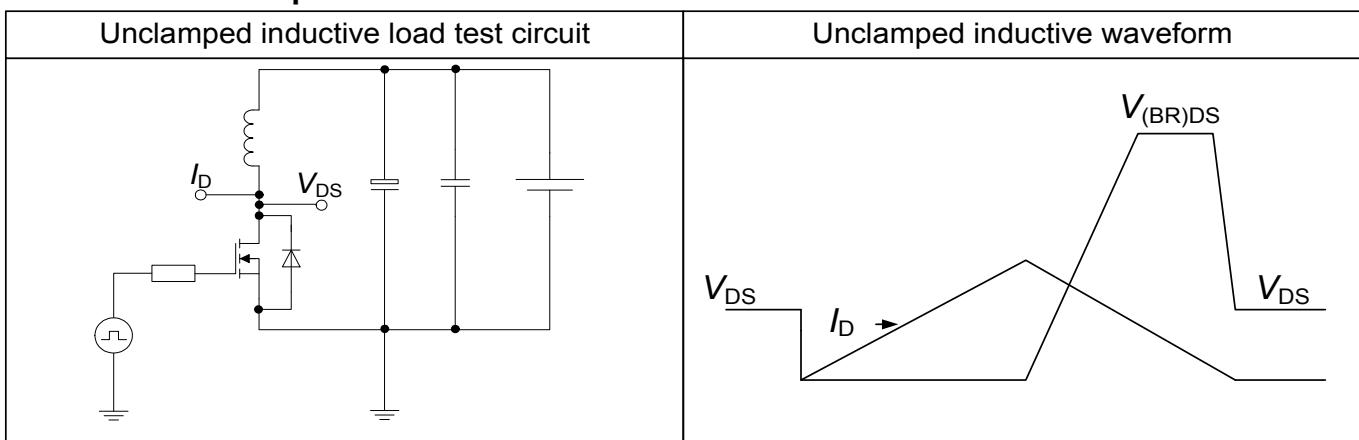
**Table 8 Diode characteristics**



**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



**Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm**

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS CFD7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS CFD7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS CFD7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA60R360CFD7

**Revision: 2020-01-31, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-06-06	Release of final version
2.1	2020-01-31	Updated package drawing and symbol ID

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