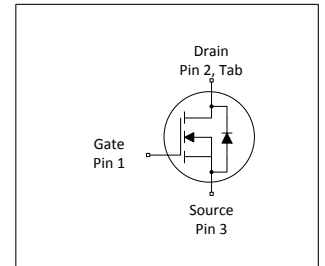
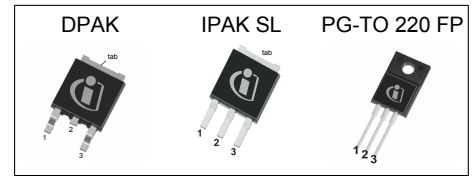


MOSFET

600V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



Features

- Extremely low losses due to very low FOM $R_{dson} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: Note1: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

*Note2: *6R400CE is Full PAK marking only*



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	400	mΩ
I_d	14.7	A
$Q_{g,typ}$	32	nC
$I_{D,pulse}$	30	A
$E_{oss}@400V$	2.8	μJ

Type / Ordering Code	Package	Marking	Related Links
IPD60R400CE	PG-TO 252	60S400CE / 6R400CE*	see Appendix A
IPS60R400CE	PG-TO 251		
IPA60R400CE	PG-TO 220 FullPAK		

Table of Contents

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	14.7 9.3	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	30	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	210	mJ	$I_D=1.8\text{A}$; $V_{DD}=50\text{V}$; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.32	mJ	$I_D=1.8\text{A}$; $V_{DD}=50\text{V}$; see table 11
Avalanche current, repetitive	I_{AR}	-	-	1.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (Non FullPAK) TO-252, TO-251	P_{tot}	-	-	112	W	$T_C=25^\circ\text{C}$
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	31	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	10.4	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	30	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9
Maximum diode commutation speed	di/dt	-	-	500	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

2 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	$^\circ\text{C/W}$	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	1.6mm (0.063 in.) from case for 10s

¹⁾ Limited by $T_{j,max}$. TO252 equivalent, Maximum duty cycle $D=0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

600V CoolMOS™ CE Power Transistor
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Table 4 Thermal characteristics TO-252, TO-251

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.12	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL3

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=0.25mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}, I_D=0.3mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=600, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.34 0.89	0.40	Ω	$V_{GS}=10V, I_D=3.8A, T_j=25^\circ C$ $V_{GS}=10V, I_D=3.8A, T_j=150^\circ C$
Gate resistance	R_G	-	7.5	-	Ω	$f=1MHz, \text{open drain}$

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	700	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	C_{oss}	-	46	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	30	-	pF	$V_{GS}=0V, V_{DS}=0...480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	136	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...480V$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega; \text{see table 10}$
Rise time	t_r	-	9	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega; \text{see table 10}$
Turn-off delay time	$t_{d(off)}$	-	56	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega; \text{see table 10}$
Fall time	t_f	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega; \text{see table 10}$

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	4	-	nC	$V_{DD}=480V, I_D=4.8A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	16	-	nC	$V_{DD}=480V, I_D=4.8A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	32	-	nC	$V_{DD}=480V, I_D=4.8A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480V, I_D=4.8A, V_{GS}=0 \text{ to } 10V$

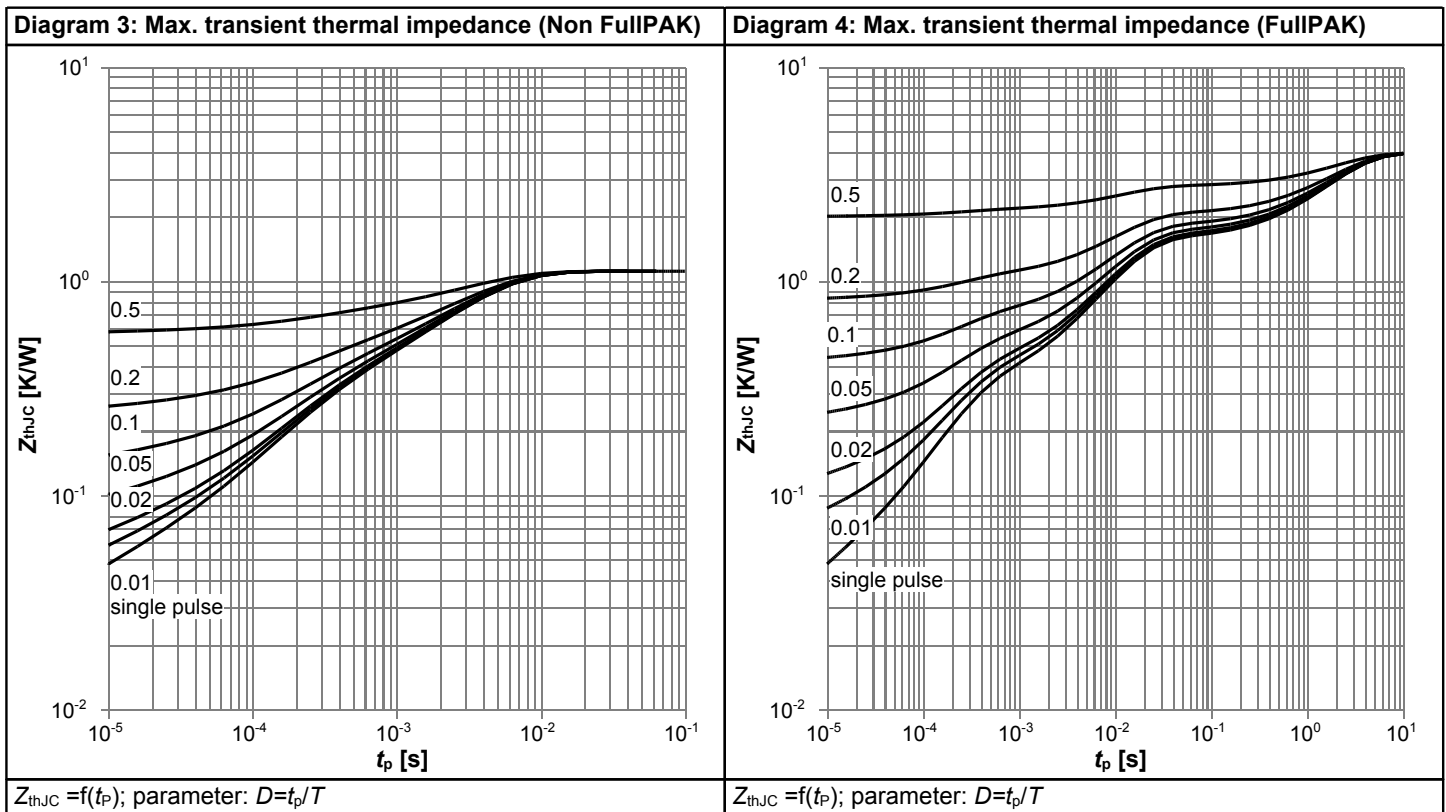
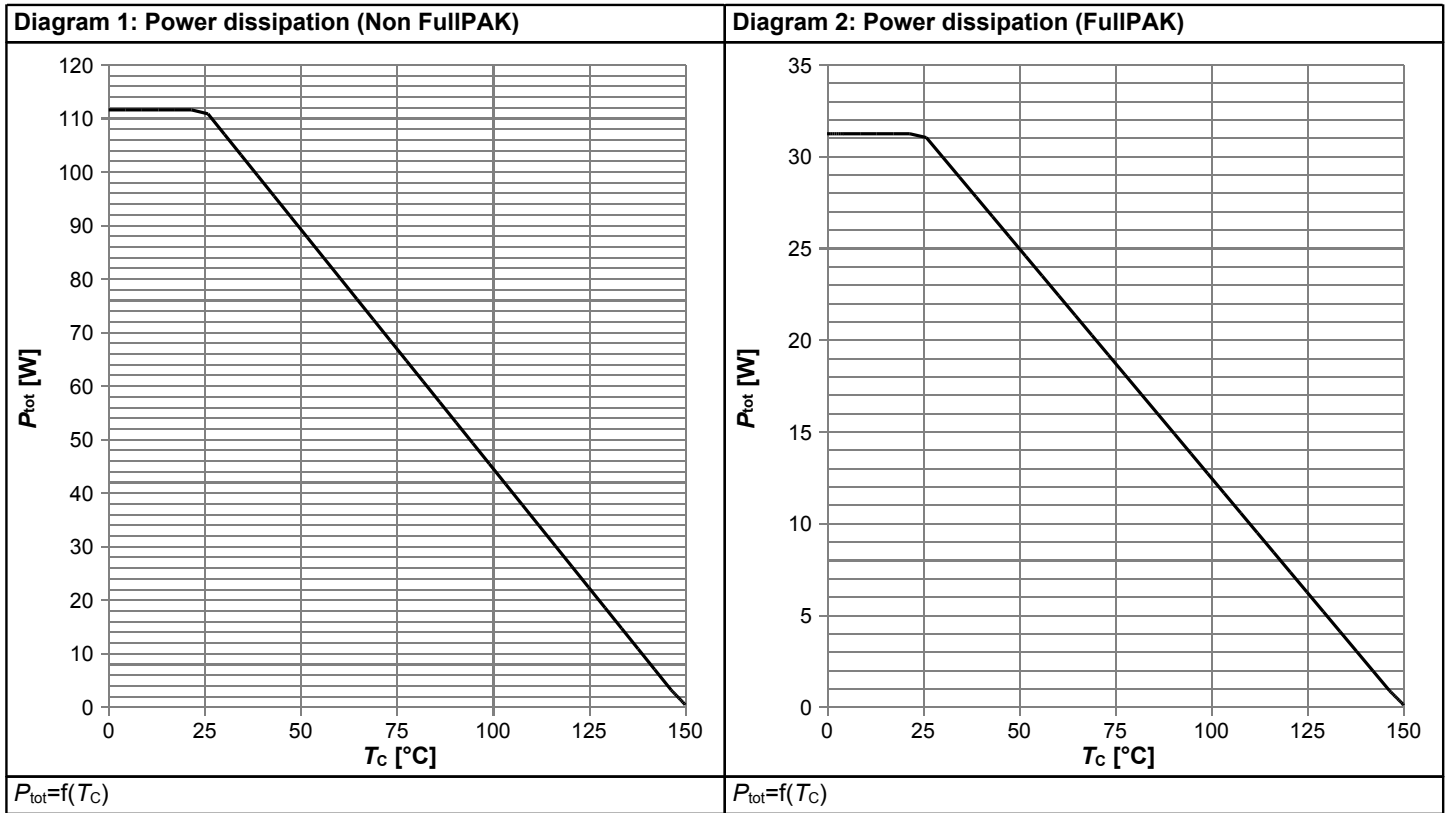
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Reverse diode characteristics

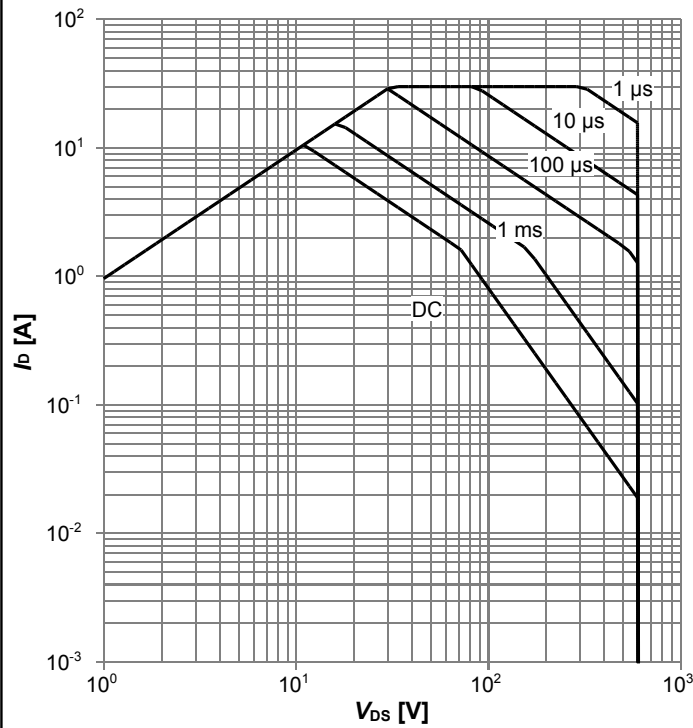
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=4.8A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	290	-	ns	$V_R=400V, I_F=4.8A, di_F/dt=100A/\mu s$; see table 9
Reverse recovery charge	Q_{rr}	-	3.3	-	μC	$V_R=400V, I_F=4.8A, di_F/dt=100A/\mu s$; see table 9
Peak reverse recovery current	I_{rrm}	-	21	-	A	$V_R=400V, I_F=4.8A, di_F/dt=100A/\mu s$; see table 9

4 Electrical characteristics diagrams



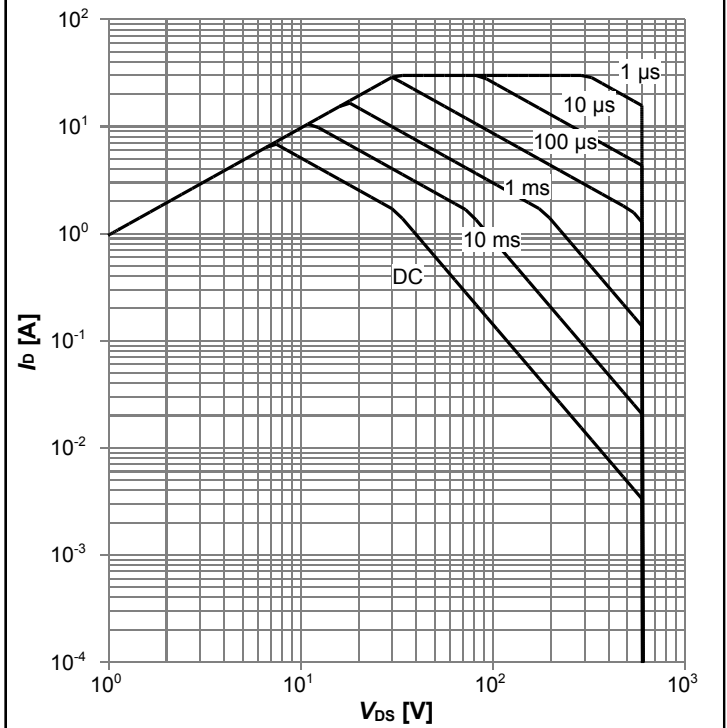
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Diagram 5: Safe operating area (Non FullPAK)



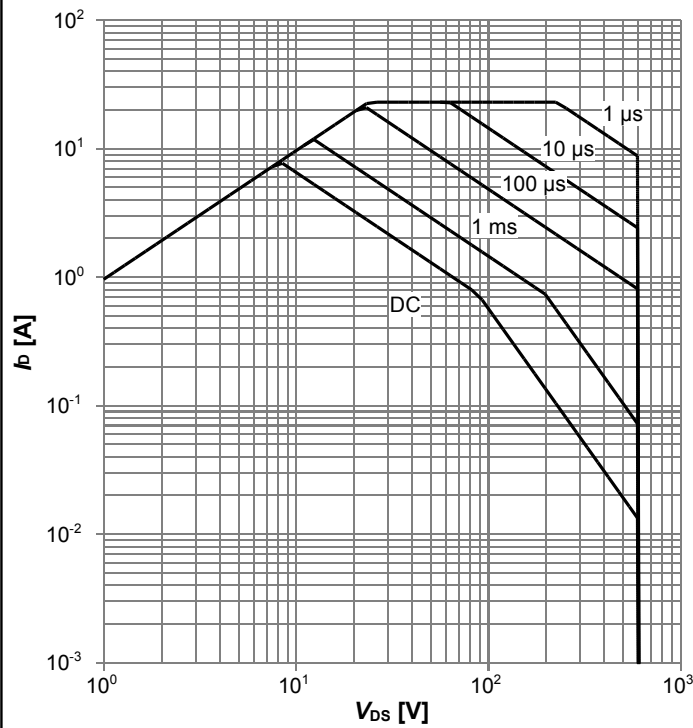
$I_b=f(V_{Ds}); T_C=25\text{ °C}; D=0; \text{parameter: } t_p$

Diagram 6: Safe operating area (FullPAK)



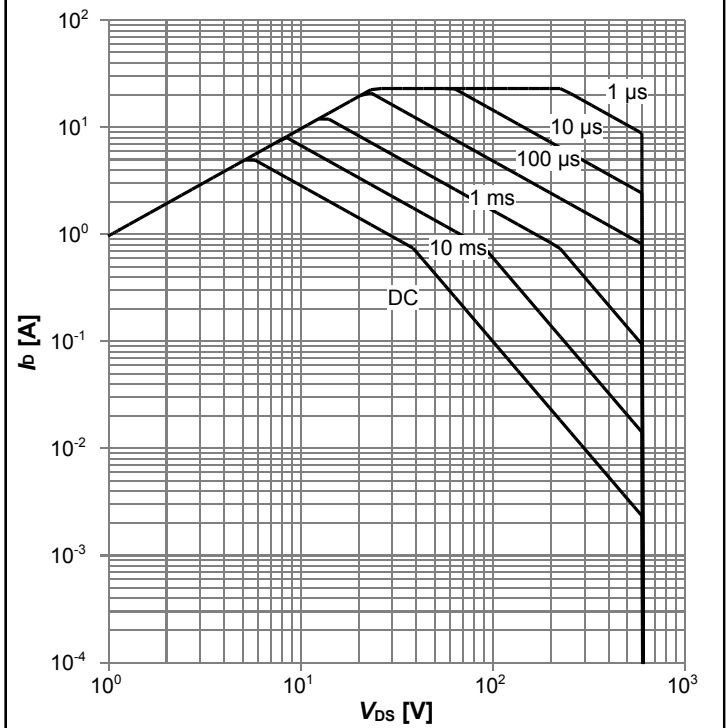
$I_b=f(V_{Ds}); T_C=25\text{ °C}; D=0; \text{parameter: } t_p$

Diagram 7: Safe operating area (Non FullPAK)



$I_b=f(V_{Ds}); T_C=80\text{ °C}; D=0; \text{parameter: } t_p$

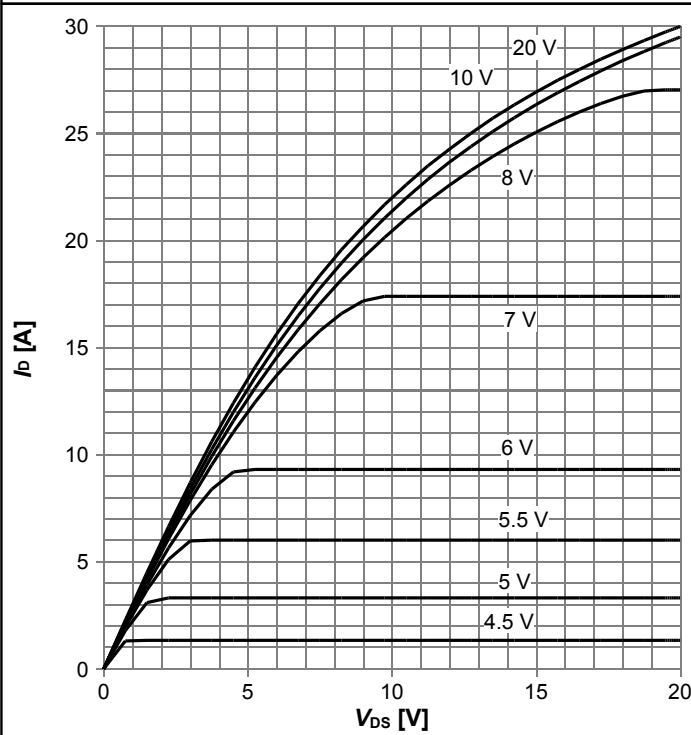
Diagram 8: Safe operating area (FullPAK)



$I_b=f(V_{Ds}); T_C=80\text{ °C}; D=0; \text{parameter: } t_p$

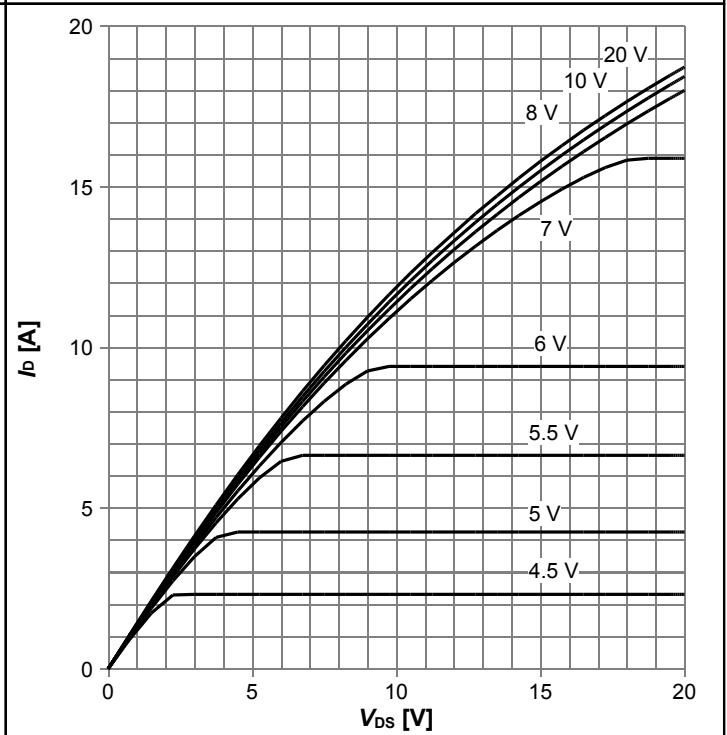
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Diagram 9: Typ. output characteristics



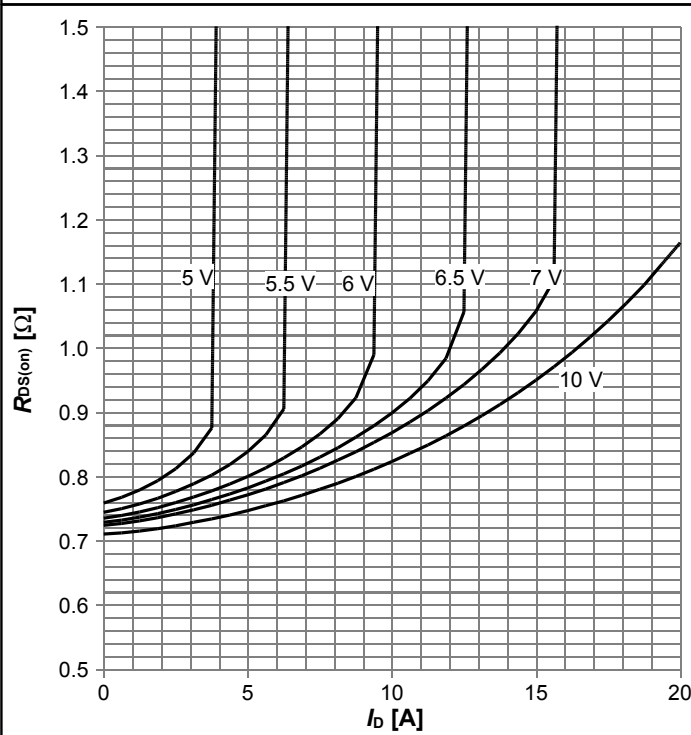
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 10: Typ. output characteristics



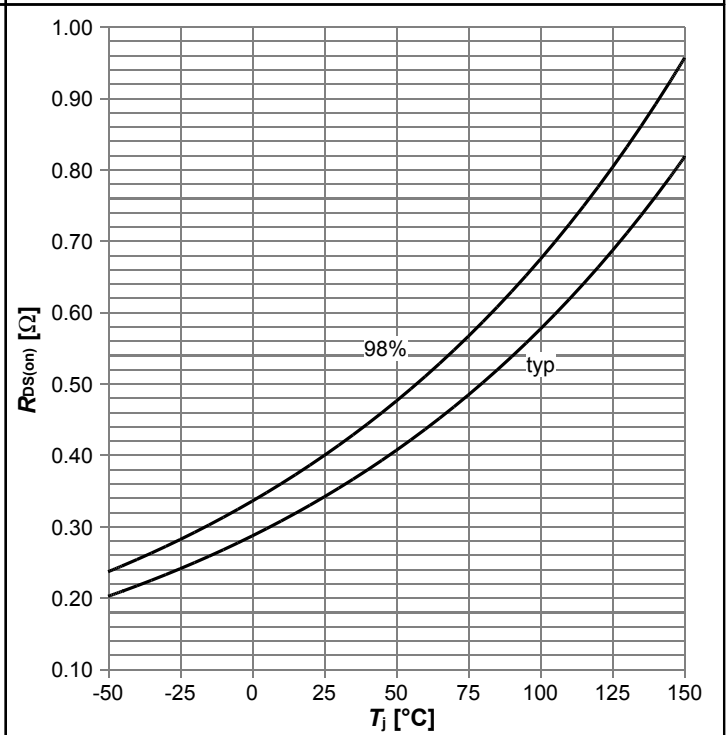
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

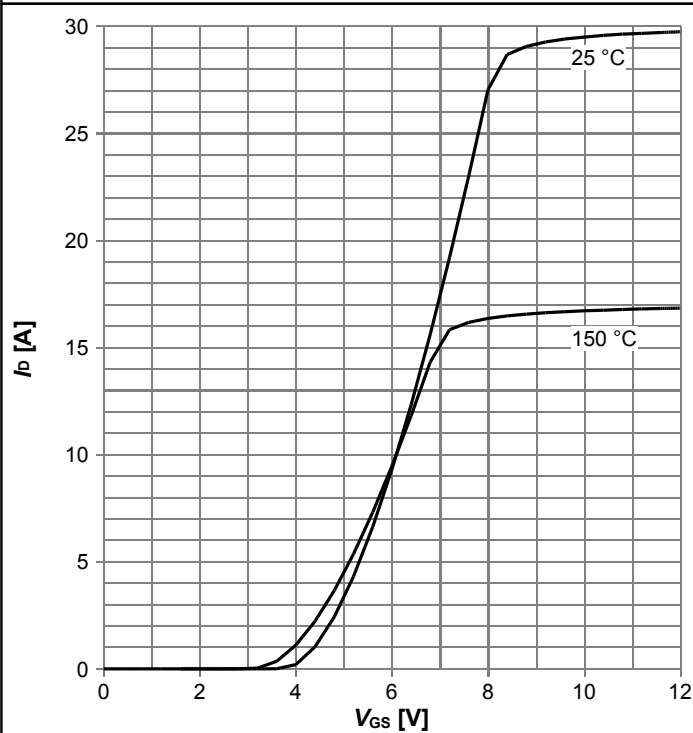
Diagram 12: Drain-source on-state resistance



$R_{DS(on)} = f(T_j)$; $I_D = 3.8\text{ A}$; $V_{GS} = 10\text{ V}$

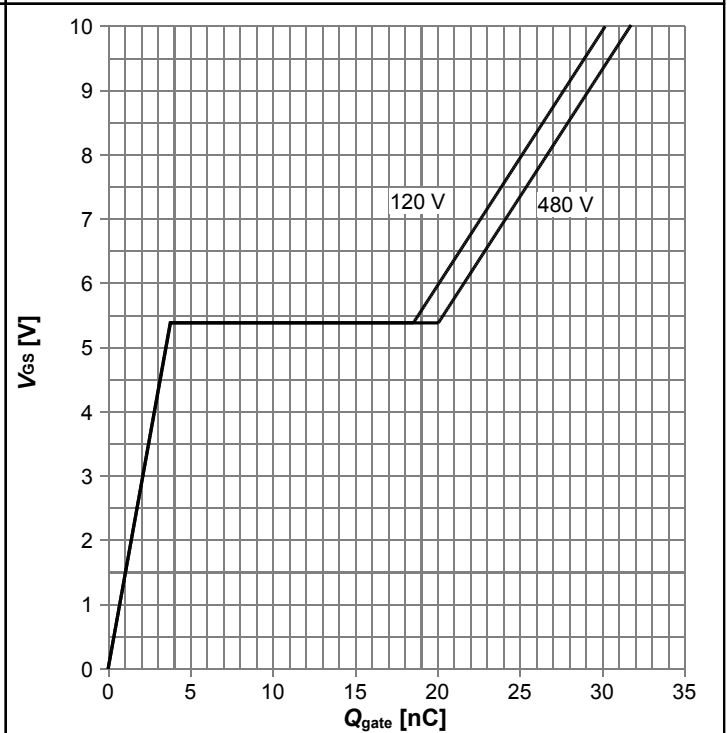
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Diagram 13: Typ. transfer characteristics



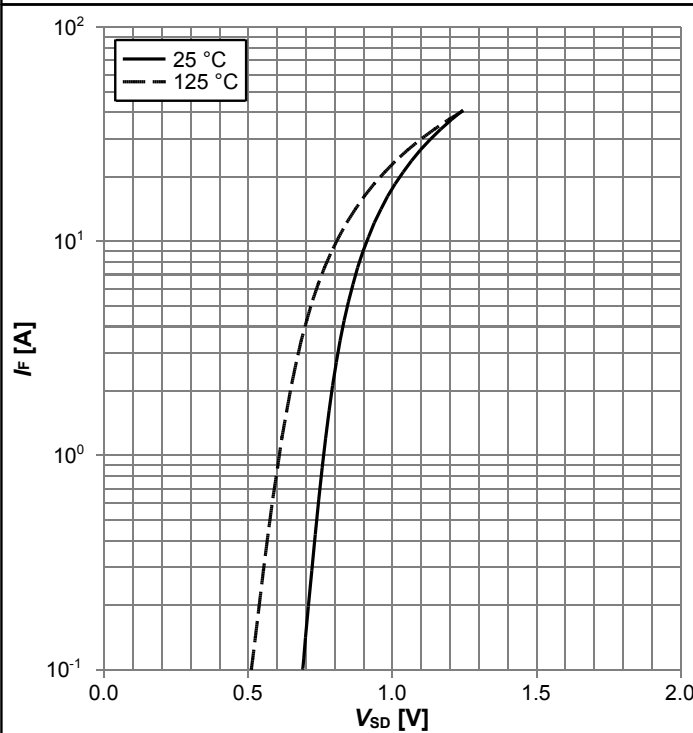
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 14: Typ. gate charge



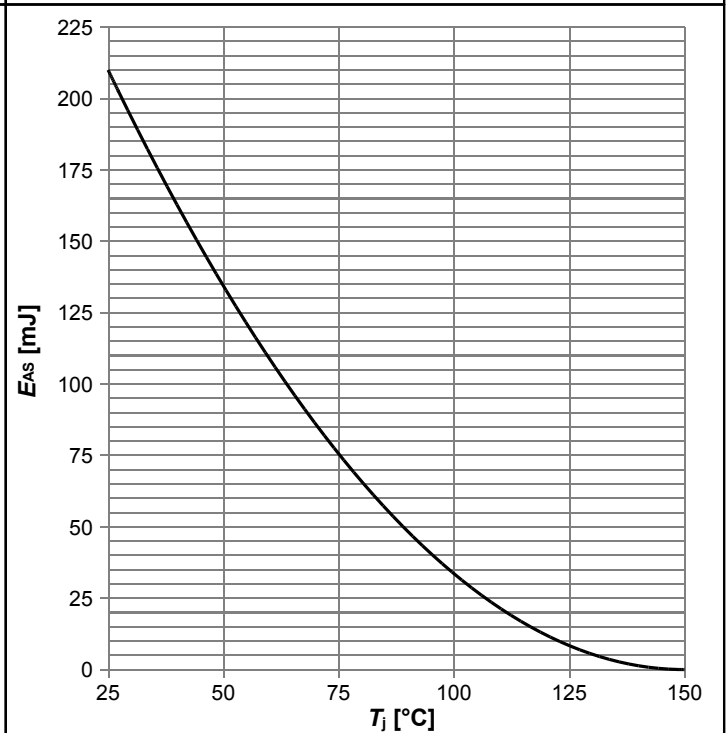
$V_{GS}=f(Q_{gate}); I_D=4.8 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 15: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

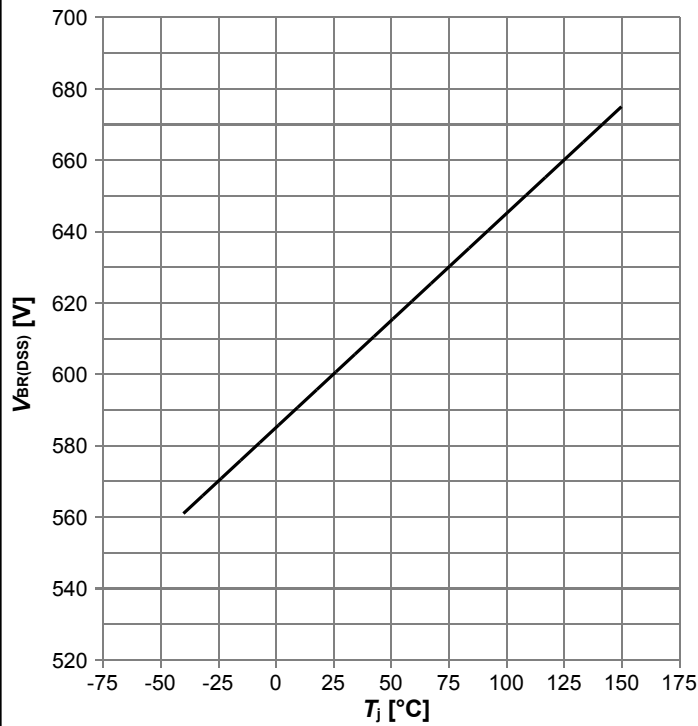
Diagram 16: Avalanche energy



$E_{AS}=f(T_j); I_D=1.8 \text{ A}; V_{DD}=50 \text{ V}$

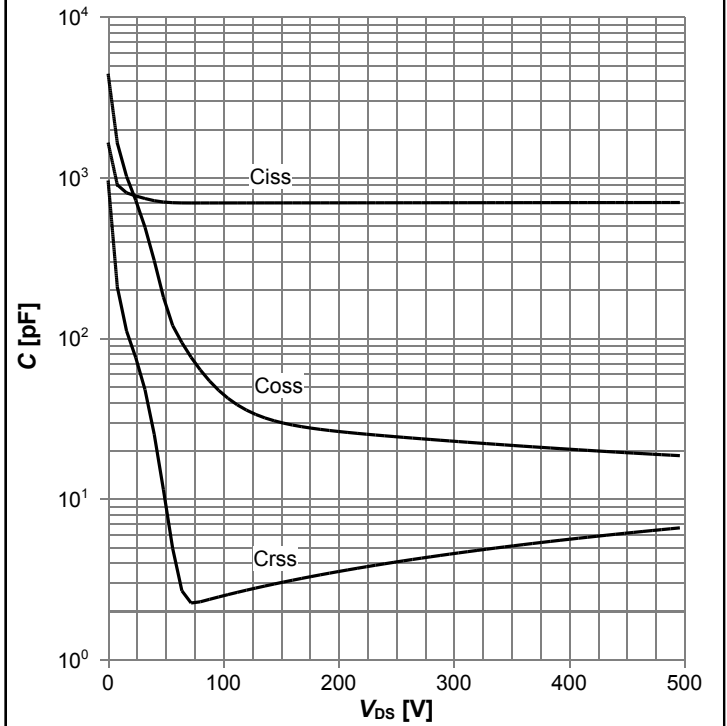
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Diagram 17: Drain-source breakdown voltage



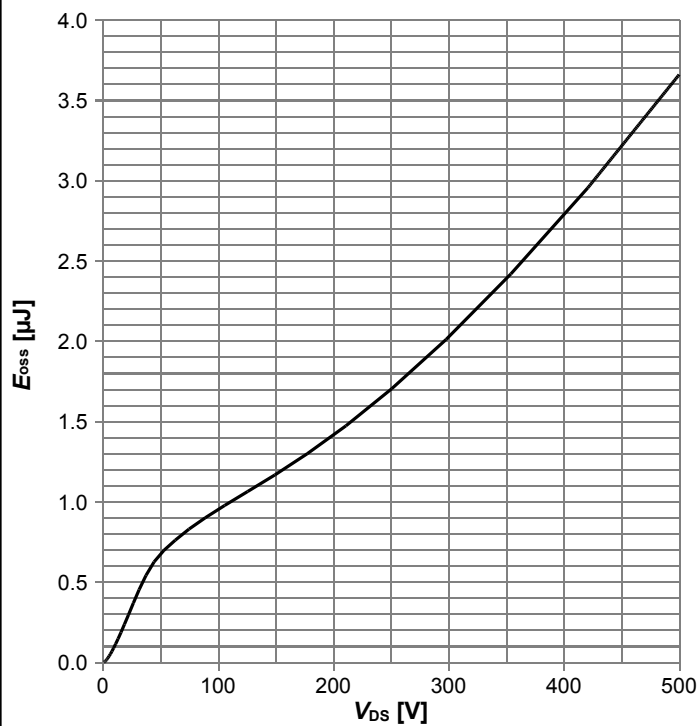
$V_{BR(DSS)}=f(T_j); I_D=0.25 \text{ mA}$

Diagram 18: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 19: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 9 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform

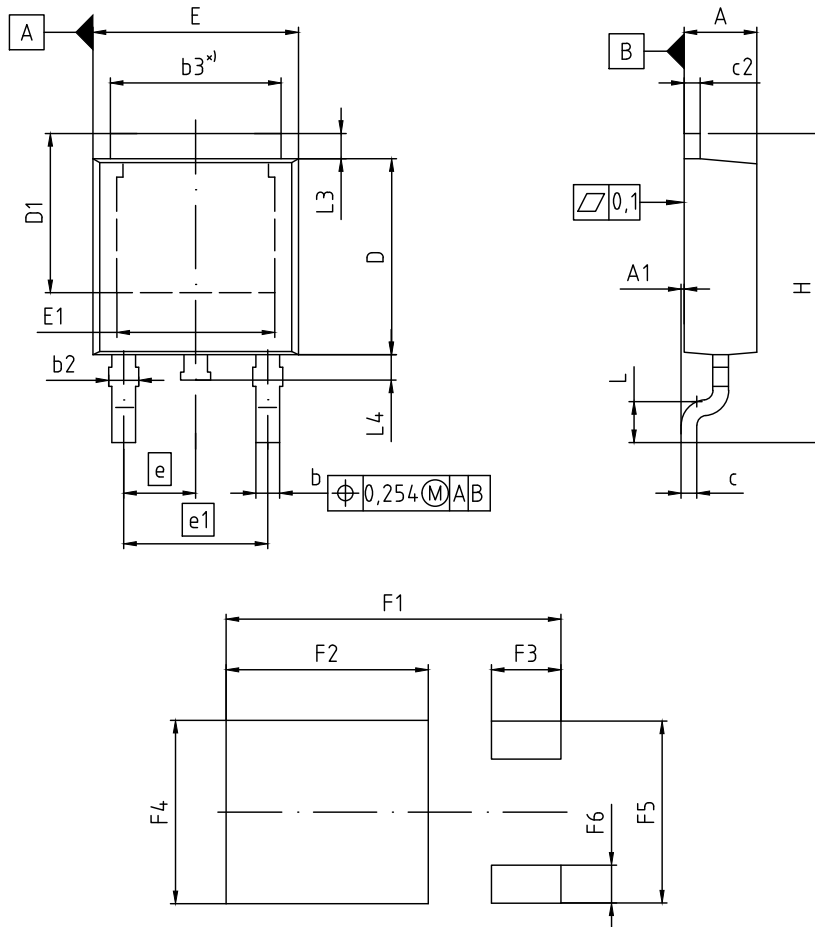
Table 10 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package Outlines



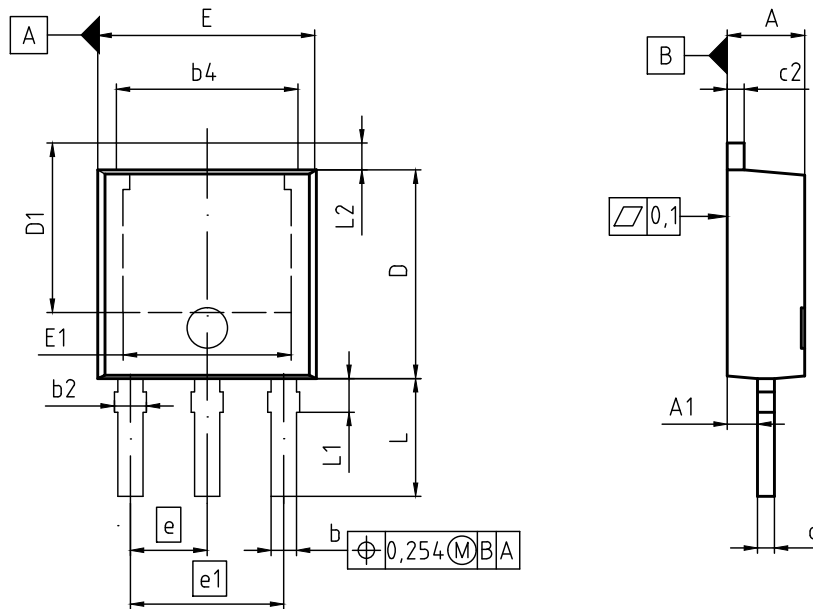
*) mold flash not included

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.60	0.185	0.220
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

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SCALE 0 2.0 4mm
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ISSUE DATE 01-09-2015
REVISION 05

Figure 1 Outline PG-TO 252, dimensions in mm/inches

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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.40	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.59	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.55	0.198	0.219
E	6.35	6.73	0.250	0.265
E1	4.60	5.21	0.181	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.00	3.60	0.118	0.142
L1	0.80	1.25	0.031	0.049
L2	0.88	1.28	0.035	0.050

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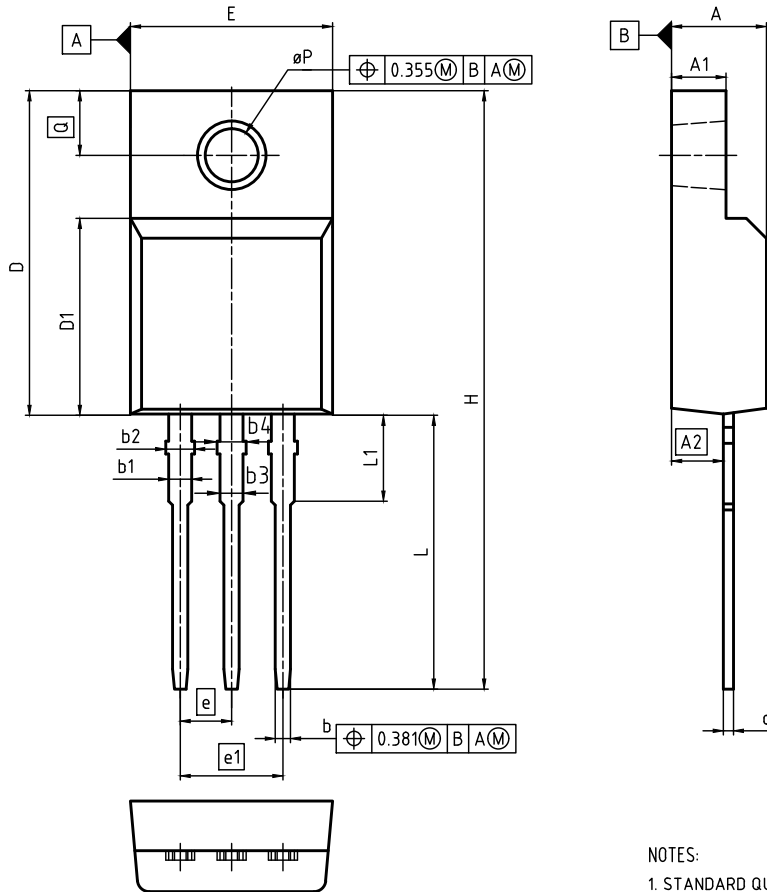
ISSUE DATE
21-10-2015

REVISION
06

Figure 2 Outline PG-TO 251, dimensions in mm/inches

600V CoolMOS™ CE Power Transistor

IPD60R400CE, IPS60R400CE, IPA60R400CE



NOTES:

1. STANDARD QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281 NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.80	0.092	0.110
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	1.20	1.50	0.047	0.059
b3	0.65	1.38	0.026	0.054
b4	1.20	1.50	0.047	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	3.00	3.38	0.118	0.133
Q	3.15	3.50	0.124	0.138

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REVISION 01

Figure 3 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 12 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

600V CoolMOS™ CE Power Transistor

IPD60R400CE, IPS60R400CE, IPA60R400CE

Revision History

IPD60R400CE, IPS60R400CE, IPA60R400CE

Revision: 2016-08-08, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-09-25	Release of final version
2.1	2016-03-31	Modified Id, Rthjc. Modified SOA & Zthjc curves. Added IPAK_SL package
2.2	2016-08-08	Revised Full PAK package drawing on page 15, solder reflow info to MSL3 on page 4 and added Full PAK marking on page 1

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Trademarks updated August 2015

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