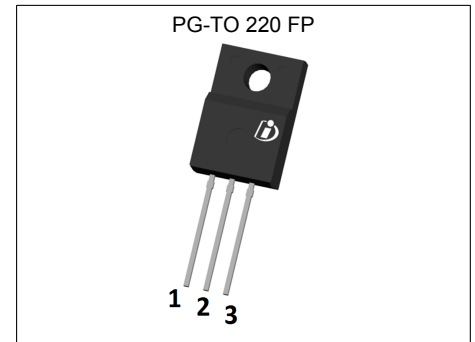


MOSFET

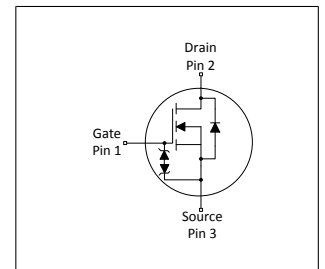
600V CoolMOS™ P7 Power Transistor

The CoolMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of body diode against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.



Features

- Suitable for hard and soft switching (PFC and LLC) due to an outstanding commutation ruggedness
- Significant reduction of switching and conduction losses
- Excellent ESD robustness >2kV (HBM) for all products
- Better $R_{DS(on)}/\text{package}$ products compared to competition enabled by a low $R_{DS(on)} \cdot A$ (below $10\text{Ohm} \cdot \text{mm}^2$)
- Product validation acc. JEDEC Standard



Benefits

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to low switching and conduction losses
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due to >2 kV ESD protection
- Suitable for a wide variety of applications and power ranges



Potential applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------|-------|------------------|
| $V_{DS} @ T_{j,max}$ | 650 | V |
| $R_{DS(on),max}$ | 180 | m Ω |
| $Q_{g,typ}$ | 25 | nC |
| $I_{D,pulse}$ | 53 | A |
| $E_{oss} @ 400V$ | 2.9 | μJ |
| Body diode di_f/dt | 900 | A/ μs |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|---------------------------------|----------|----------------|
| IPAN60R180P7S | PG-TO 220 FullPAK - Narrow Lead | 60S180P7 | see Appendix A |

Table of Contents

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------------|--------|------|----------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 18 11 | A | $T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 53 | A | $T_C=25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 56 | mJ | $I_D=4.0\text{A}$; $V_{DD}=50\text{V}$; see table 10 |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.28 | mJ | $I_D=4.0\text{A}$; $V_{DD}=50\text{V}$; see table 10 |
| Avalanche current, single pulse | I_{AS} | - | - | 4.0 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 80 | V/ns | $V_{DS}=0\dots400\text{V}$ |
| Gate source voltage (static) | V_{GS} | -20 | - | 20 | V | static; |
| Gate source voltage (dynamic) | V_{GS} | -30 | - | 30 | V | AC ($f>1\text{ Hz}$) |
| Power dissipation | P_{tot} | - | - | 26 | W | $T_C=25^\circ\text{C}$ |
| Storage temperature | T_{stg} | -40 | - | 150 | $^\circ\text{C}$ | - |
| Operating junction temperature | T_j | -40 | - | 150 | $^\circ\text{C}$ | - |
| Mounting torque | - | - | - | 50 | Ncm | M2.5 screws |
| Continuous diode forward current | I_S | - | - | 18 | A | $T_C=25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 53 | A | $T_C=25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 50 | V/ns | $V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 18\text{A}$, $T_j=25^\circ\text{C}$ see table 8 |
| Maximum diode commutation speed | di _F /dt | - | - | 900 | A/ μs | $V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 18\text{A}$, $T_j=25^\circ\text{C}$ see table 8 |
| Insulation withstand voltage | V_{ISO} | - | - | 2500 | V | V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$ |

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$; TO-220 equivalent

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 4.85 | °C/W | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 62 | °C/W | leaded |
| Thermal resistance, junction - ambient for SMD version | R_{thJA} | - | - | - | °C/W | - |
| Soldering temperature, wavesoldering only allowed at leads | T_{sold} | - | - | 260 | °C | 1.6mm (0.063 in.) from case for 10s |

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|----------------|------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 600 | - | - | V | $V_{GS}=0\text{V}$, $I_D=1\text{mA}$ |
| Gate threshold voltage | $V_{(GS)th}$ | 3 | 3.5 | 4 | V | $V_{DS}=V_{GS}$, $I_D=0.28\text{mA}$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$ |
| Gate-source leakage current | I_{GSS} | - | - | 1000 | nA | $V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.145 0.340 | 0.180 - | Ω | $V_{GS}=10\text{V}$, $I_D=5.6\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=5.6\text{A}$, $T_j=150^\circ\text{C}$ |
| Gate resistance | R_G | - | 11 | - | Ω | $f=1\text{MHz}$, open drain |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 1081 | - | pF | $V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$ |
| Output capacitance | C_{oss} | - | 19 | - | pF | $V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 36 | - | pF | $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 381 | - | pF | $I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 14 | - | ns | $V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.6\text{A}$, $R_G=10.0\Omega$; see table 9 |
| Rise time | t_r | - | 12 | - | ns | $V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.6\text{A}$, $R_G=10.0\Omega$; see table 9 |
| Turn-off delay time | $t_{d(off)}$ | - | 85 | - | ns | $V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.6\text{A}$, $R_G=10.0\Omega$; see table 9 |
| Fall time | t_f | - | 8 | - | ns | $V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.6\text{A}$, $R_G=10.0\Omega$; see table 9 |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|----------------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{GS} | - | 6 | - | nC | $V_{DD}=400\text{V}$, $I_D=5.6\text{A}$, $V_{GS}=0$ to 10V |
| Gate to drain charge | Q_{gd} | - | 8 | - | nC | $V_{DD}=400\text{V}$, $I_D=5.6\text{A}$, $V_{GS}=0$ to 10V |
| Gate charge total | Q_g | - | 25 | - | nC | $V_{DD}=400\text{V}$, $I_D=5.6\text{A}$, $V_{GS}=0$ to 10V |
| Gate plateau voltage | V_{plateau} | - | 5.2 | - | V | $V_{DD}=400\text{V}$, $I_D=5.6\text{A}$, $V_{GS}=0$ to 10V |

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.9 | - | V | $V_{GS}=0V, I_F=5.6A, T_j=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 175 | - | ns | $V_R=400V, I_F=2A, di_F/dt=100A/\mu s$; see table 8 |
| Reverse recovery charge | Q_{rr} | - | 1.3 | - | μC | $V_R=400V, I_F=2A, di_F/dt=100A/\mu s$; see table 8 |
| Peak reverse recovery current | I_{rrm} | - | 15 | - | A | $V_R=400V, I_F=2A, di_F/dt=100A/\mu s$; see table 8 |

4 Electrical characteristics diagrams

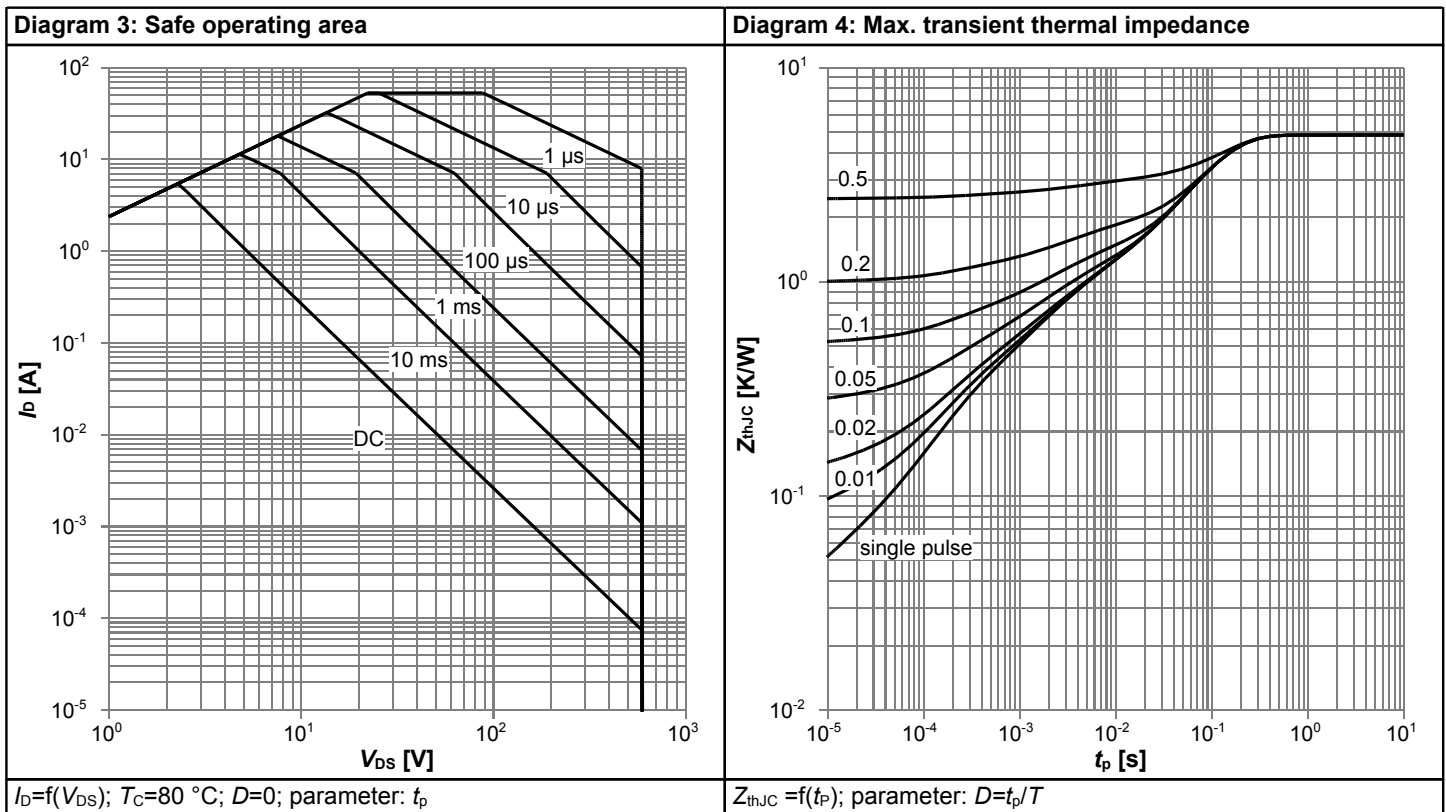
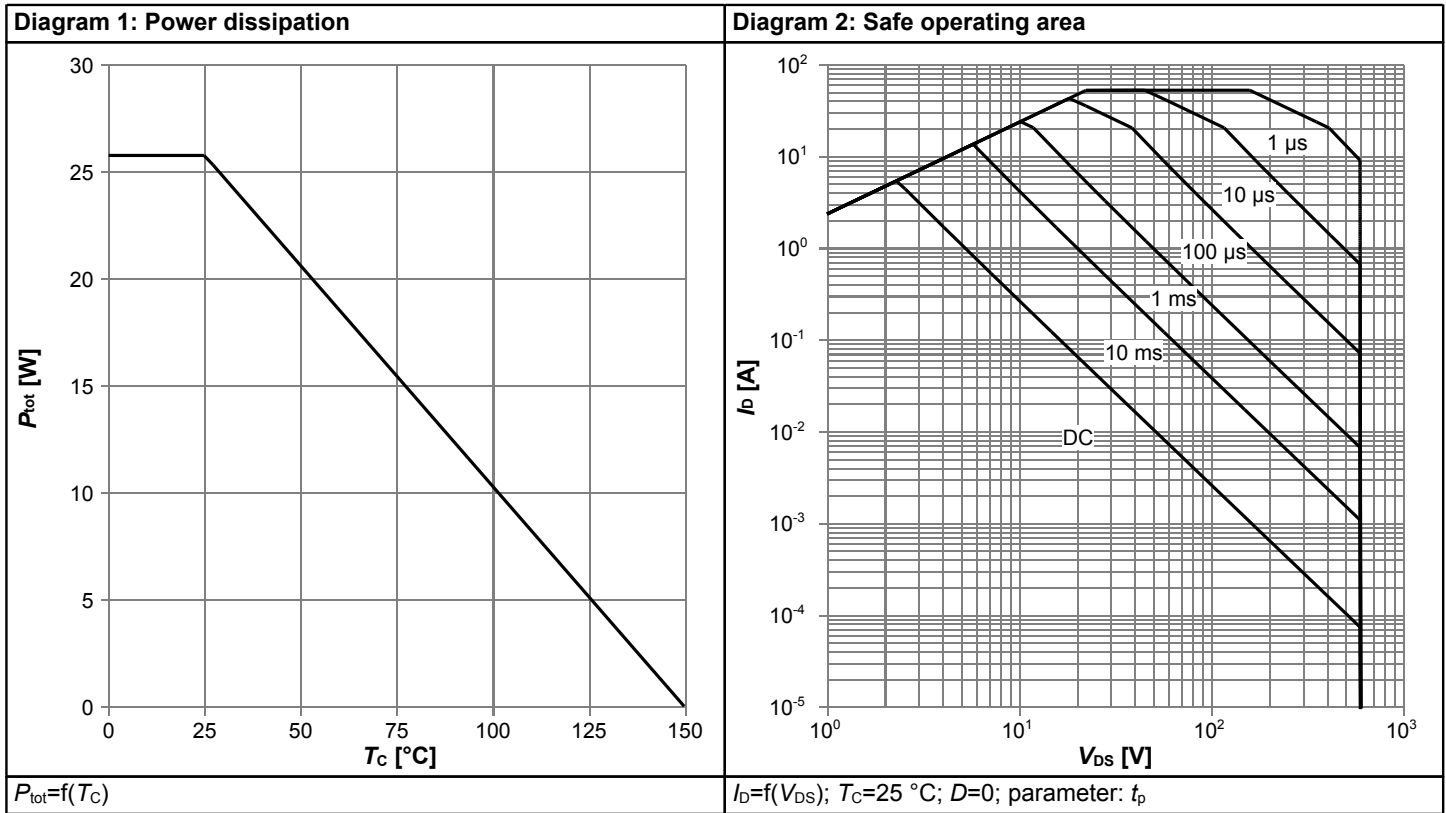
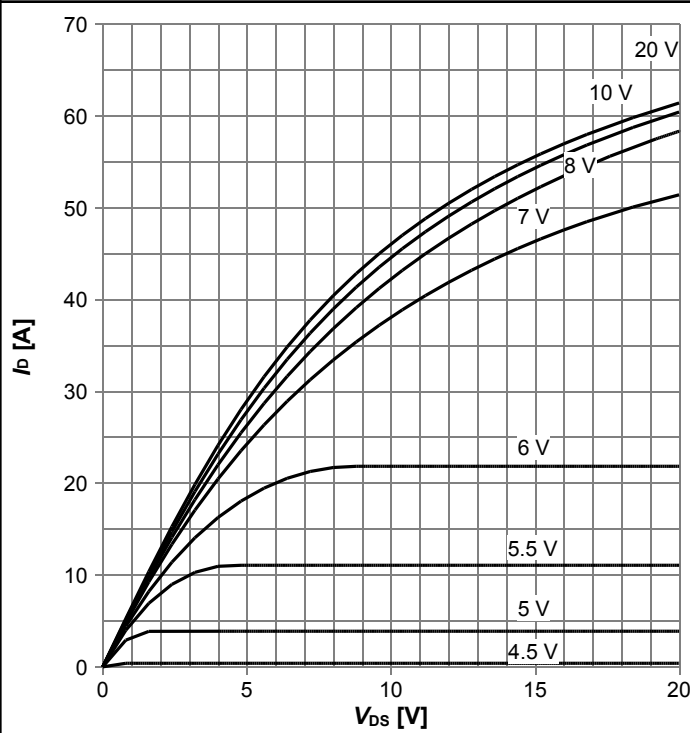
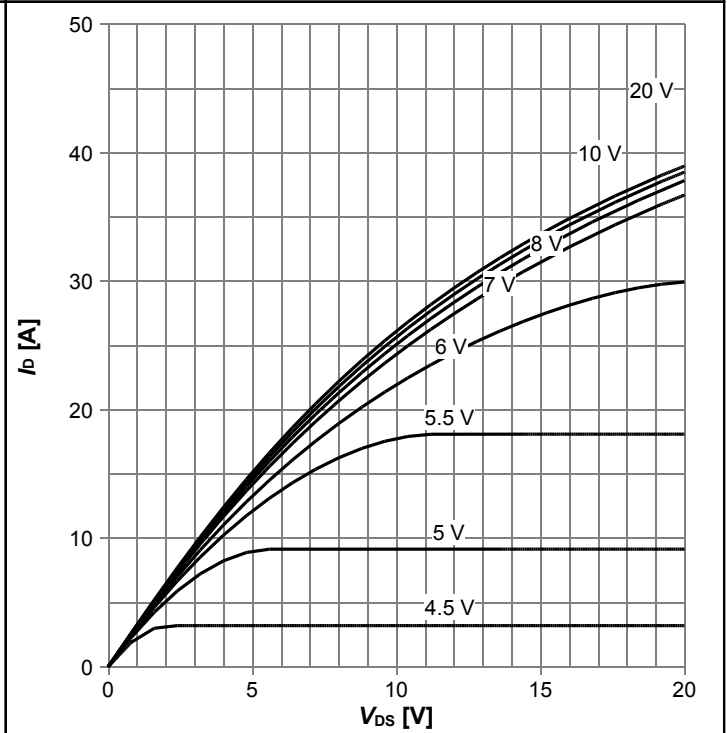


Diagram 5: Typ. output characteristics



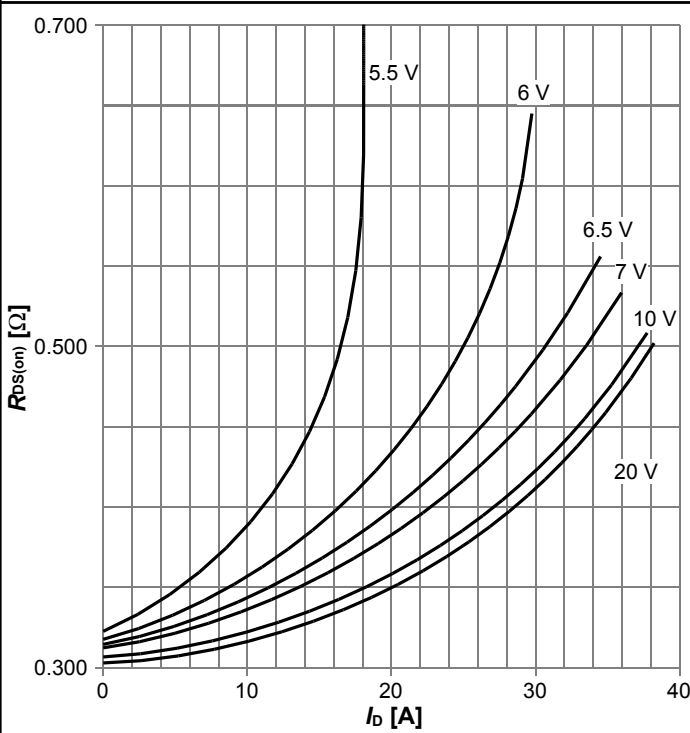
$I_D=f(V_{DS}); T_j=25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. output characteristics



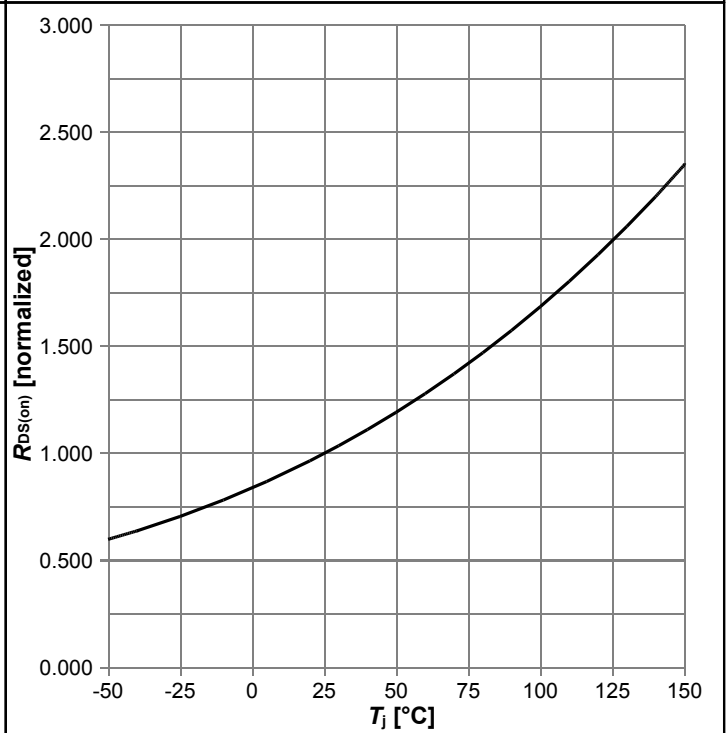
$I_D=f(V_{DS}); T_j=125\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



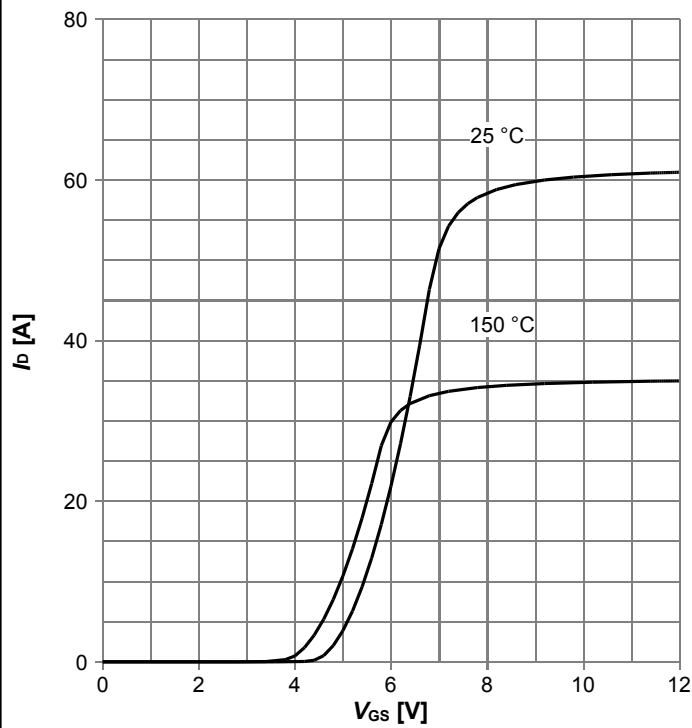
$R_{DS(on)}=f(I_D); T_j=125\text{ °C};$ parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



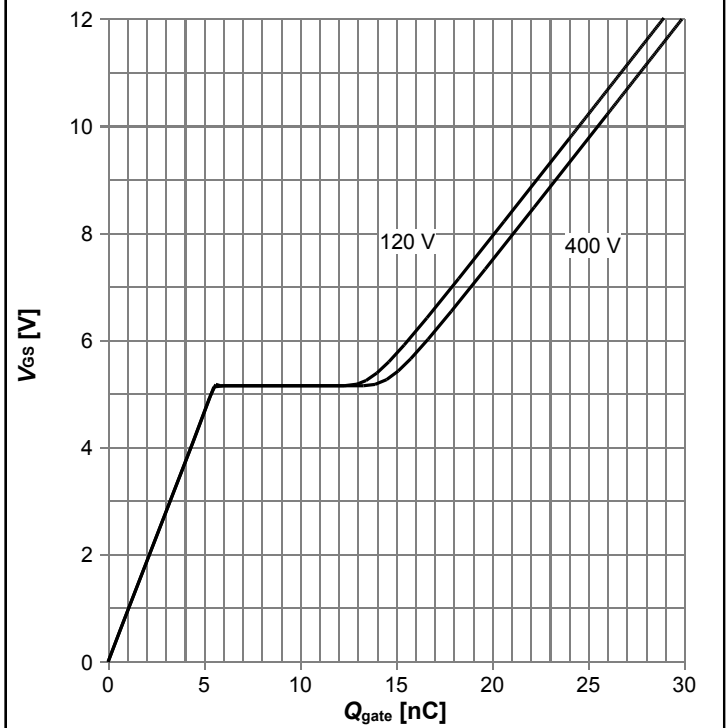
$R_{DS(on)}=f(T_j); I_D=5.6\text{ A}; V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



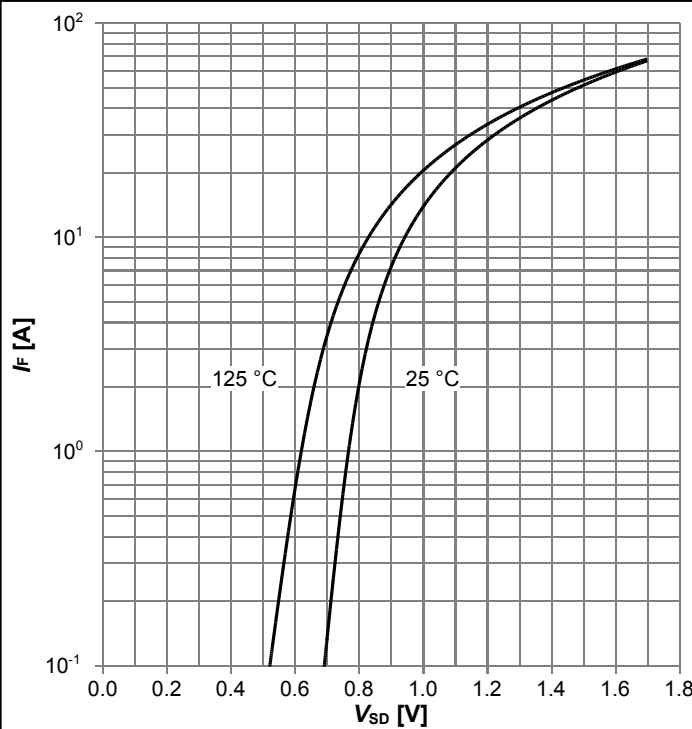
$I_D=f(V_{GS}); V_{DS}=20V$; parameter: T_j

Diagram 10: Typ. gate charge



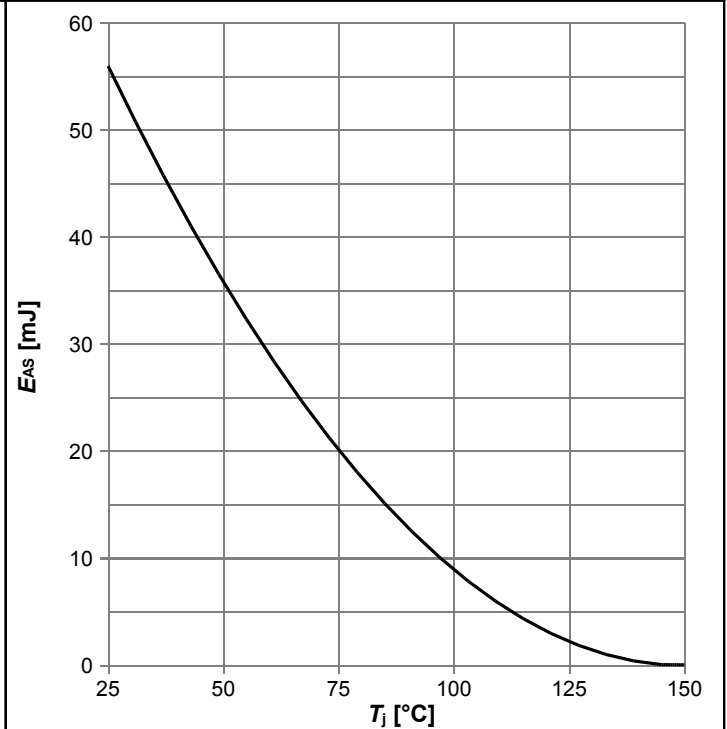
$V_{GS}=f(Q_{gate}); I_D=5.6$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



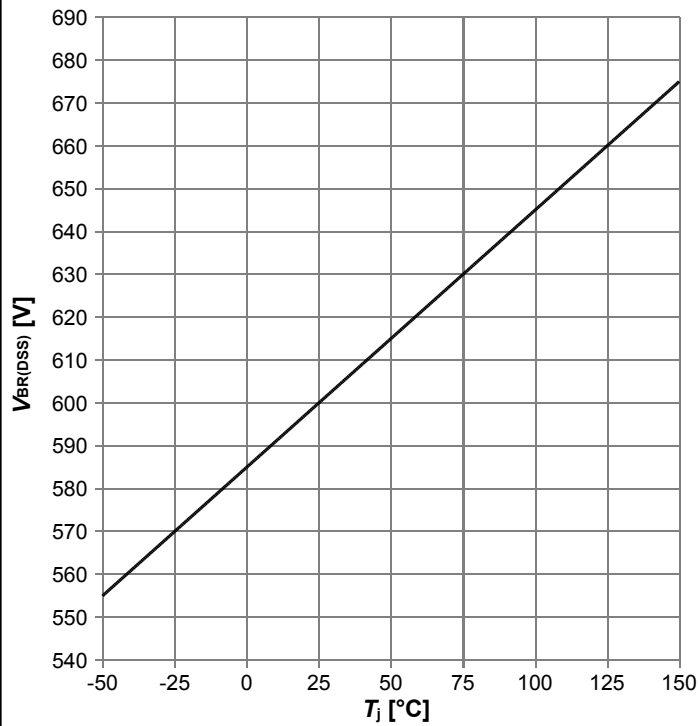
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



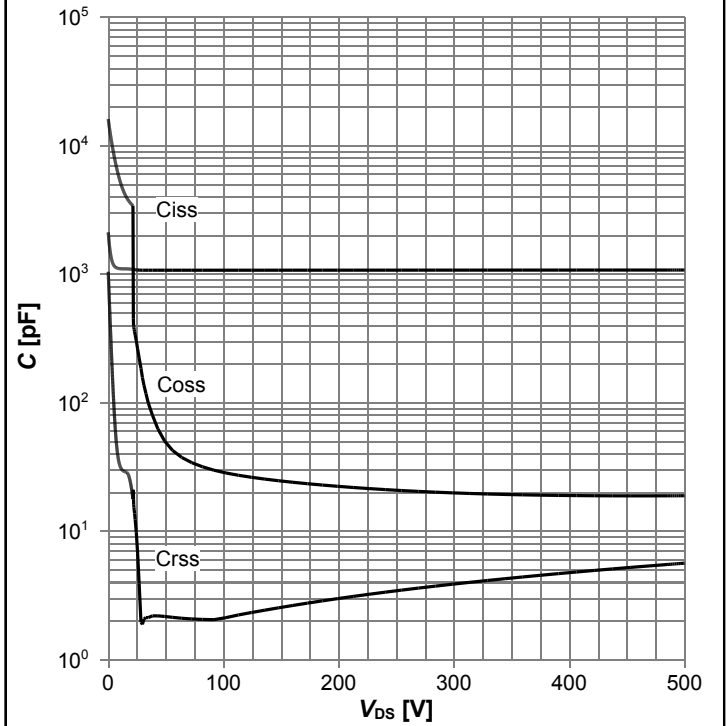
$E_{AS}=f(T_j); I_D=4.0$ A; $V_{DD}=50$ V

Diagram 13: Drain-source breakdown voltage



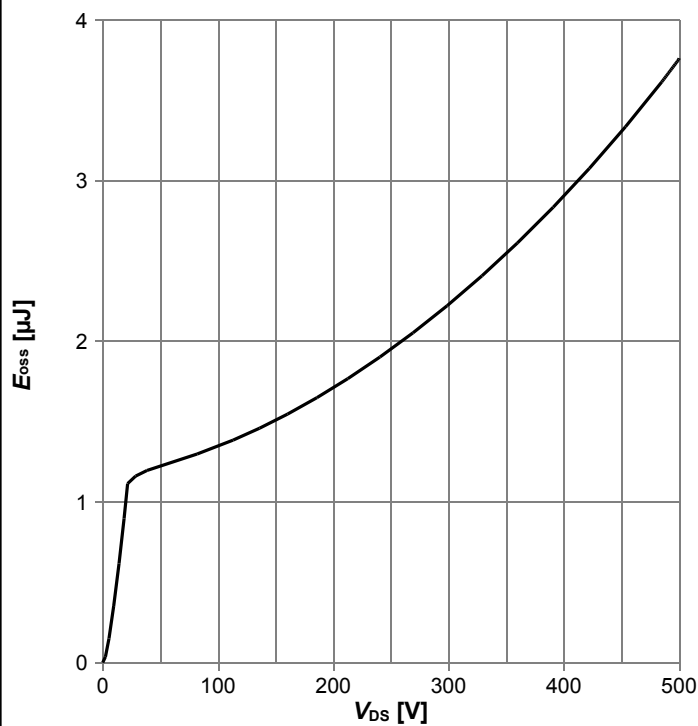
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

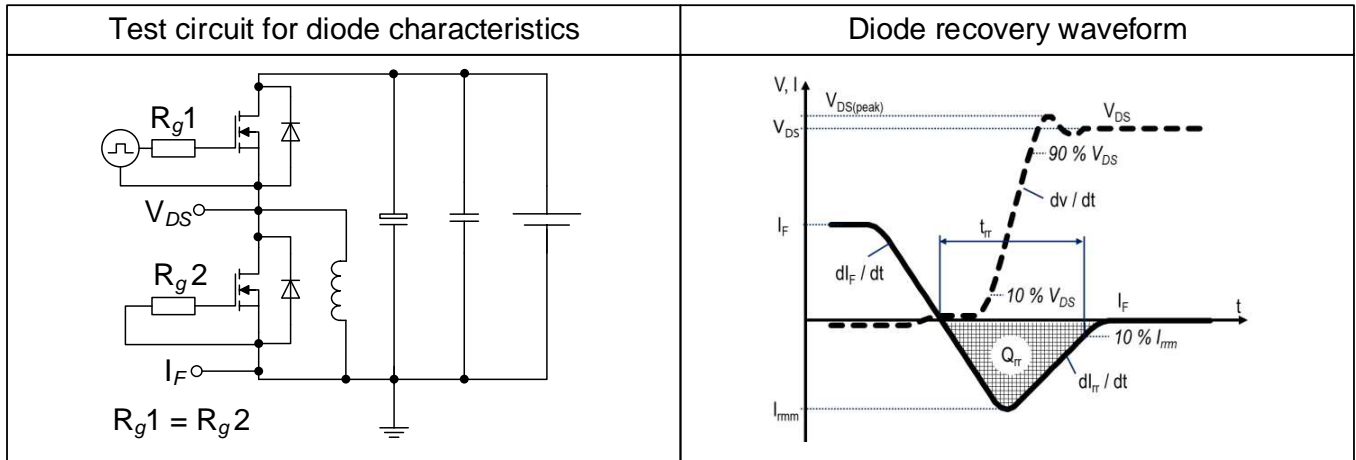


Table 9 Switching times

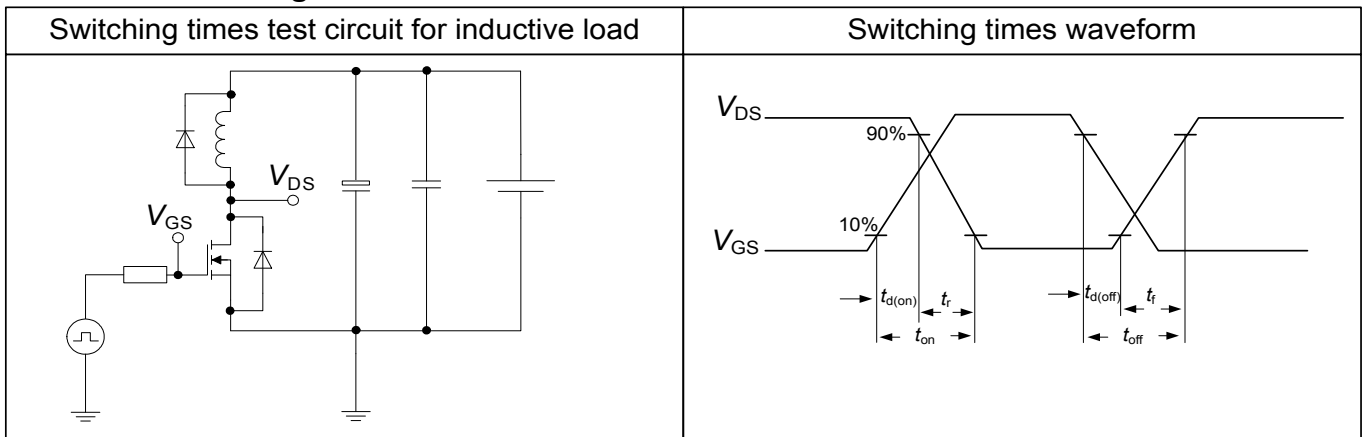
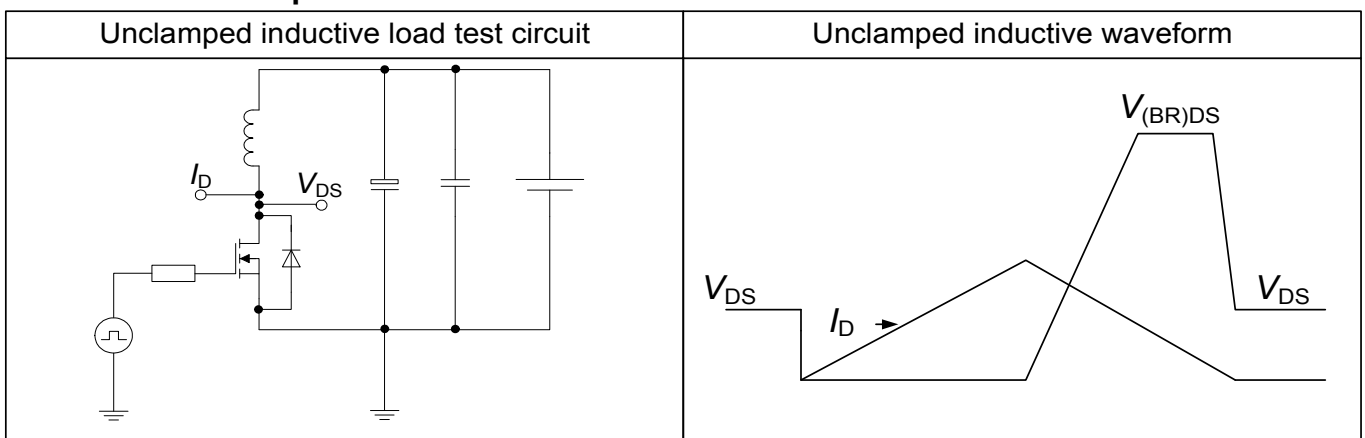
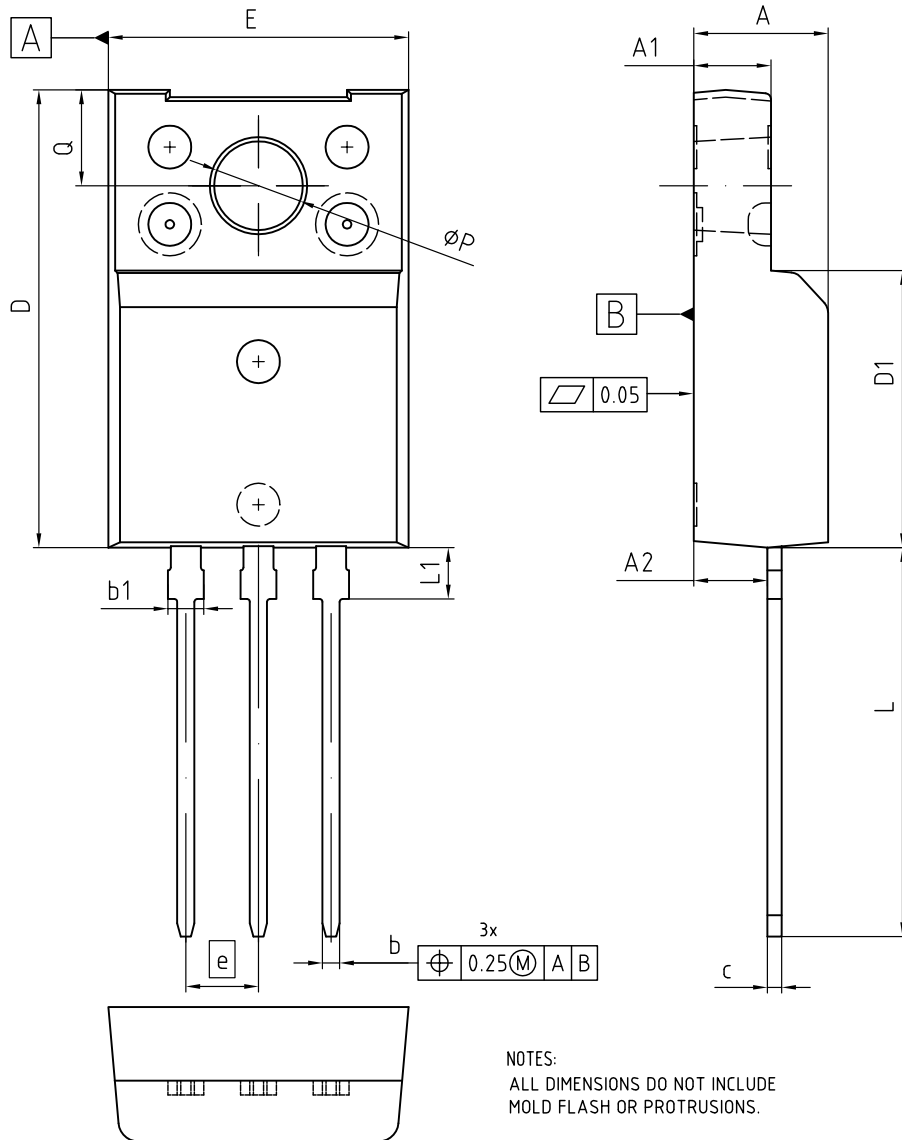


Table 10 Unclamped inductive load



6 Package Outlines



NOTES:
 ALL DIMENSIONS DO NOT INCLUDE
 MOLD FLASH OR PROTRUSIONS.

| DIMENSIONS | MILLIMETERS | |
|------------|-------------|-------|
| | MIN. | MAX. |
| A | 4.60 | 4.80 |
| A1 | 2.60 | 2.80 |
| A2 | 2.47 | 2.67 |
| b | 0.56 | 0.69 |
| b1 | 1.01 | 1.15 |
| c | 0.46 | 0.59 |
| D | 15.90 | 16.10 |
| D1 | 9.58 | 9.78 |
| E | 10.40 | 10.60 |
| e | 2.54 | |
| N | 3 | |
| L | 13.45 | 13.75 |
| L1 | 1.70 | 1.90 |
| øP | 3.00 | 3.20 |
| Q | 3.25 | 3.45 |

| |
|------------------------------------|
| DOCUMENT NO. Z8B00180155 |
| REVISION 04 |
| SCALE 5:1 0 1 2 3 4 5mm |
| EUROPEAN PROJECTION |
| ISSUE DATE 07.11.2016 |

Figure 1 Outline PG-TO 220 FullPAK - Narrow Lead, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS P7 Webpage: www.infineon.com
- IFX CoolMOS P7 application note: www.infineon.com
- IFX CoolMOS P7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPAN60R180P7S

Revision: 2018-07-09, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2018-07-09 | Release of final version |

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