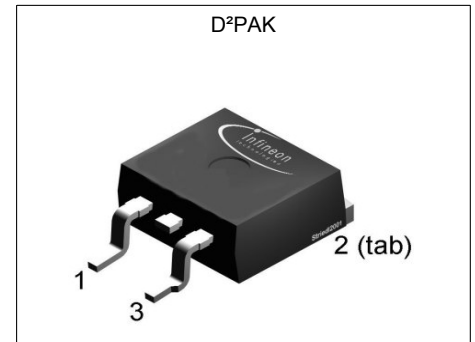


# MOSFET

## OptiMOS™ 5 Power-Transistor, 80 V

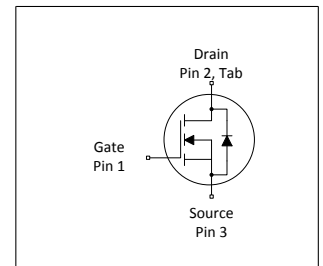
### Features

- Ideal for high frequency switching and sync. rec.
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	80	V
$R_{DS(on),max}$	2.4	m $\Omega$
$I_D$	166	A
$Q_{oss}$	116	nC
$Q_G(0V..10V)$	99	nC



Type / Ordering Code	Package	Marking	Related Links
IPB024N08N5	PG-TO 263-3	024N08N5	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	166 127	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	664	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	374	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	214	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.5	0.7	K/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	40	K/W	-
Soldering temperature, wave and reflow soldering are allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

<sup>1)</sup> See Diagram 3 for more detailed information

<sup>2)</sup> See Diagram 13 for more detailed information

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$ , $I_D=154\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1 2.6	2.4 3.1	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=50\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.4	2.1	$\Omega$	-
Transconductance	$g_{fs}$	89	177	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=100\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	6900	8970	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	1100	8970	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	49	86	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	14	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	46	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	15	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	33	-	nC	$V_{DD}=40\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	21	32	nC	$V_{DD}=40\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	35	-	nC	$V_{DD}=40\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	99	123	nC	$V_{DD}=40\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=40\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	85	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	116	155	nC	$V_{DD}=40\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	140	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	664	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.92	1.2	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	84	168	ns	$V_R=40\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	187	374	nC	$V_R=40\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

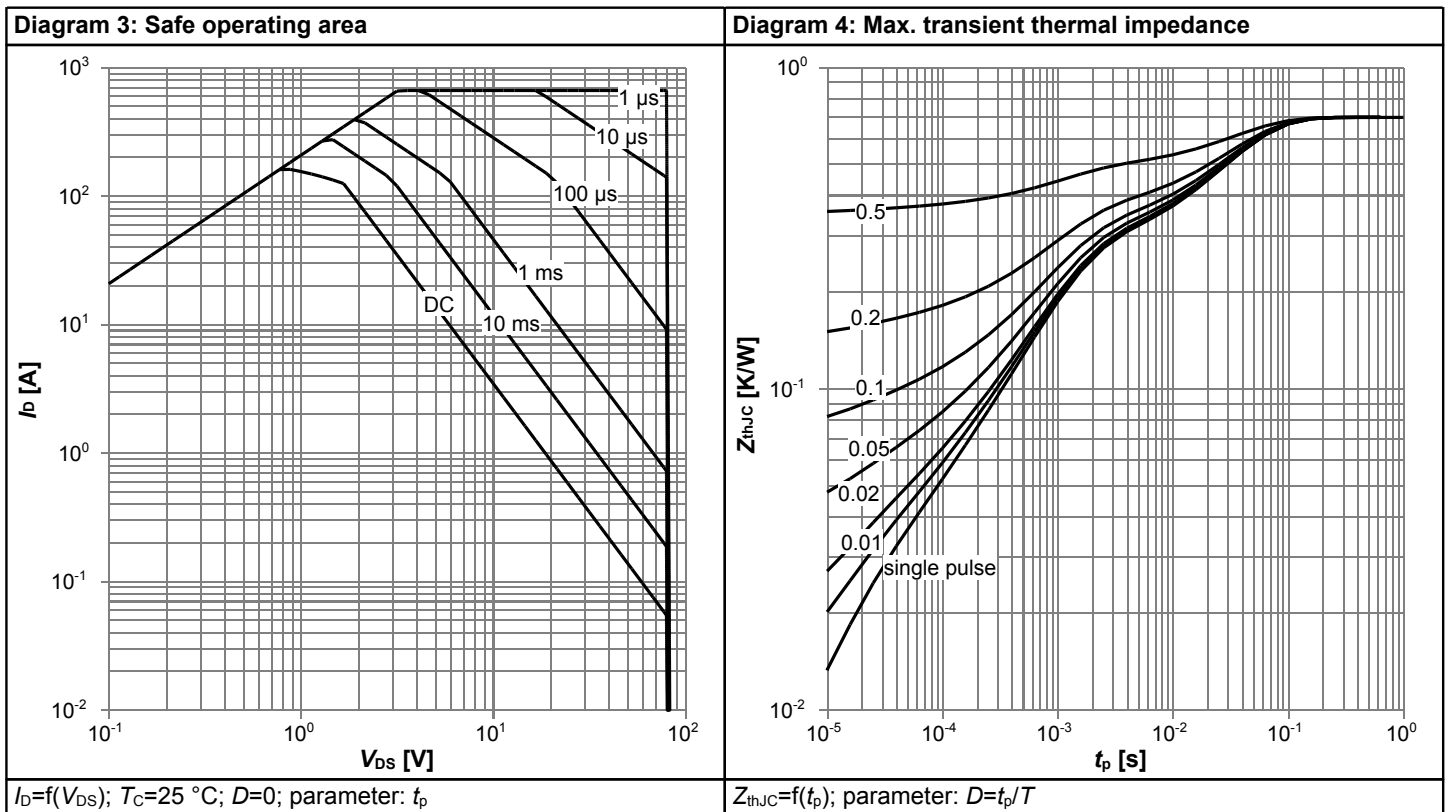
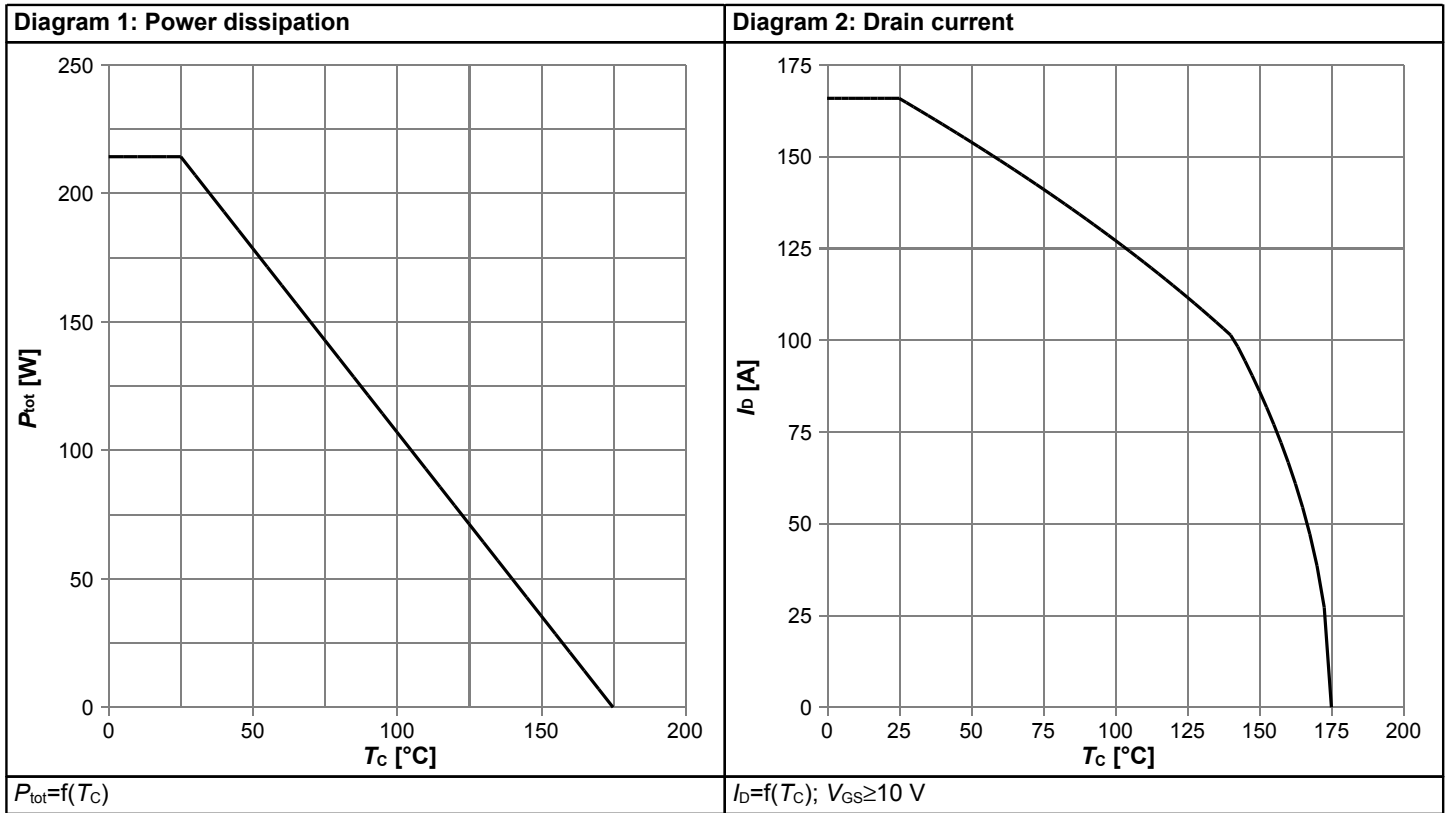
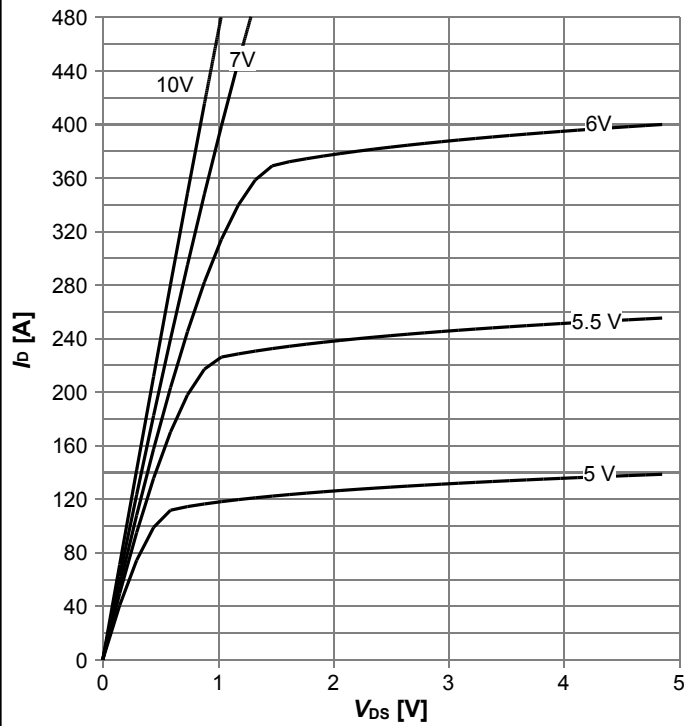
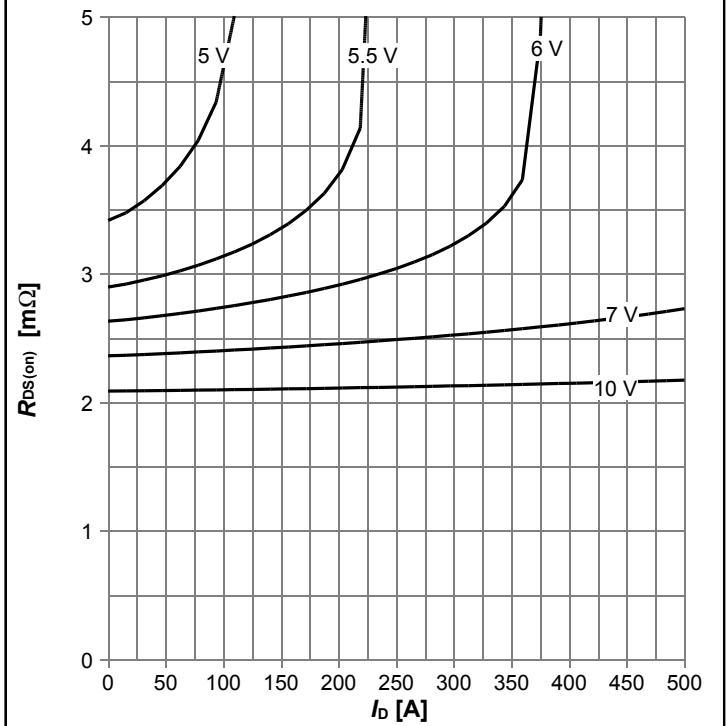


Diagram 5: Typ. output characteristics



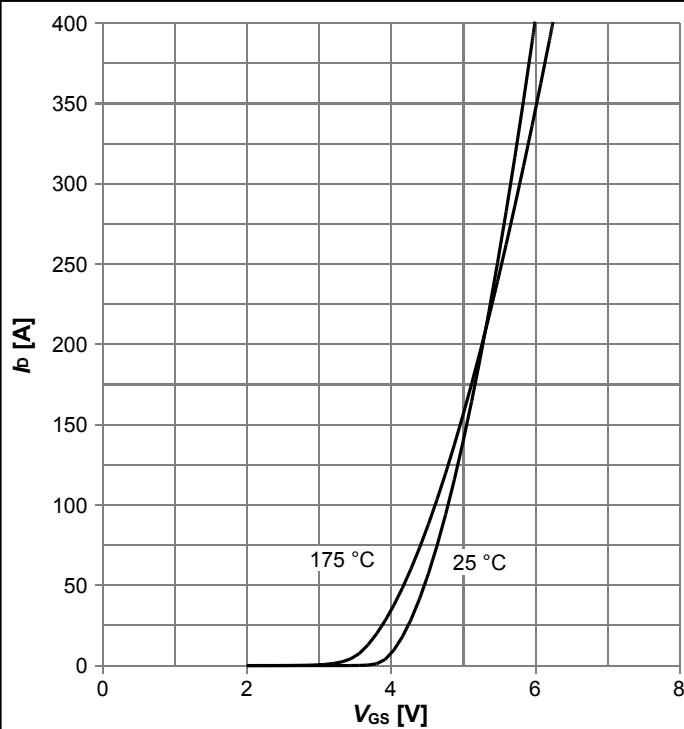
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



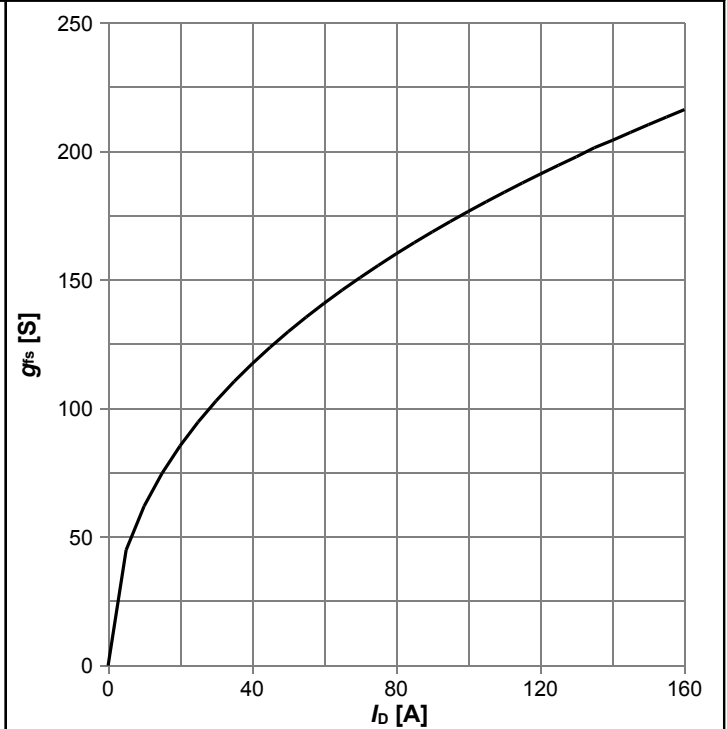
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



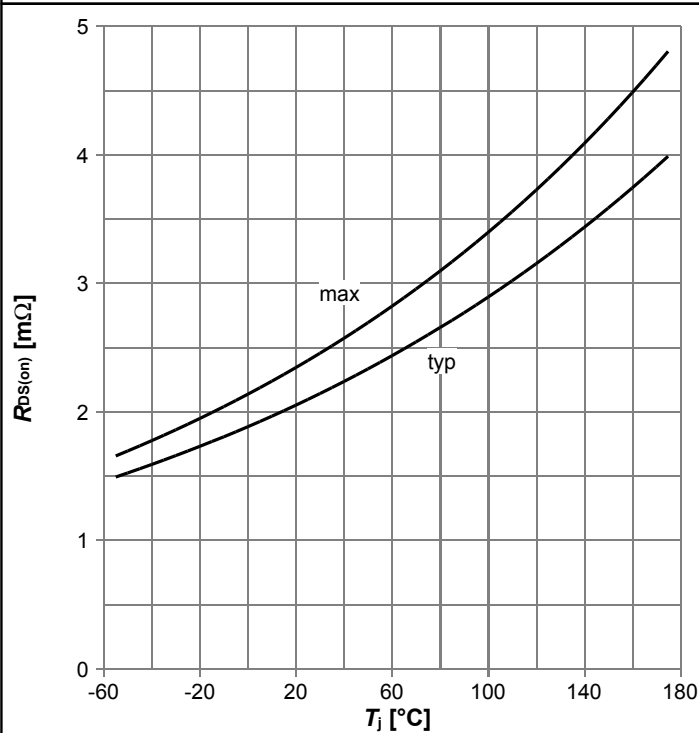
$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



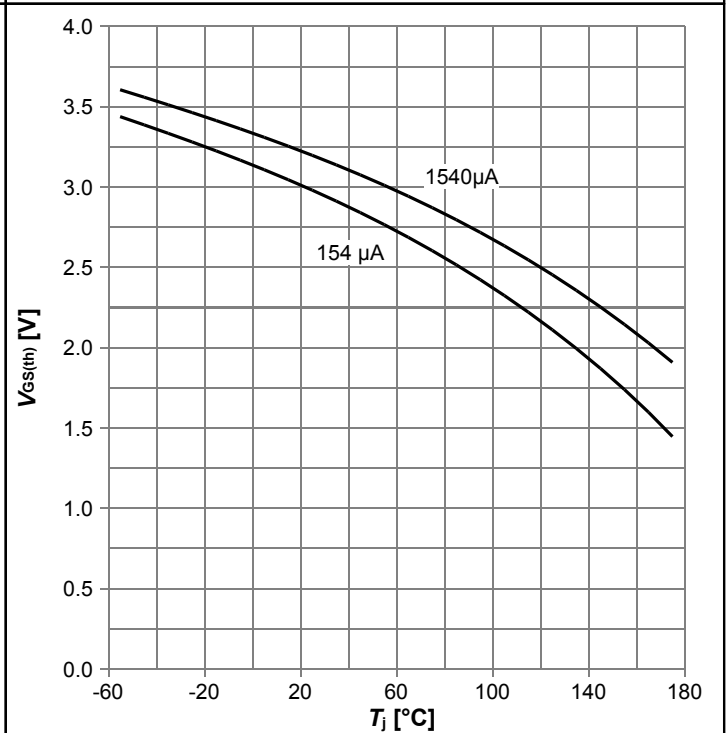
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



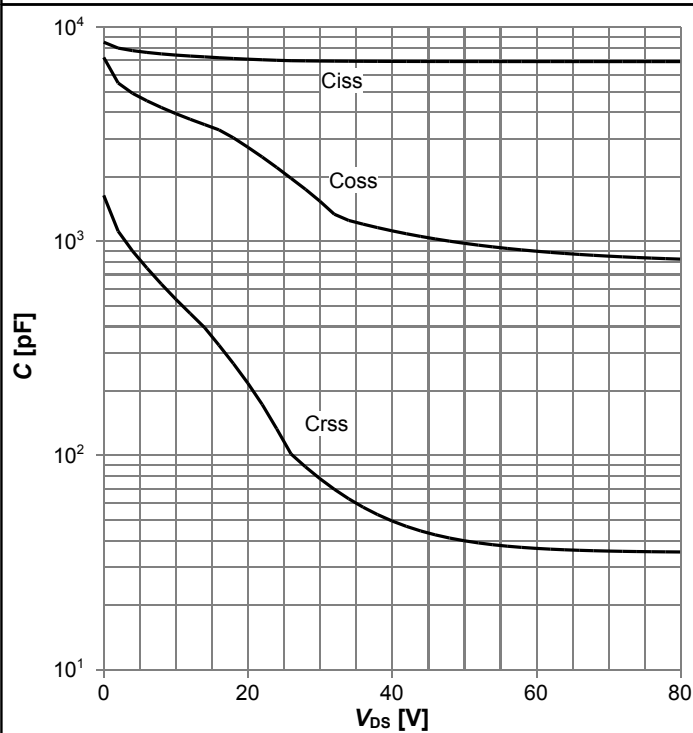
$R_{DS(on)}=f(T_j)$ ;  $I_D=100\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



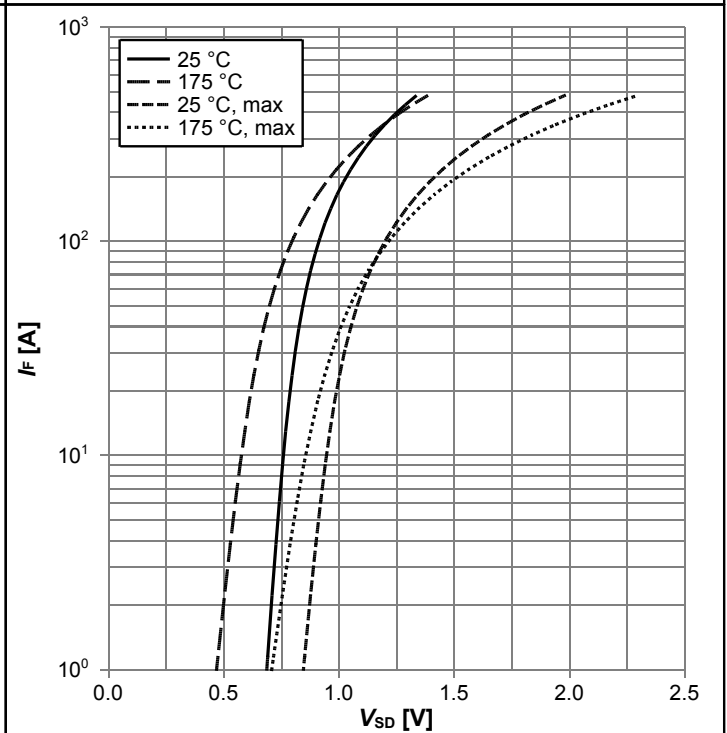
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

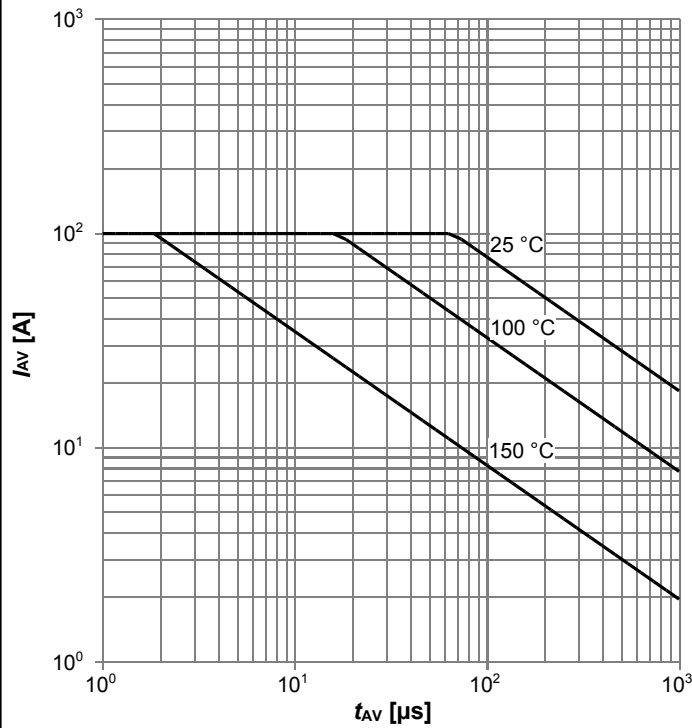
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

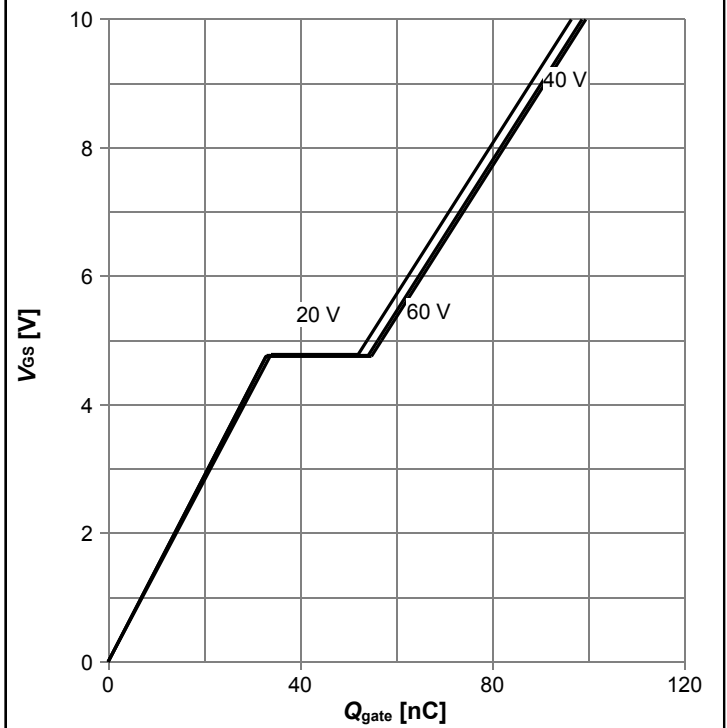


Diagram 13: Avalanche characteristics



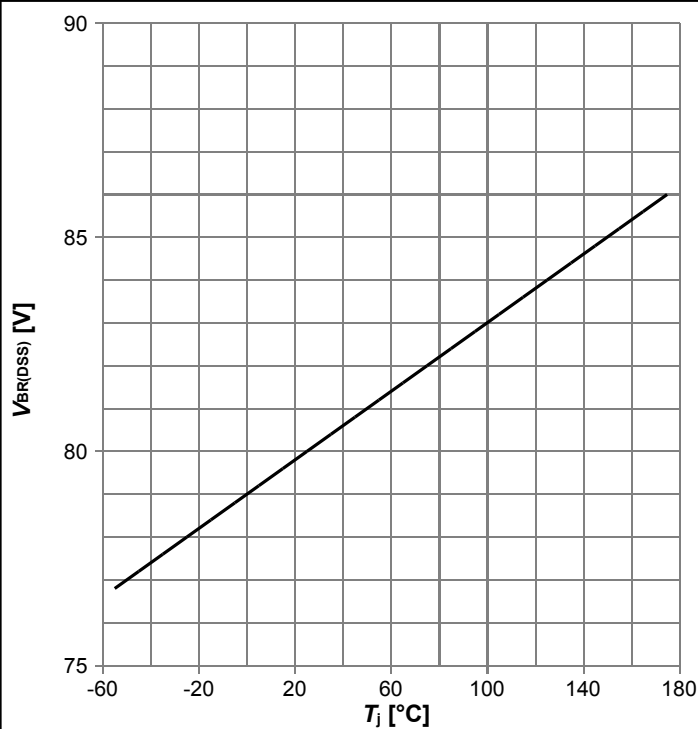
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



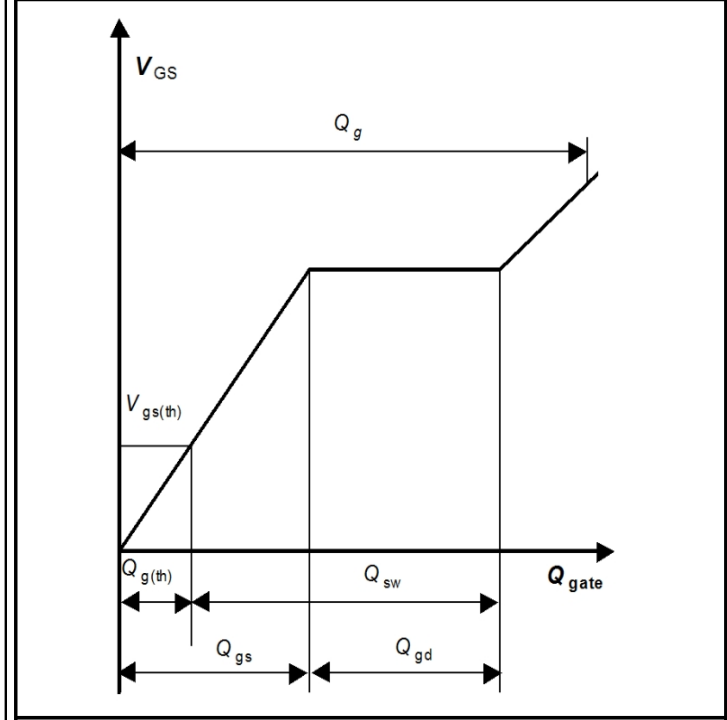
$V_{GS}=f(Q_{gate}); I_D=100 \text{ A pulsed}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



## 5 Package Outlines



**Figure 1 Outline PG-TO 263-3, dimensions in mm/inches**

## Revision History

IPB024N08N5

**Revision: 2017-07-11, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-17	Release of final version
2.1	2017-07-11	Update product current

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