

**OptiMOS®-P2 Power-Transistor**

**Product Summary**

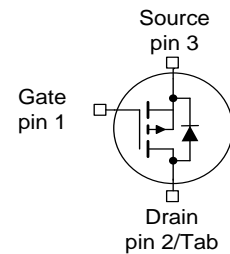
$V_{DS}$	-40	V
$R_{DS(on)}$ (SMD Version)	3.1	m $\Omega$
$I_D$	-120	A

**Features**

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested



Type	Package	Marking
IPB120P04P4L-03	PG-TO263-3-2	4PP04L03
IP1120P04P4L-03	PG-TO262-3-1	4PP04L03
IPP120P04P4L-03	PG-TO220-3-1	4PP04L03


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=-10\text{V}$	-120	A
		$T_C=100\text{ °C}$ , $V_{GS}=-10\text{V}^{2)}$	-114	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	-480	
Avalanche energy, single pulse	$E_{AS}$	$I_D=-60\text{A}$	78	mJ
Avalanche current, single pulse	$I_{AS}$	-	-120	A
Gate source voltage	$V_{GS}$	-	+5/-16	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	136	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>2)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$	-	-	-	1.1	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	-	62	
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D = -1mA$	-40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-340\mu A$	-1.2	-1.7	-2.2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=-32V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-0.05	-1	$\mu A$
		$V_{DS}=-32V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-20	-200	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=-16V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-100A$	-	4.0	5.2	m $\Omega$
		$V_{GS}=-4.5V, I_D=-100A, \text{SMD version}$	-	3.7	4.9	
		$V_{GS}=-10V, I_D=-100A$	-	2.9	3.4	
		$V_{GS}=-10V, I_D=-100A, \text{SMD version}$	-	2.6	3.1	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	11380	15000	pF
Output capacitance	$C_{oss}$		-	3410	5000	
Reverse transfer capacitance	$C_{rss}$		-	135	270	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-120A,$ $R_G=3.5\Omega$	-	21	-	ns
Rise time	$t_r$		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	85	-	
Fall time	$t_f$		-	57	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=-32V,$ $I_D=-120A,$ $V_{GS}=0$ to $-10V$	-	40	52	nC
Gate to drain charge	$Q_{gd}$		-	32	64	
Gate charge total	$Q_g$		-	180	234	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25^\circ C$	-	-	-120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	-480	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=-100A,$ $T_j=25^\circ C$	-	-1	-1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$	-	54		ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	60		nC

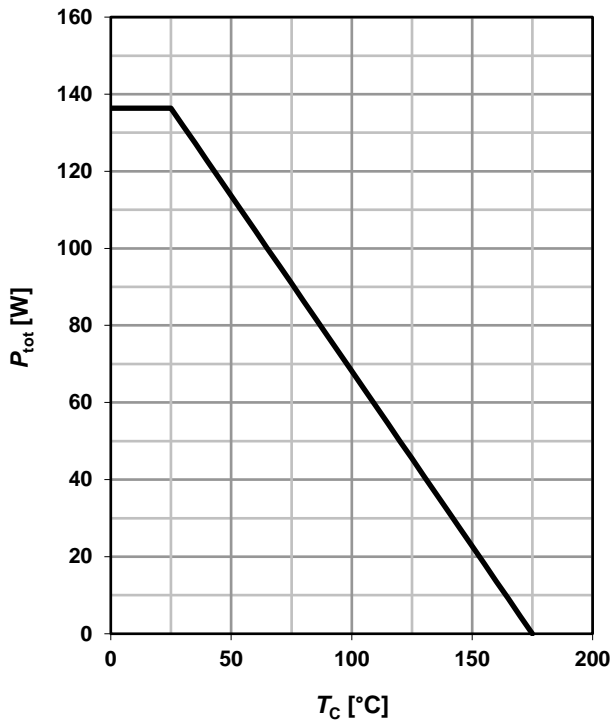
<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 1.1K/W$  the chip is able to carry -171A at 25°C.

<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

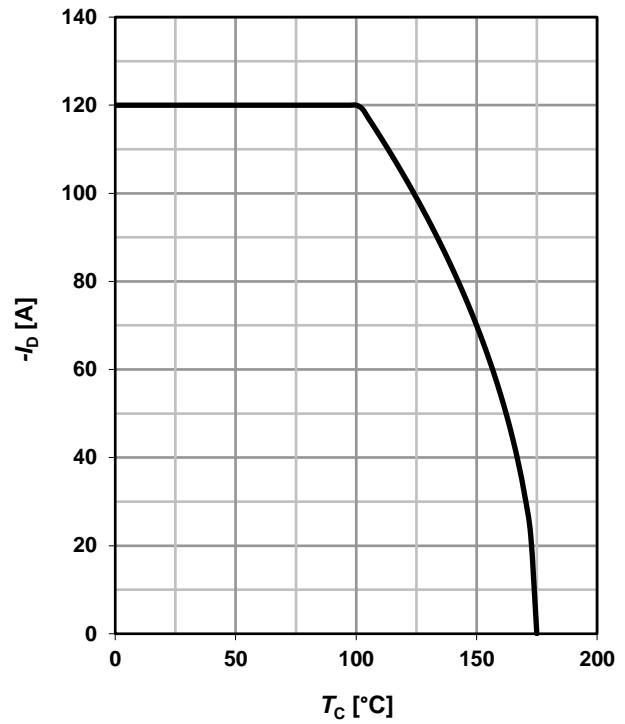
**1 Power dissipation**

$P_{tot} = f(T_C); V_{GS} \leq -6V$



**2 Drain current**

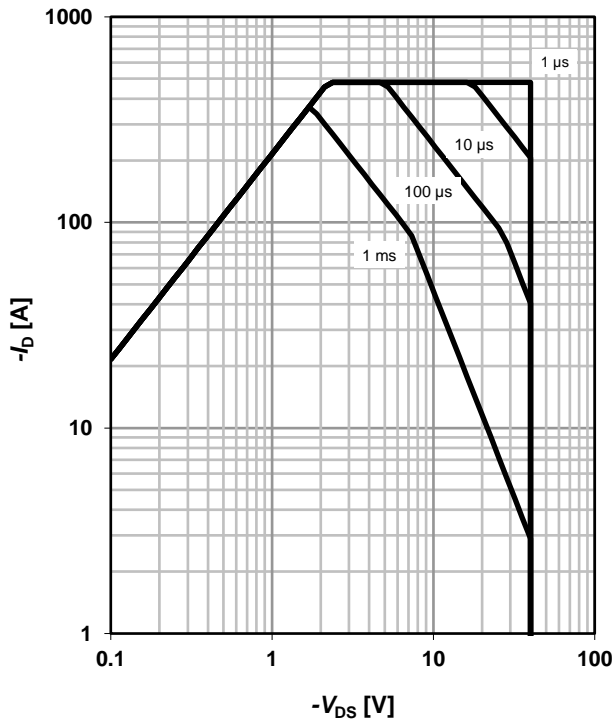
$I_D = f(T_C); V_{GS} \leq -6V; SMD$



**3 Safe operating area**

$I_D = f(V_{DS}); T_C = 25^\circ C; D = 0; SMD$

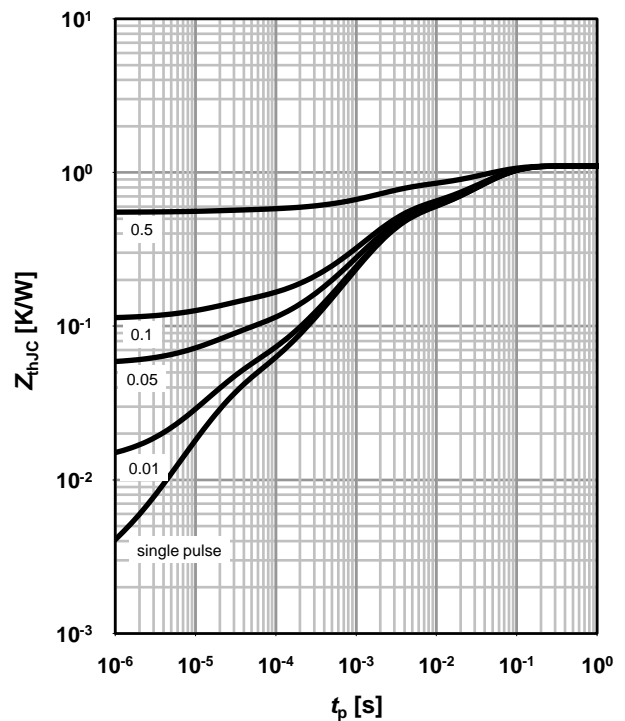
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC} = f(t_p)$

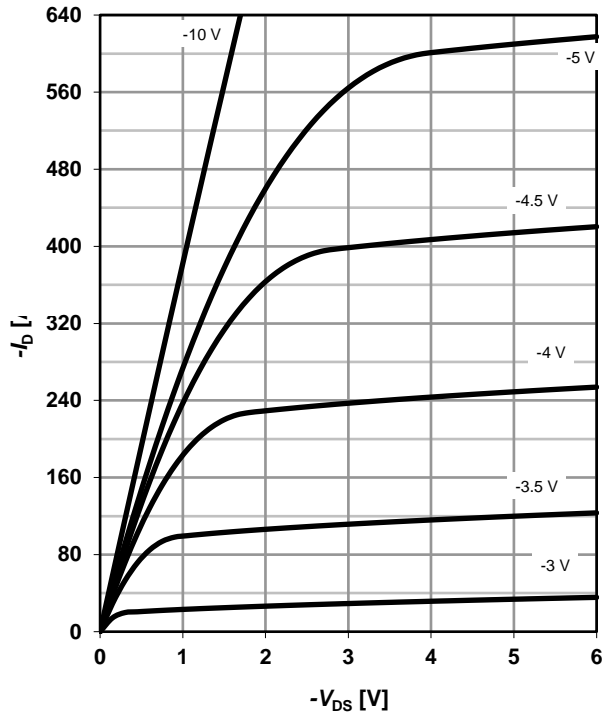
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{SMD}$

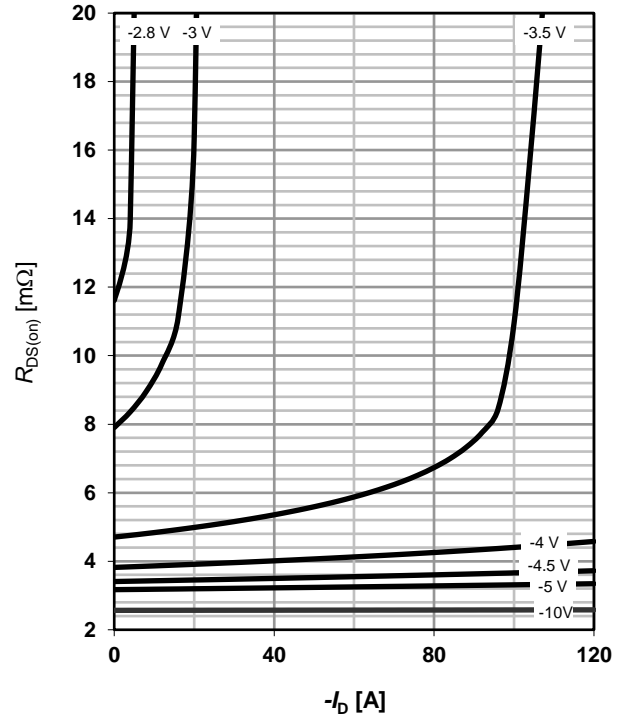
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{SMD}$

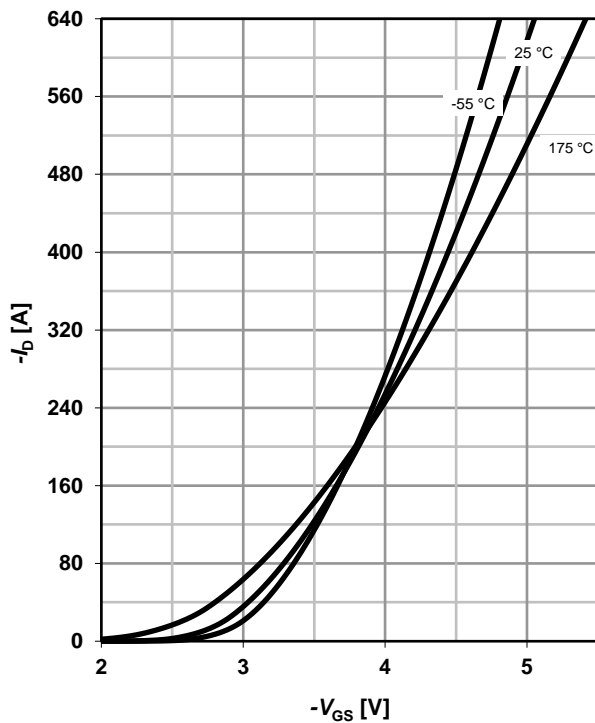
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

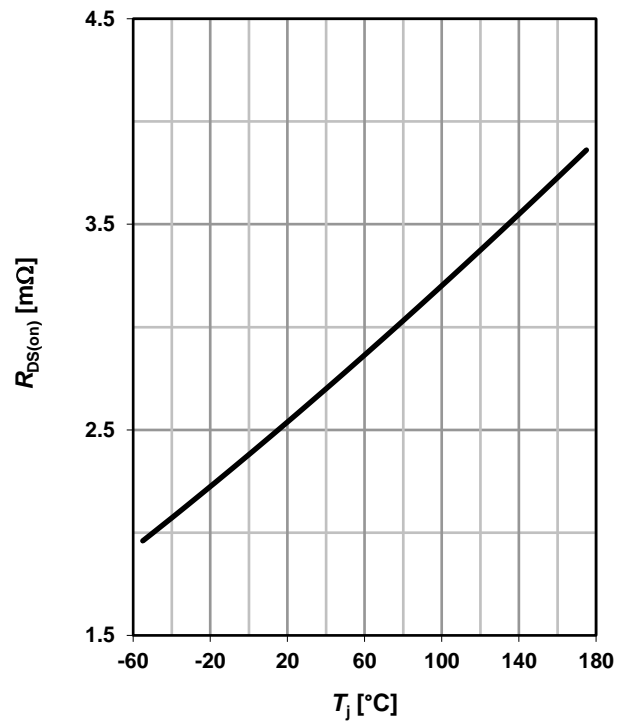
$I_D = f(V_{GS}); V_{DS} = -6V$

parameter:  $T_j$



**8 Typ. drain-source on-state resistance**

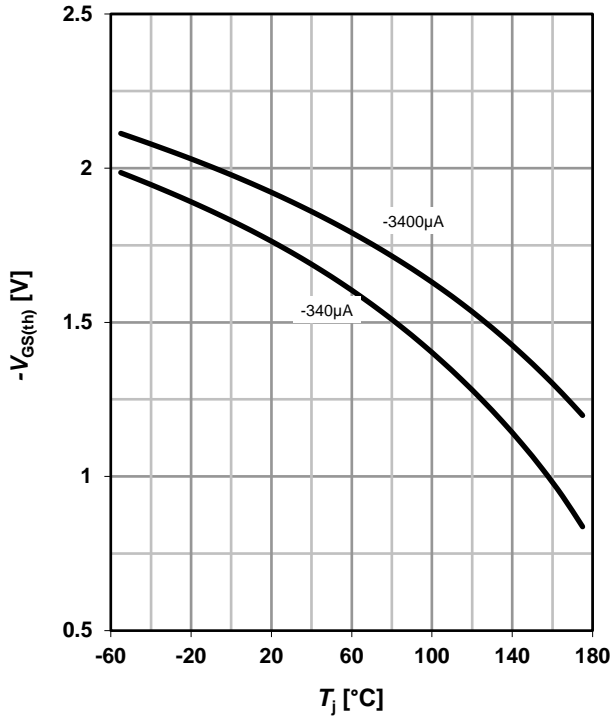
$R_{DS(on)} = f(T_j); I_D = -100\text{ A}; V_{GS} = -10\text{ V}; \text{SMD}$



**9 Typ. gate threshold voltage**

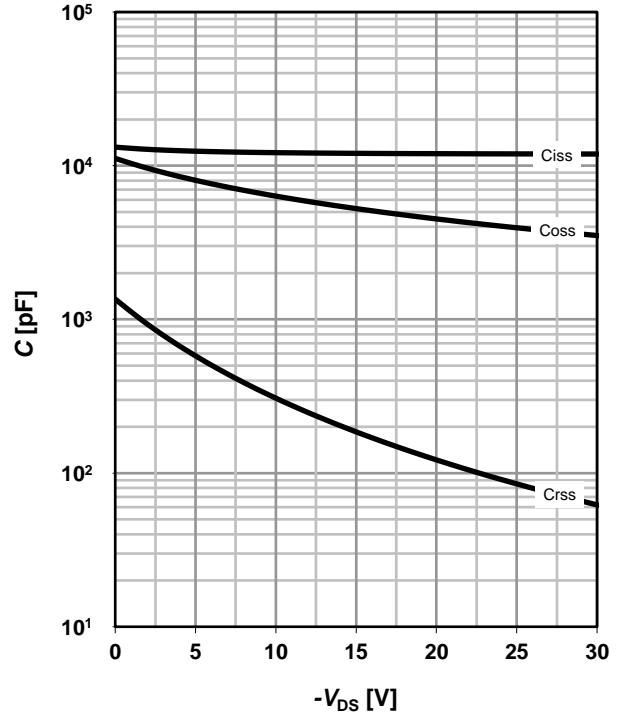
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**10 Typ. capacitances**

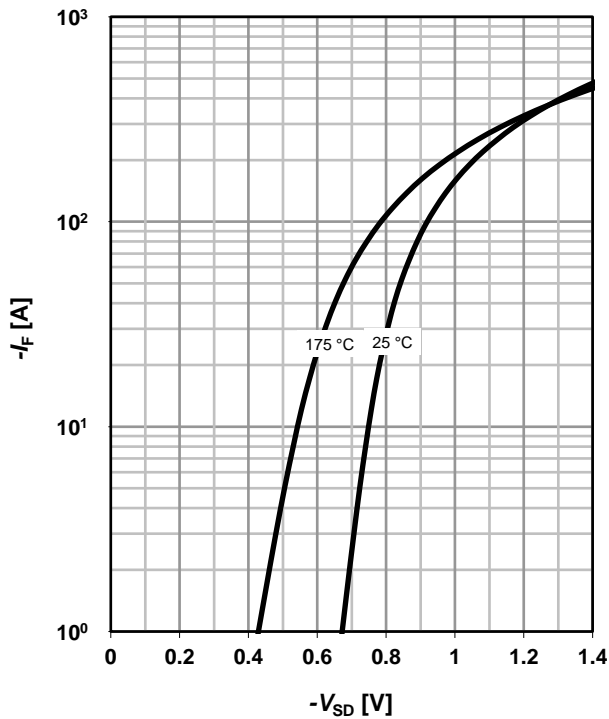
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



**11 Typical forward diode characteristics**

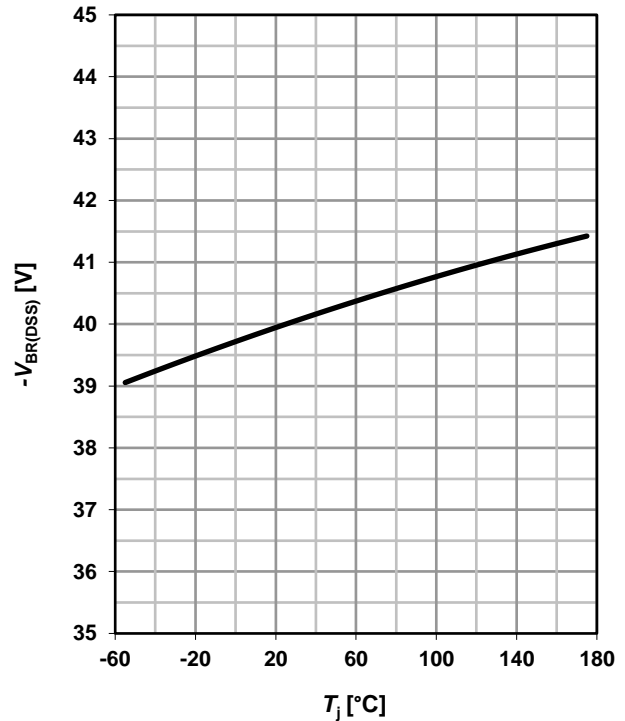
$I_F = f(V_{SD})$

parameter:  $T_j$



**12 Drain-source breakdown voltage**

$V_{BR(DSS)} = f(T_j); I_D = -1 mA$

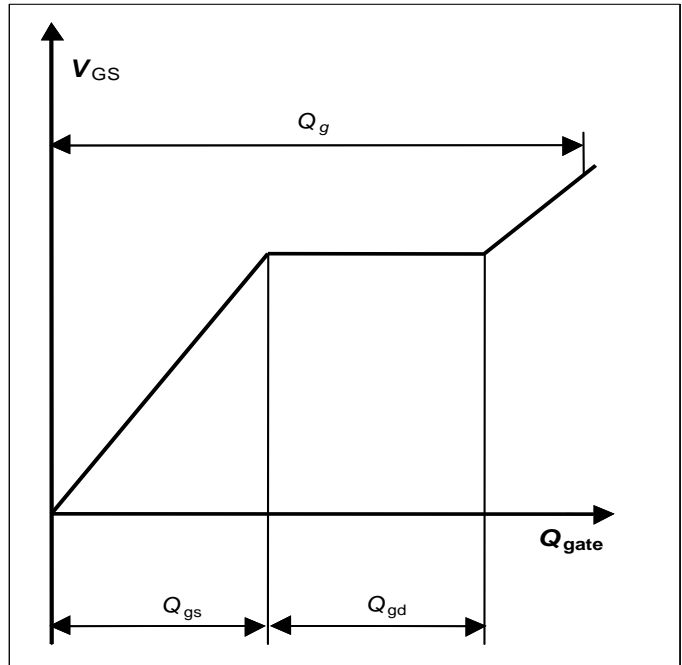
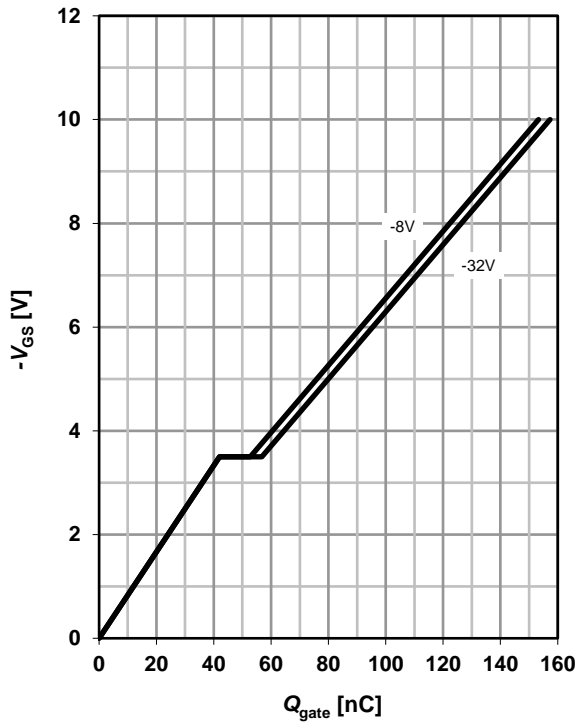


13 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = -120\text{ A pulsed}$

parameter:  $V_{DD}$

14 Gate charge waveforms



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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## Revision History

Version	Date	Changes
1.0	24.01.2011	Final Data Sheet
1.1	27.05.2015	Update of marking
1.2	03.07.2019	V <sub>GS</sub> changed

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