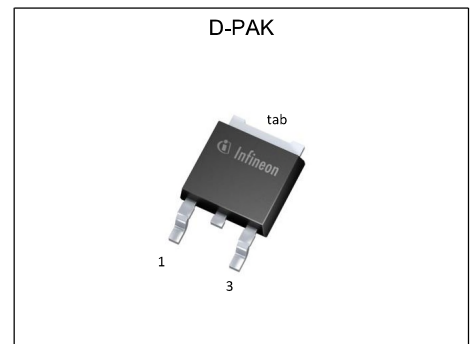


MOSFET

OptiMOS™ Power-Transistor, -100 V

Features

- P-channel
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- Logic level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

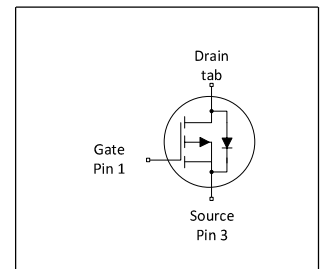


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-100	V
$R_{DS(on),max}$	178	m Ω
I_D	-13.9	A
Q_{oss}	-13	nC
Q_G	-42	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPD18DP10LM	PG-TO252-3	18DP10LM	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-13.9 -9.9 -9.3 -2.5	A	$V_{GS}=-10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	-56	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	240	mJ	$I_D=-13\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	83 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.8	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area	R_{thJA}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint ²⁾	R_{thJA}	-	-	75	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-1.5	-2.0	V	$V_{DS}=V_{GS}$, $I_D=-1040\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1.0 -100	μA	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	140.3 142.9	178 200	$\text{m}\Omega$	$V_{GS}=-10\text{ V}$, $I_D=-13\text{ A}$ $V_{GS}=-4.5\text{ V}$, $I_D=-10\text{ A}$
Gate resistance	R_G	-	5.1	-	Ω	-
Transconductance	g_{fs}	-	24	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=-13\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	1600	2100	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	110	140	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	25	44	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	5.72	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-13\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	2.75	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-13\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	39.85	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-13\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	24.75	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-13\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-5.2	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-2.4	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	-10.9	-16.4	nC	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Switching charge	Q_{sw}	-	-13.6	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	-21	-26	nC	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	-3.2	-	V	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total	Q_g	-	-42	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-13\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	-13.1	-17.4	nC	$V_{DS}=-50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-13.9	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-56	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-0.87	-1.2	V	$V_{GS}=0\text{ V}, I_F=-13\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	65	130	ns	$V_R=-50\text{ V}, I_F=-13\text{ A}, di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	216.91	433.82	nC	$V_R=-50\text{ V}, I_F=-13\text{ A}, di_F/dt=-100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

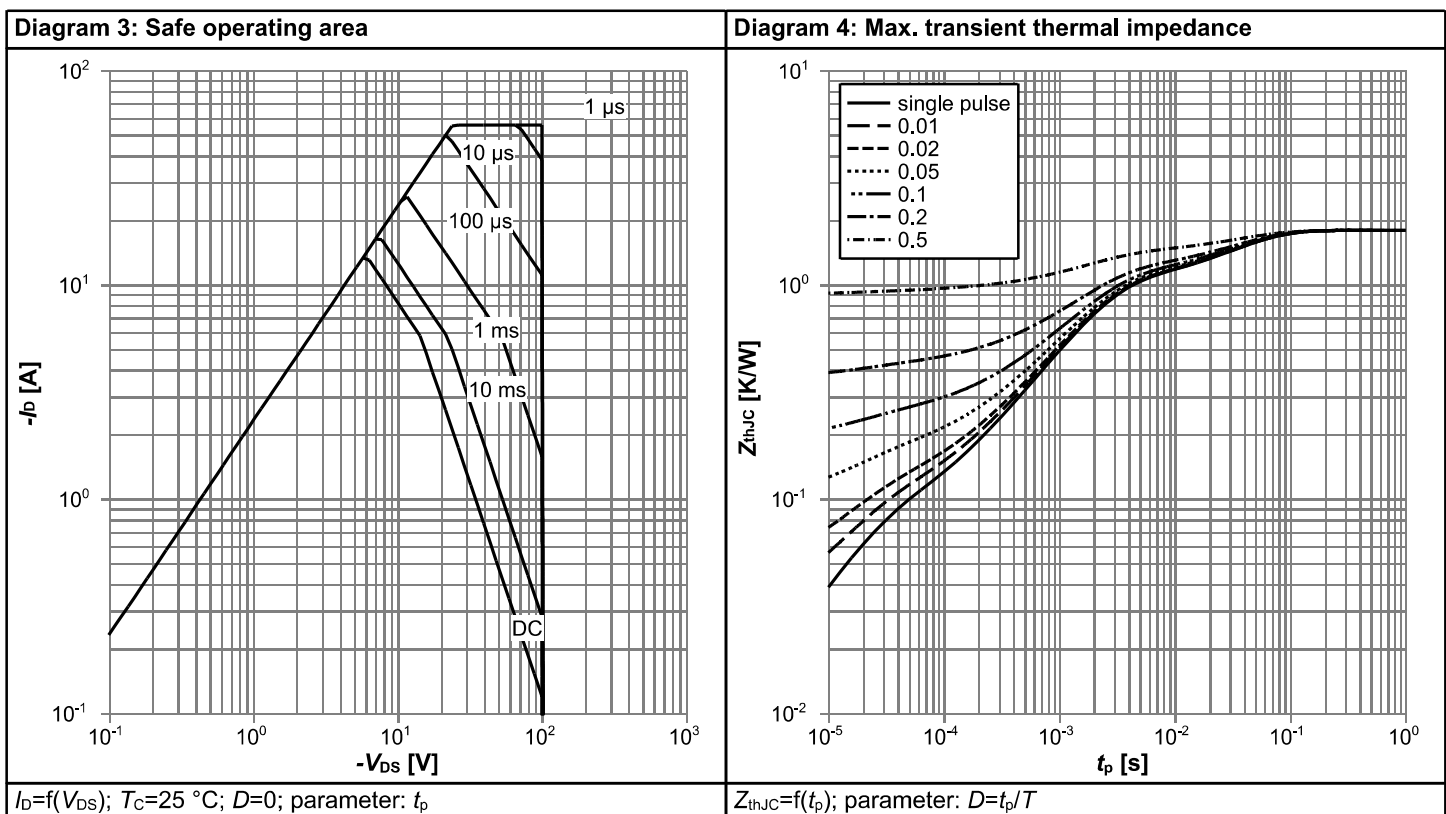
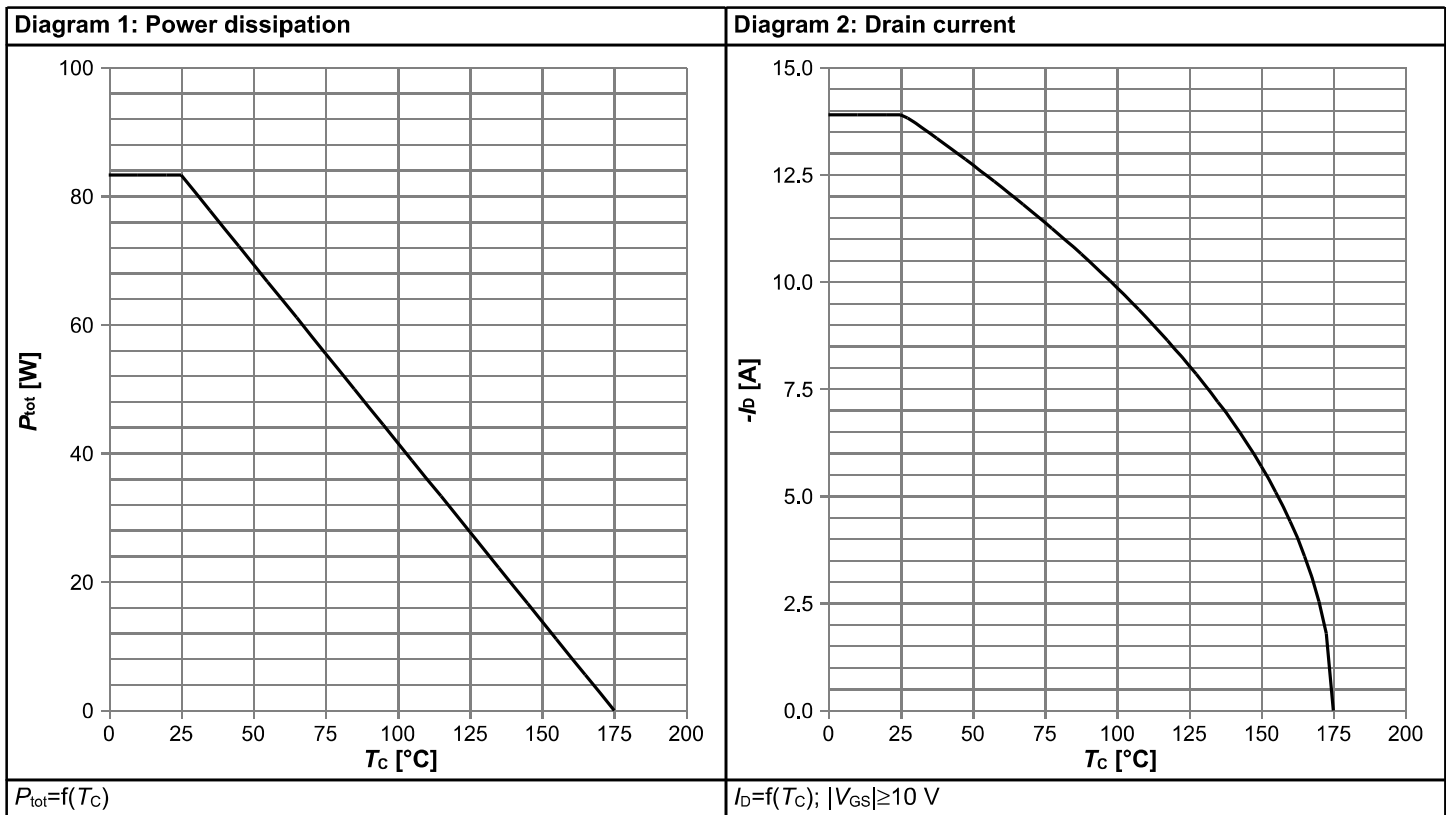
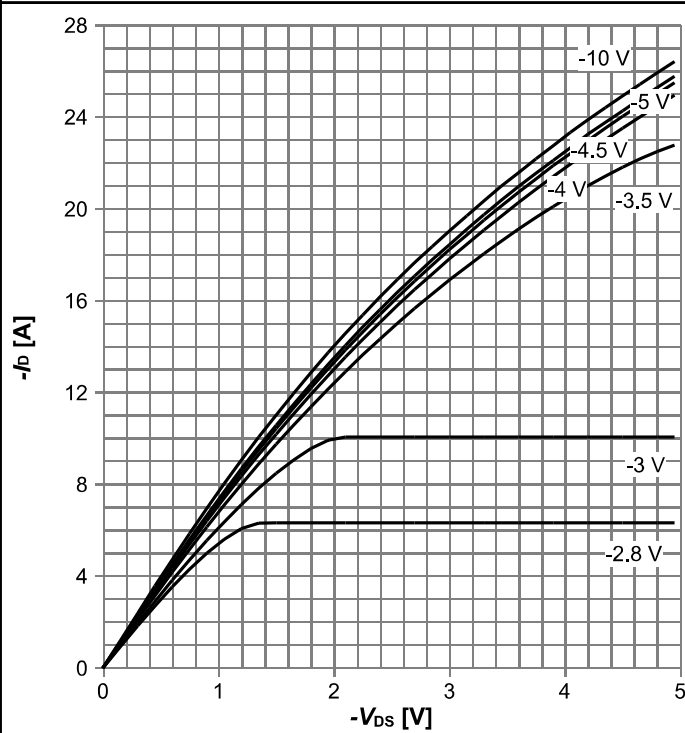
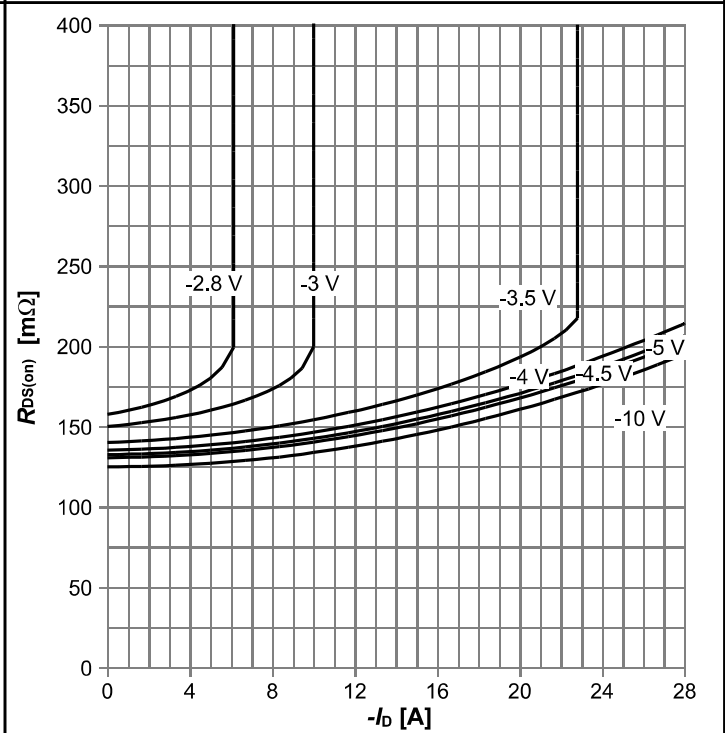


Diagram 5: Typ. output characteristics



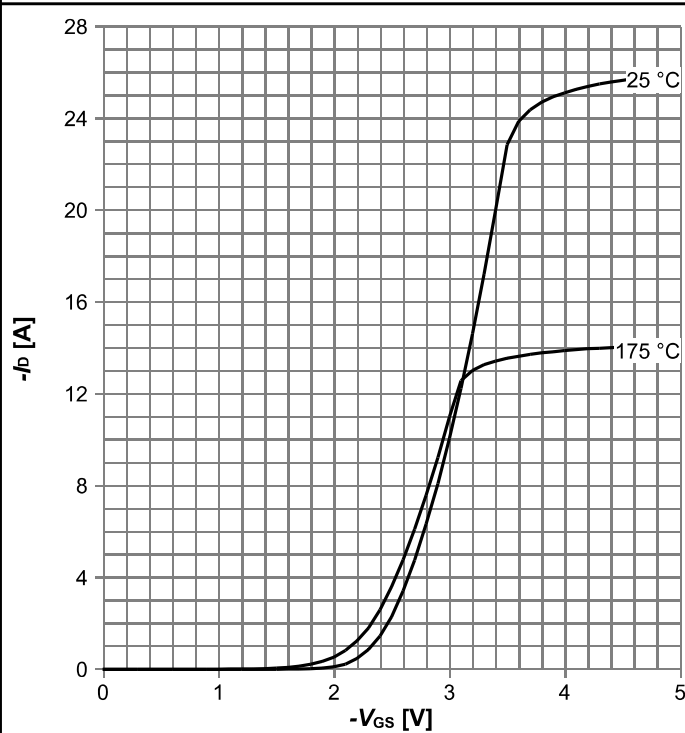
$I_D=f(V_{DS})$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



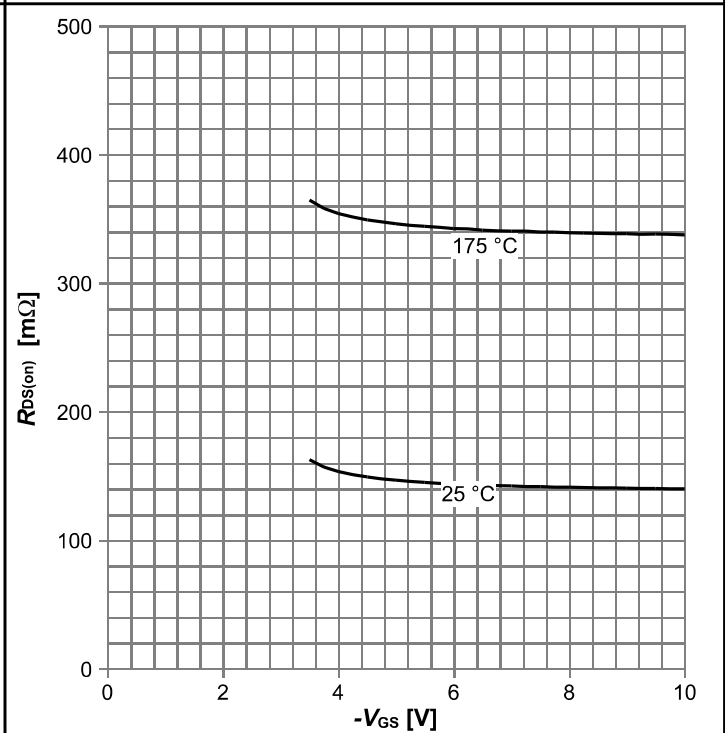
$R_{DS(on)}=f(I_D)$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



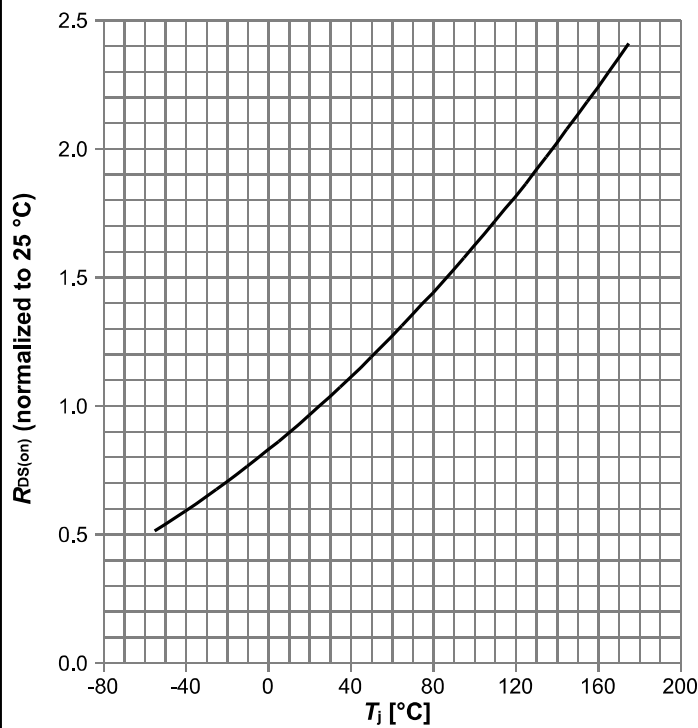
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



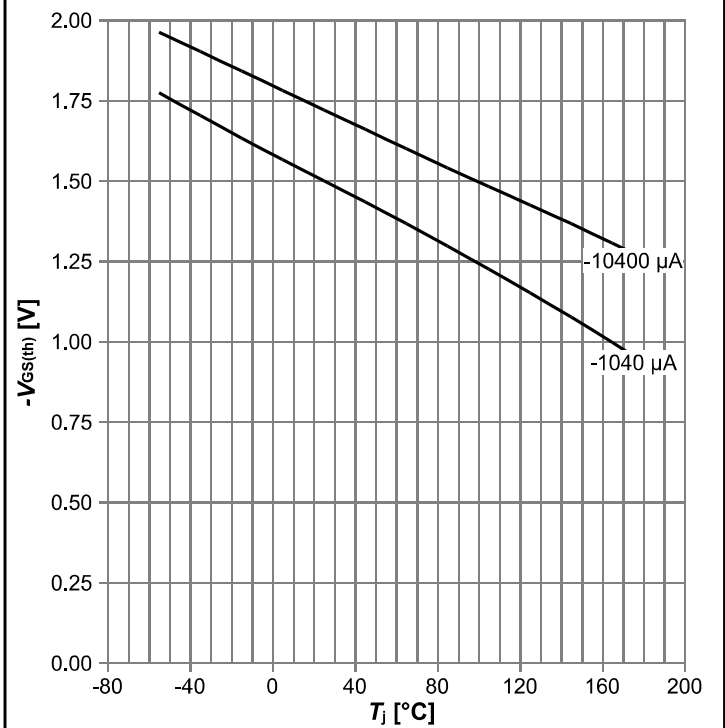
$R_{DS(on)}=f(V_{GS})$, $I_D=-13\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



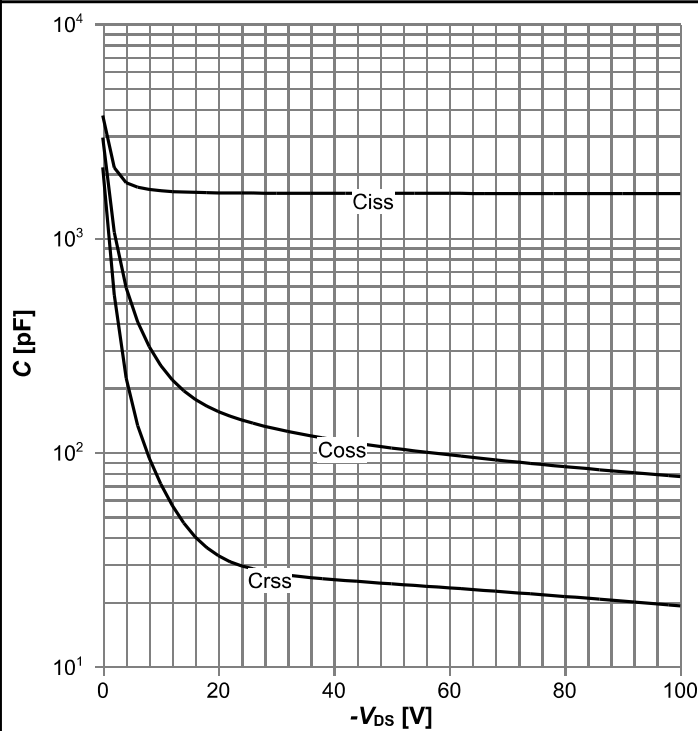
$R_{DS(on)}=f(T_j)$, $I_D=-13$ A, $V_{GS}=-10$ V

Diagram 10: Typ. gate threshold voltage



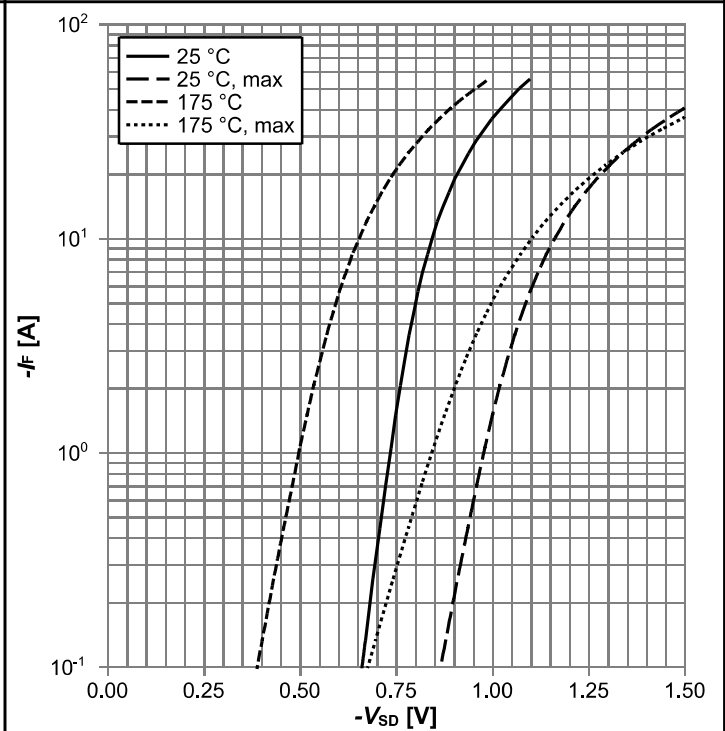
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



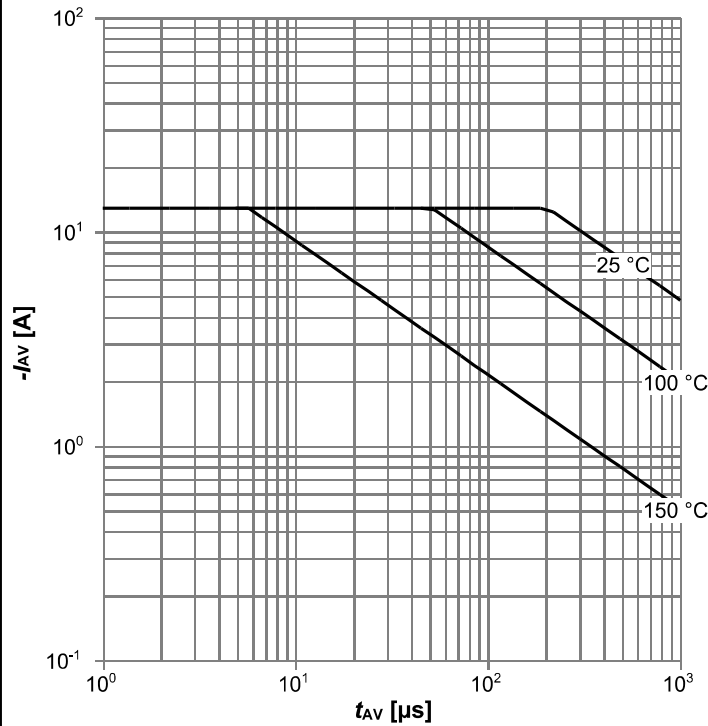
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



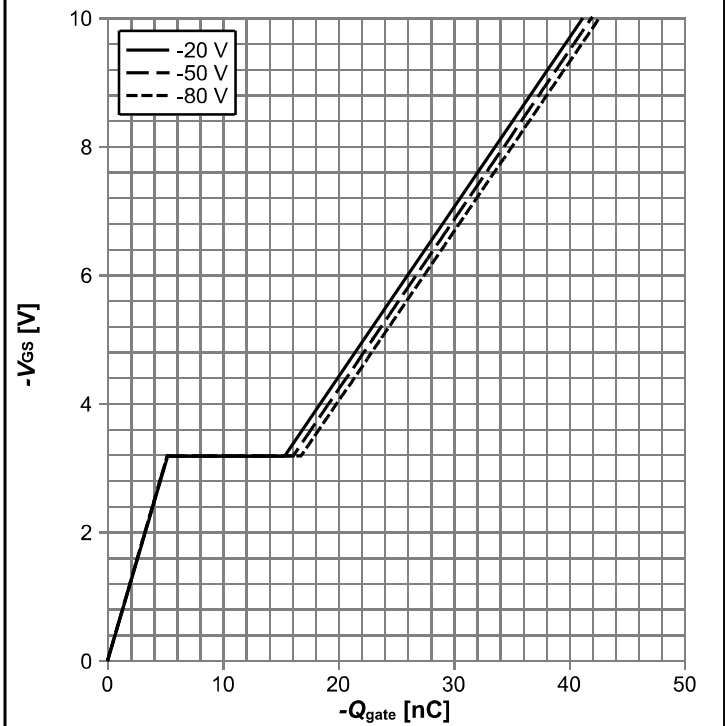
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



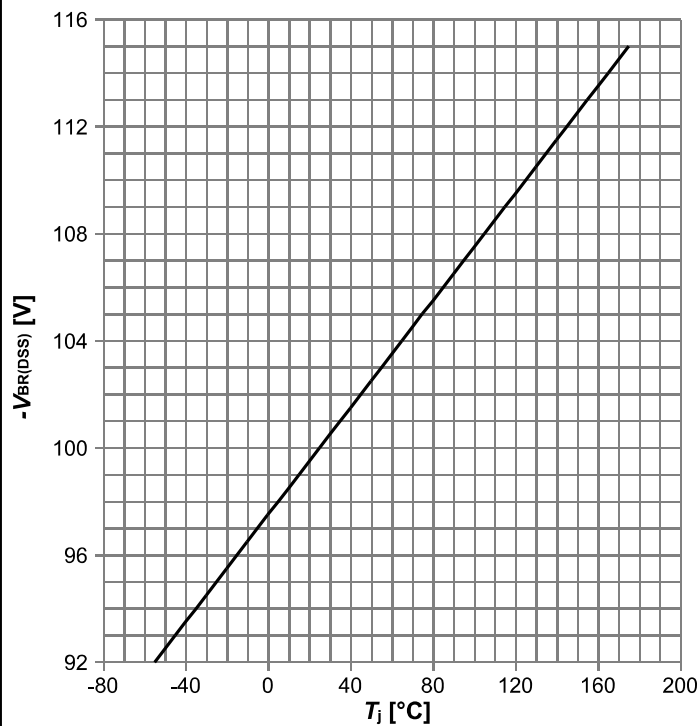
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



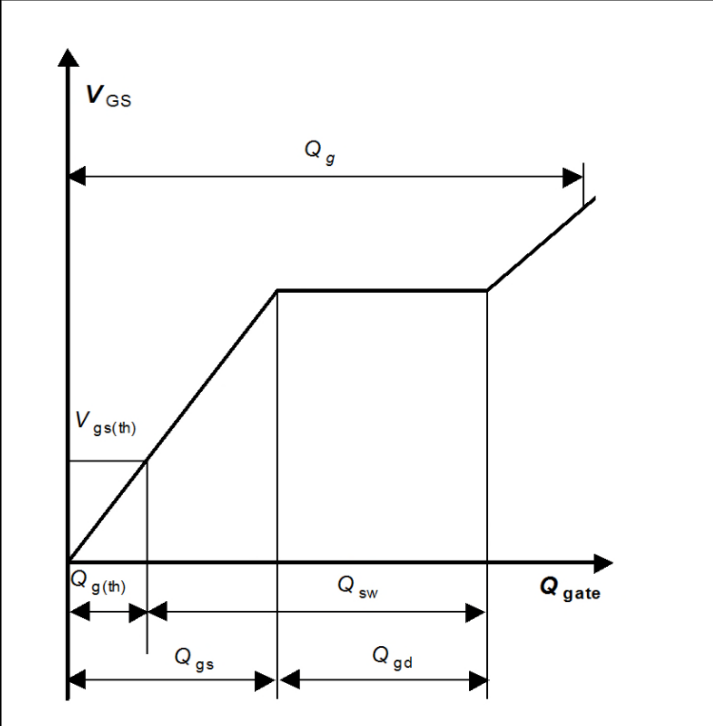
$V_{GS}=f(Q_{gate}), I_D=-13 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

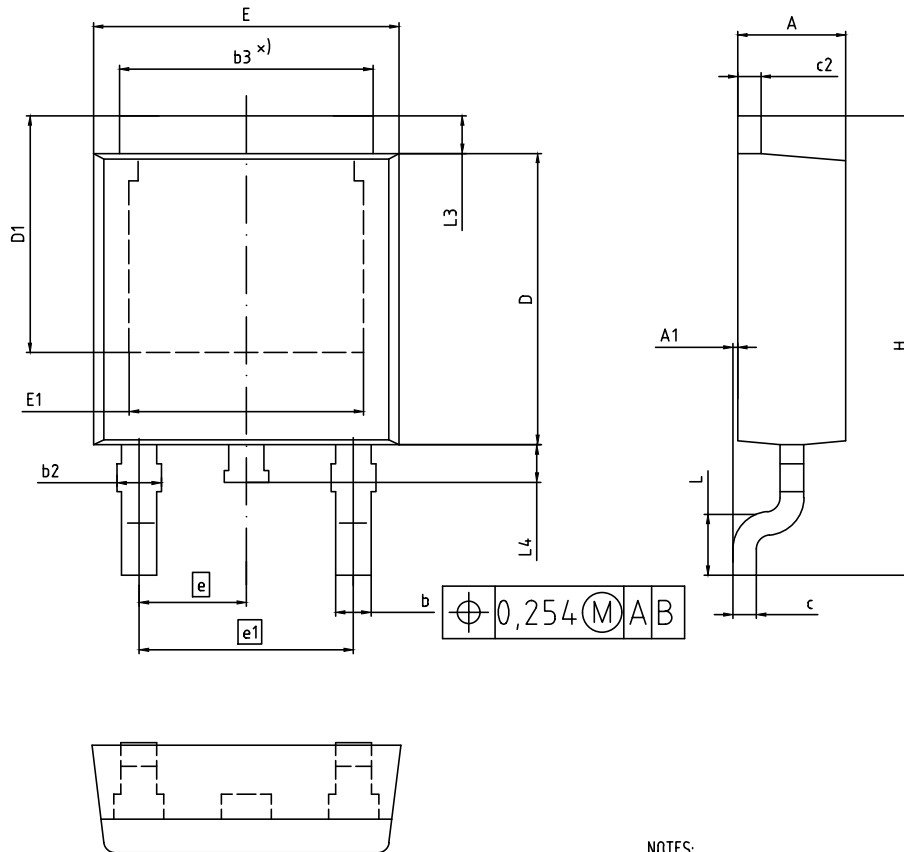


$V_{BR(DSS)}=f(T_j); I_D=-1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



NOTES:

1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2,16	2,41	0,085	0,095
A1	0,00	0,15	0,000	0,006
b	0,64	0,89	0,025	0,035
b2	0,65	1,15	0,026	0,045
b3	4,95	5,50	0,195	0,217
c	0,46	0,61	0,018	0,024
c2	0,40	0,98	0,016	0,039
D	5,97	6,22	0,235	0,245
D1	5,02	5,84	0,198	0,230
E	6,35	6,73	0,250	0,265
E1	4,32	5,21	0,185	0,205
e	2,29 (BSC)		0,090 (BSC)	
e1	4,57 (BSC)		0,180 (BSC)	
N	3		3	
H	9,40	10,48	0,370	0,413
L	1,18	1,78	0,046	0,070
L3	0,89	1,27	0,035	0,050
L4	0,51	1,02	0,020	0,040

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EUROPEAN PROJECTION
ISSUE DATE 05-02-2016
REVISION 06

Figure 1 Outline PG-T0252-3, dimensions in mm/inches

Revision History

IPD18DP10LM

Revision: 2021-05-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-05-10	Release of final version

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