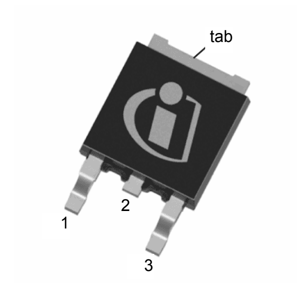
MOSFET

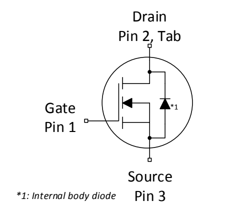
650V CoolMOS™ C7 Power Device

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.

DPAK





Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to lowest in market FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g
- Best in class $R_{DS(on)}$ in TO220/TO247/DPAK and D2PAK
- Easy to use/drive
- Pb-free plating, halogen free mold compound

Benefits

- Enabling higher system efficiency
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures

Potential applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	225	mΩ
$Q_{g.typ}$	20	nC
$I_{D,pulse}$	41	A
E_{oss}@400V	2.3	µJ
Body diode di/dt	55	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPD65R225C7	PG-TO252-3	65C7225	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	11 7	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	41	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	48	mJ	I_D=4.8A; V_{DD}=50V
Avalanche energy, repetitive	E_{AR}	-	-	0.24	mJ	I_D=4.8A; V_{DD}=50V
Avalanche current, single pulse	I_{AS}	-	-	4.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	63	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	11	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	41	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	1	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed	di_f/dt	-	-	55	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.99	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.24mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=650, V_{GS}=0V, T_j=25°C V_{DS}=650, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.199 0.478	0.225 -	Ω	V_{GS}=10V, I_D=4.8A, T_j=25°C V_{GS}=10V, I_D=4.8A, T_j=150°C
Gate resistance	R_G	-	1.2	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	996	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	14	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	29	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	313	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.8A, R_G=10Ω
Rise time	t_r	-	6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.8A, R_G=10Ω
Turn-off delay time	$t_{d(off)}$	-	48	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.8A, R_G=10Ω
Fall time	t_f	-	10	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=4.8A, R_G=10Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	6	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	20	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V

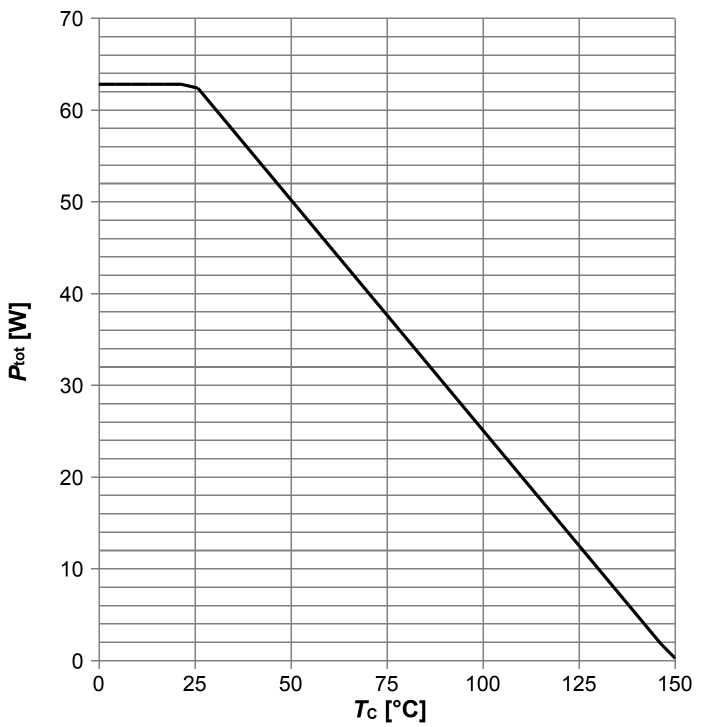
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=4.8A, T_j=25°C
Reverse recovery time	t_{rr}	-	890	-	ns	V_R=400V, I_F=11A, di_F/dt=55A/µs
Reverse recovery charge	Q_{rr}	-	6	-	µC	V_R=400V, I_F=11A, di_F/dt=55A/µs
Peak reverse recovery current	I_{rrm}	-	16	-	A	V_R=400V, I_F=11A, di_F/dt=55A/µs

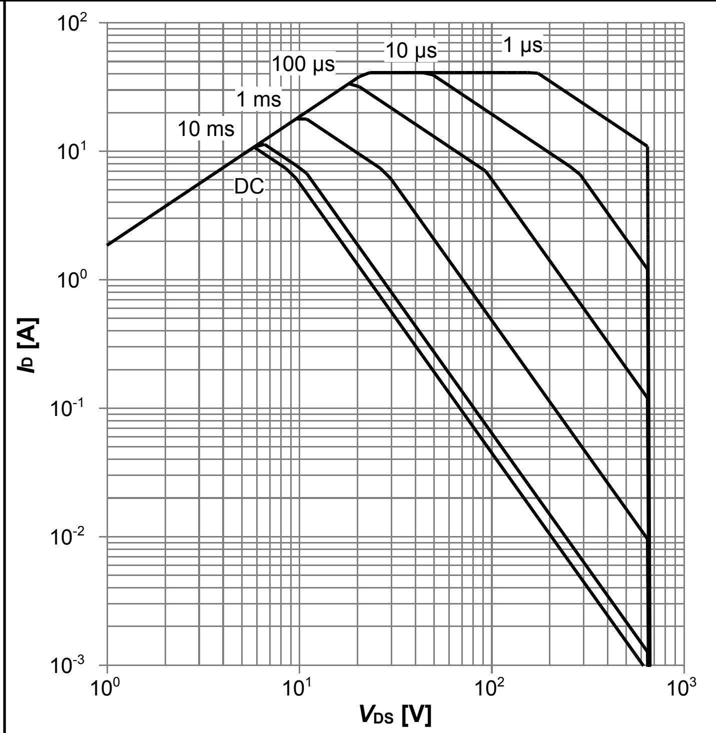
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



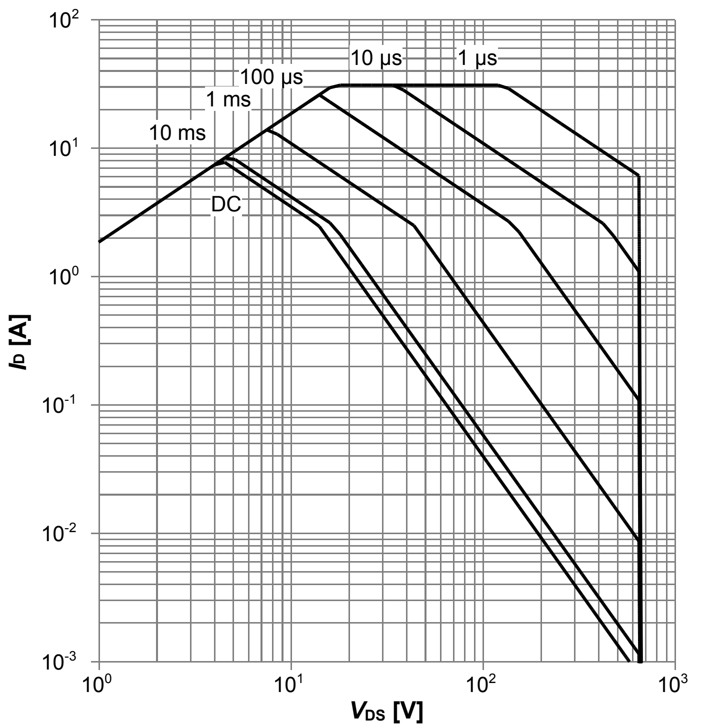
P_{tot}=f(T_C)

Diagram 2: Safe operating area



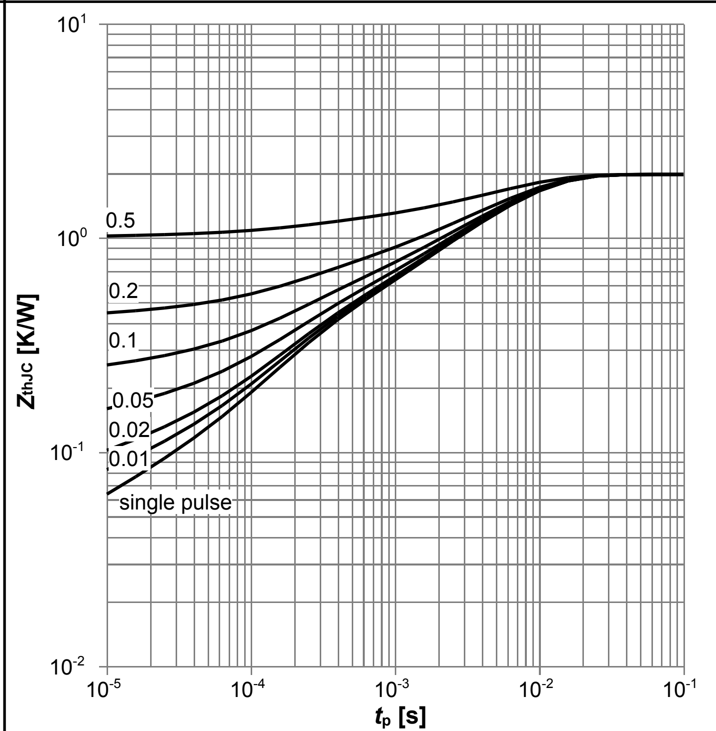
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



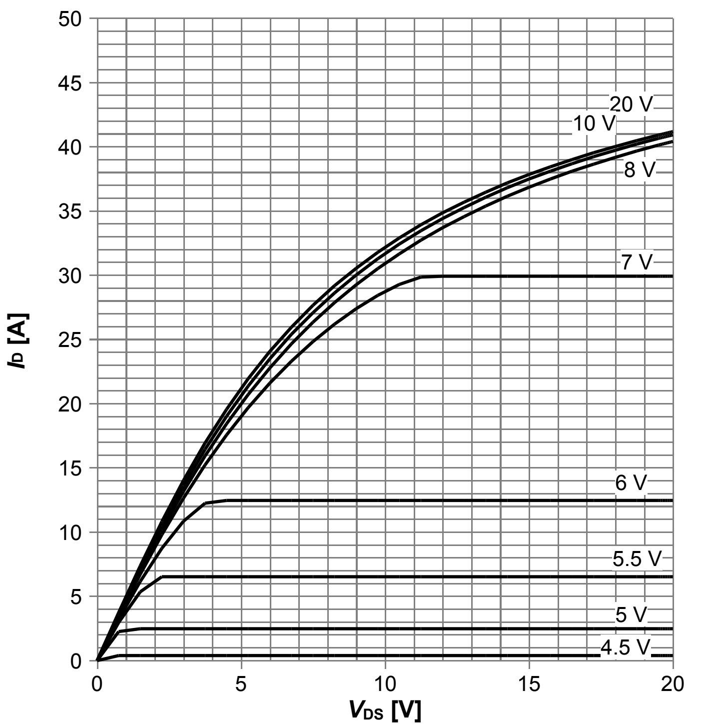
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



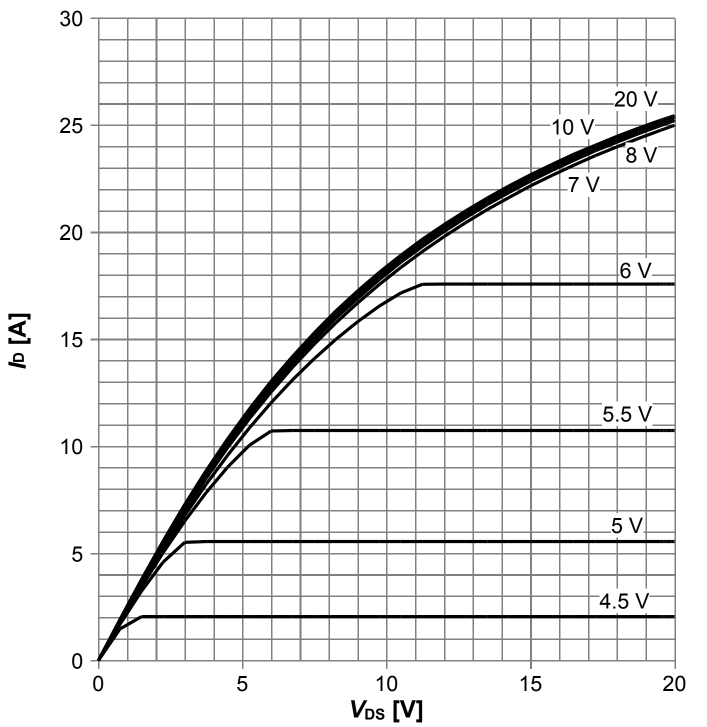
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



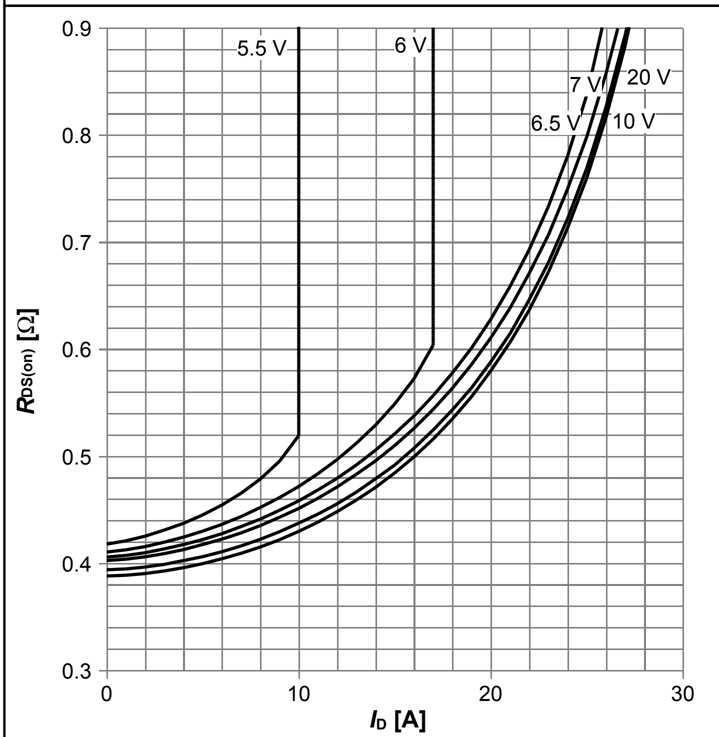
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



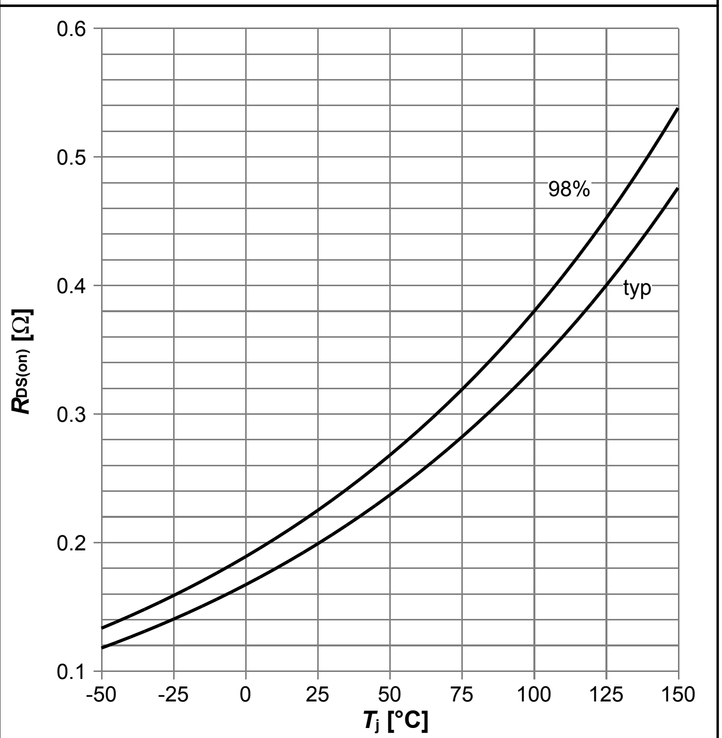
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



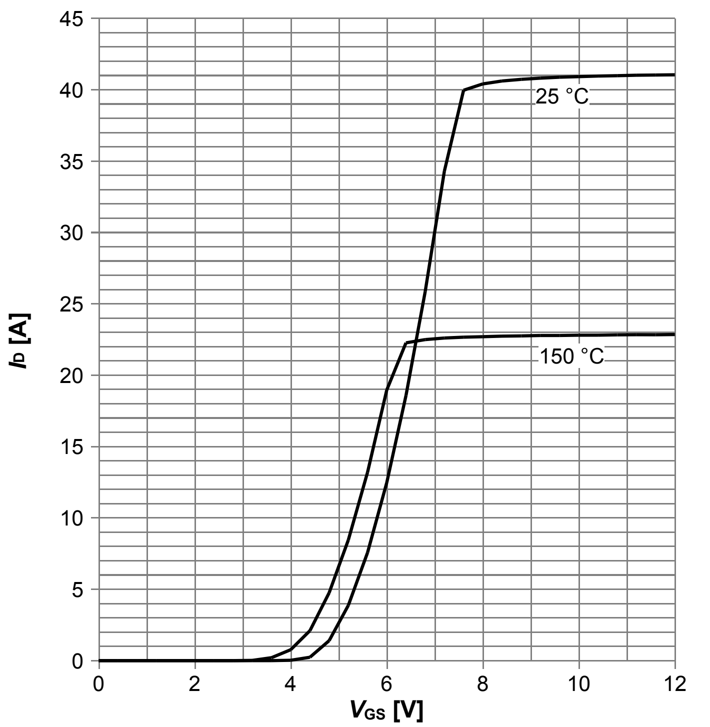
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



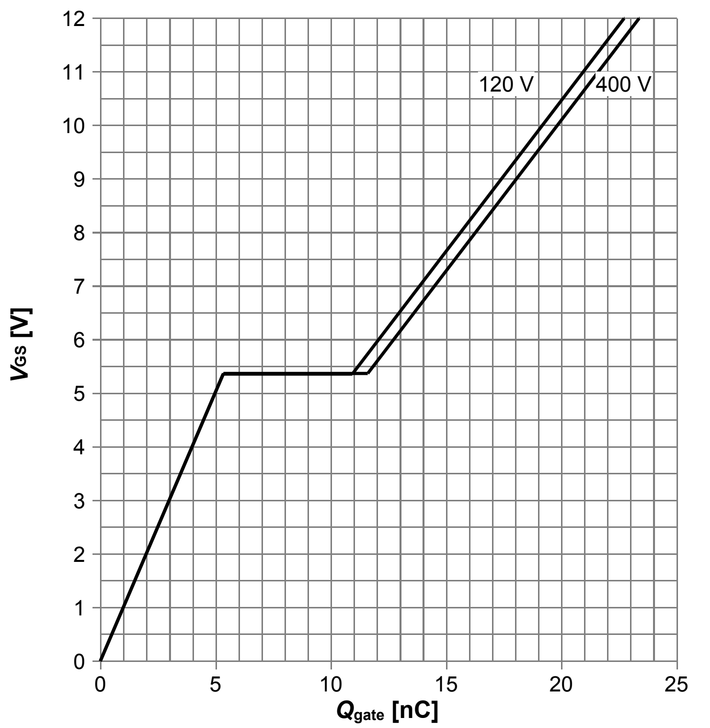
$R_{DS(on)}$=f(T_j); I_D=4.8 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



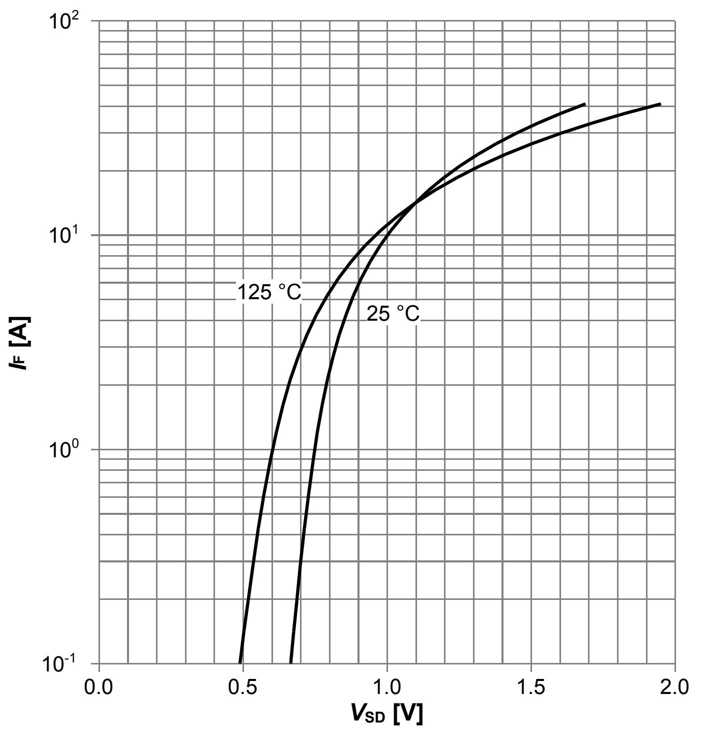
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



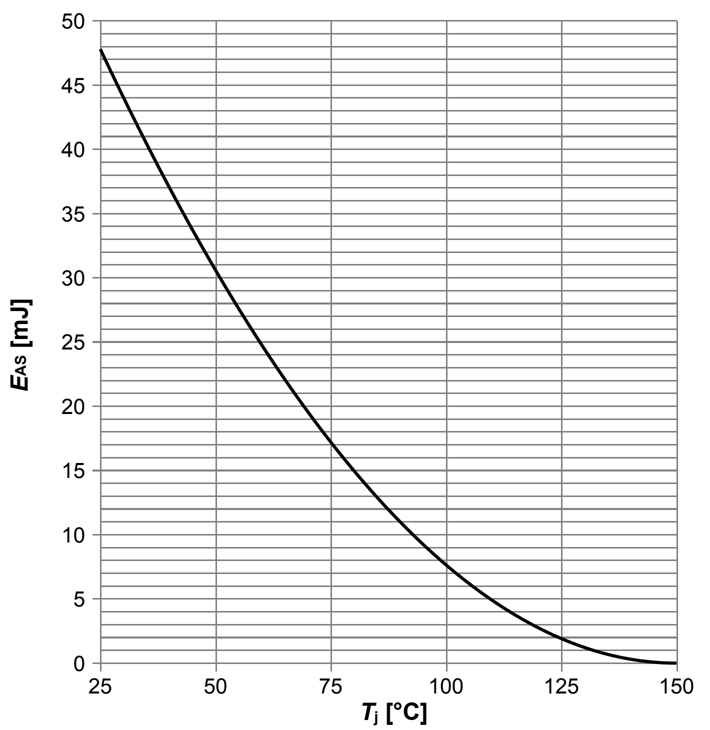
V_{GS}=f(Q_{gate}); I_D=4.8 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



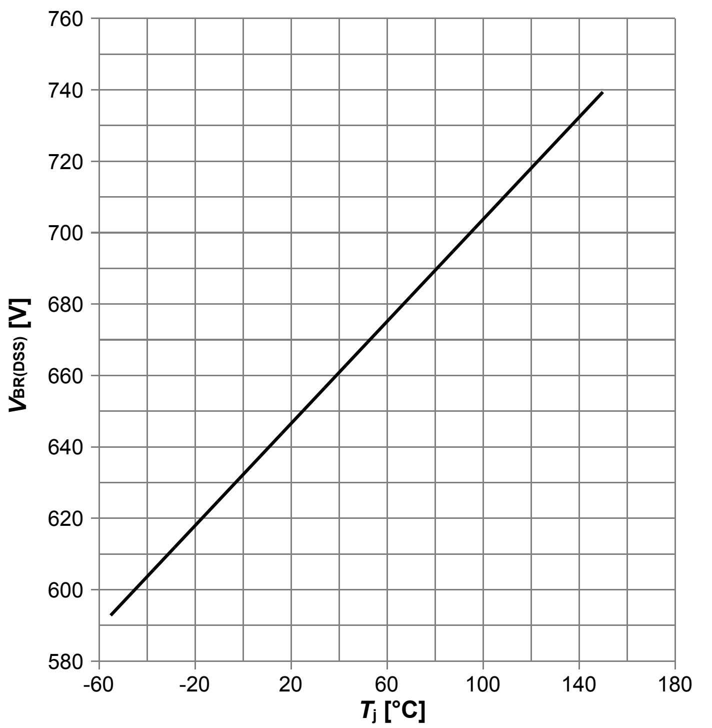
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



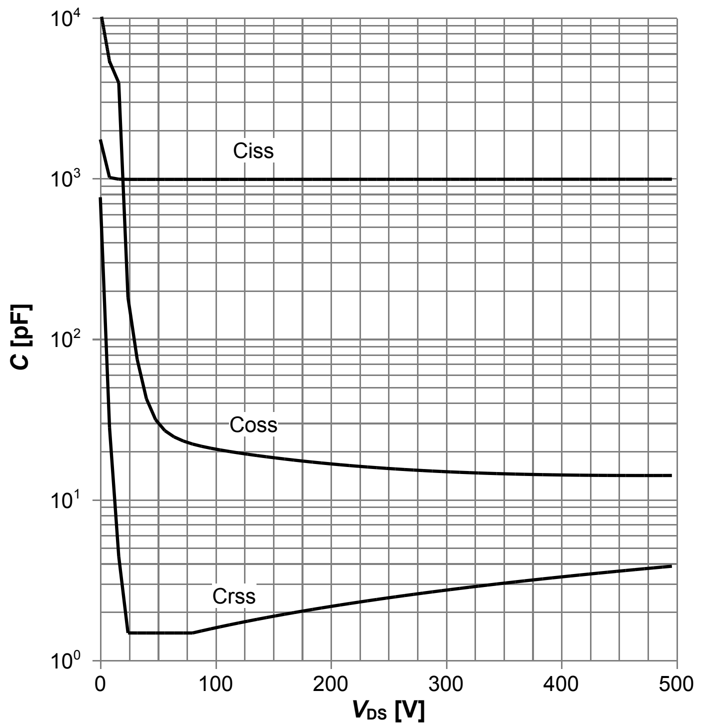
E_{AS}=f(T_j); I_D=4.8 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



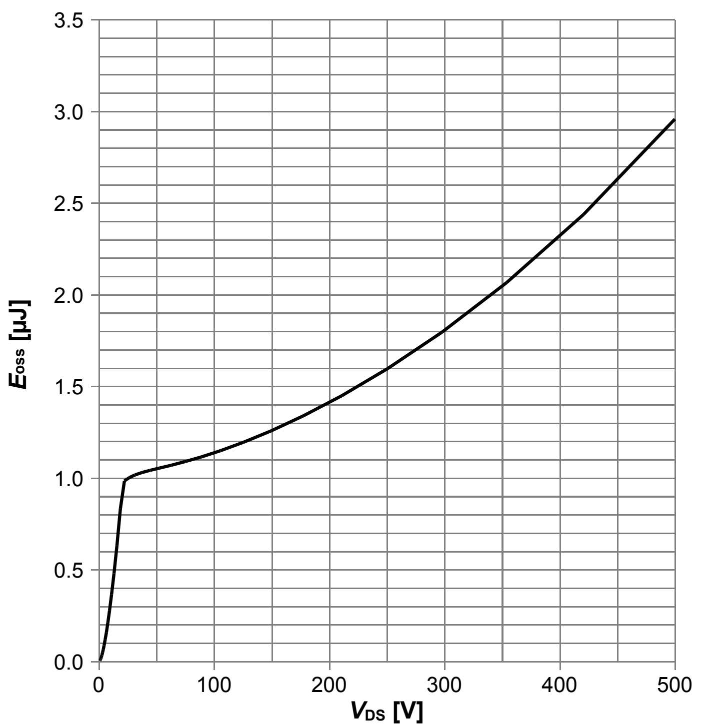
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

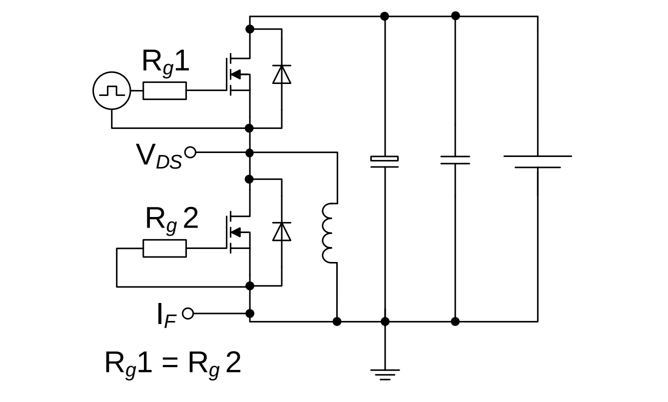


E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform



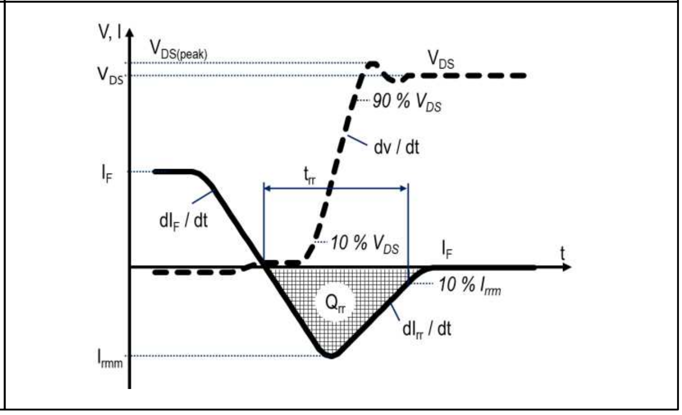
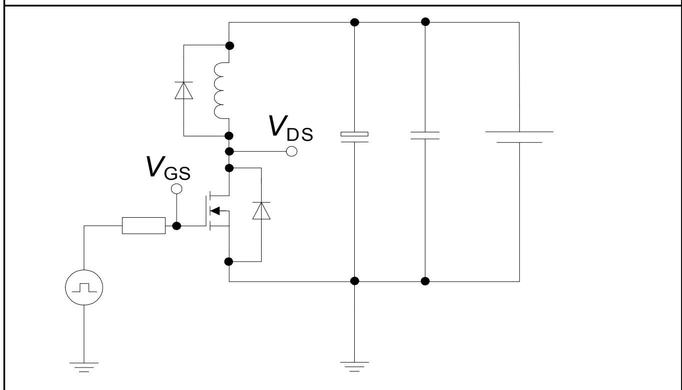


Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform



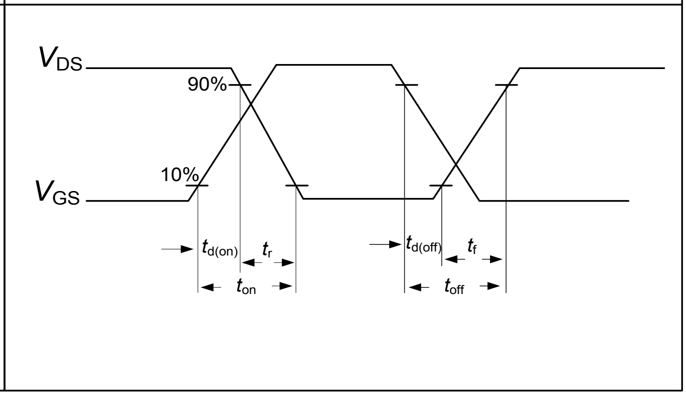
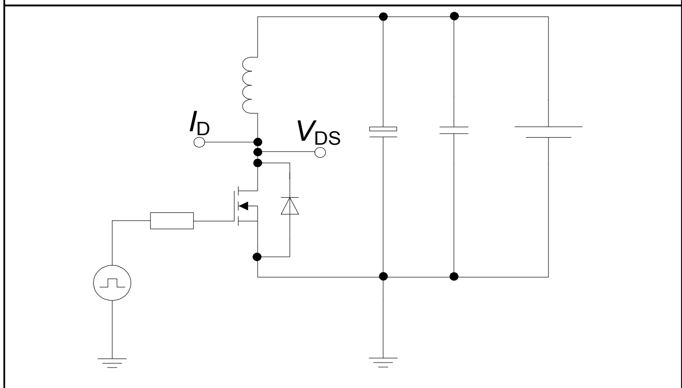
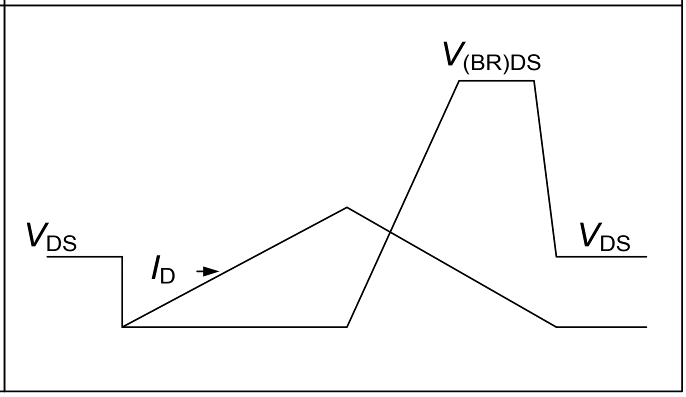


Table 10 Unclamped inductive load

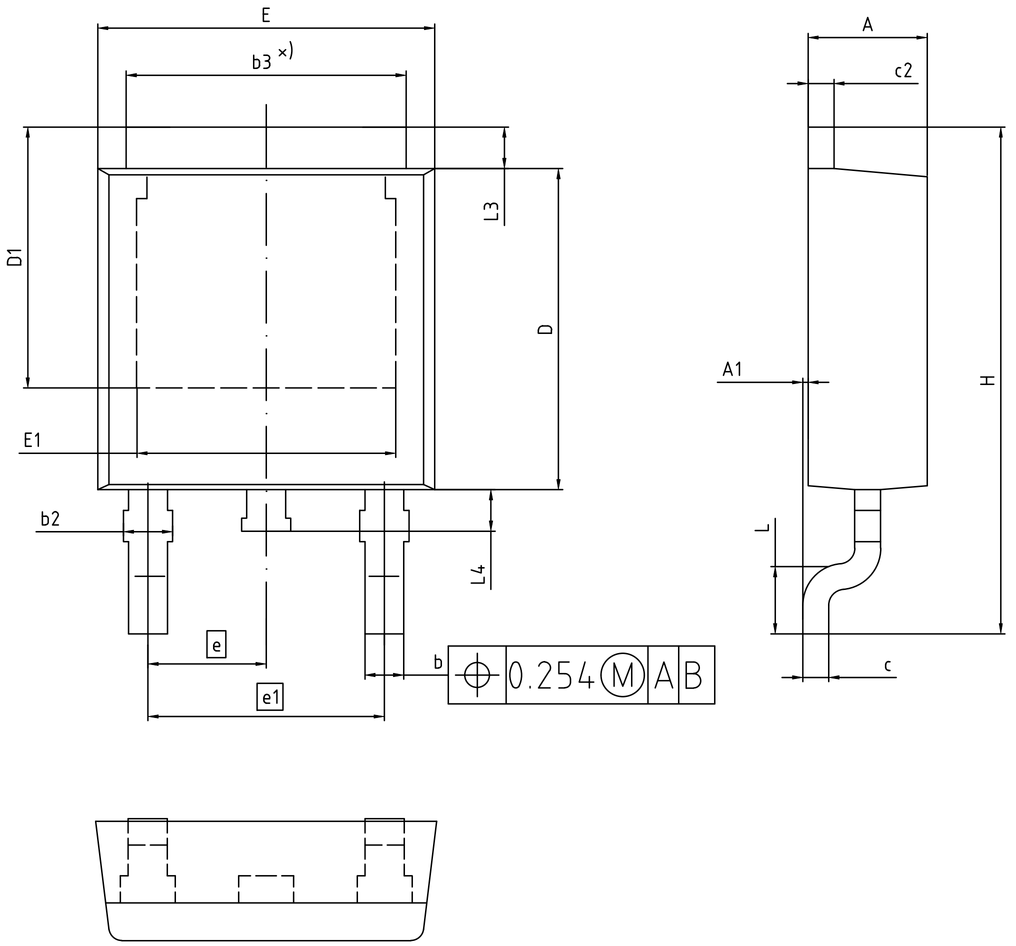
Unclamped inductive load test circuit	Unclamped inductive waveform





6 Package Outlines

PG-TO252-3 (DPAK)



ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4,95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

DOCUMENT NO. Z8B00003328
REVISION 07
SCALE: 10:1 0 1 2mm
EUROPEAN PROJECTION
ISSUE DATE 01.04.2020

Figure 1 Outline PG-TO252-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPD65R225C7

Revision: 2020-05-26, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-04-18	Release of final version
2.1	2020-05-26	Updated package/symbol drawing, and product validation

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