

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ E6 650V

650V CoolMOS™ E6 Power Transistor
IPD65R250E6

Data Sheet

Rev. 2.2
Final

Industrial & Multimarket

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ E6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

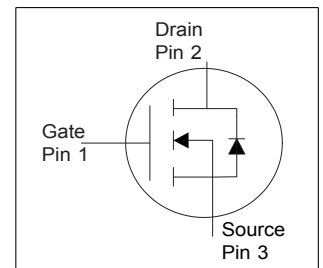
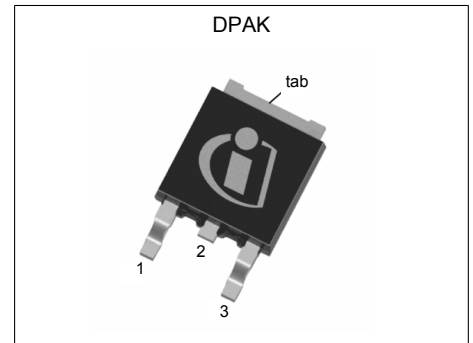


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	0.25	Ω
Q_g,typ	45	nC
$I_D,pulse$	46	A
$E_{oss} @ 400V$	3.7	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPD65R250E6	PG-TO 252	65E6250	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			16.1	A	$T_C = 25^\circ\text{C}$
				11.3		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			46	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			290	mJ	$I_D = 2.4\text{A}$, $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}			0.44	mJ	$I_D = 2.4\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			2.4	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{Hz}$)
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Continuous diode forward current	I_S			17.9	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			46	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed	di/dt			500	A/ μs	
Power dissipation (non FullPAK)	P_{tot}			208	W	$T_C = 25^\circ\text{C}$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j,max}$, identical low and high side switch with same R_g

3 Thermal characteristics

Table 3 Thermal characteristics DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			0.6	°C/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	°C/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS} = V_{GS}, I_D = 0.4mA$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			10			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.230	0.25	Ω	$V_{GS} = 10V, I_D = 4.4A, T_j = 25^\circ C$
			0.590			$V_{GS} = 10V, I_D = 4.4A, T_j = 150^\circ C$
Gate resistance	R_G		7		Ω	$f = 1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		950		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	C_{oss}		60			
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		40		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		183		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 480V$
Turn-on delay time	$t_{d(on)}$		11		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 6.6A, R_G = 3.4\Omega$
Rise time	t_r		9			
Turn-off delay time	$t_{d(off)}$		76			
Fall time	t_f		9			

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		5		nC	$V_{DD} = 480V, I_D = 6.6A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		24			
Gate charge total	Q_g		45			
Gate plateau voltage	$V_{plateau}$		5.5			

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 6.6A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		260		ns	$V_R = 400V, I_F = 6.6A,$ $di_F/dt = 100A/\mu s$
Reverse recovery charge	Q_{rr}		2.4		μC	
Peak reverse recovery current	I_{rrm}		18		A	

5 Electrical characteristics diagrams

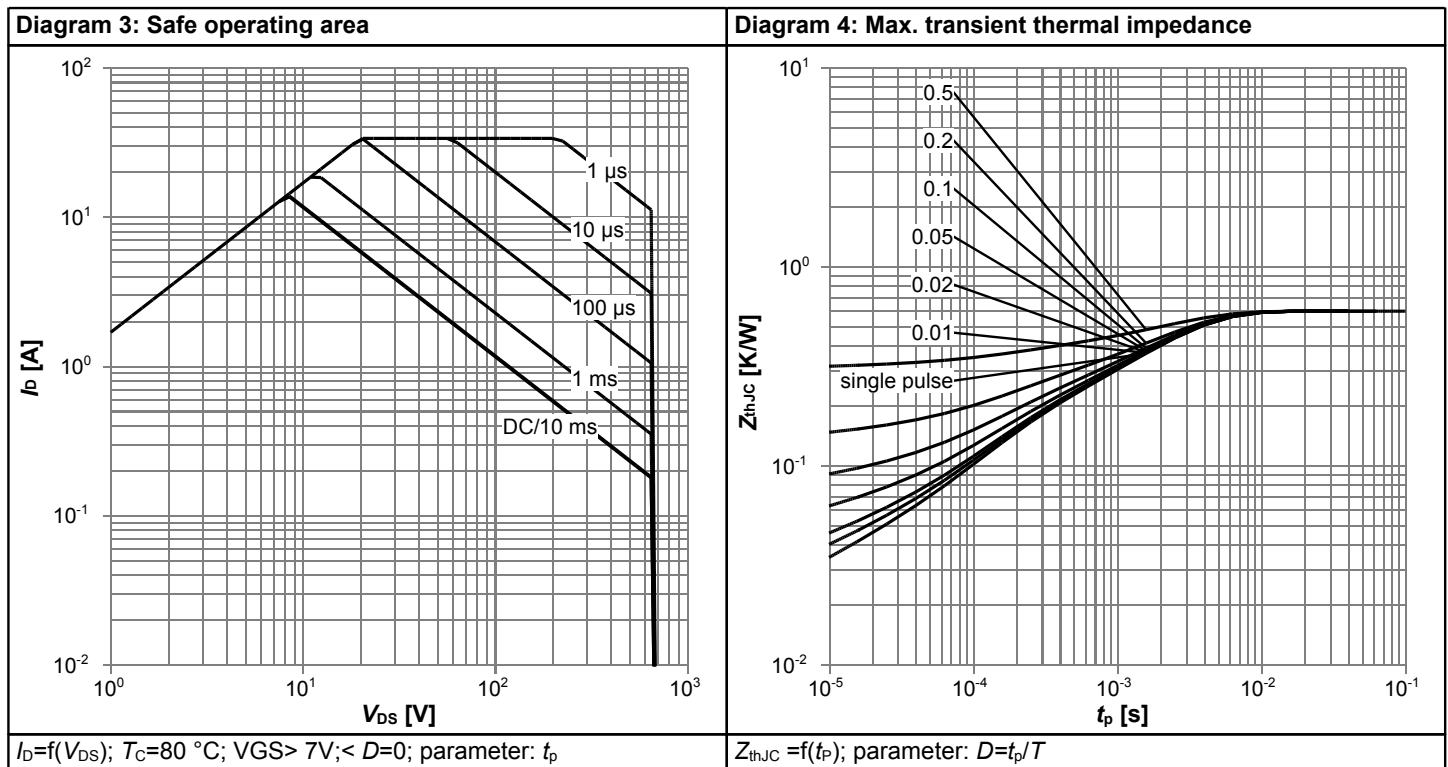
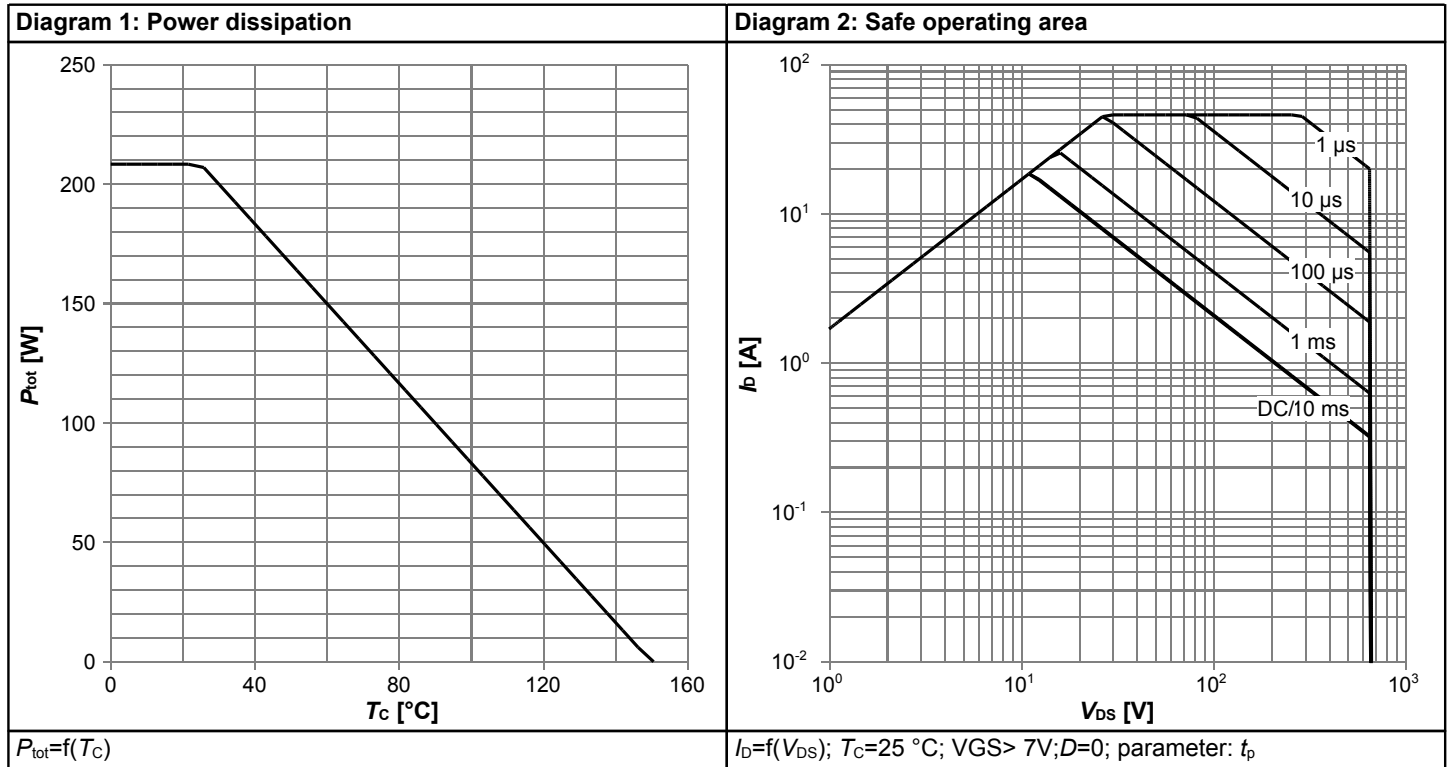
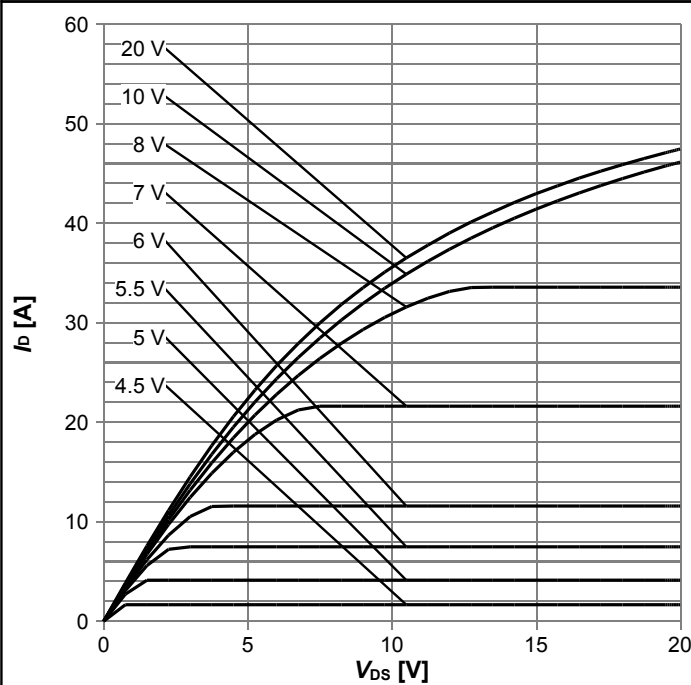
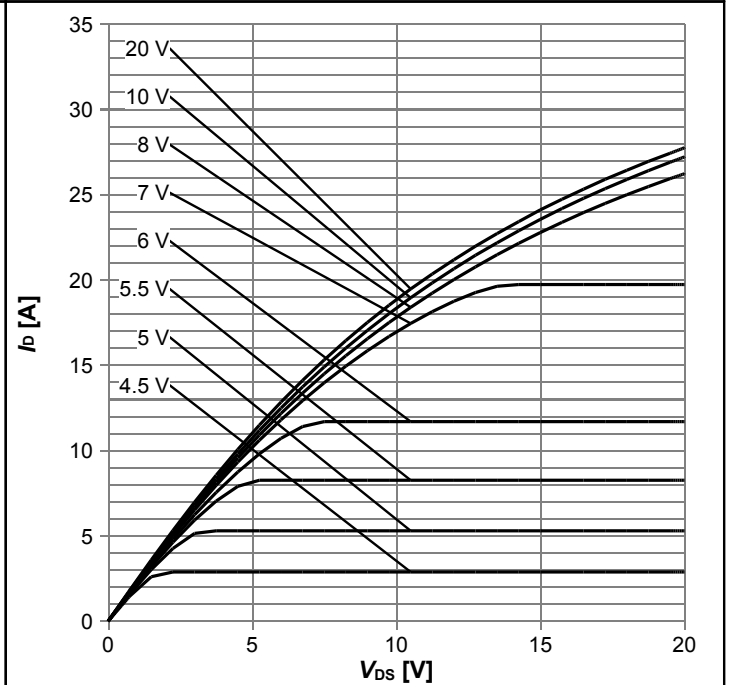


Diagram 5: Typ. output characteristics



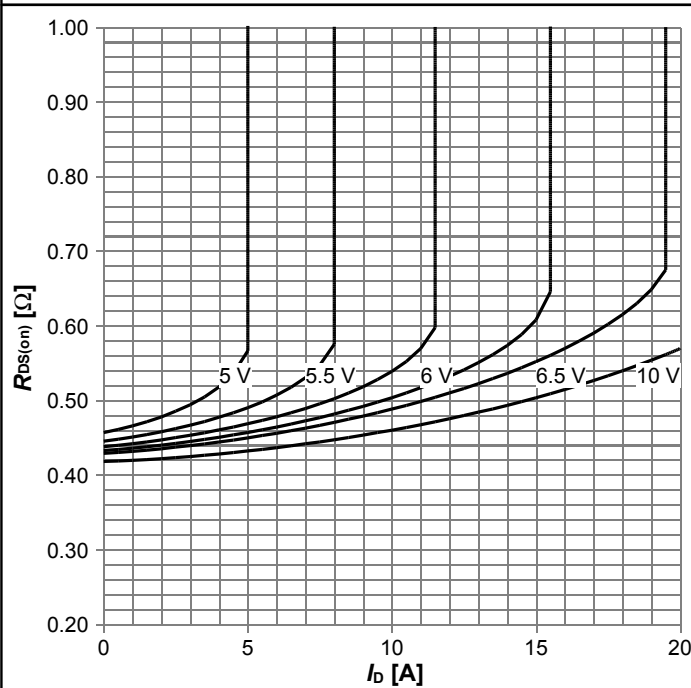
$I_D=f(V_{DS}); T_j=25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. output characteristics



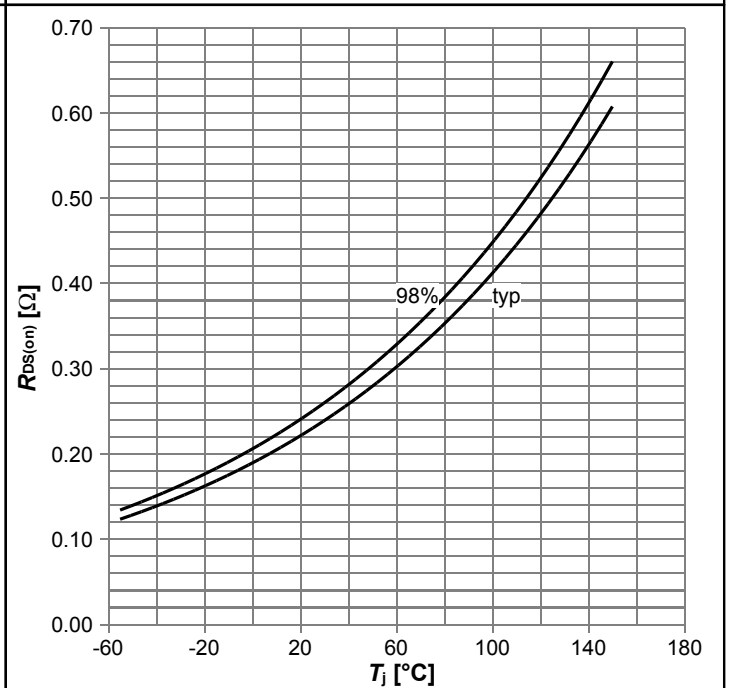
$I_D=f(V_{DS}); T_j=125\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



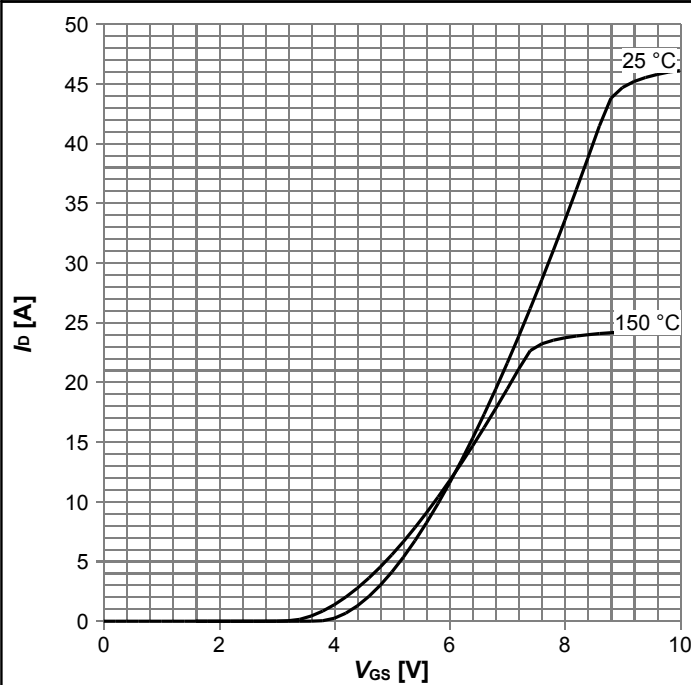
$R_{DS(on)}=f(I_D); T_j=125\text{ °C};$ parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



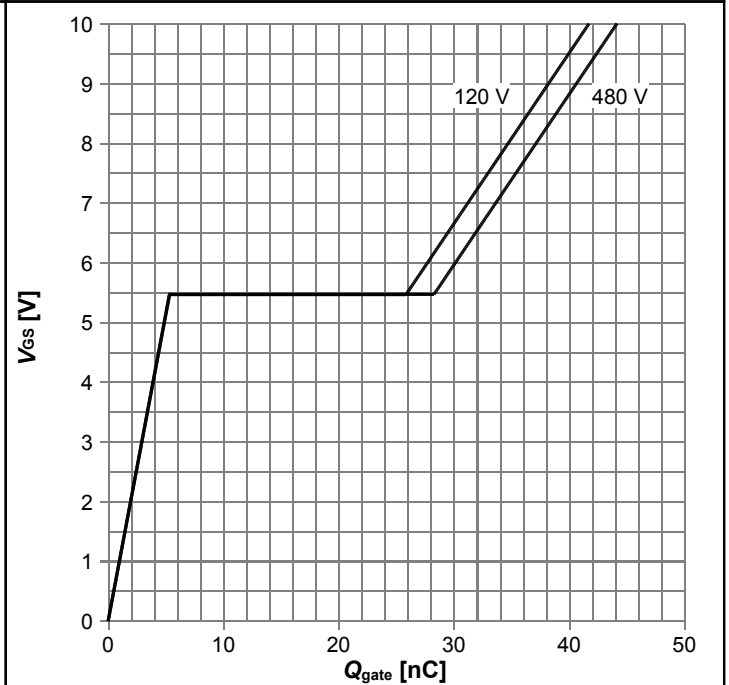
$R_{DS(on)}=f(T_j); I_D=4,4\text{ A}; V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



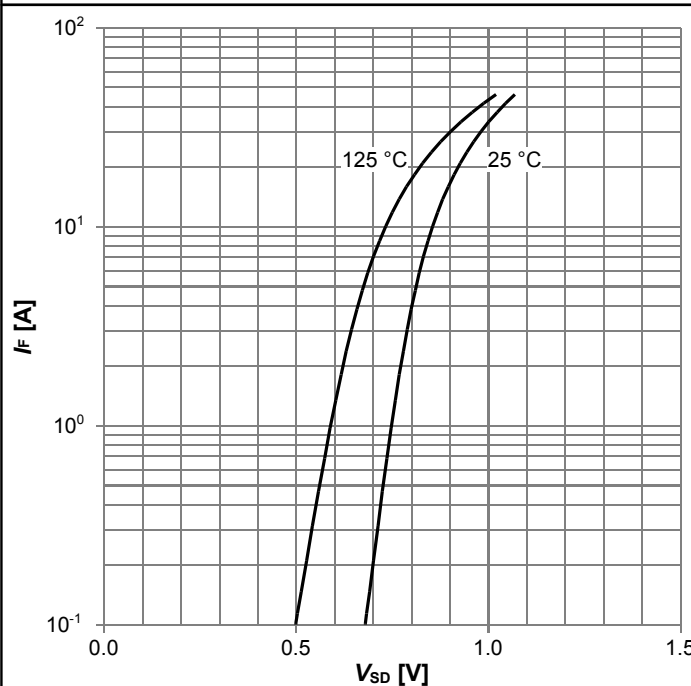
$I_D=f(V_{GS}); |V_{DS}|=20V;$

Diagram 10: Typ. gate charge



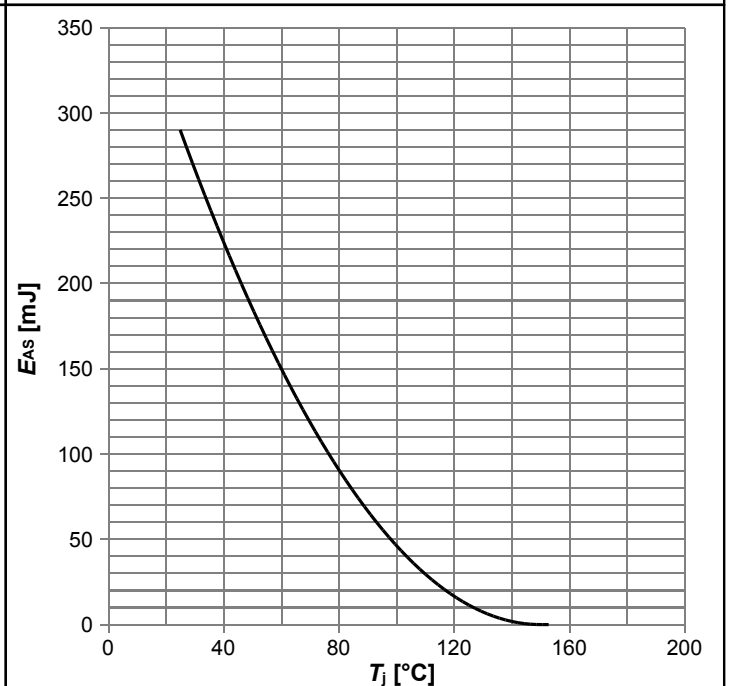
$V_{GS}=f(Q_{gate}); I_D=6.6 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



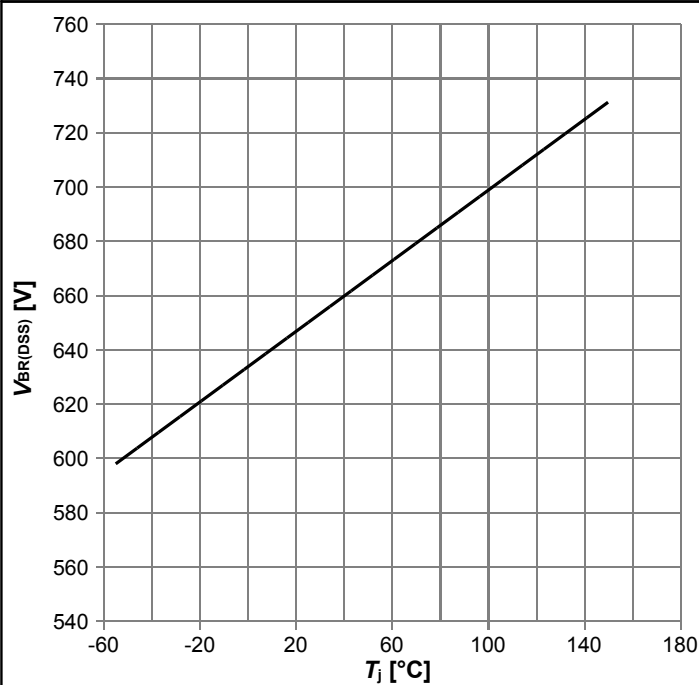
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



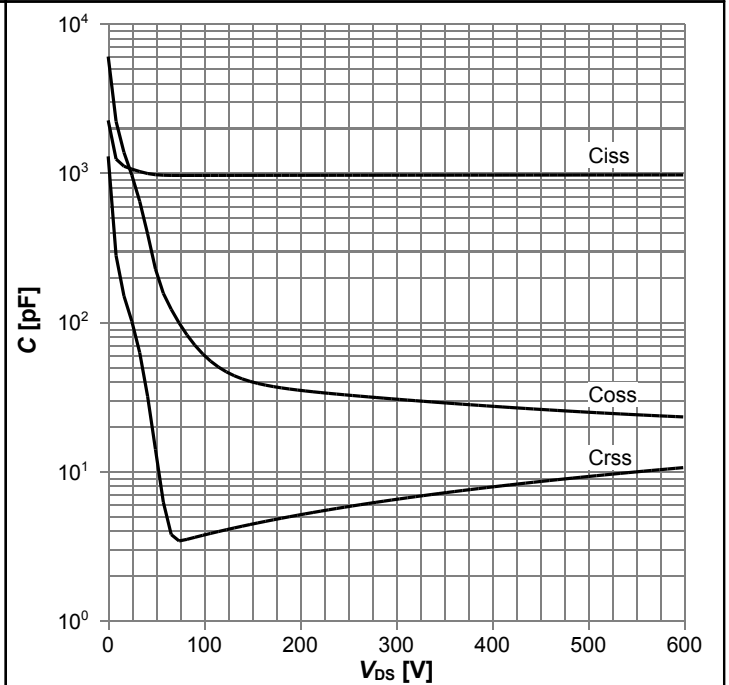
$E_{AS}=f(T_j); I_D=2,4 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



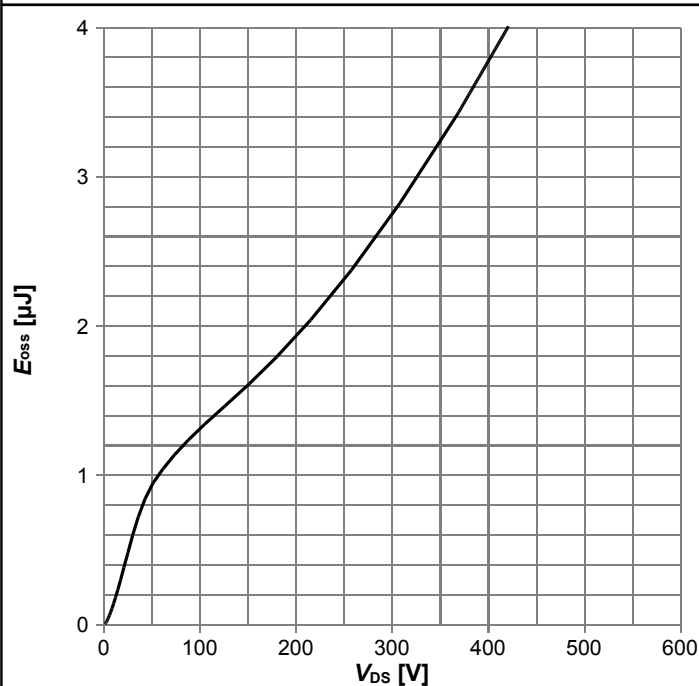
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

6 Test Circuits

Table 8 Diode characteristics

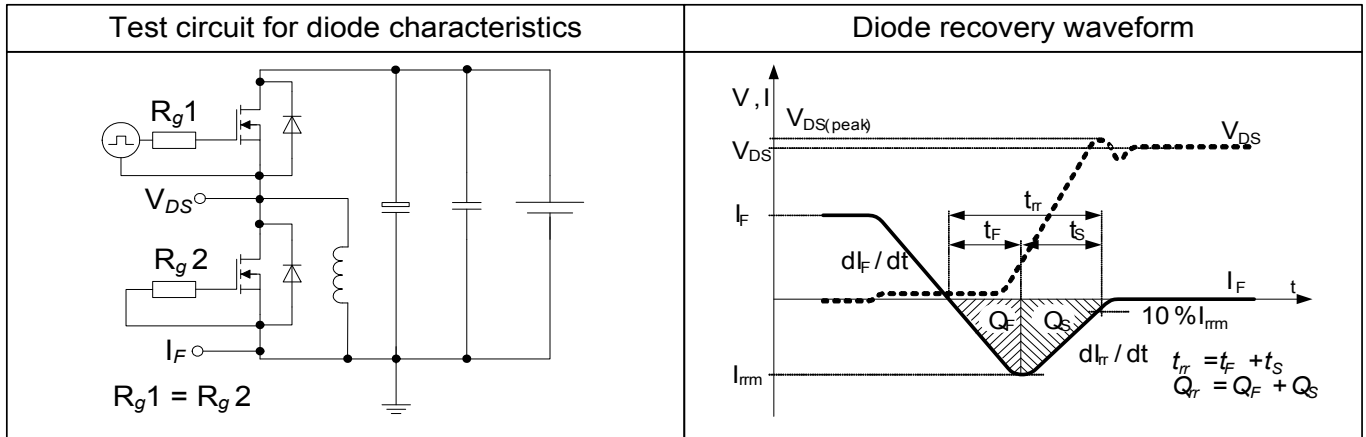


Table 9 Switching times

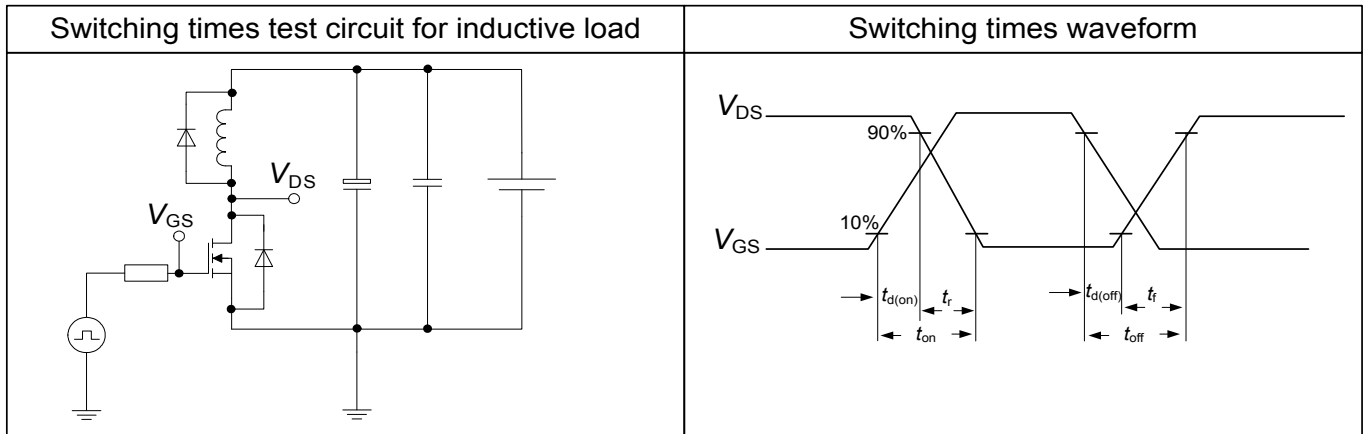
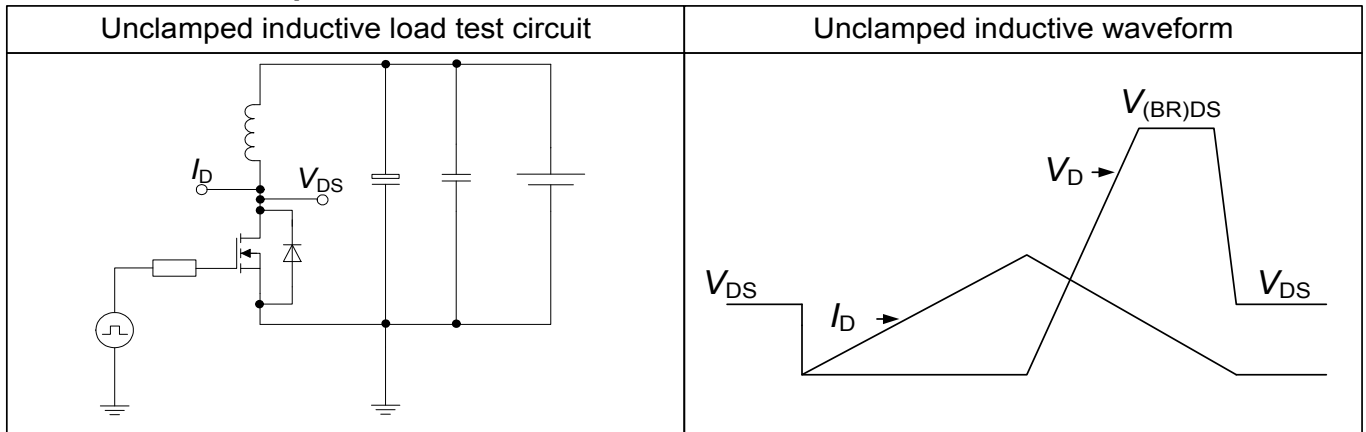


Table 10 Unclamped inductive load



7 Package Outlines

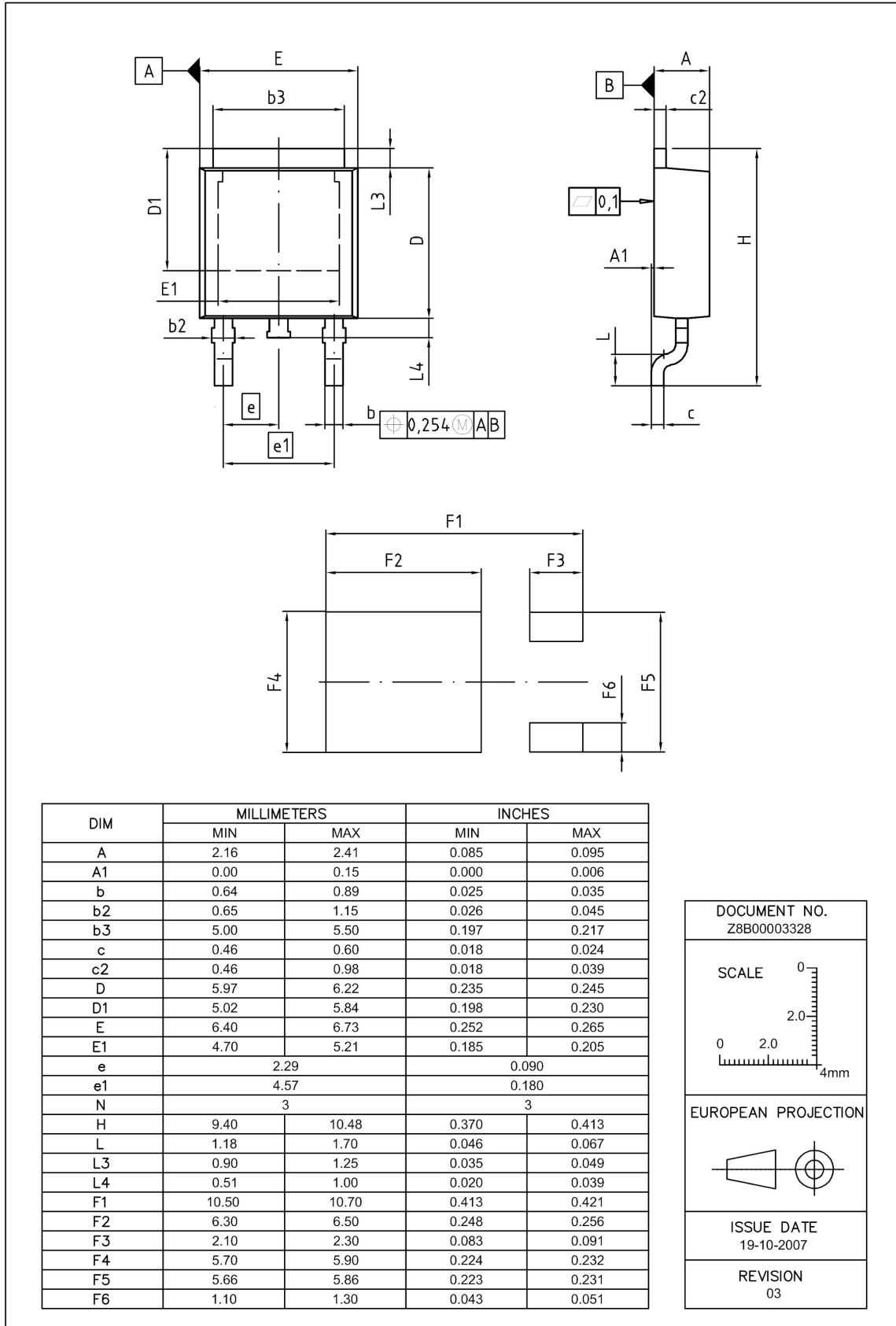


Figure 1 Outline PG-TO 252, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- **IFX C6 Product Brief:** www.infineon.com
- **IFX C6 Portfolio:** www.infineon.com
- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design Tools:** www.infineon.com

Revision History

IPD65R250E6

Revision: 2013-07-30, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2011-07-08	release of final datasheet
2.2	2013-07-30	add halogen free mold compound logo

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