

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CFD2 650V

650V CoolMOS™ CFD2 Power Transistor
IPD65R950CFD

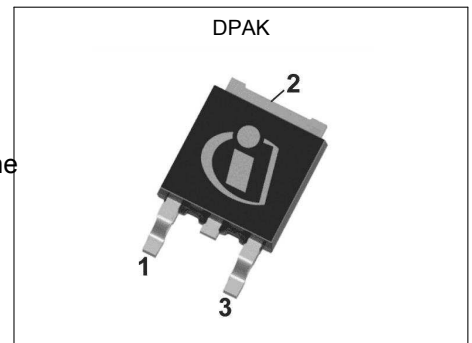
Data Sheet

Rev. 2.2
Final

Industrial & Multimarket

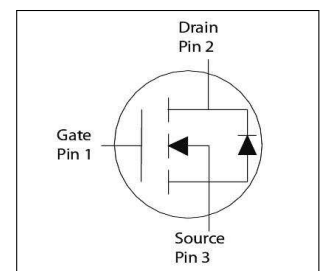
1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.



Features

- Ultra-fast body diode
- Easy to use/drive
- Very high commutation ruggedness
- Pb-free plating, available in Halogen free mold compound^{a)}
- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Fully qualified according to JEDEC for Industrial Applications



Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server and Telecom.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j \max}$	700	V
$R_{DS(on), \max}$	0.95	Ω
Q_g, typ	14.1	nC
I_D, pulse	11	A
$E_{oss} @ 400V$	1.4	μJ
Body diode di/dt	900	A/ μs
Q_{rr}	0.12	μC
t_{rr}	53	ns
I_{rrm}	4	A



Type / Ordering Code	Package	Marking	Related Links
IPD65R950CFD	PG-TO 252	65F6950	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			3.9	A	$T_C = 25^\circ\text{C}$
				2.4		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			11	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			50	mJ	$I_D = 1.0\text{A}$, $V_{DD} = 50\text{V}$ (see table 18)
Avalanche energy, repetitive	E_{AR}			0.10	mJ	$I_D = 1.0\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			1.0	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{Hz}$)
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Continuous diode forward current	I_S			3.9	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			11	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ (see table 16)
Maximum diode commutation speed	di_t/dt			900	A/ μs	
Power dissipation	P_{tot}			36.7	W	$T_C = 25^\circ\text{C}$

¹⁾ Limited by $T_{j,max}$. Maximum

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j,max}$, identical low and high side switch with same R_g

3 Thermal characteristics

Table 3 Thermal characteristics DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			3.4	°C/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	°C/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0\text{V}$, $I_D = 1\text{mA}$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}$, $I_D = 0.2\text{mA}$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 25^\circ\text{C}$
			100			$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 150^\circ\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20\text{V}$, $V_{DS} = 0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$		0.855	0.95	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$, $T_j = 25^\circ\text{C}$
			2.223			$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$, $T_j = 150^\circ\text{C}$
Gate resistance	R_G		8		Ω	$f = 1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		380		pF	$V_{GS} = 0\text{V}$, $V_{DS} = 100\text{V}$, $f = 1\text{MHz}$
Output capacitance	C_{oss}		23		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		16		pF	$V_{GS} = 0\text{V}$, $V_{DS} = 0 \dots 400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		68		pF	$I_D = \text{constant}$, $V_{GS} = 0\text{V}$, $V_{DS} = 0 \dots 400\text{V}$
Turn-on delay time	$t_{d(on)}$		9		ns	$V_{DD} = 400\text{V}$, $V_{GS} = 13\text{V}$, $I_D = 2.2\text{A}$, $R_G = 10.2\Omega$ (see table 17)
Rise time	t_r		6.5		ns	
Turn-off delay time	$t_{d(off)}$		43		ns	
Fall time	t_f		13.8		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		2.5		nC	$V_{DD} = 480\text{V}$, $I_D = 2.2\text{A}$, $V_{GS} = 0 \text{ to } 10\text{V}$
Gate to drain charge	Q_{gd}		8		nC	
Gate charge total	Q_g		14.1		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 2.2A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		53		ns	$V_R = 400V, I_F = 2.2A,$ $di_F/dt = 100A/\mu s$ (see table 16)
Reverse recovery charge	Q_{rr}		0.12		μC	
Peak reverse recovery current	I_{rrm}		4		A	

5 Electrical characteristics diagrams

Table 8

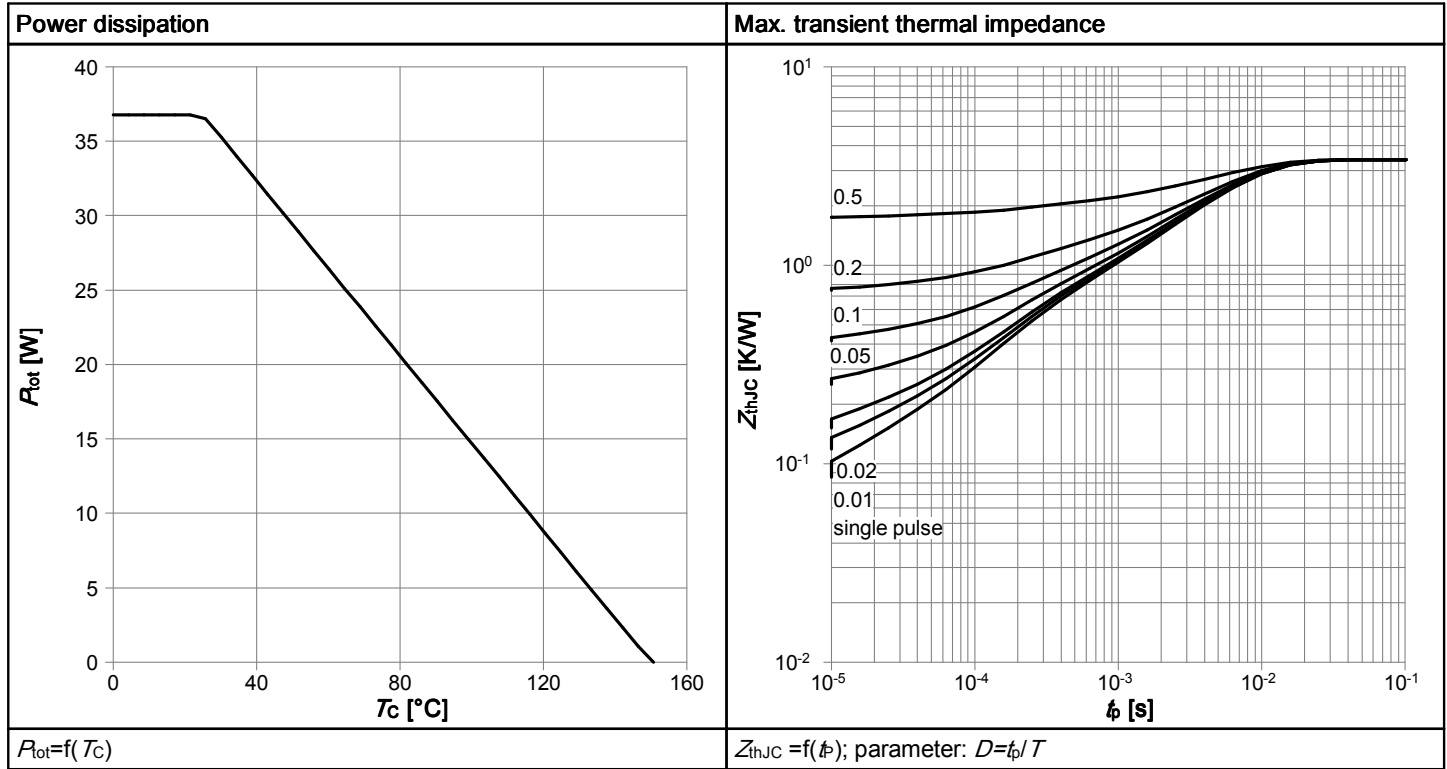


Table 9

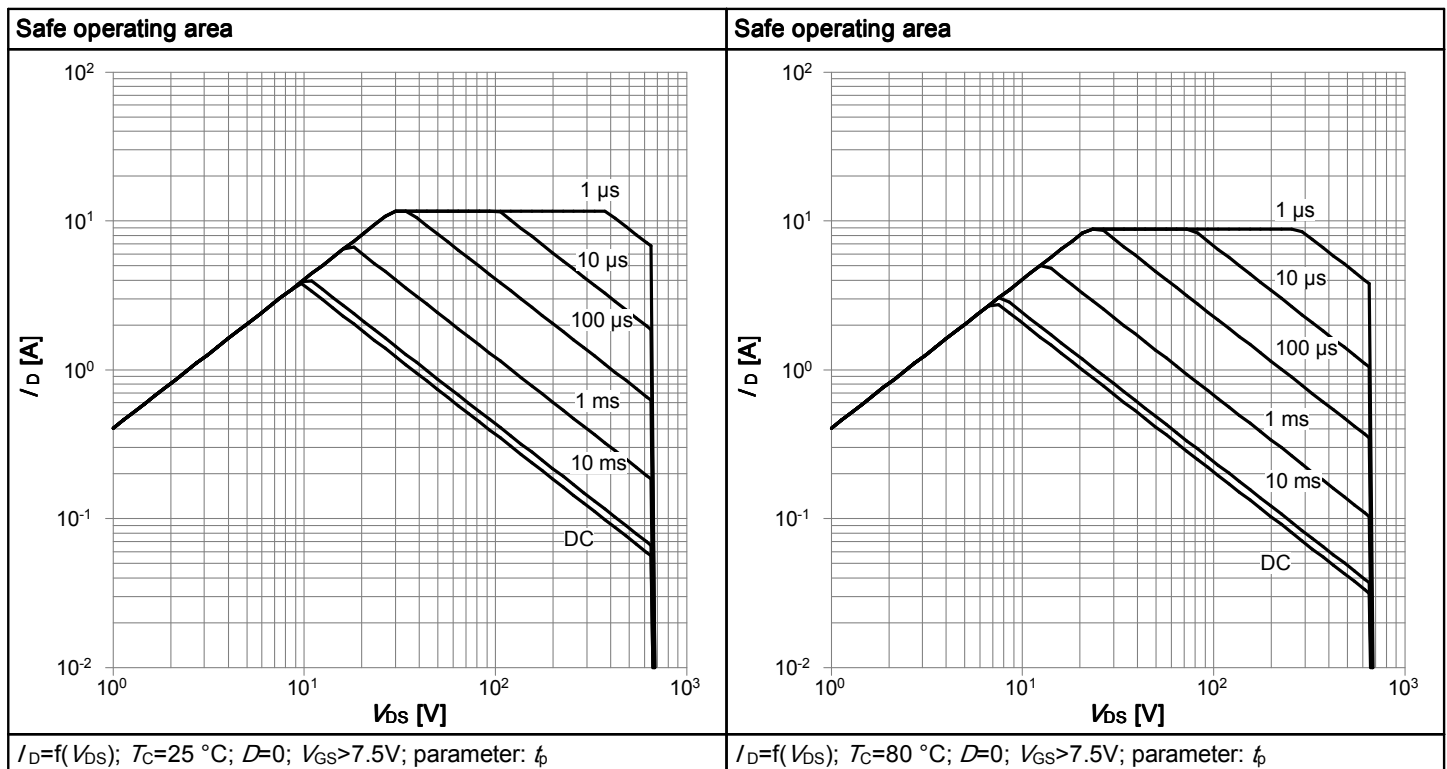


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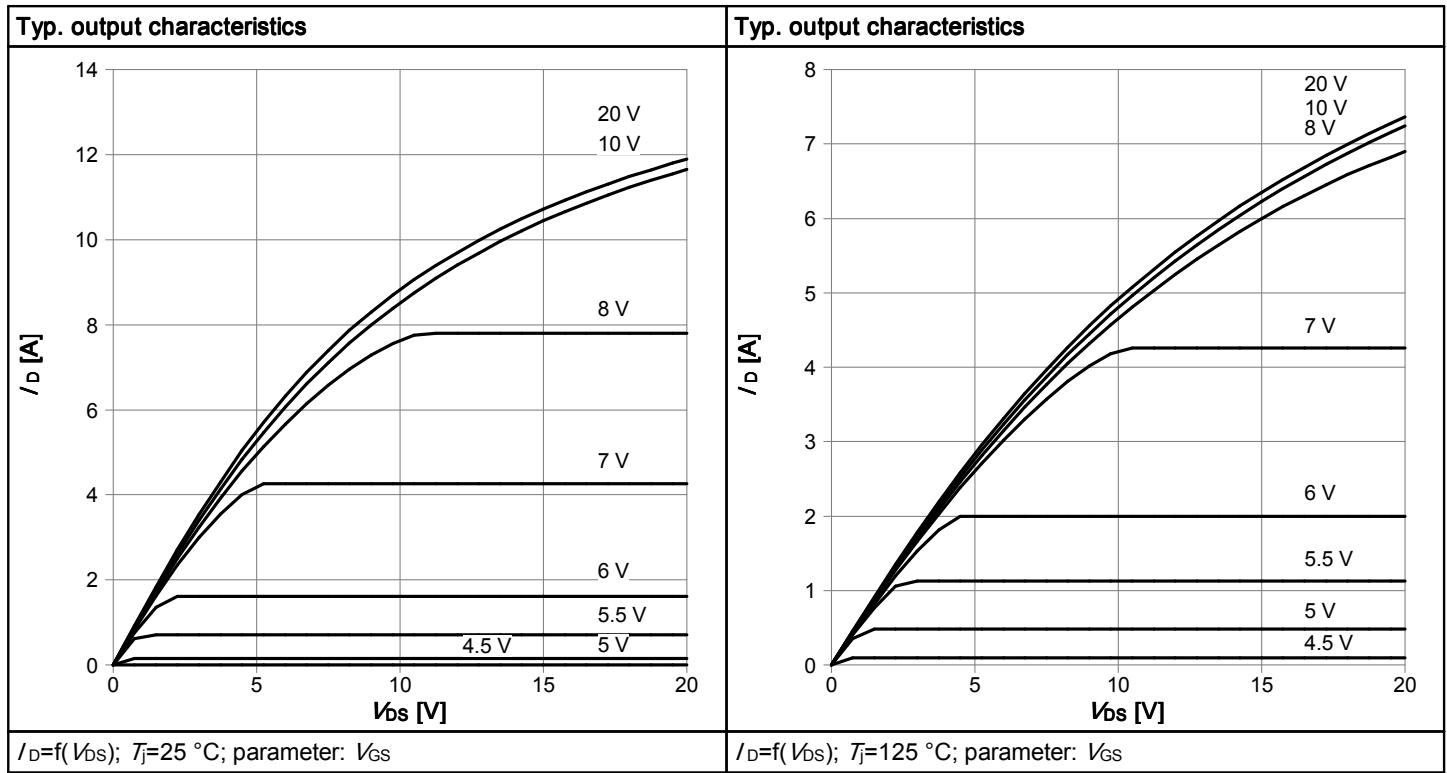


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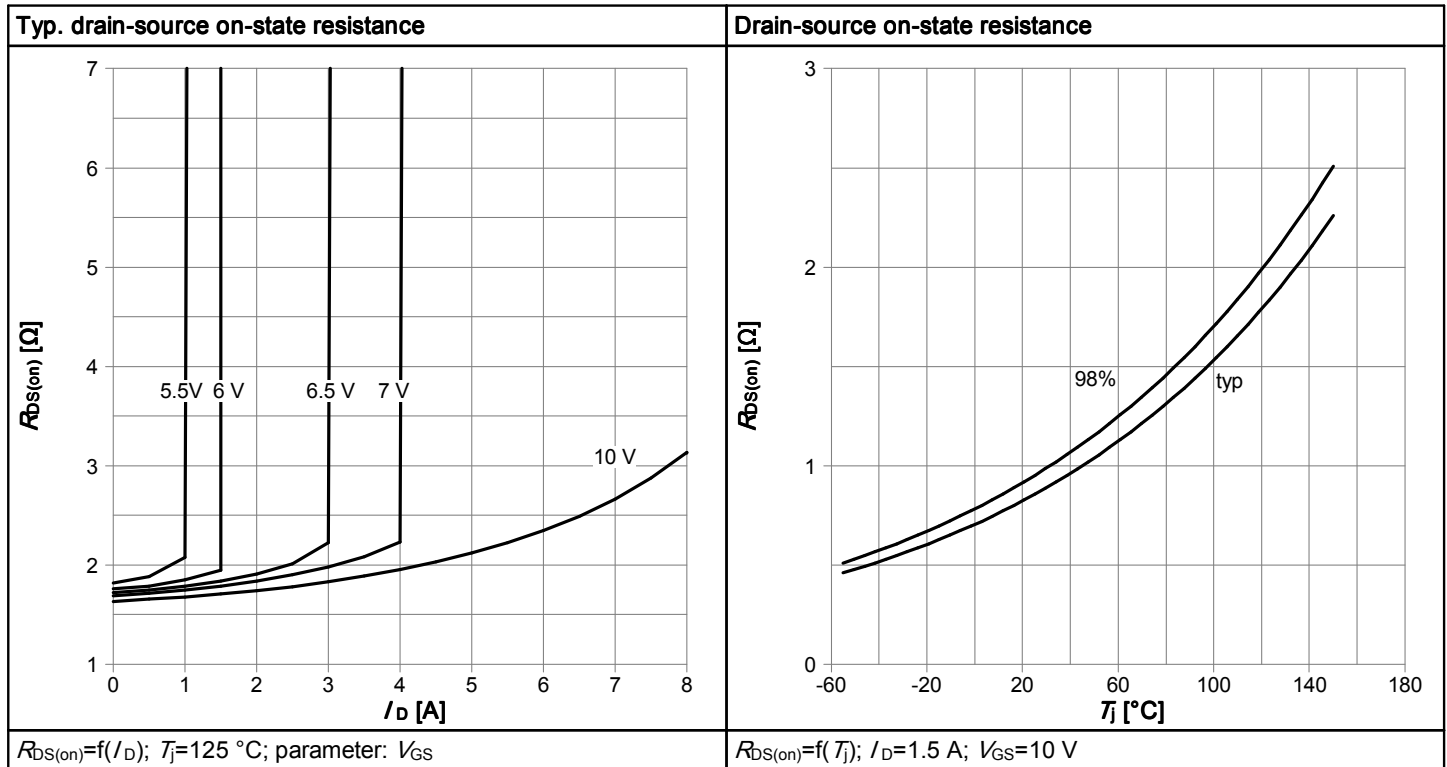


Table 12

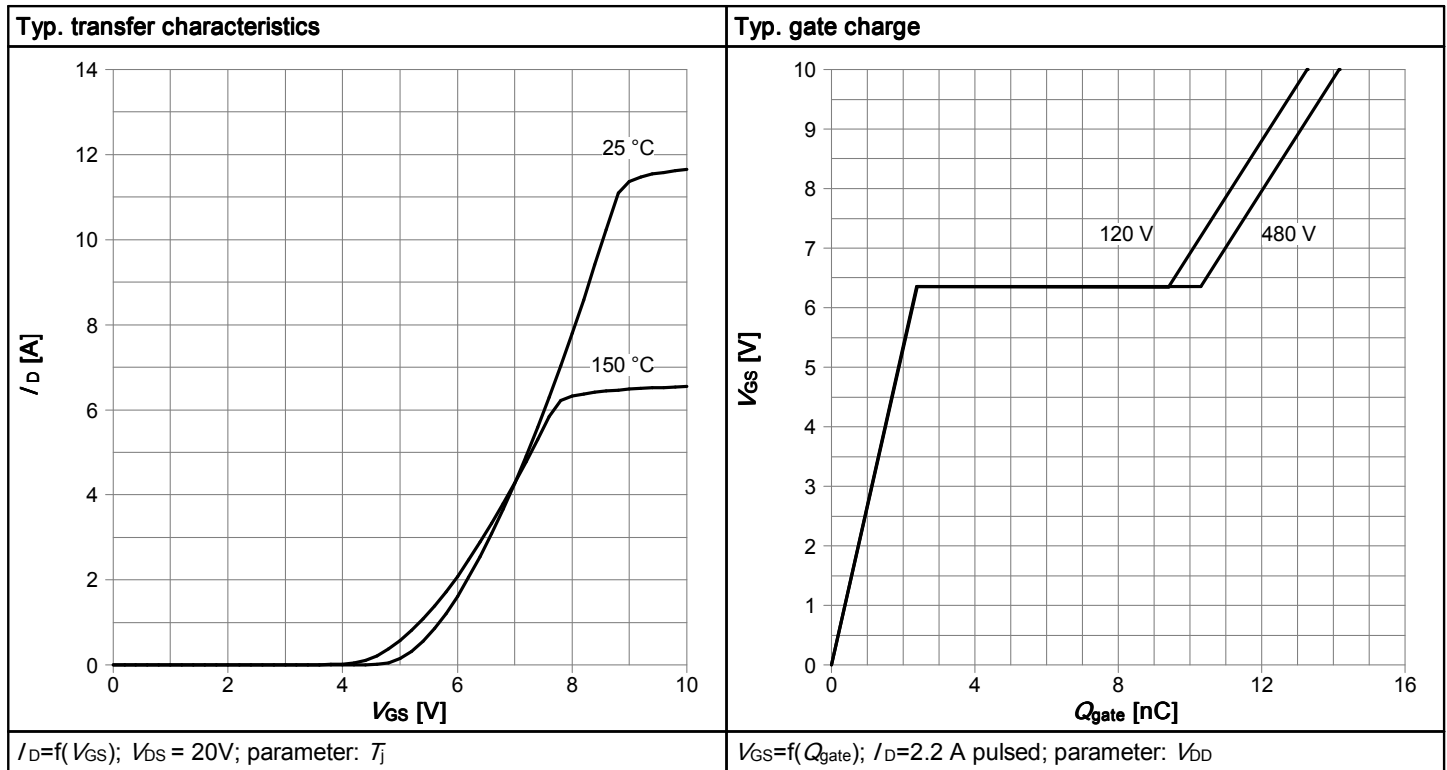


Table 13

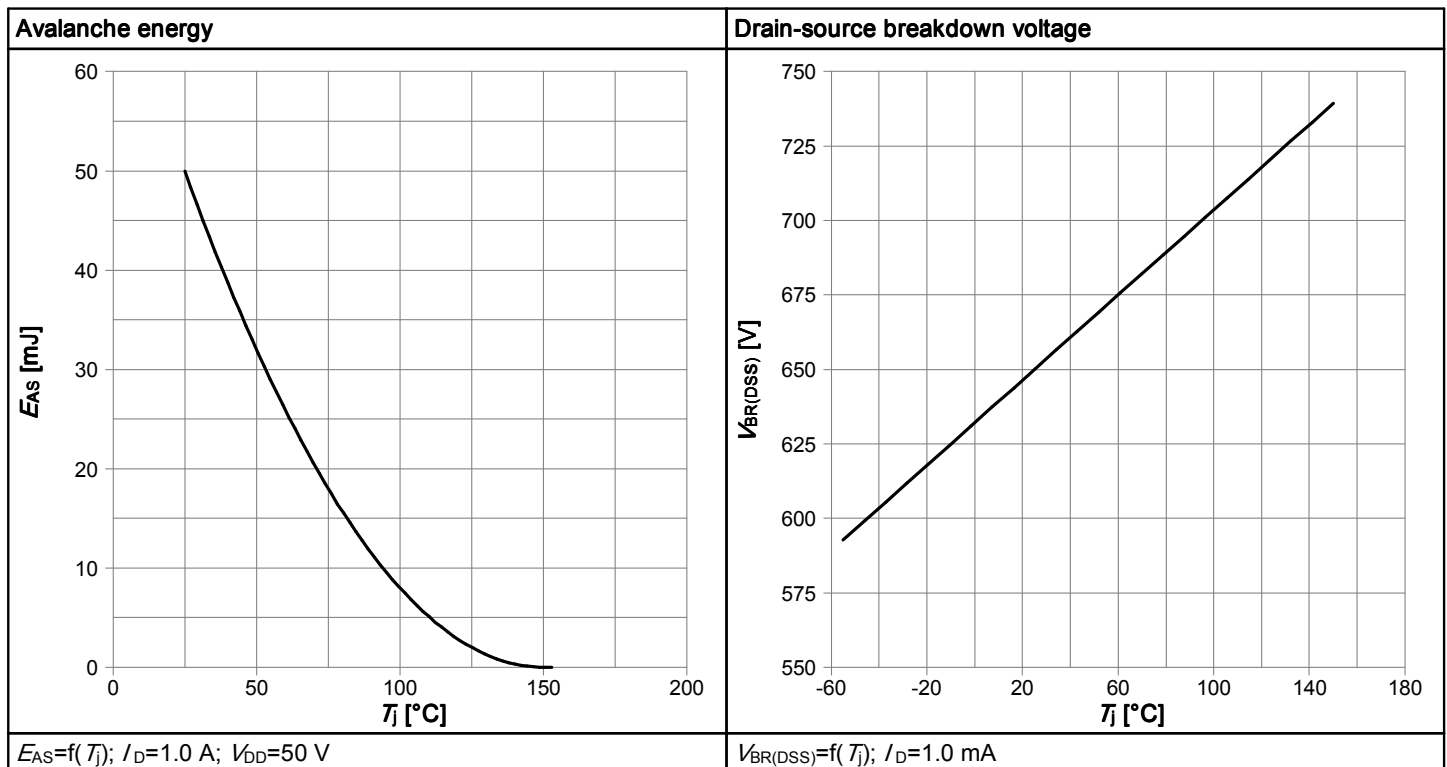


Table 14

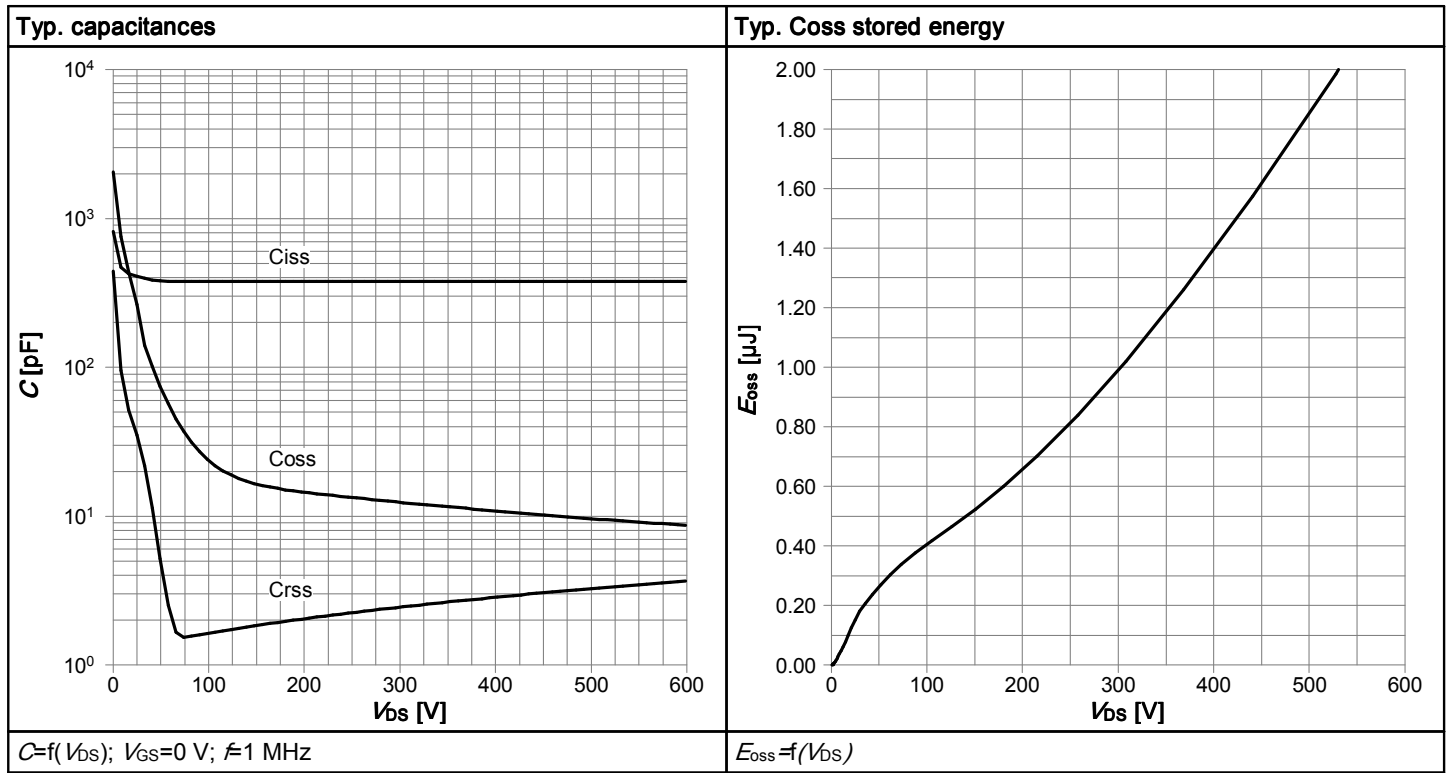
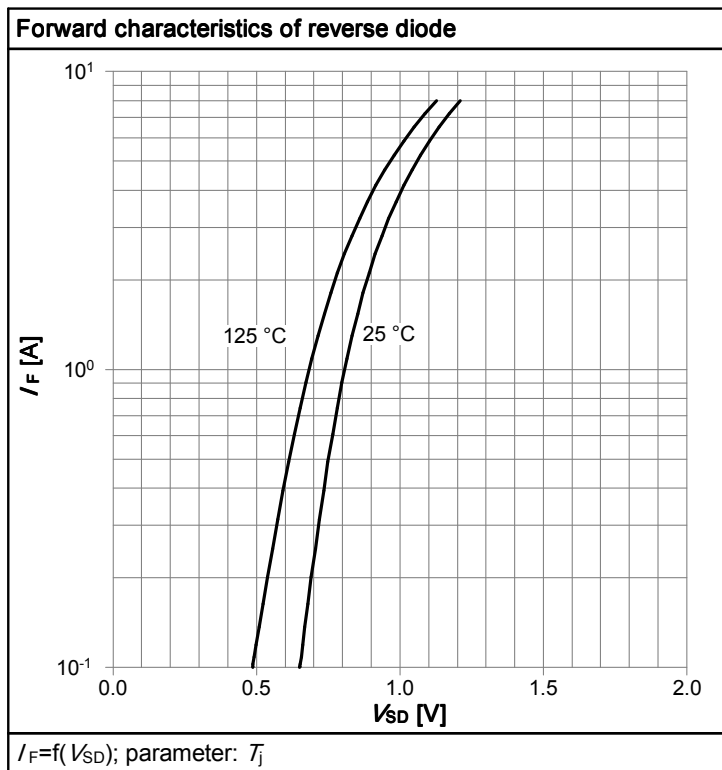


Table 15



6 Test Circuits

Table 16 Diode characteristics

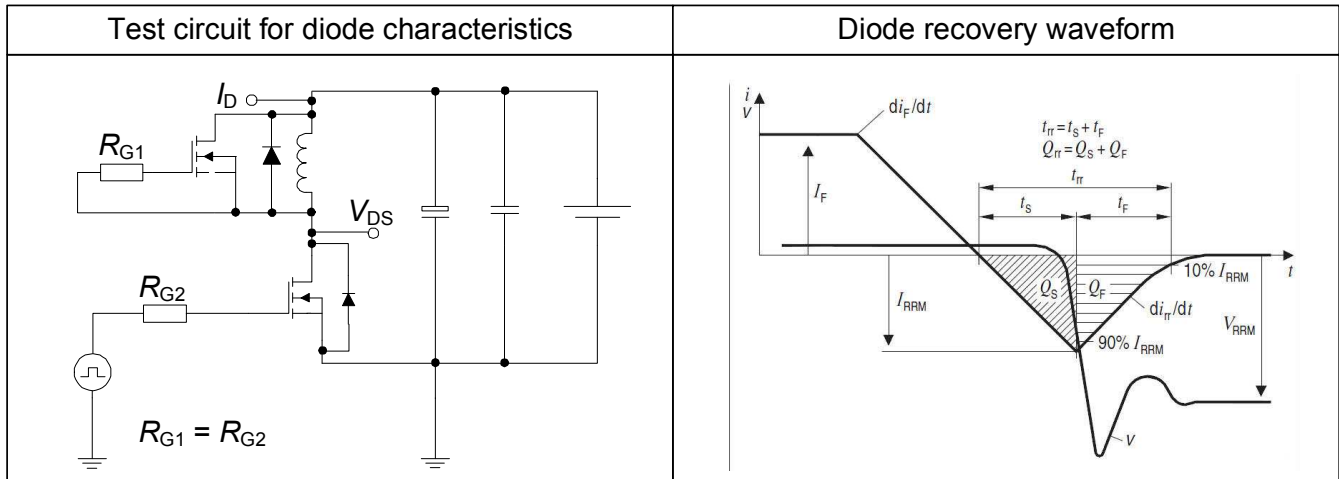


Table 17 Switching times

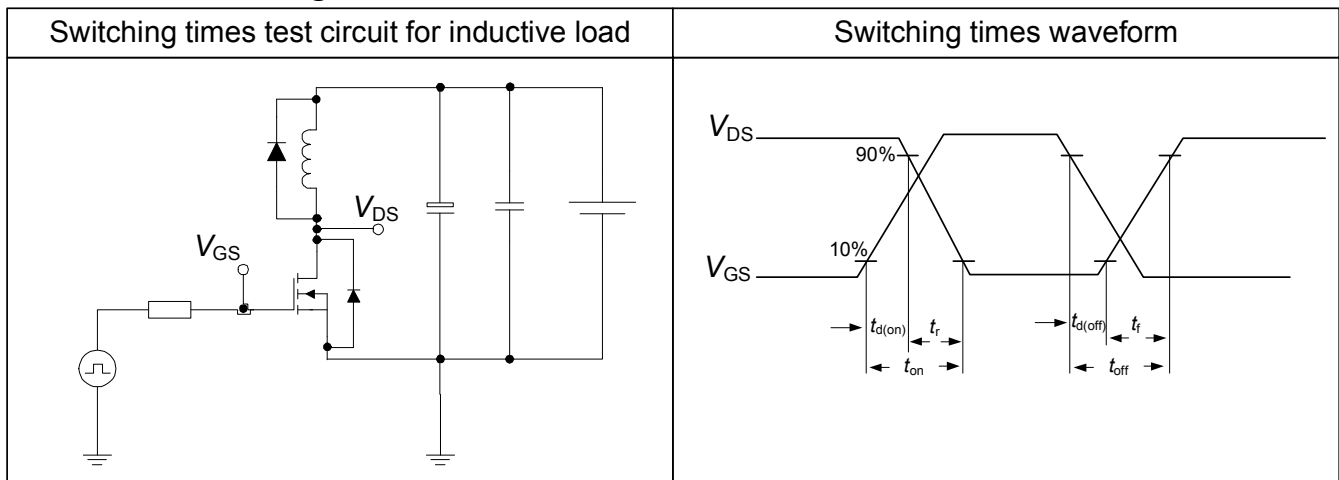
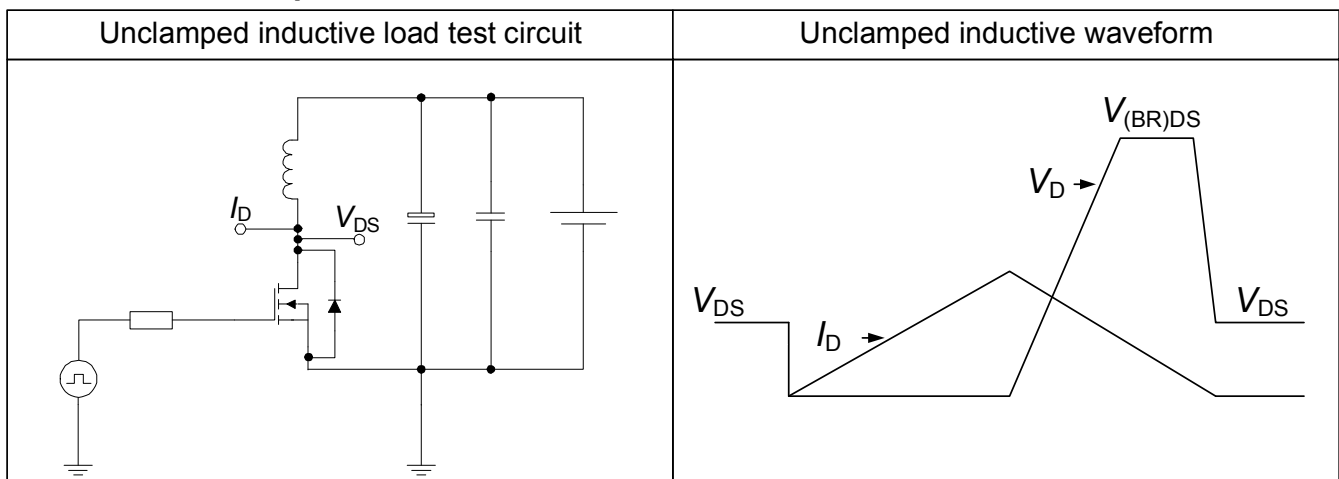
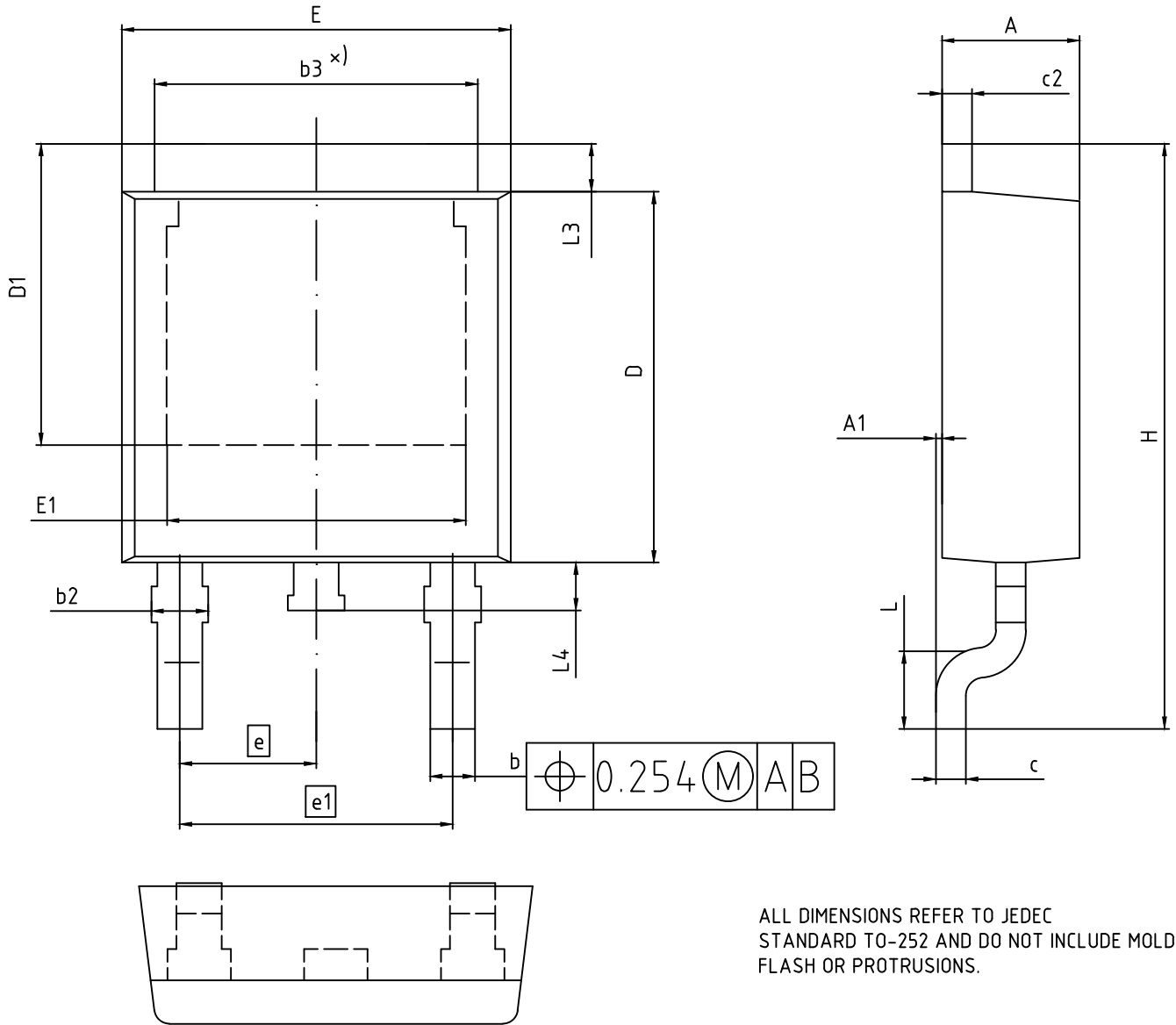


Table 18 Unclamped inductive



7 Package Outlines



ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

DOCUMENT NO. Z8B00003328
REVISION 07
SCALE: 10:1 0 1 2mm
EUROPEAN PROJECTION
ISSUE DATE 01.04.2020

Figure 1 Outline PG-TO 252, dimensions in mm/inches

8 Appendix A

Table 19 Related Links

- **IFX Design Tools:**
<http://www.infineon.com/cms/en/product/promopages/designtools/index.html>
- **IFX CoolMOS Webpage:**
<http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8>

Revision History

IPD65R950CFD

Revision: 2020-05-26, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-08-28	Release of final version
2.2	2020-05-26	Update package outline

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