MOSFET

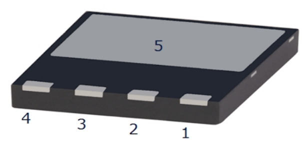
600V CoolMOS™ CP Power Transistor

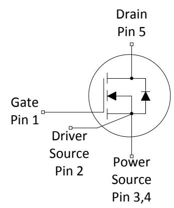
The CoolMOS™ CP series offers devices which provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler..

ThinPAK

ThinPAK is a a new leadless SMD package for HV MOSFETs. The new package has a very small footprint of only 64mm² (vs. 150mm² for the D²PAK) and a very low profile with only 1mm height (vs. 4.4mm for the D²PAK). The significantly smaller package size, combined with benchmark low parasitic inductances, provides designers with a new and effective way to decrease system solution size in power-density driven designs.

ThinPAK 8x8





Features

- Reduced board space consumption
- Increased power density
- Short commutation loop
- Smooth switching waveform
- easy to use products
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Quallfied according to JEDEC (J-STD20 and JESD22) for target applications (Server, Adapter)
- Pb-free plating, Halogen free

Potential applications

Server, Adapter

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{ds} @ T_{jmax}	650	V
$R_{DS(on),max}$	0.299	Ω
$Q_{g,typ}$	22	nC
$I_{D,pulse}$	34	A
E_{oss} @ 400V	4.2	µJ
Body diode di_F/dt	200	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPL60R299CP	PG-VSON-4	6R299P	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	11.1 7.0	A	T_C = 25°C T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	34	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	290	mJ	I_D =4.4 A; V_{DD} = 50 V
Avalanche energy, repetitive[3]	E_{AR}	-	-	0.44	mJ	I_D =4.4 A; V_{DD} = 50 V
Avalanche current, repetitive[3]	I_{AR}	-	-	4.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS} =0...480 V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	96	W	T_C=25 °C
Operating Temperature	T_j	-40	-	150	°C	-
Storage Temperature	T_{stg}	-40	-	125	°C	-
Continuous diode forward current	I_S	-	-	11.1	A	T_C=25 °C
Diode pulse current[2]	$I_{S,pulse}$	-	-	34	A	T_C = 25°C
Reverse diode dv/dt[4]	dv/dt	-	-	15	V/ns	V_{DS} =0...400 V, I_{SD}<= I_D, T_j=25 °C see table 8
Maximum diode commutation speed	di_F/dt	-	-	200	A/µs	V_{DS} =0...400 V, I_{SD}<= I_D, T_j=25 °C see table 8

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.3	°C/W	-
Thermal resistance, junction - ambient[5]	R_{thJA}	-	-	45	°C/W	SMD version, device on PCB, 6cm² cooling area
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL2a

[1] Limited by $T_{j\,max}$. Maximum duty cycle
[2] Pulse width t_p limited by $T_{j,max}$
[3] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$; Pulse width t_p limited by $T_{j,max}$
[4] Identical low side and high side switch with identical R_G
[5] Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm2 copper area (thickness 70?m) for drain connection. PCB is vertical without air stream cooling.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0 V, I_D=0.25 mA
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	V_{DS}=V_{GS}, I_D=0.44 mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C
Gate-source leakage curent	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.27 0.70	0.299 -	Ω	V_{GS}=10 V, I_D=6.6A, T_j=25 °C V_{GS}=10 V, I_D=6.6 A, T_j=150 °C
Gate resistance	R_G	-	1.9	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1100	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance	C_{oss}	-	60	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	46	-	pF	V_{GS}=0 V, V_{DS}=0...480V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	120	-	pF	I_D=constant, V_{GS}=0 V, V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=6.6 A, R_G=4.3Ω; see table 9
Rise time	t_r	-	5	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=6.6 A, R_G=4.3Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=6.6 A, R_G=4.3Ω; see table 9
Fall time	t_f	-	5	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=6.6 A, R_G=4.3Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=480 V, I_D=6.6 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	8	-	nC	V_{DD}=480 V, I_D=6.6 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	22	-	nC	V_{DD}=480 V, I_D=6.6 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	V_{DD}=480 V, I_D=6.6 A, V_{GS}=0 to 10 V

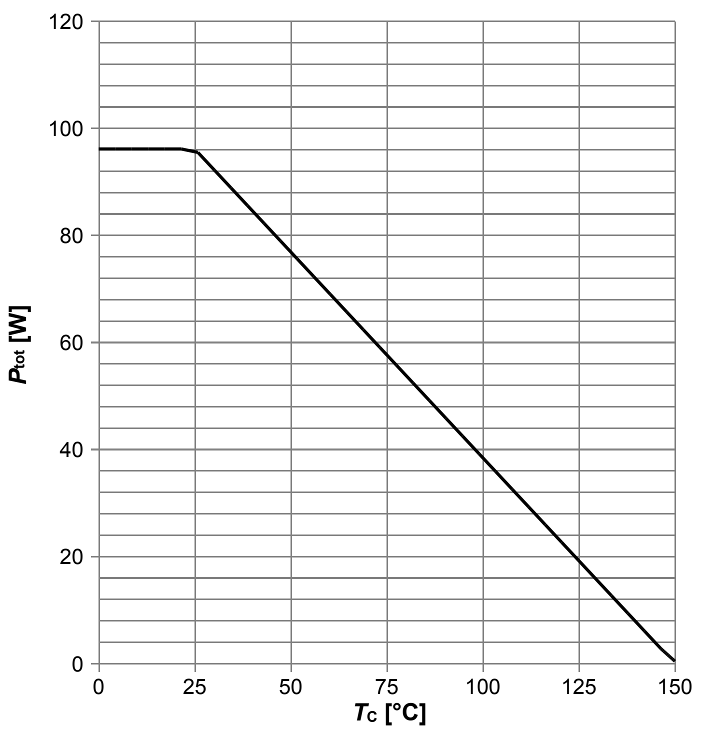
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0 V, I_F=6.6 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	300	-	ns	V_R=400 V, I_F=6.6 di_F/dt=100 A/µs see table 8
Reverse recovery charge	Q_{rr}	-	3.9	-	µC	V_R=400 V, I_F=6.6 di_F/dt=100 A/µs see table 8
Peak reverse recovery current	I_{rrm}	-	26	-	A	V_R=400 V, I_F=6.6 di_F/dt=100 A/µs see table 8

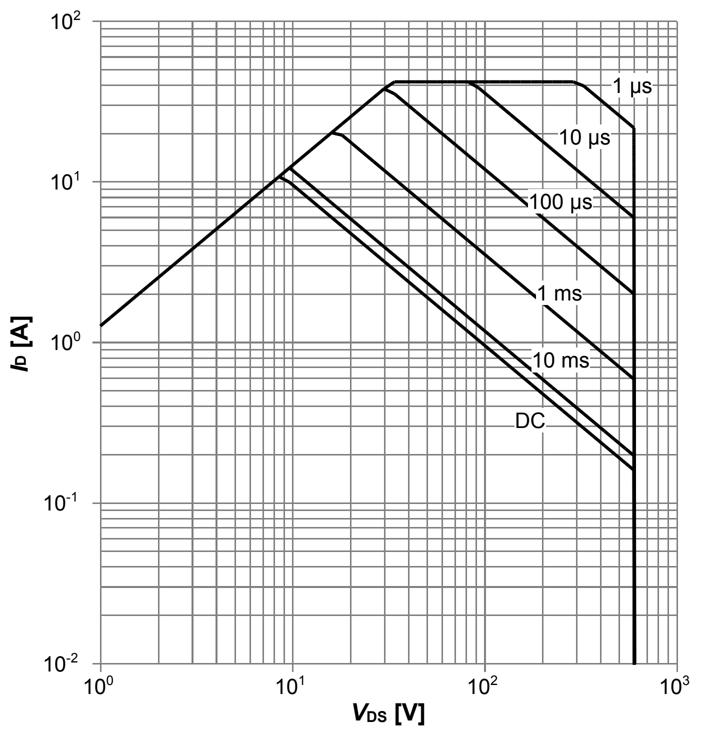
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



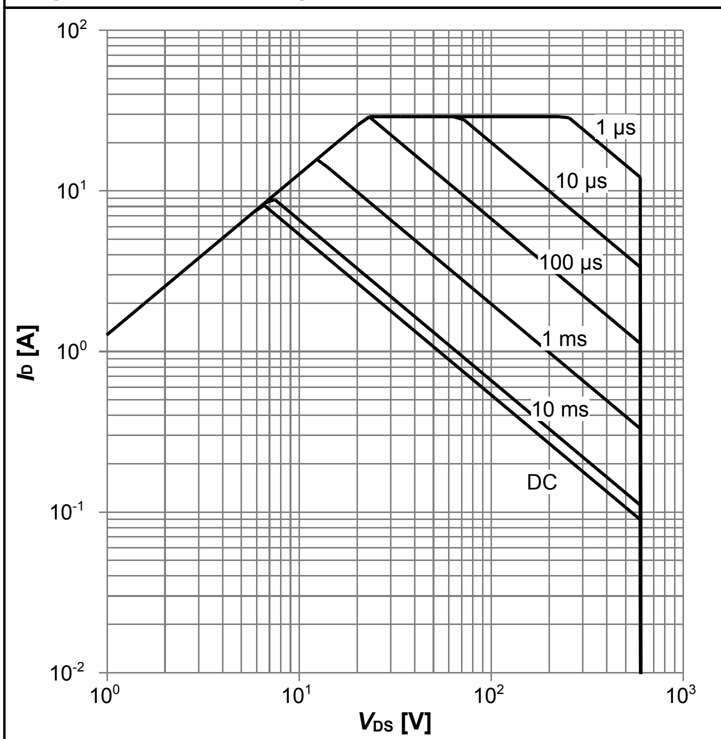
P_{tot}=f(T_C)

Diagram 2: Safe operating area



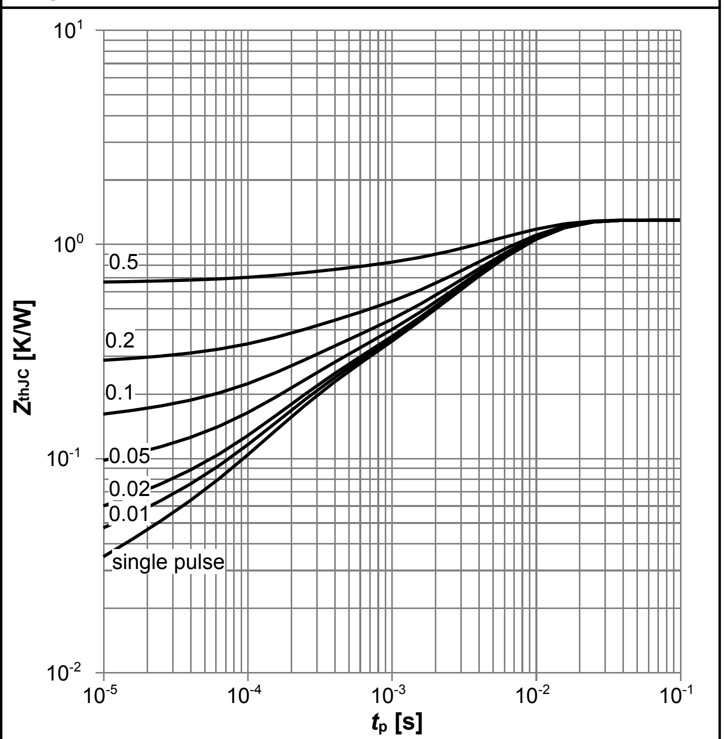
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

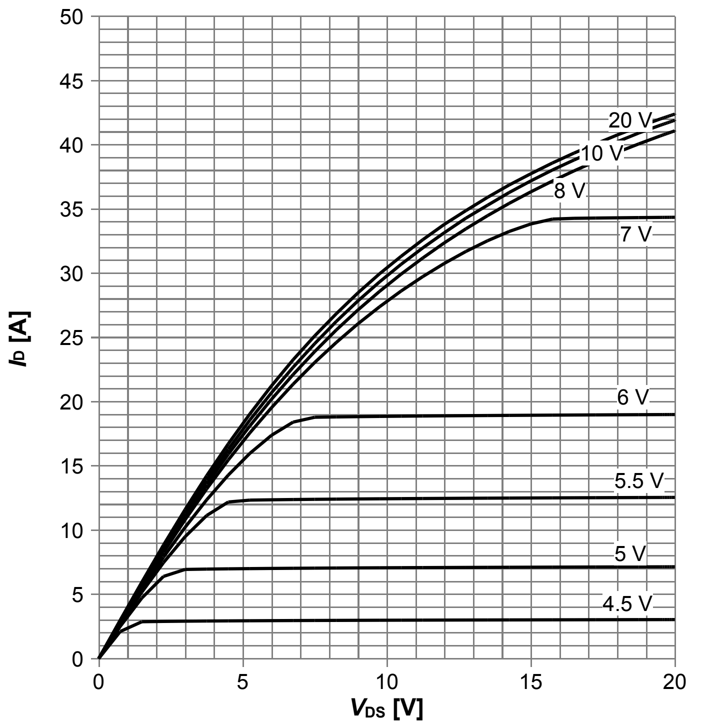
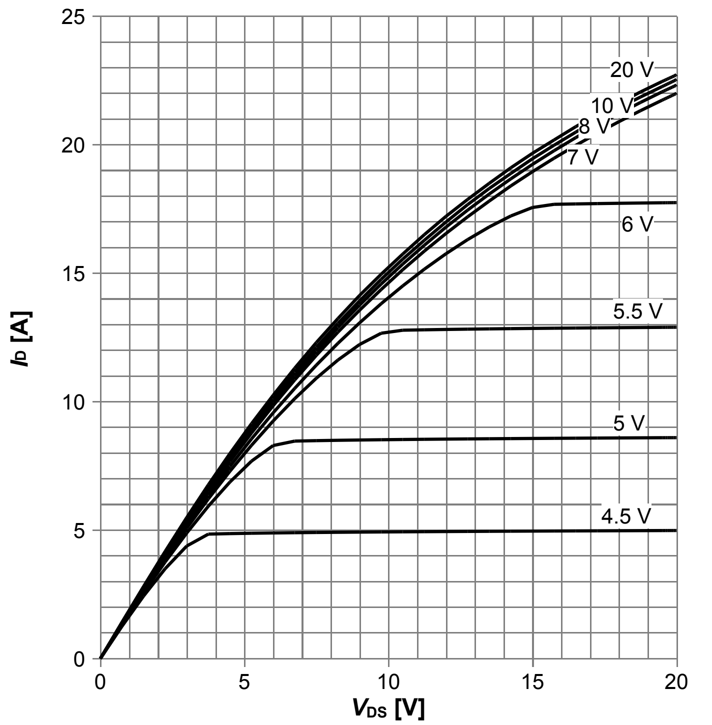
Diagram 5: Typ. output characteristics	**Diagram 6: Typ. output characteristics**
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

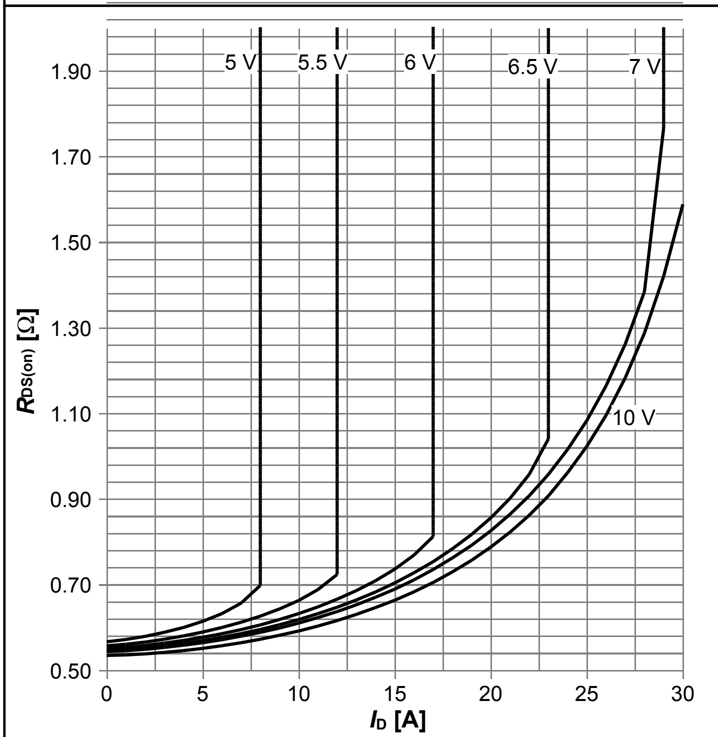
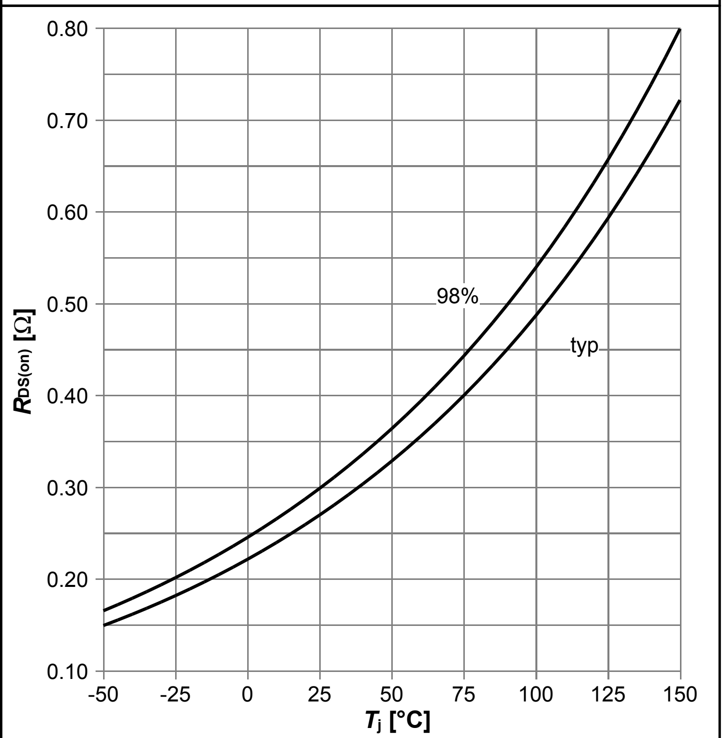
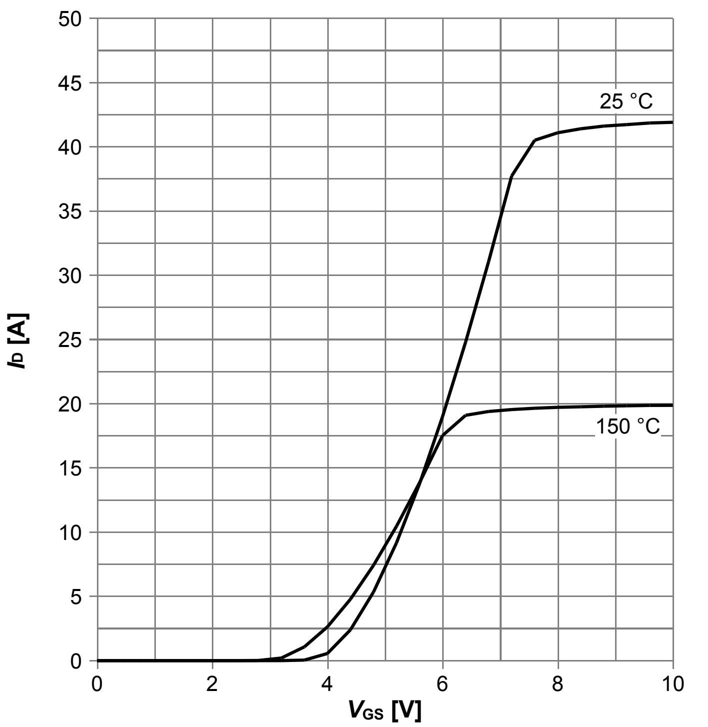
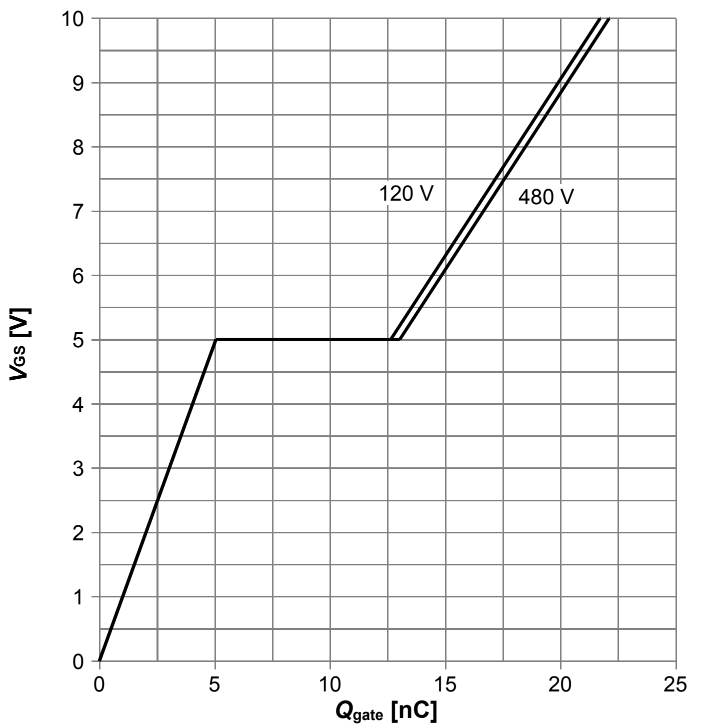
Diagram 7: Typ. drain-source on-state resistance	**Diagram 8: Drain-source on-state resistance**
	
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}$=f(T_j); I_D=6.6 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



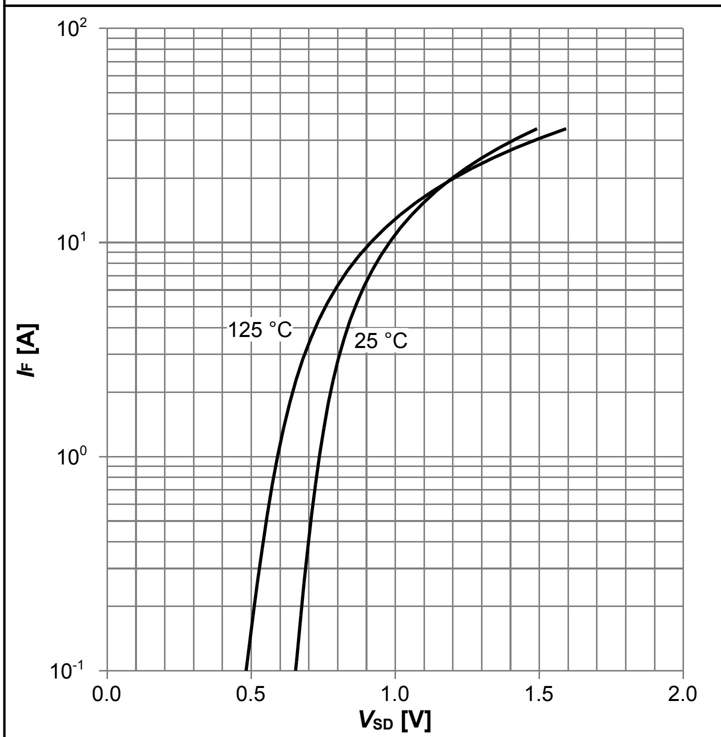
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



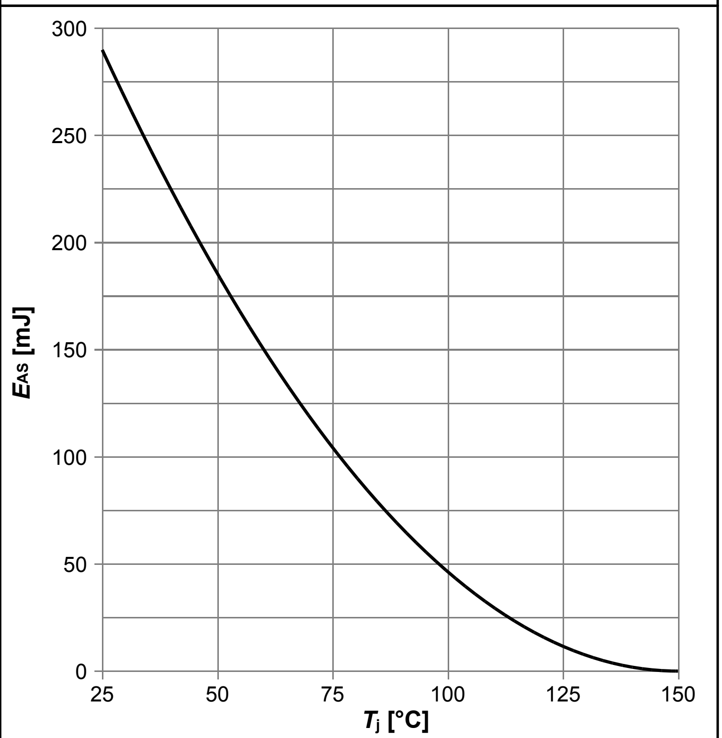
V_{GS}=f(Q_{gate}); I_D=6.6 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



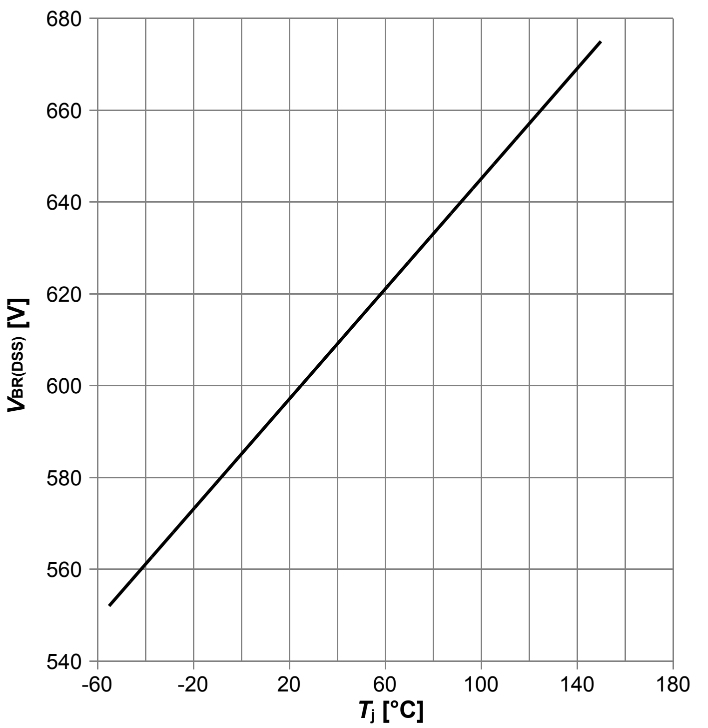
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



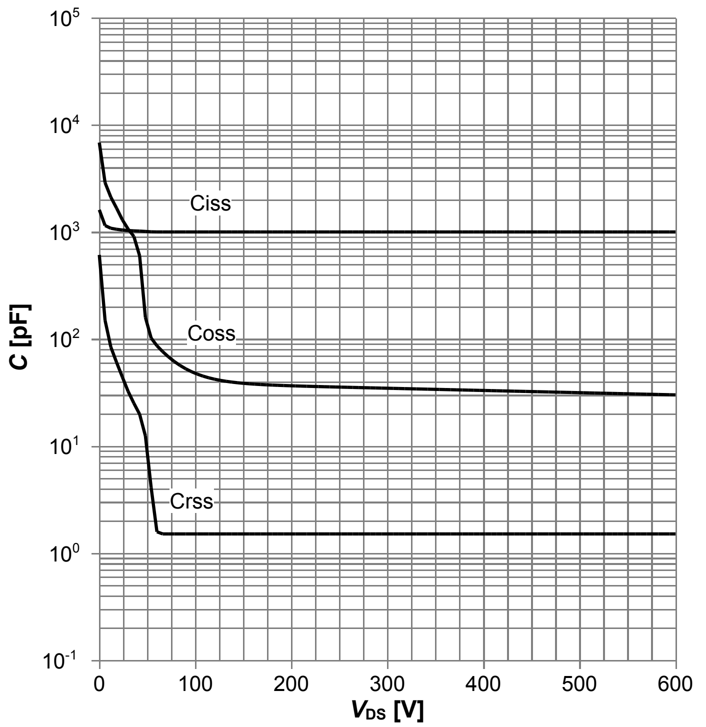
E_{AS}=f(T_j); I_D=4.4 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



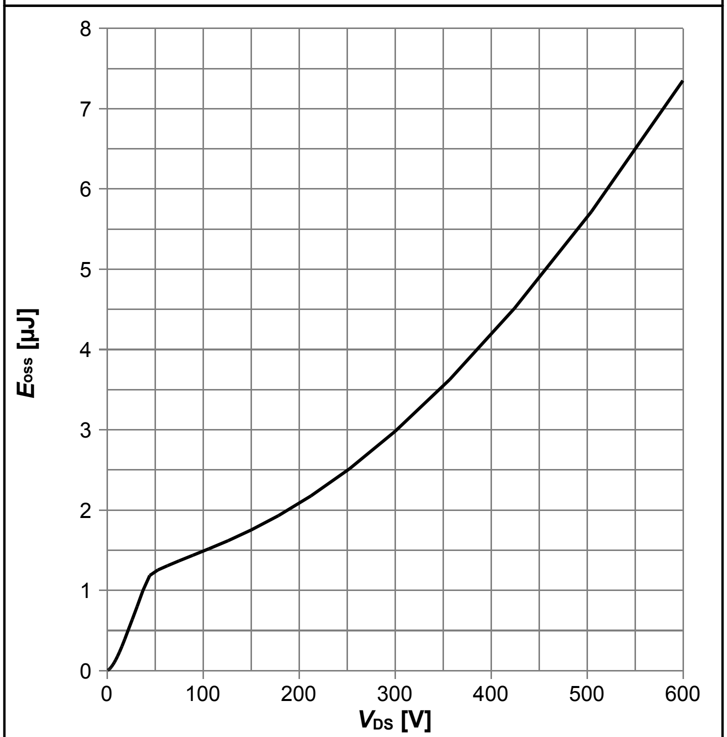
$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

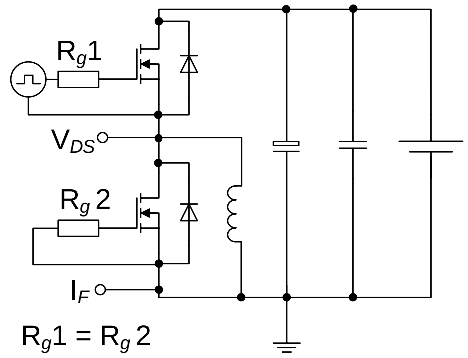
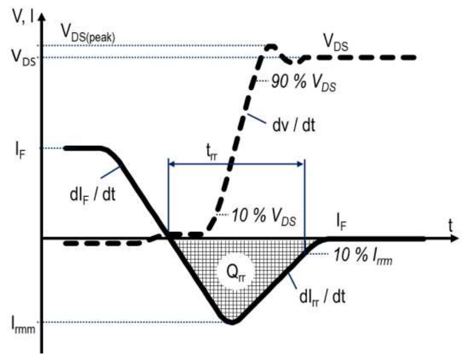
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 switching times (ss)

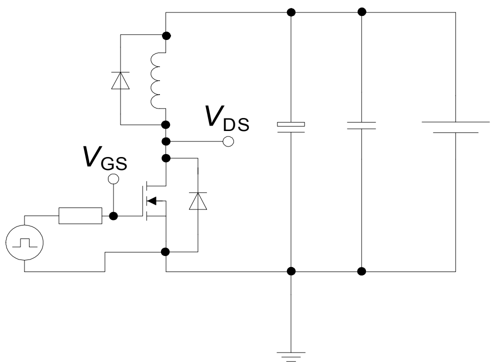
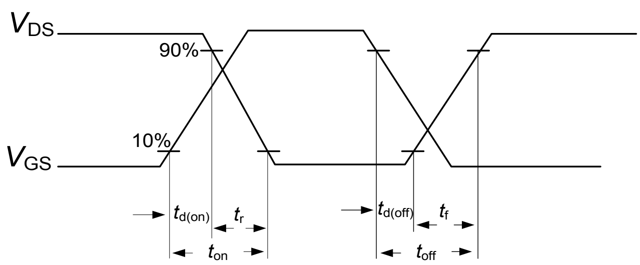
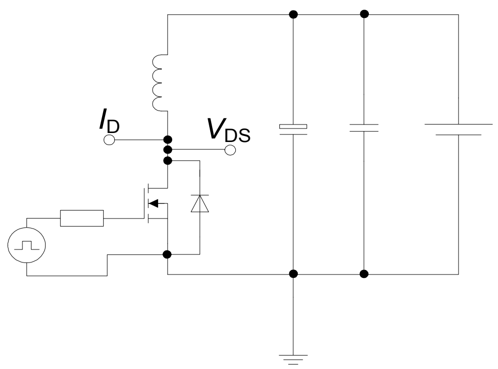
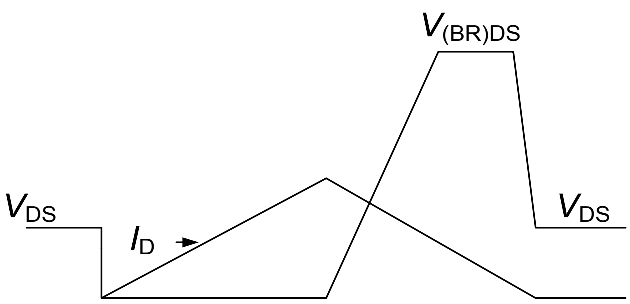
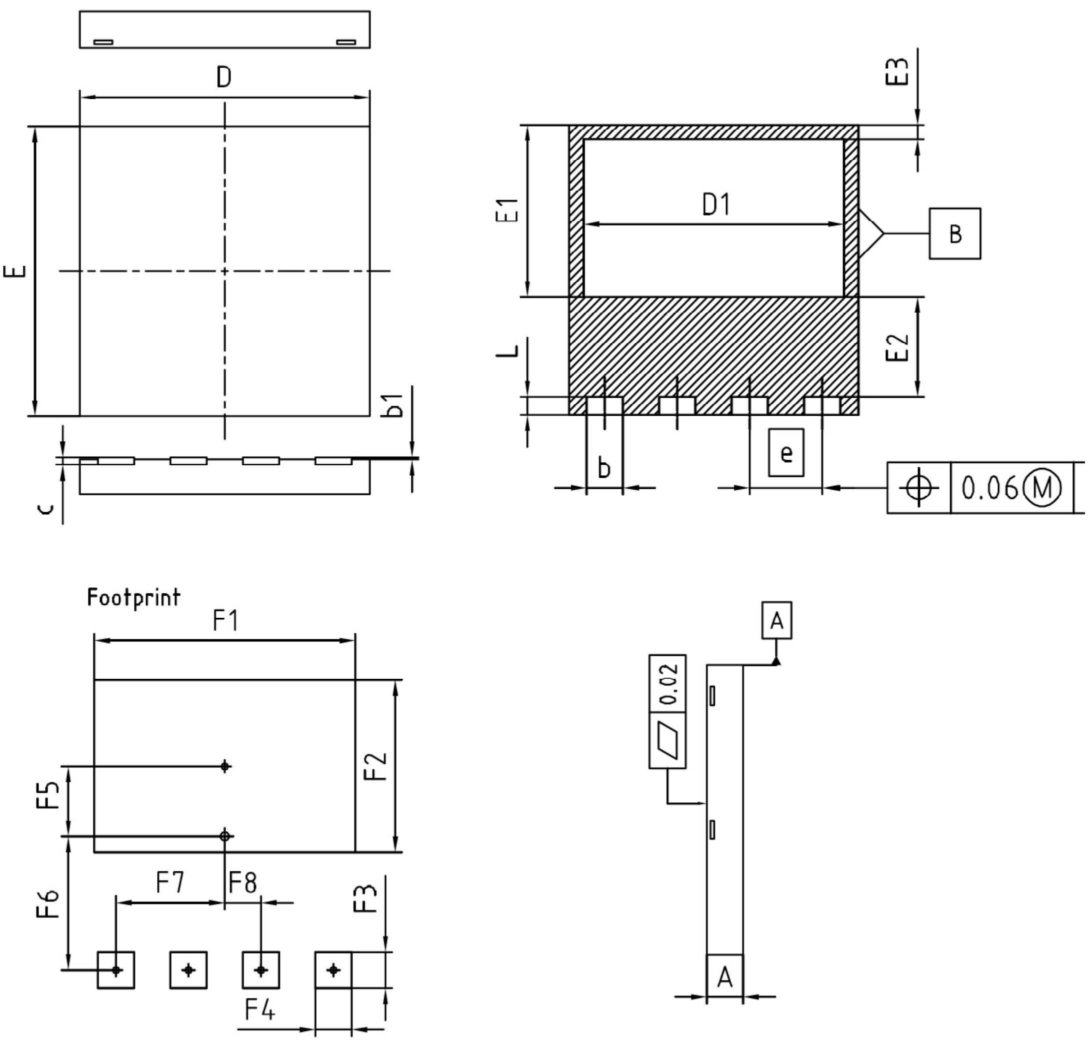
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

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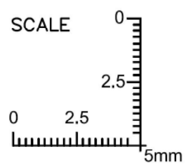
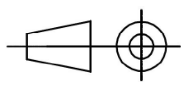


EUROPEAN PROJECTION



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01

Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL60R299CP

Revision: 2017-09-06, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.2	2017-09-06	Updated MSL; style updated

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