

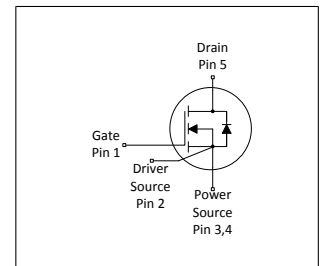
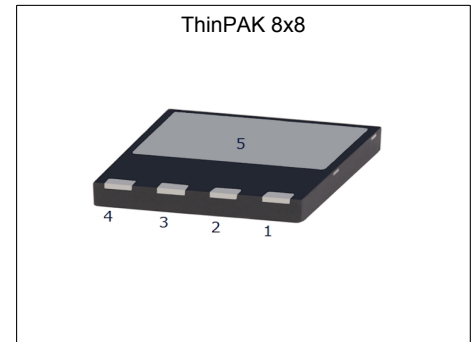
MOSFET

650V CoolMOS™ CFD2 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.

ThinPAK

ThinPAK is a new leadless SMD package for HV MOSFETs. The new package has a very small footprint of only 64mm² (vs. 150mm² for the D²PAK) and a very low profile with only 1mm height (vs. 4.4mm for the D²PAK). The significantly smaller package size, combined with benchmark low parasitic inductances, provides designers with a new and effective way to decrease system solution size in power-density driven designs.



Features

- Reduced board space consumption
- Increased power density
- Short commutation loop
- Smooth switching waveform
- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Easy to use/drive
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free plating, Halogen free mold compound



Potential applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching stages for e.g. PC Silverbox, LCD TV, Lighting, Server and Telecom.

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------|-------|------------|
| $V_{ds} @ T_{jmax}$ | 700 | V |
| $R_{DS(on),max}$ | 0.165 | Ω |
| $Q_{g,typ}$ | 86 | nC |
| $I_{D,pulse}$ | 67 | A |
| $E_{oss} @ 400V$ | 6.8 | μJ |
| Body diode di_F/dt | 900 | A/ μs |
| Q_{rr} | 0.7 | μC |
| t_r | 140 | ns |
| I_{rrm} | 8.8 | A |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-----------|---------|----------------|
| IPL65R165CFD | PG-VSON-4 | 65F6165 | see Appendix A |

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------------|------------|------|--------------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 21.3 13.5 | A | $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 67 | A | $T_C = 25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 614 | mJ | $I_D = 4.3\text{ A}$; $V_{DD} = 50\text{ V}$ |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.93 | mJ | $I_D = 4.3\text{ A}$; $V_{DD} = 50\text{ V}$ |
| Avalanche current, repetitive | I_{AR} | - | - | 4.3 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS} = 0 \dots 400\text{ V}$ |
| Gate source voltage | V_{GS} | -20 -30 | - | 20 30 | V | static; AC ($f > 1\text{ Hz}$) |
| Power dissipation | P_{tot} | - | - | 195 | W | $T_C = 25^\circ\text{C}$ |
| Operating and storage temperature | T_j, T_{stg} | -40 | - | 150 | $^\circ\text{C}$ | - |
| Continuous diode forward current | I_S | - | - | 21.3 | A | $T_C = 25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 67 | A | $T_C = 25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 50 | V/ns | $V_{DS} = 0 \dots 400\text{ V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ see table 8 |
| Maximum diode commutation speed | di _f /dt | - | - | 900 | A/ μs | $V_{DS} = 0 \dots 400\text{ V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ see table 8 |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|----------|--------------------|--|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 0.64 | $^\circ\text{C/W}$ | - |
| Thermal resistance, junction - ambient ⁴⁾ | R_{thJA} | - | - | 62 45 | $^\circ\text{C/W}$ | SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm ² cooling area |
| Soldering temperature, wavesoldering only allowed at leads | T_{sold} | - | - | 260 | $^\circ\text{C}$ | reflow MSL2a |

¹⁾ Limited by $T_{j,max}$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

⁴⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70 μm) for drain connection. PCB is vertical without air steam cooling.

3 Electrical characteristics

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|-------|-------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 650 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{(GS)th}$ | 3.5 | 4 | 4.5 | V | $V_{DS}=V_{GS}$, $I_D=0.9\text{ mA}$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.149 | 0.165 | Ω | $V_{GS}=10\text{ V}$, $I_D=9.3\text{ A}$, $T_j=25\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}$, $I_D=9.3\text{ A}$, $T_j=150\text{ }^\circ\text{C}$ |
| Gate resistance | R_G | - | 1.5 | - | Ω | $f=1\text{ MHz}$, open drain |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 2340 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance | C_{oss} | - | 110 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 90 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=0\dots400\text{ V}$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 420 | - | pF | $I_D=\text{constant}$, $V_{GS}=0\text{ V}$, $V_{DS}=0\dots400\text{ V}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 12.4 | - | ns | $V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=14\text{ A}$, $R_G=1.8\Omega$; see table 9 |
| Rise time | t_r | - | 7.6 | - | ns | $V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=14\text{ A}$, $R_G=1.8\Omega$; see table 9 |
| Turn-off delay time | $t_{d(off)}$ | - | 52.8 | - | ns | $V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=14\text{ A}$, $R_G=1.8\Omega$; see table 9 |
| Fall time | t_f | - | 5.6 | - | ns | $V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=14\text{ A}$, $R_G=1.8\Omega$; see table 9 |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 15 | - | nC | $V_{DD}=480\text{ V}$, $I_D=14\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge | Q_{gd} | - | 47 | - | nC | $V_{DD}=480\text{ V}$, $I_D=14\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total | Q_g | - | 86 | - | nC | $V_{DD}=480\text{ V}$, $I_D=14\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 6.4 | - | V | $V_{DD}=480\text{ V}$, $I_D=14\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------------|--|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.9 | - | V | $V_{GS}=0\text{ V}$, $I_F=14\text{ A}$, $T_j=25\text{ °C}$ |
| Reverse recovery time | t_{rr} | - | 140 | - | ns | $V_R=400\text{ V}$, $I_F=14\text{ A}$ $di_F/dt=100\text{ A}/\mu\text{s}$ see table 8 |
| Reverse recovery charge | Q_{rr} | - | 0.7 | - | μC | $V_R=400\text{ V}$, $I_F=14\text{ A}$ $di_F/dt=100\text{ A}/\mu\text{s}$ see table 8 |
| Peak reverse recovery current | I_{rrm} | - | 8.8 | - | A | $V_R=400\text{ V}$, $I_F=14\text{ A}$ $di_F/dt=100\text{ A}/\mu\text{s}$ see table 8 |

4 Electrical characteristics diagrams

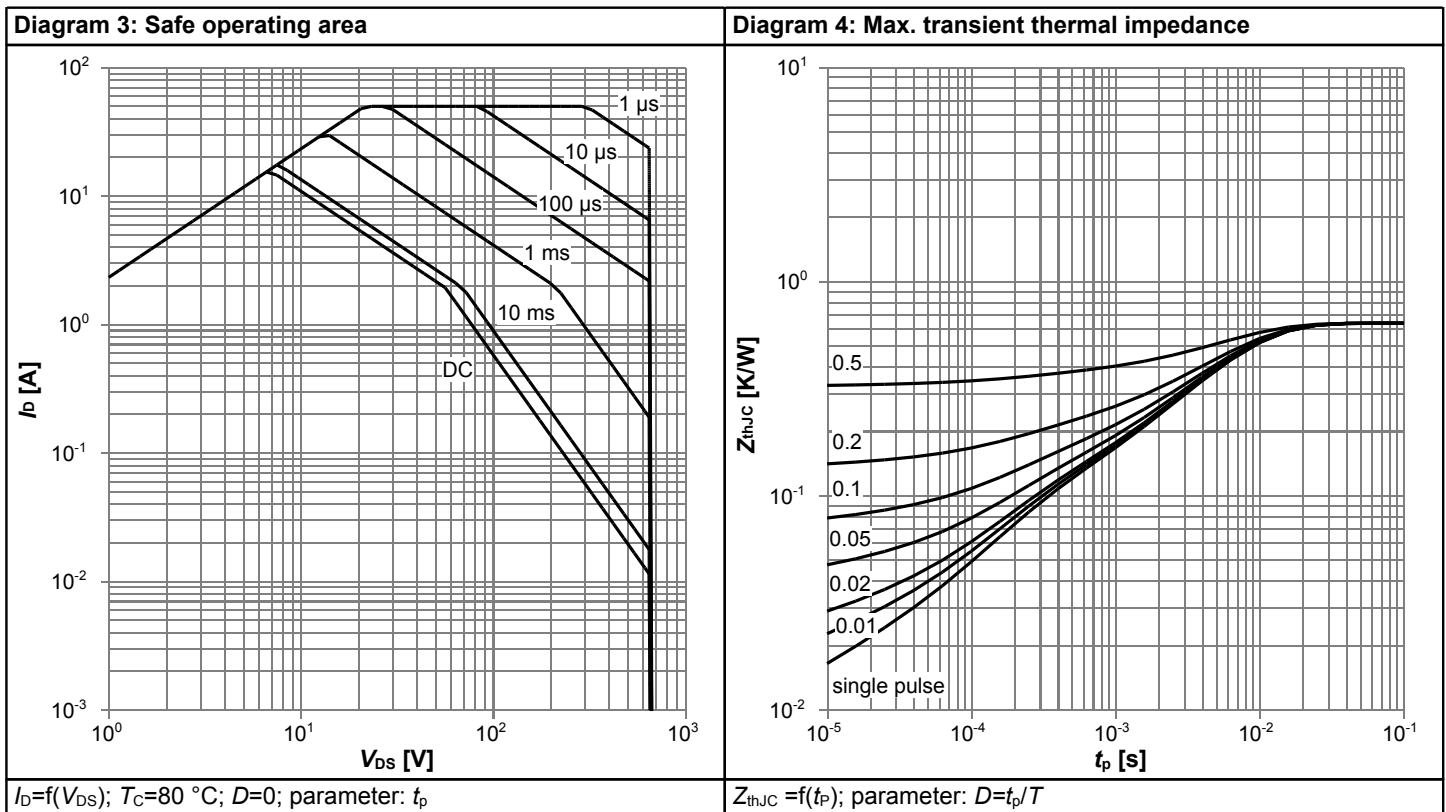
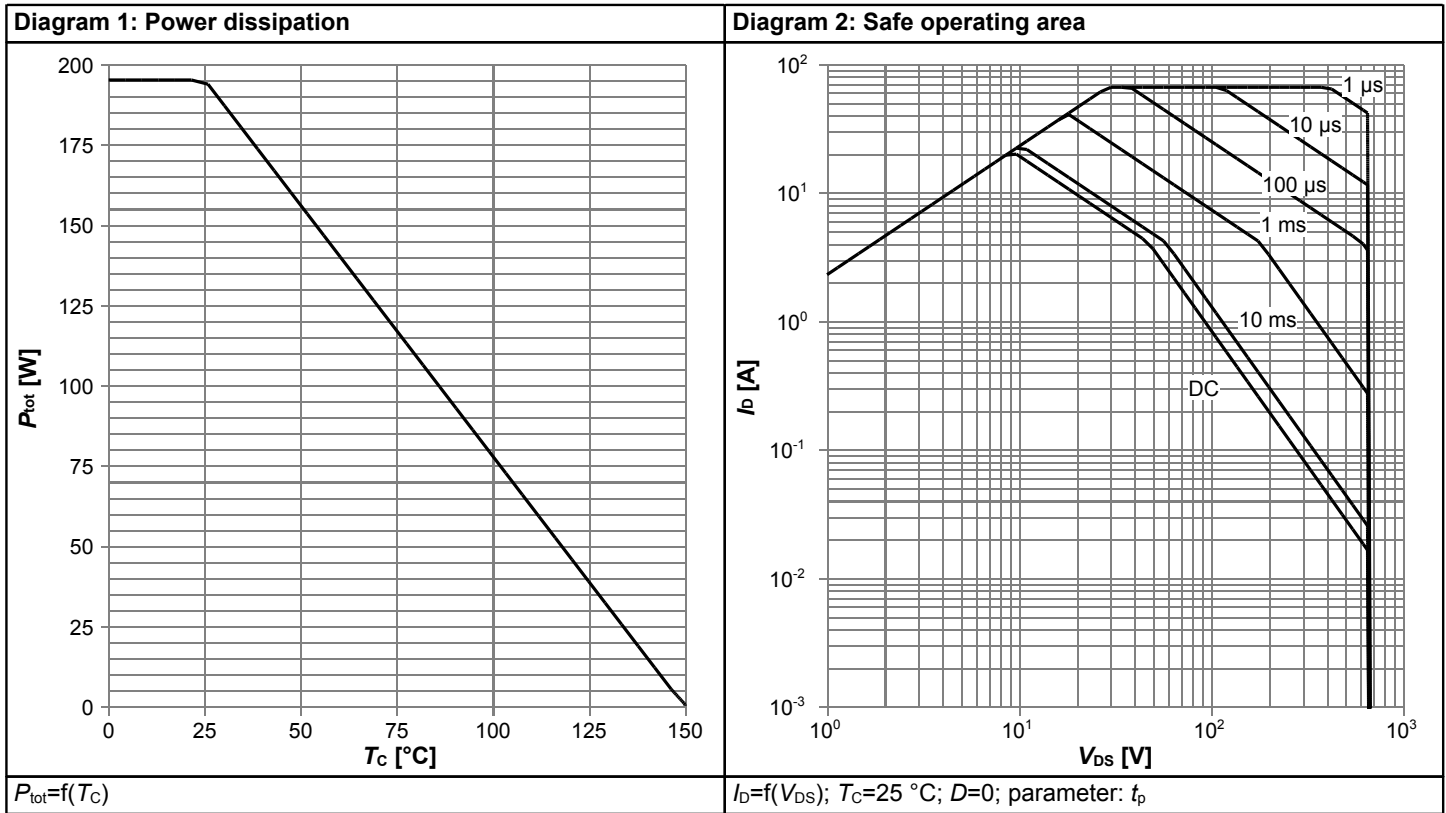
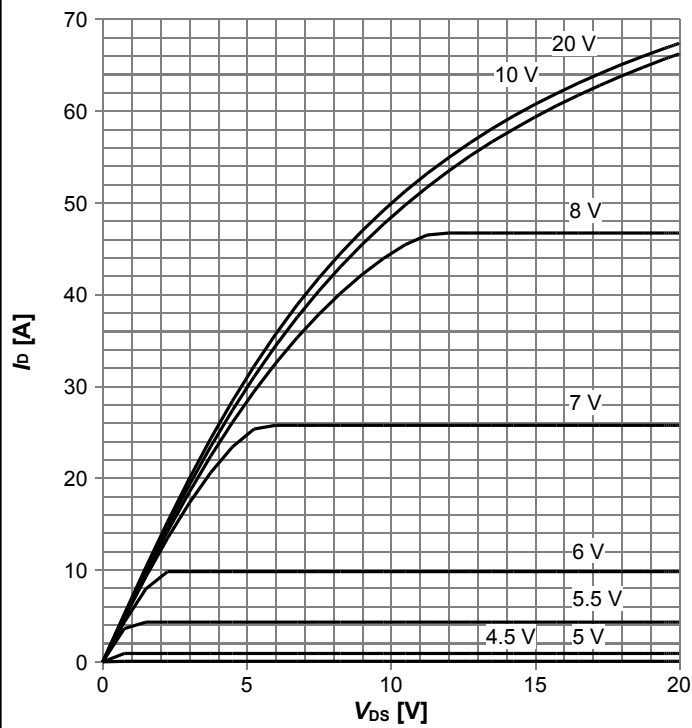
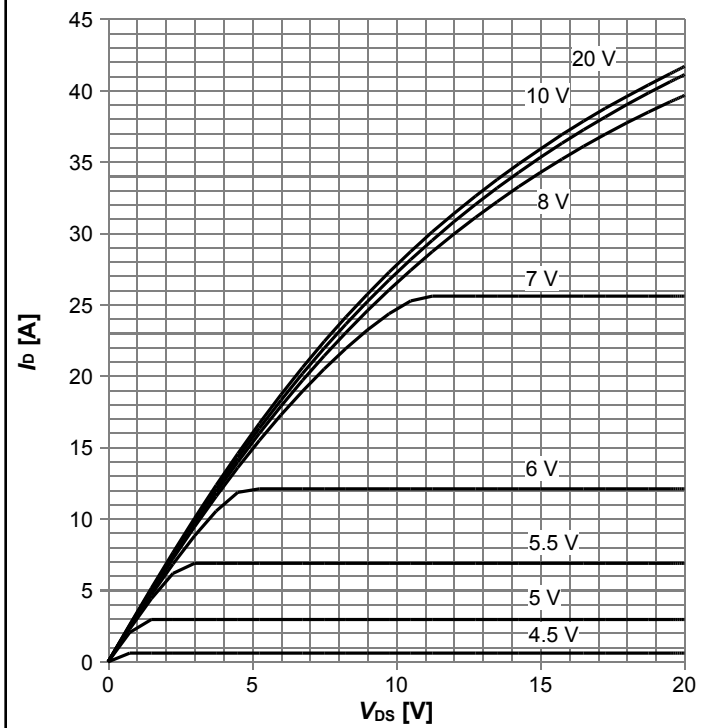


Diagram 5: Typ. output characteristics



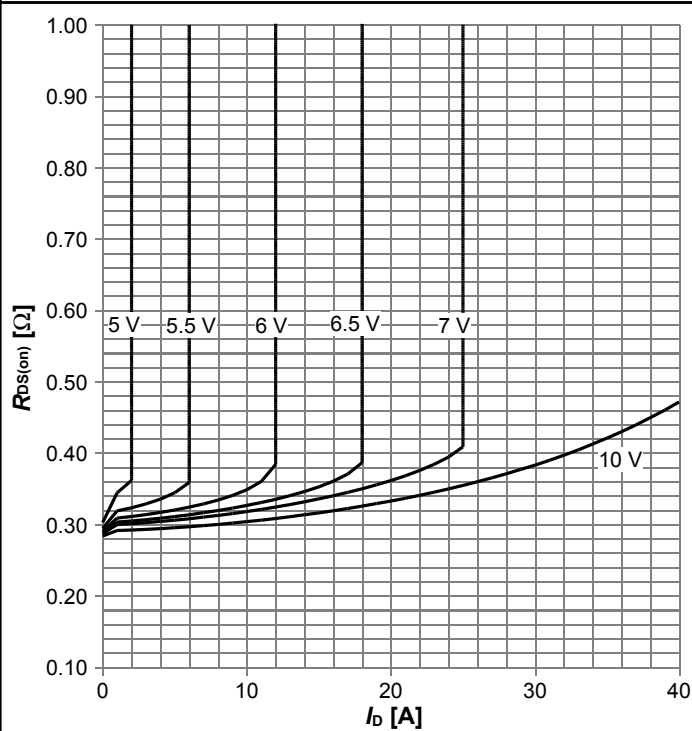
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 6: Typ. output characteristics



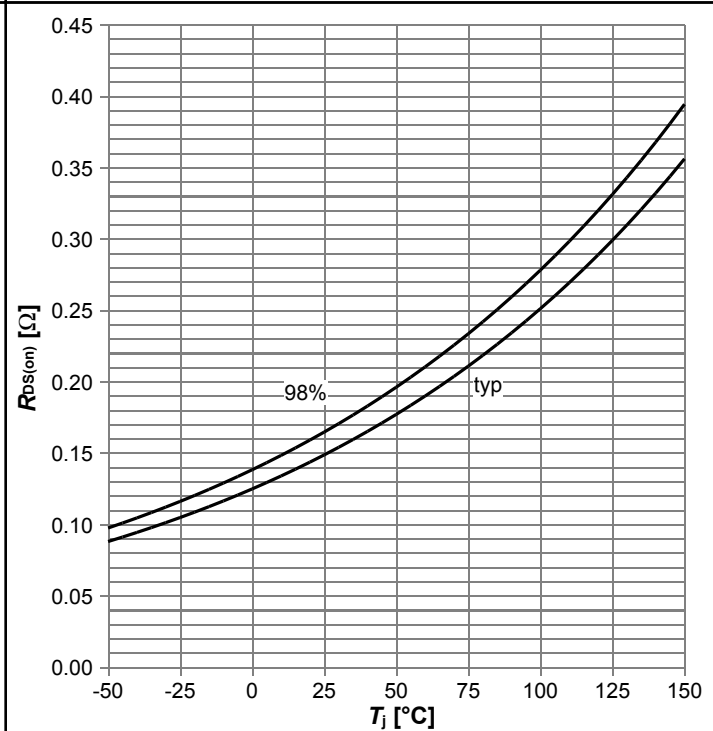
$I_D=f(V_{DS}); T_j=125\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D); T_j=125\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 8: Drain-source on-state resistance

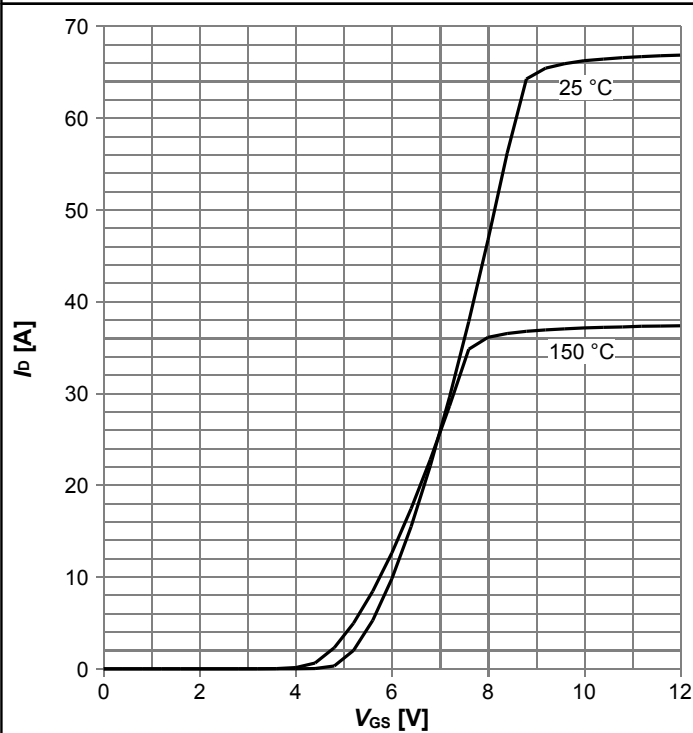


$R_{DS(on)}=f(T_j); I_D=9.3\text{ A}; V_{GS}=10\text{ V}$

650V CoolMOS™ CFD2 Power Transistor

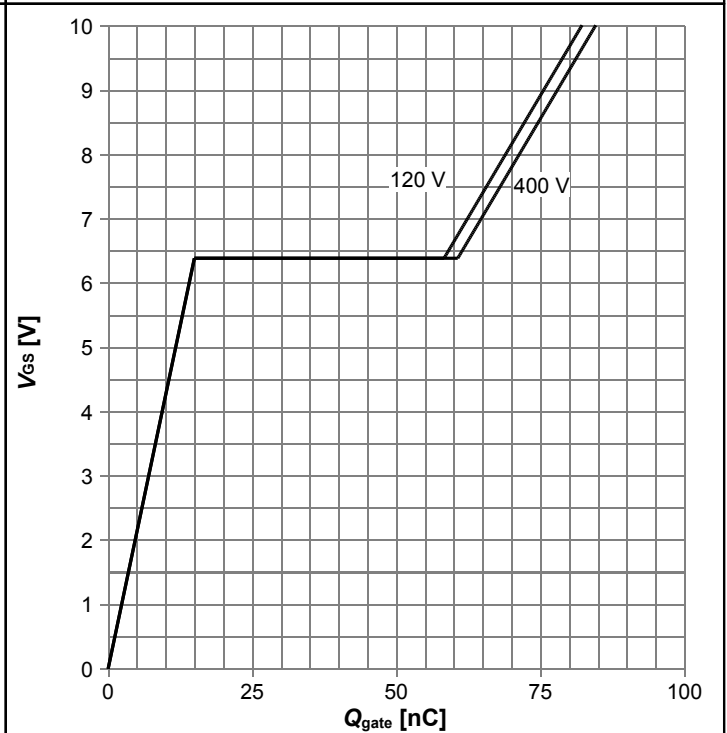
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Diagram 9: Typ. transfer characteristics



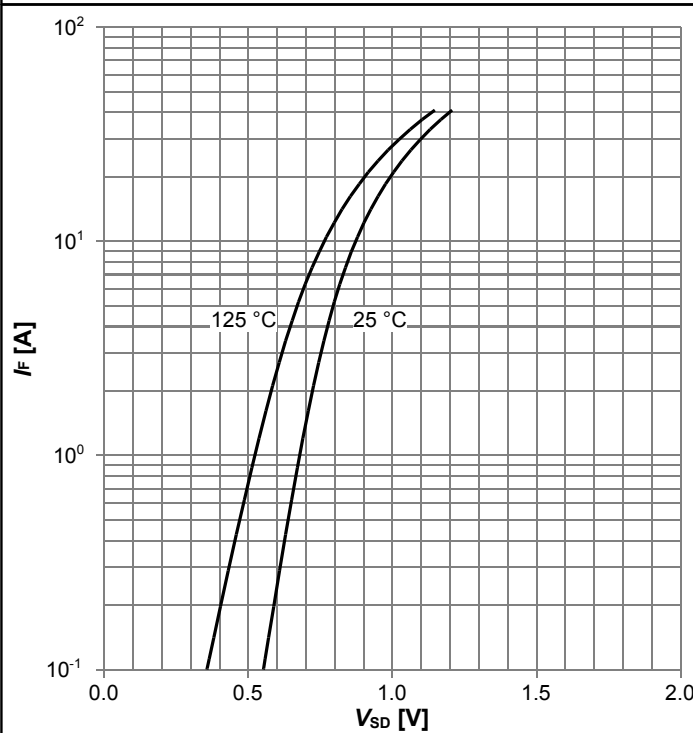
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



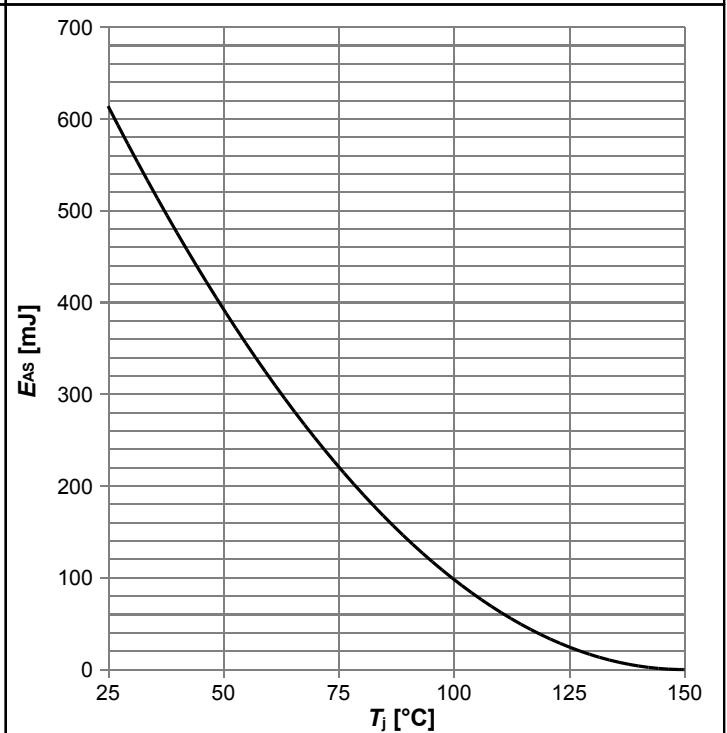
$V_{GS} = f(Q_{gate}); I_D = 14 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

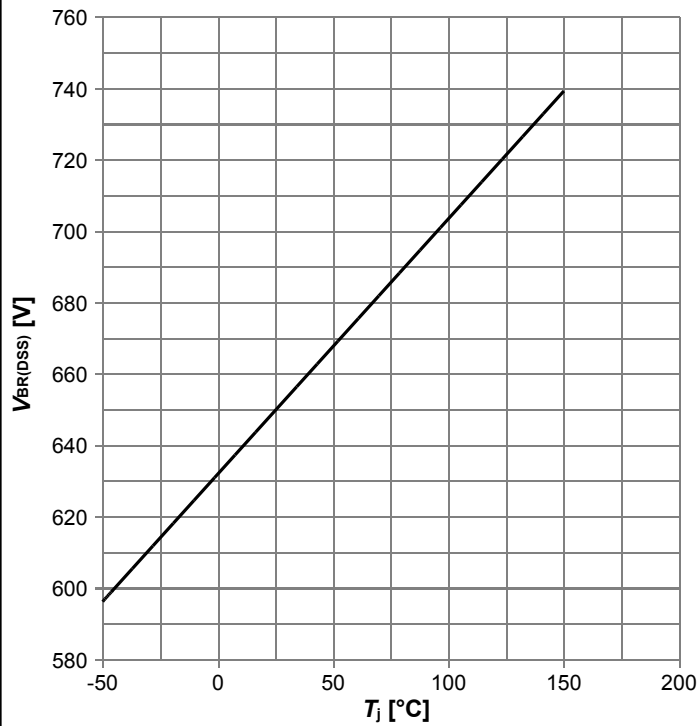


$E_{AS} = f(T_j); I_D = 4.3 \text{ A}; V_{DD} = 50 \text{ V}$

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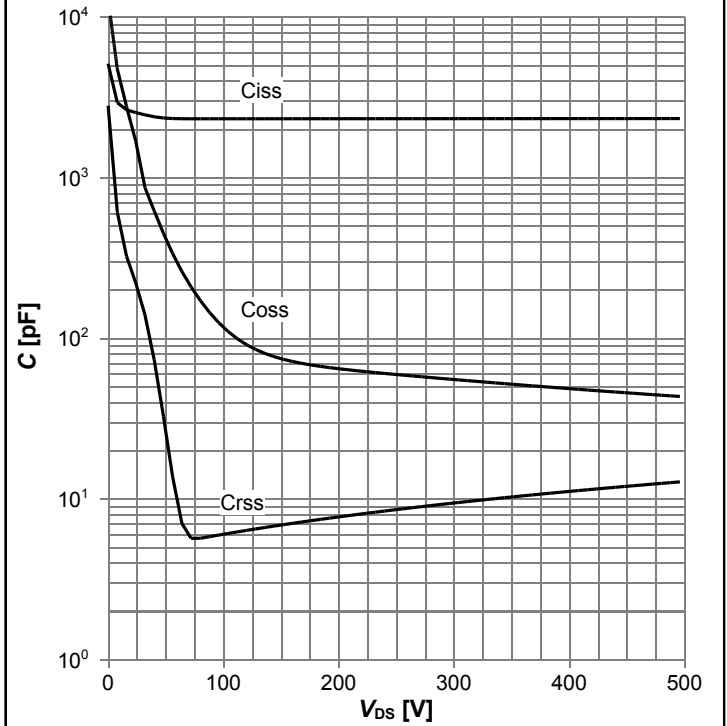
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Diagram 13: Drain-source breakdown voltage



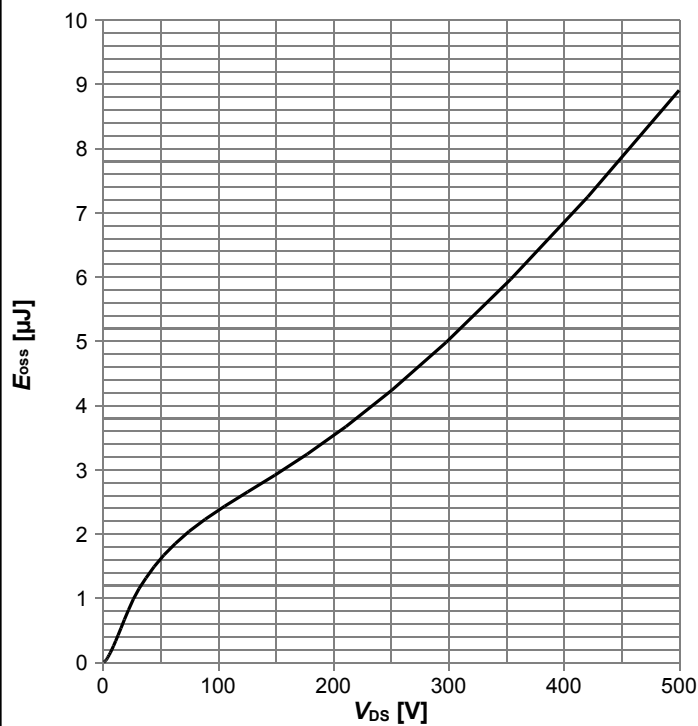
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

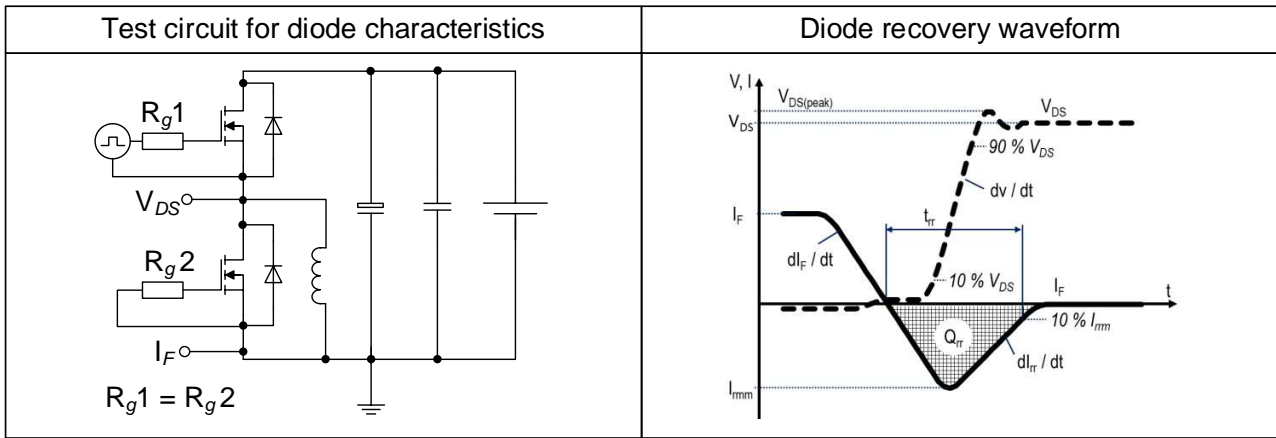


Table 9 switching times (ss)

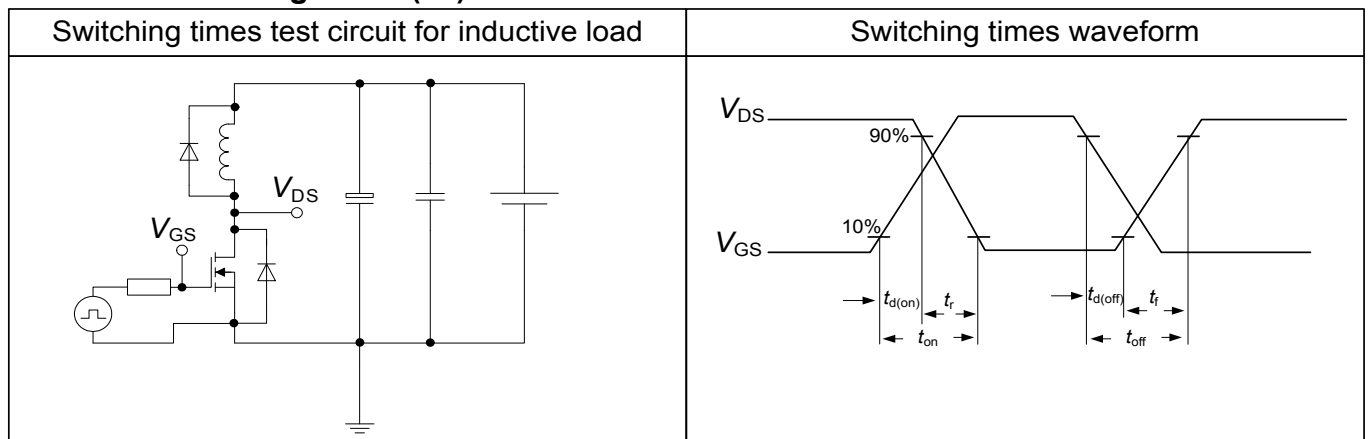
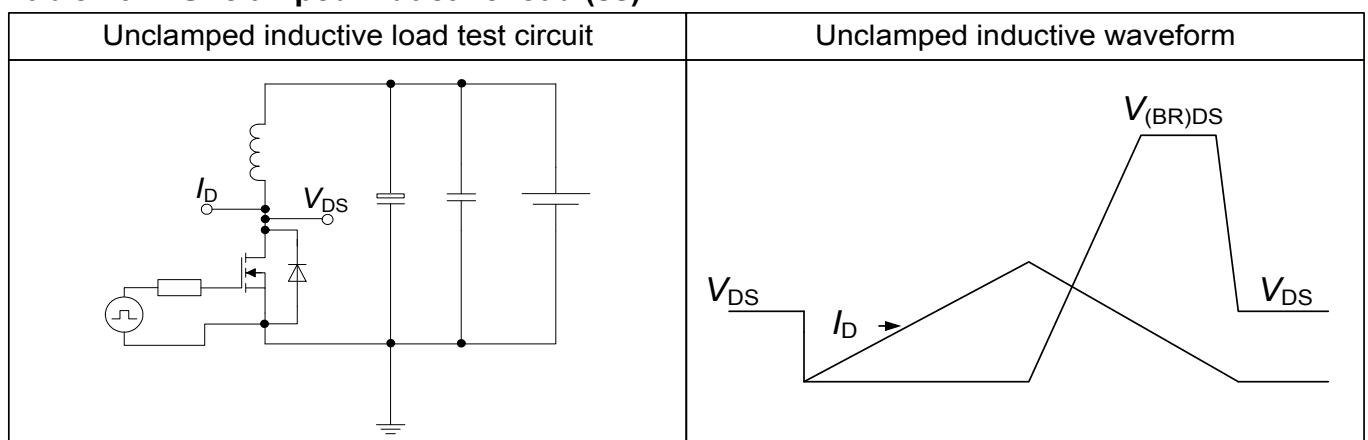


Table 10 Unclamped inductive load (ss)



6 Package Outlines

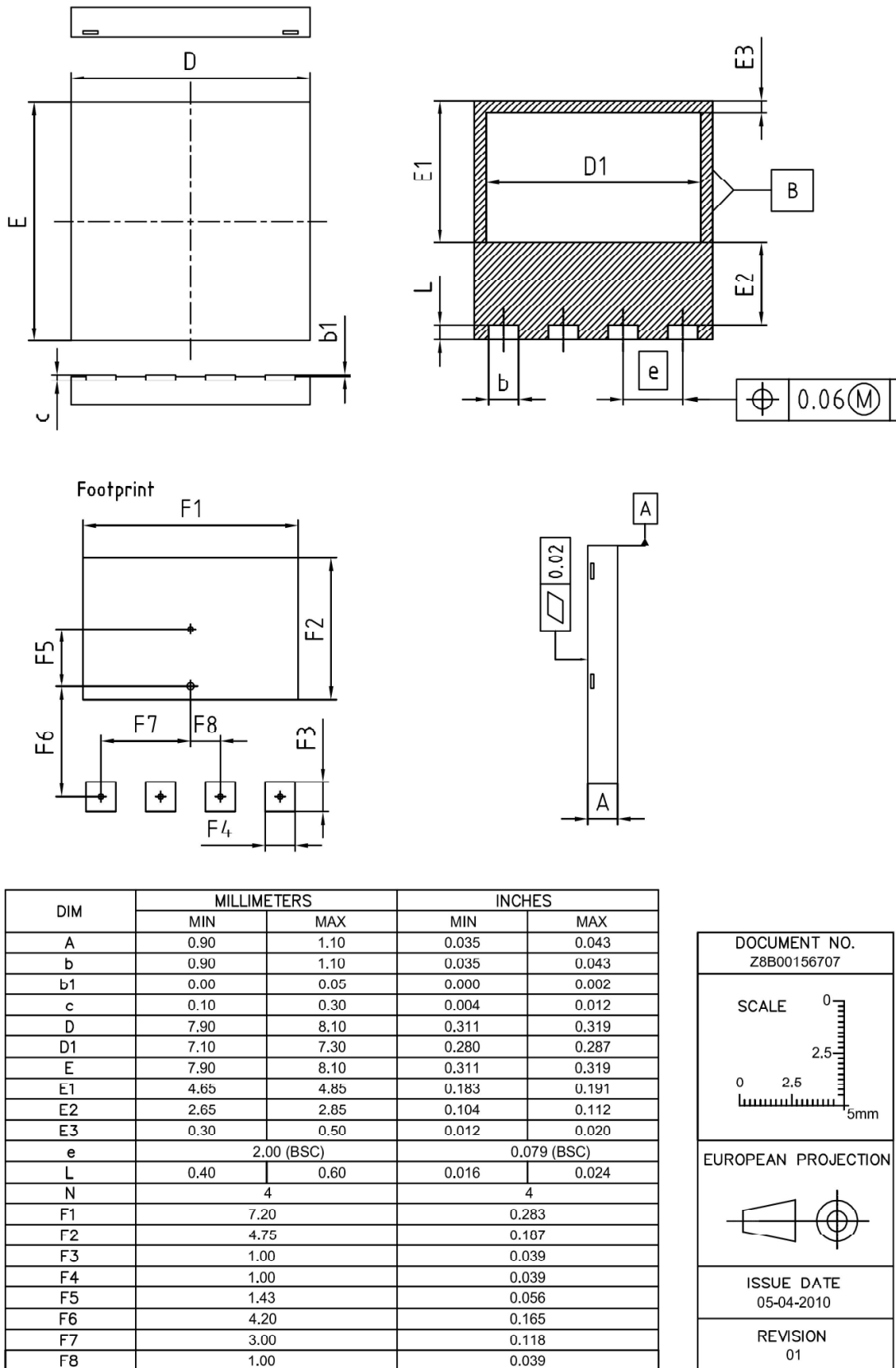


Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPL65R165CFD

Revision: 2017-09-07, Rev. 2.1

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2014-03-19 | Release of final version |
| 2.1 | 2017-09-07 | Updated MSL; style updated |

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