

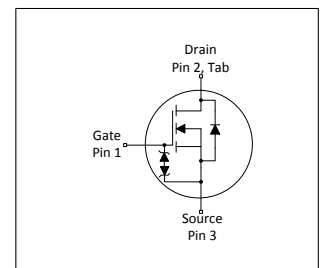
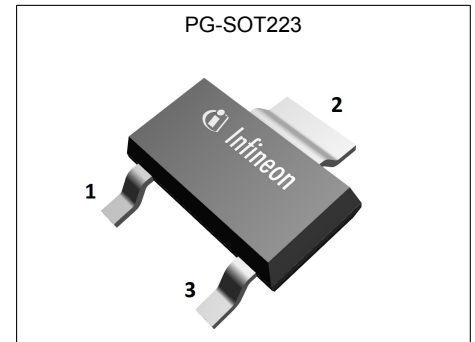
## MOSFET

### 700V CoolMOS™ P7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

The latest CoolMOS™ P7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, lighting, TV, etc.

The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- Excellent thermal behavior
- Integrated ESD protection diode
- Low switching losses ( $E_{oss}$ )
- Product validation acc. JEDEC Standard

### Benefits

- Cost competitive technology
- Lower temperature
- High ESD ruggedness
- Enables efficiency gains at higher switching frequencies
- Enables high power density designs and small form factors

### Potential applications

Recommended for Flyback topologies for example used in Chargers, Adapters, Lighting Applications, etc.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J=25^{\circ}C$	700	V
$R_{DS(on),max}$	1.2	$\Omega$
$Q_{g,typ}$	4.8	nC
$I_{D,pulse}$	9.4	A
$E_{oss} @ 400V$	0.7	$\mu J$
$V_{(GS)th,typ}$	3	V
ESD class (HBM)	1C	

Type / Ordering Code	Package	Marking	Related Links
IPN70R1K2P7S	PG-SOT223	70S1K2	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	4.5 3.0	A	$T_C = 20^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	9.4	A	$T_C=25^\circ\text{C}$
Application (Flyback) relevant avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	-	1.6	A	measured with standard leakage inductance of transformer of $5\mu\text{H}$
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	$V_{GS}$	-16 -30	-	16 30	V	static; AC ( $f > 1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	6.3	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	1.5	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	9.4	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>4)</sup>	dv/dt	-	-	1	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Maximum diode commutation speed <sup>4)</sup>	di/dt	-	-	50	A/ $\mu\text{s}$	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{ min}$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	$R_{thJS}$	-	-	19.7	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient for minimal footprint	$R_{thJA}$	-	-	160	$^\circ\text{C/W}$	minimal footprint
Thermal resistance, junction - ambient soldered on copper area	$R_{thJA}$	-	-	75	$^\circ\text{C/W}$	Device on $40\text{mm} \times 40\text{mm} \times 1.5$ epoxy PCB FR4 with $6\text{cm}^2$ (one layer $70\mu\text{m}$ thick) copper area for drain connection and cooling. PCB is vertical without blown air.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	$^\circ\text{C}$	reflow MSL1

<sup>1)</sup> DPAK / IPAK equivalent. Limited by  $T_{j,max}$ .  $T_j = 20^\circ\text{C}$ . Maximum duty cycle  $D=0.5$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Proven during verification test. For explanation please read AN - CoolMOS™ 700V P7.

<sup>4)</sup>  $V_{DClink}=400\text{V}$ ;  $V_{DS,peak} < V_{(BR)DSS}$ ; identical low side and high side switch with identical  $R_G$

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.04mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=700V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=700V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current incl. Zener diode	$I_{GSS}$	-	-	1	$\mu A$	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.98	1.20	$\Omega$	$V_{GS}=10V, I_D=0.9A, T_j=25^\circ C$ $V_{GS}=10V, I_D=0.9A, T_j=150^\circ C$
Gate resistance	$R_G$	-	1.6	-	$\Omega$	$f=1\text{ MHz}, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	174	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	3.6	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	10	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	132	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.6A,$ $R_G=8.2\Omega$
Rise time	$t_r$	-	4.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.6A,$ $R_G=8.2\Omega$
Turn-off delay time	$t_{d(off)}$	-	60	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.6A,$ $R_G=8.2\Omega$
Fall time	$t_f$	-	48	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.6A,$ $R_G=8.2\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	0.8	-	nC	$V_{DD}=400V, I_D=0.6A, V_{GS}=0\text{ to }10V$
Gate to drain charge	$Q_{gd}$	-	1.9	-	nC	$V_{DD}=400V, I_D=0.6A, V_{GS}=0\text{ to }10V$
Gate charge total	$Q_g$	-	4.8	-	nC	$V_{DD}=400V, I_D=0.6A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	$V_{DD}=400V, I_D=0.6A, V_{GS}=0\text{ to }10V$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=1.1A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	145	-	ns	$V_R=400V, I_F=0.6A, di_F/dt=50A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	0.5	-	$\mu C$	$V_R=400V, I_F=0.6A, di_F/dt=50A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	6	-	A	$V_R=400V, I_F=0.6A, di_F/dt=50A/\mu s$

### 4 Electrical characteristics diagrams

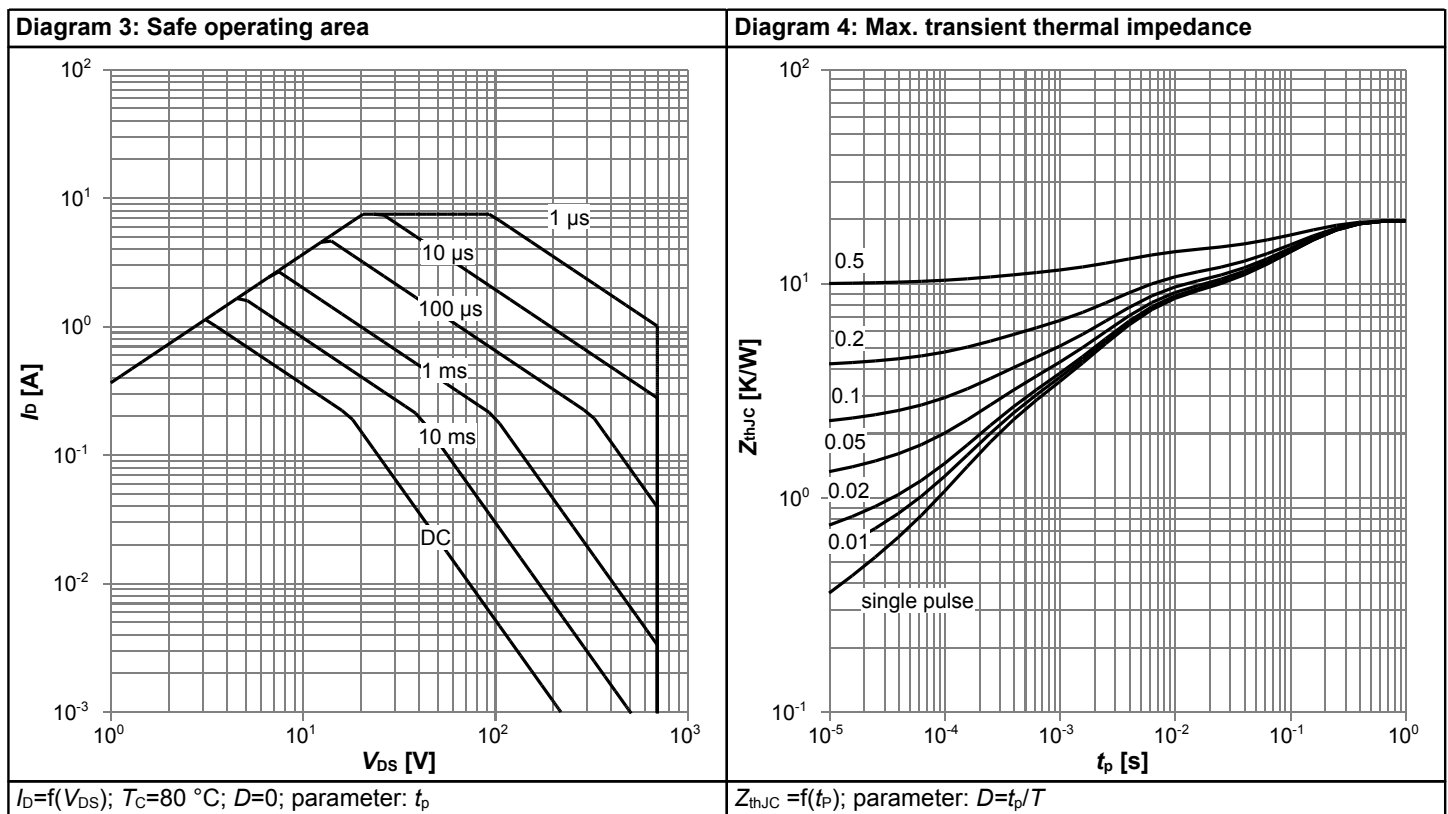
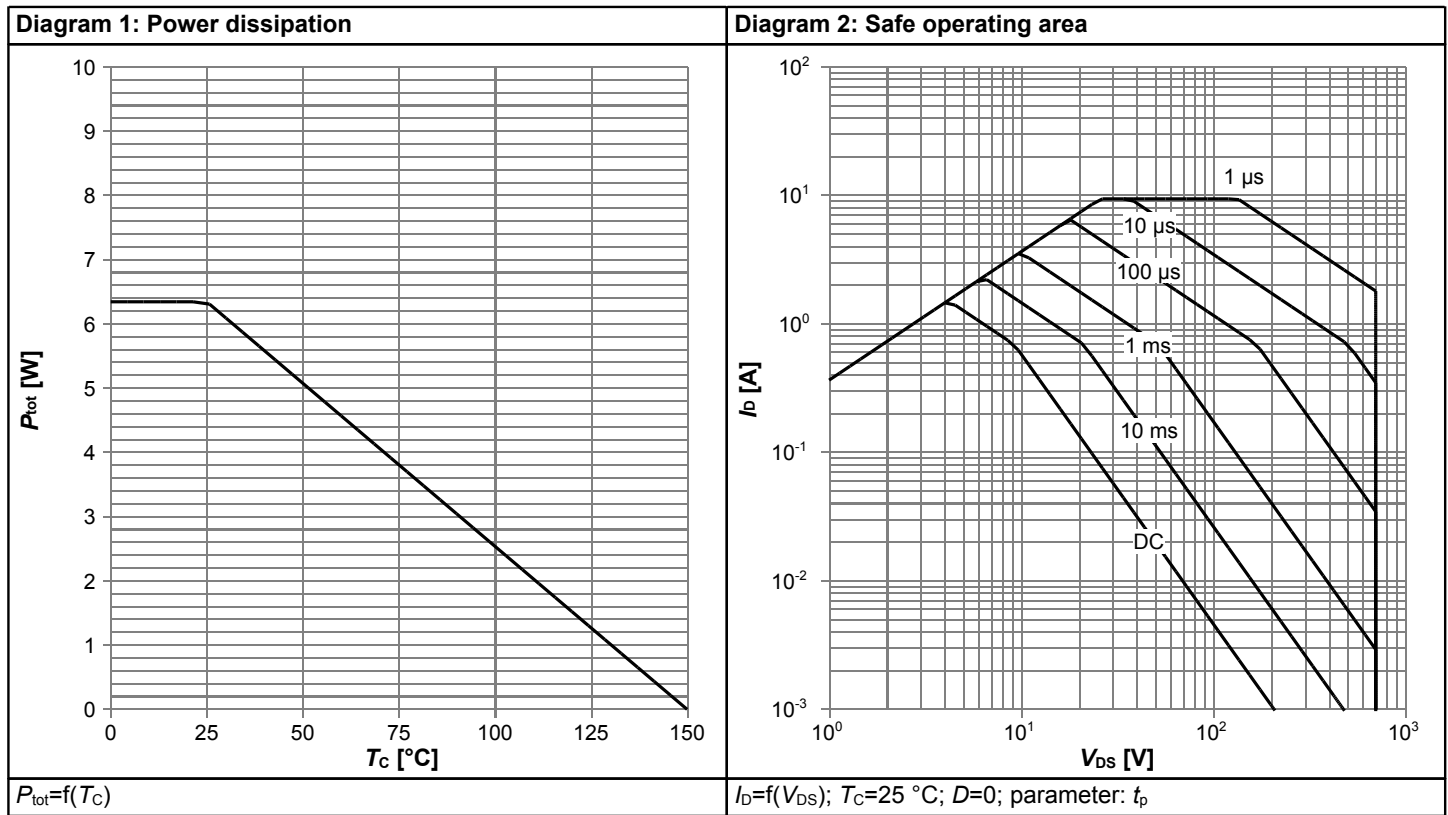
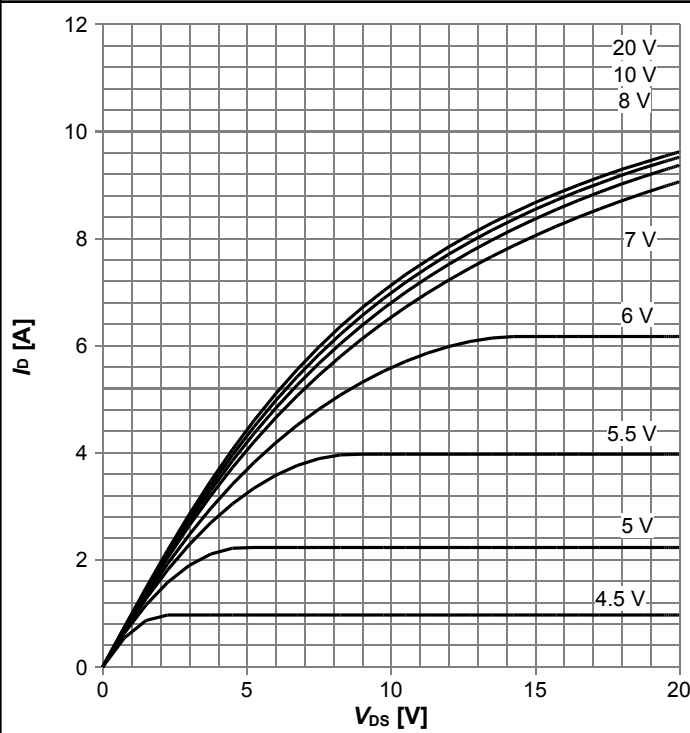
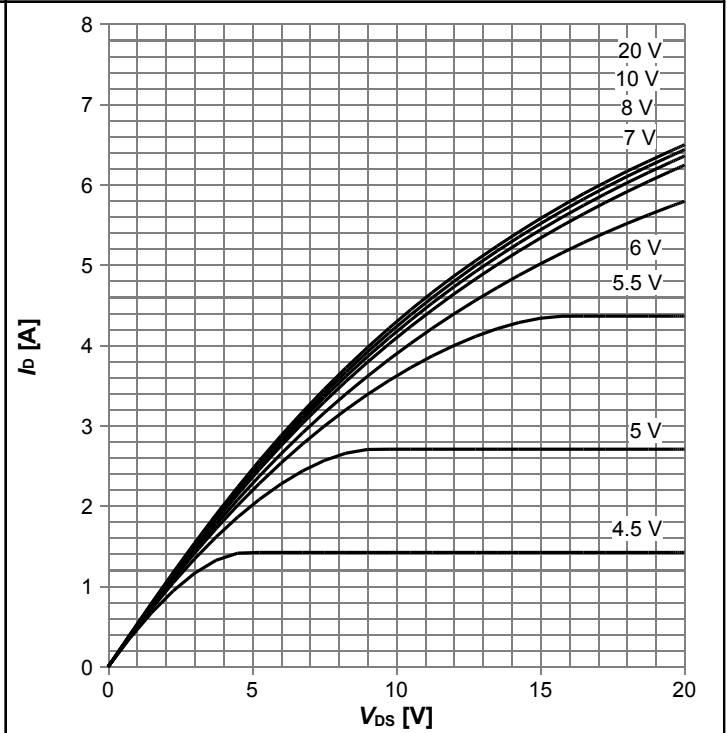


Diagram 5: Typ. output characteristics



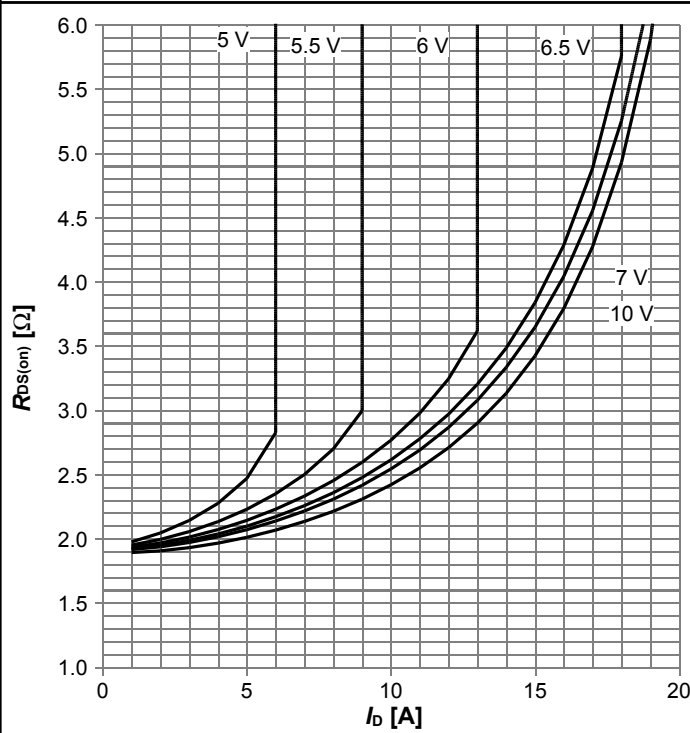
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



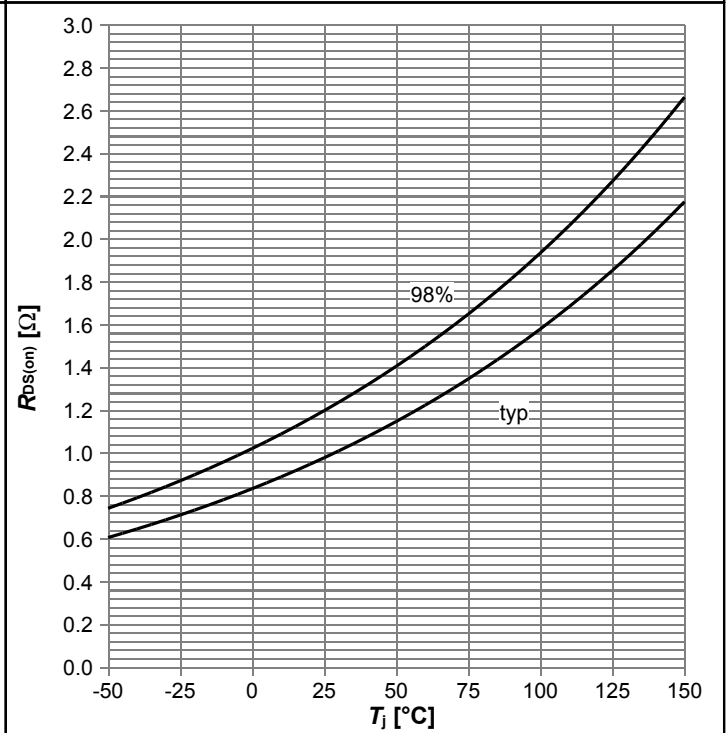
$I_D = f(V_{DS})$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



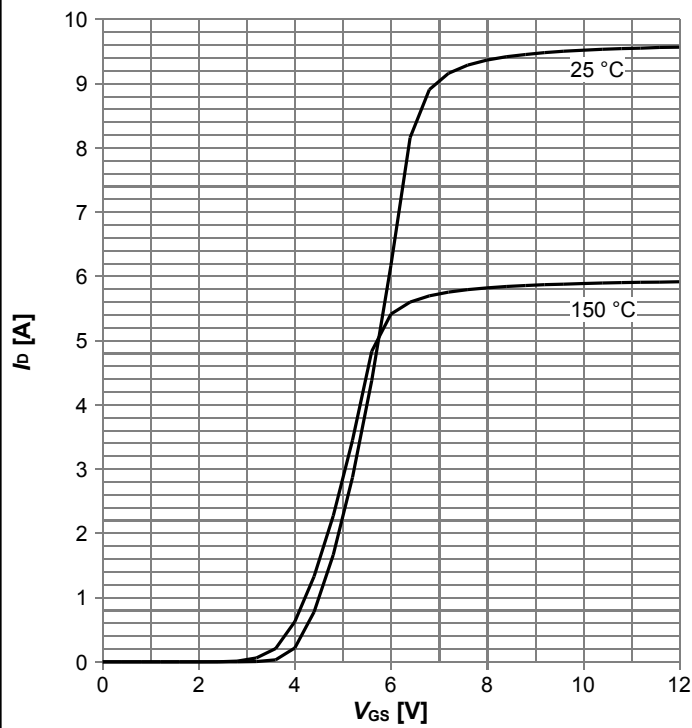
$R_{DS(on)} = f(I_D)$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



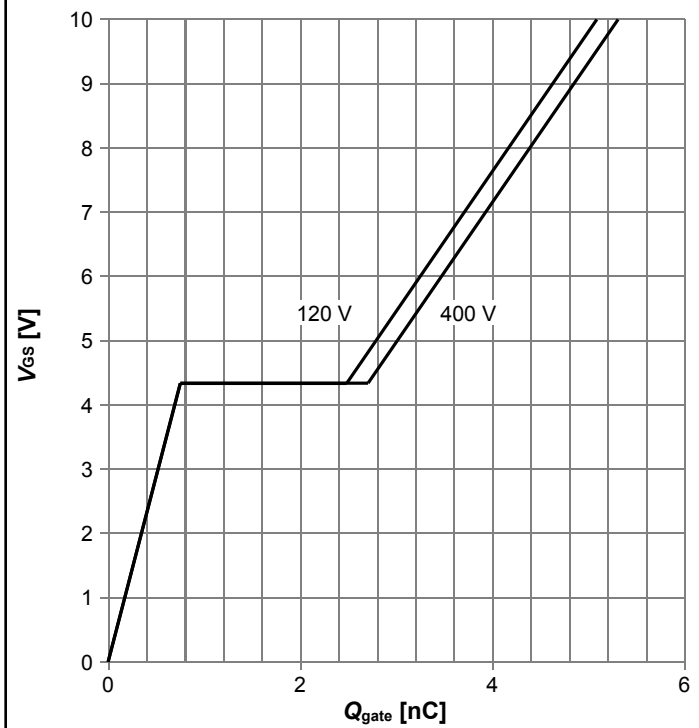
$R_{DS(on)} = f(T_j)$ ;  $I_D = 0.9\text{ A}$ ;  $V_{GS} = 10\text{ V}$

**Diagram 9: Typ. transfer characteristics**



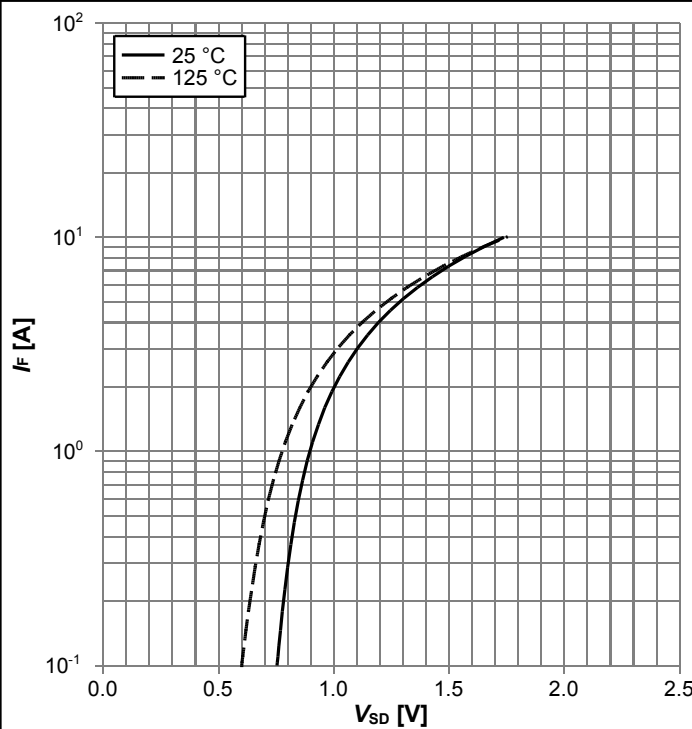
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

**Diagram 10: Typ. gate charge**



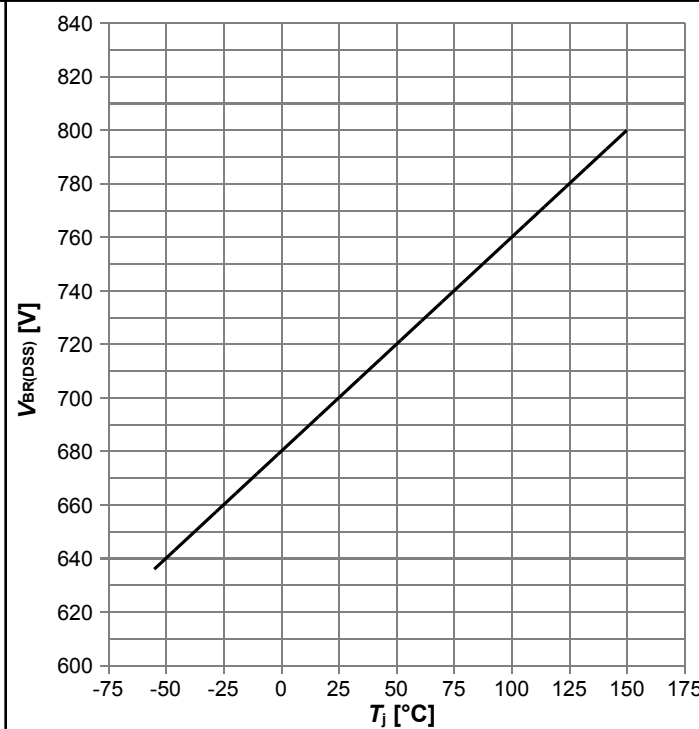
$V_{GS} = f(Q_{gate}); I_D = 0.6 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



$I_F = f(V_{SD}); \text{parameter: } T_j$

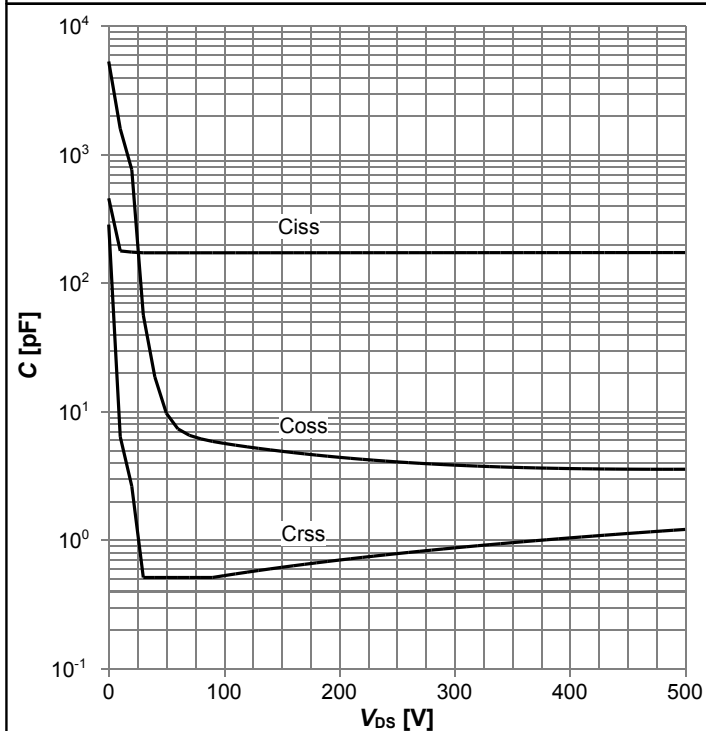
**Diagram 13: Drain-source breakdown voltage**



$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$

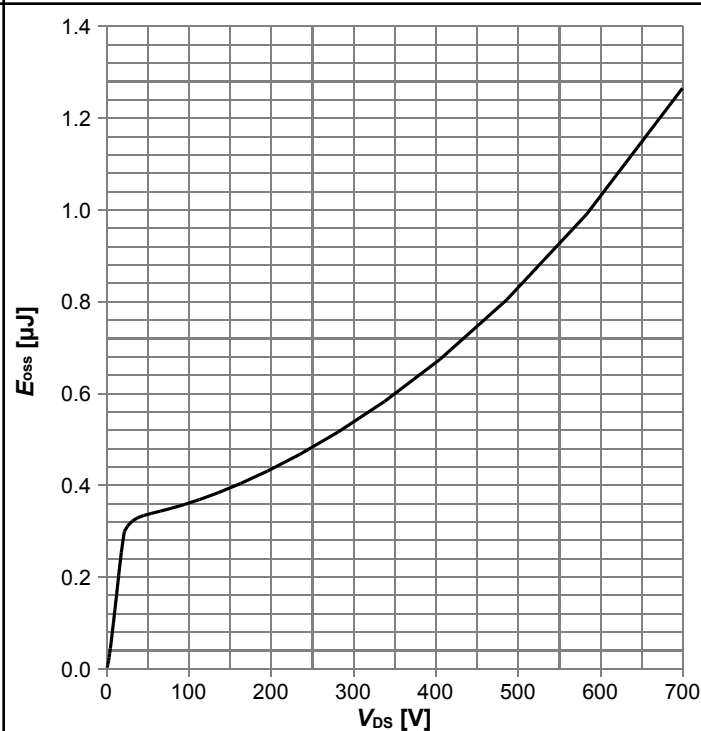


Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

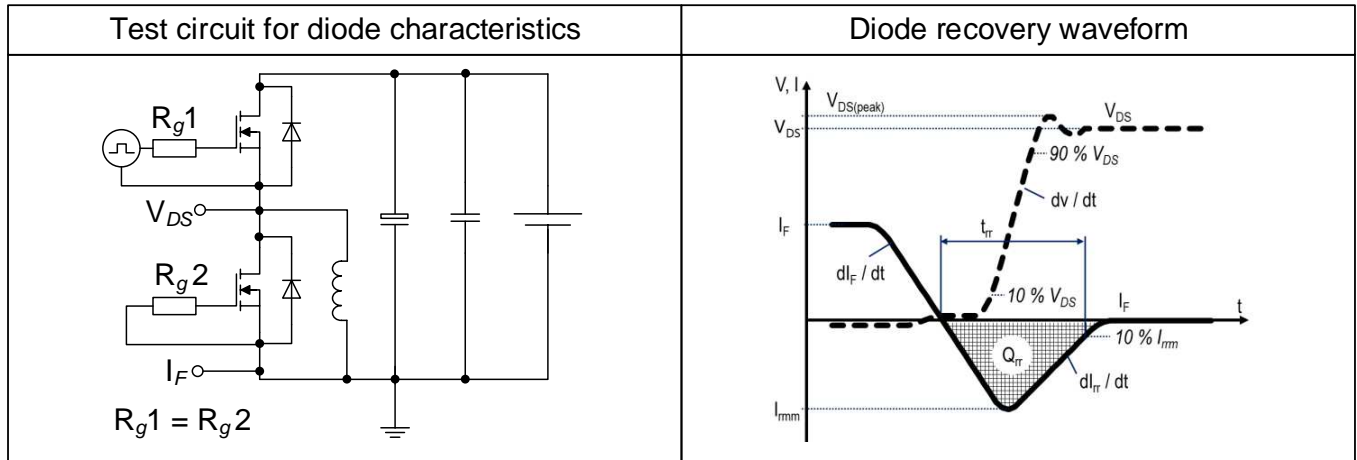
Diagram 15: Typ. Coss stored energy



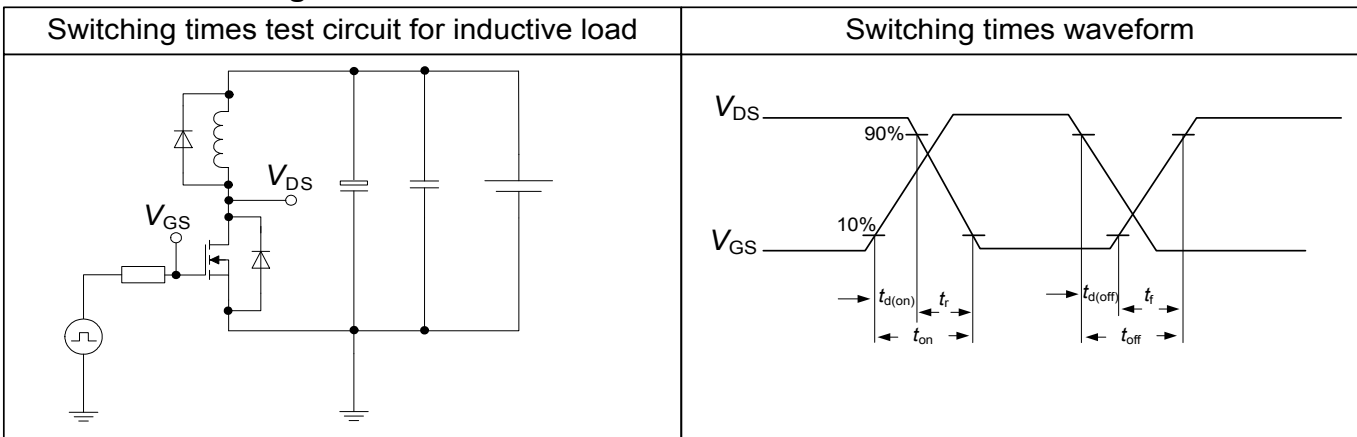
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

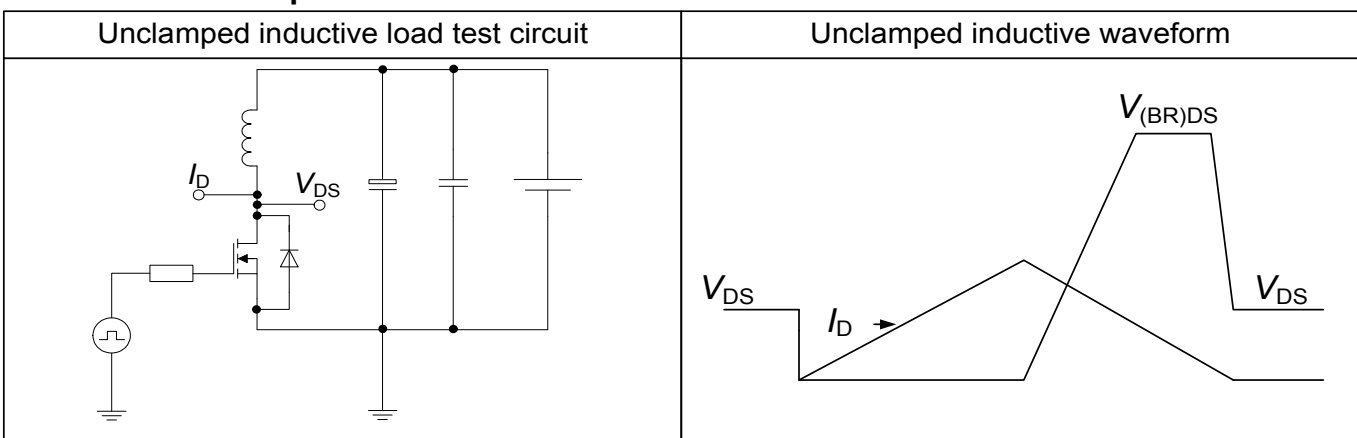
**Table 8 Diode characteristics**



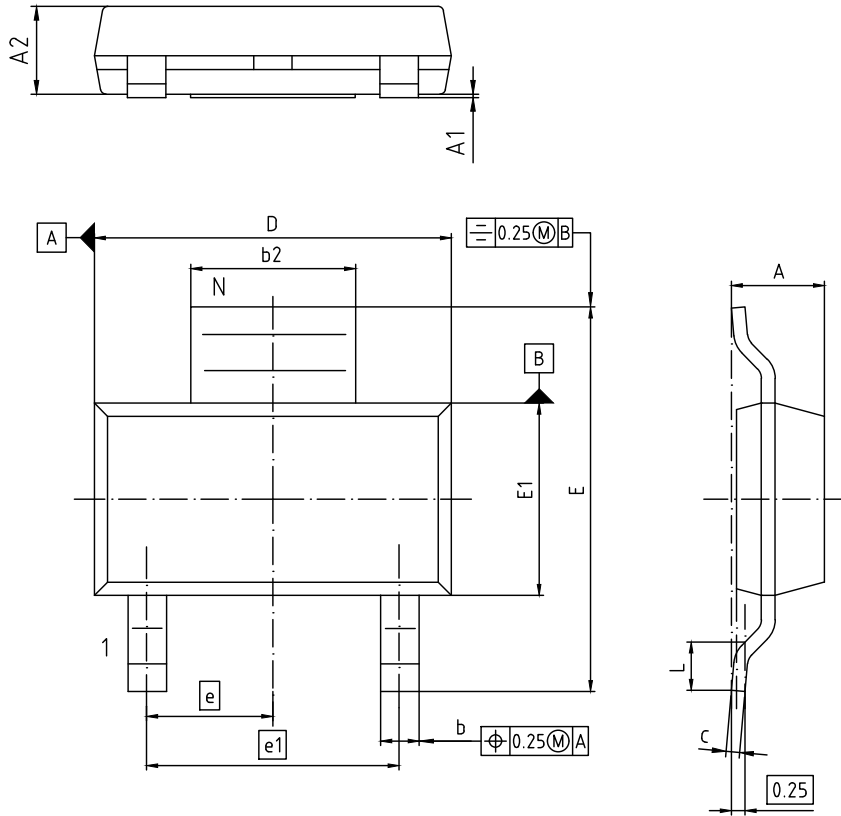
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

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Figure 1 Outline PG-SOT223, dimensions in mm/inches

## **7 Appendix A**

### **Table 11 Related Links**

- **IFX CoolMOS™ P7 Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

## Revision History

IPN70R1K2P7S

**Revision: 2018-02-12, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-09-15	Release of final version
2.1	2018-02-12	Corrected front page text

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