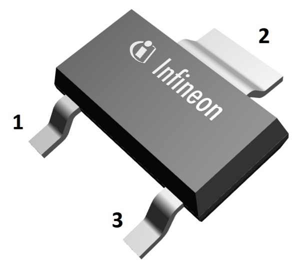
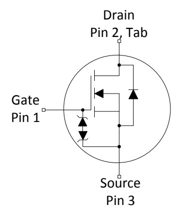
MOSFET

800V CoolMOS™ P7 Power Transistor

The latest 800V CoolMOS™ P7 series sets a new benchmark in 800V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

PG-SOT223





Features

- Best-in-class FOM $R_{DS(on)}$ * E_{oss}; reduced Q_g, C_{iss}, and C_{oss}
- Best-in-class DPAK $R_{DS(on)}$
- Best-in-class $V_{(GS)th}$ of 3V and smallest $V_{(GS)th}$ variation of ±0.5V
- Integrated Zener Diode ESD protection
- Fully qualified acc. JEDEC for Industrial Applications
- Fully optimized portfolio

Benefits

- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

Potential applications

Recommended for hard and soft switching flyback topologies for LED Lighting, low power Chargers and Adapters, Audio, AUX power and Industrial power. Also suitable for PFC stage in Consumer applications and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j=25°C}$	800	V
$R_{DS(on),max}$	0.90	Ω
$Q_{g,typ}$	15	nC
I_D	6	A
E_{oss} @ 500V	1.4	µJ
$V_{GS(th),typ}$	3	V
ESD class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPN80R900P7	PG-SOT223	80R900	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	6 3.9	A	T_C=25°C T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	14	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	13	mJ	I_D=0.9A; V_{DD}=50V
Avalanche energy, repetitive	E_{AR}	-	-	0.11	mJ	I_D=0.9A; V_{DD}=50V
Avalanche current, repetitive	I_{AR}	-	-	0.9	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0 to 400V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	7.0	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-
Continuous diode forward current	I_S	-	-	1.7	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	14	A	T_C=25°C
Reverse diode dv/dt[3)]	dv/dt	-	-	1	V/ns	V_{DS}=0 to 400V, I_{SD}<=1.1A, T_j=25°C
Maximum diode commutation speed[3)]	di_f/dt	-	-	50	A/µs	V_{DS}=0 to 400V, I_{SD}<=1.1A, T_j=25°C

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJS}	-	-	17.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	160	°C/W	Device on PCB, minimal footprint
Thermal resistance, junction - ambient soldered on copper area	R_{thJA}	-	-	75	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) DPAK equivalent. Limited by $T_{j\,max}$. Maximum duty cycle D=0.5
2) Pulse width t_p limited by $T_{j,max}$
3) V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G; t_{cond}<2µs

3 Electrical characteristics

at T_j = 25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	V_{DS}=V_{GS}, I_D=0.11mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=800V, V_{GS}=0V, T_j=25°C V_{DS}=800V, V_{GS}=0V, T_j=150°C
Gate-source leakage curent incl. zener diode	I_{GSS}	-	-	1	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.77 1.99	0.90 -	Ω	V_{GS}=10V, I_D=2.2A, T_j=25°C V_{GS}=10V, I_D=2.2A, T_j=150°C
Gate resistance	R_G	-	1.4	-	Ω	f=250kHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	350	-	pF	V_{GS}=0V, V_{DS}=500V, f=250kHz
Output capacitance	C_{oss}	-	6	-	pF	V_{GS}=0V, V_{DS}=500V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	11	-	pF	V_{GS}=0V, V_{DS}=0 to 500V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	135	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0 to 500V
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15Ω
Rise time	t_r	-	8	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15Ω
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15Ω
Fall time	t_f	-	20	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=15Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2	-	nC	V_{DD}=640V, I_D=2.2A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	6	-	nC	V_{DD}=640V, I_D=2.2A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	15	-	nC	V_{DD}=640V, I_D=2.2A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	V_{DD}=640V, I_D=2.2A, V_{GS}=0 to 10V

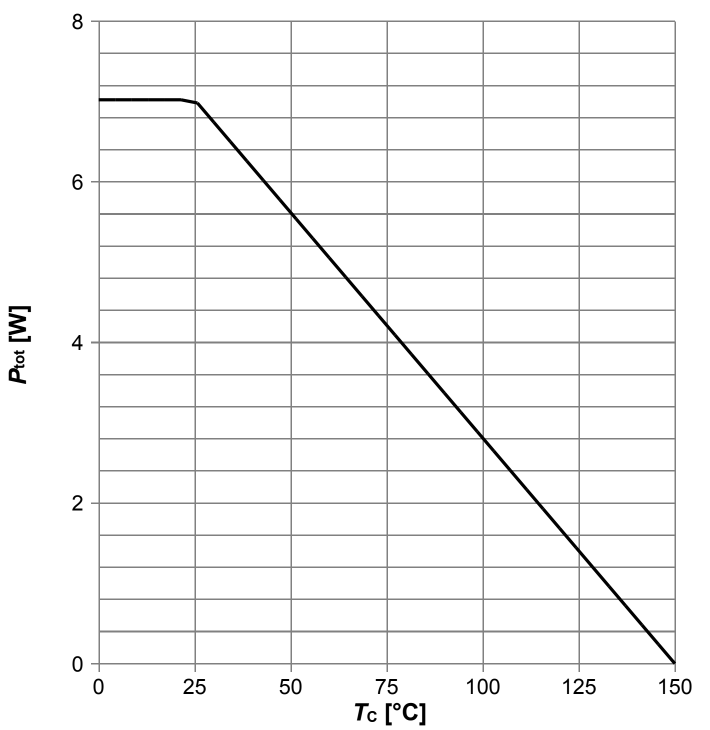
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=2.2A, T_j=25°C
Reverse recovery time	t_{rr}	-	610	-	ns	V_R=400V, I_F=1.1A, di_F/dt=50A/µs
Reverse recovery charge	Q_{rr}	-	5	-	µC	V_R=400V, I_F=1.1A, di_F/dt=50A/µs
Peak reverse recovery current	I_{rrm}	-	11	-	A	V_R=400V, I_F=1.1A, di_F/dt=50A/µs

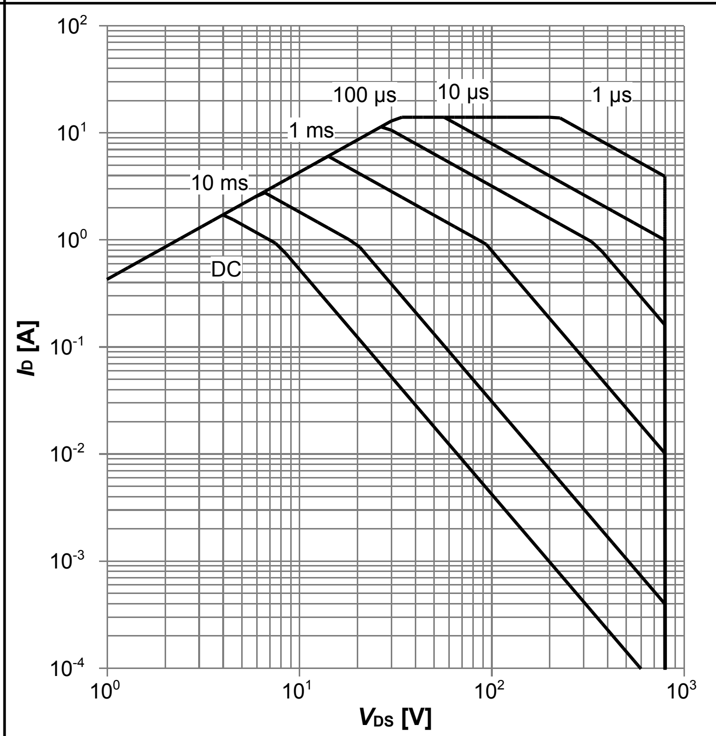
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



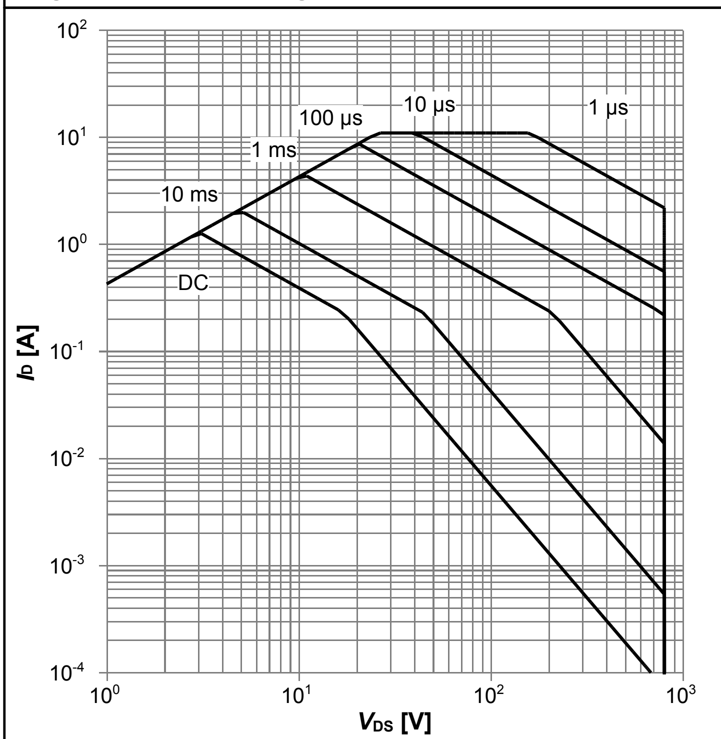
P_{tot}=f(T_C)

Diagram 2: Safe operating area



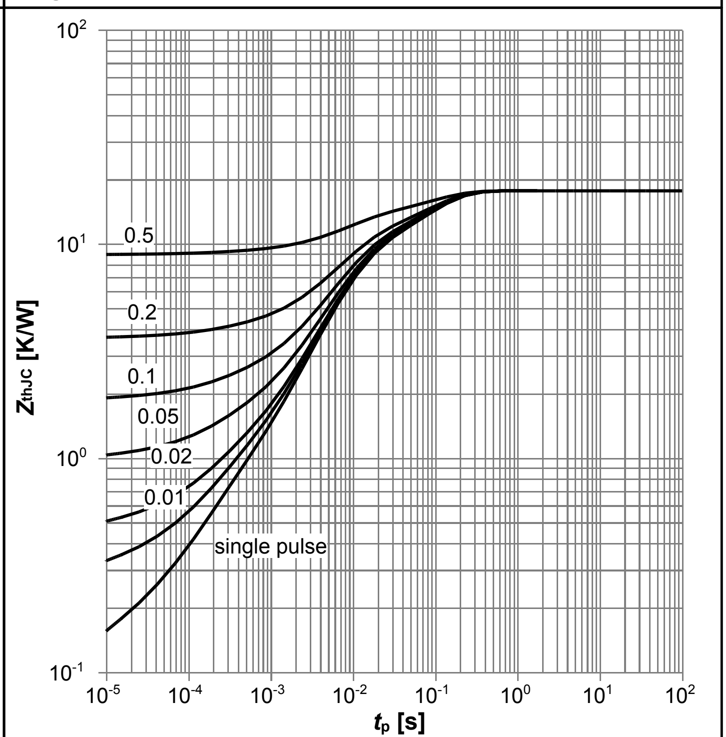
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



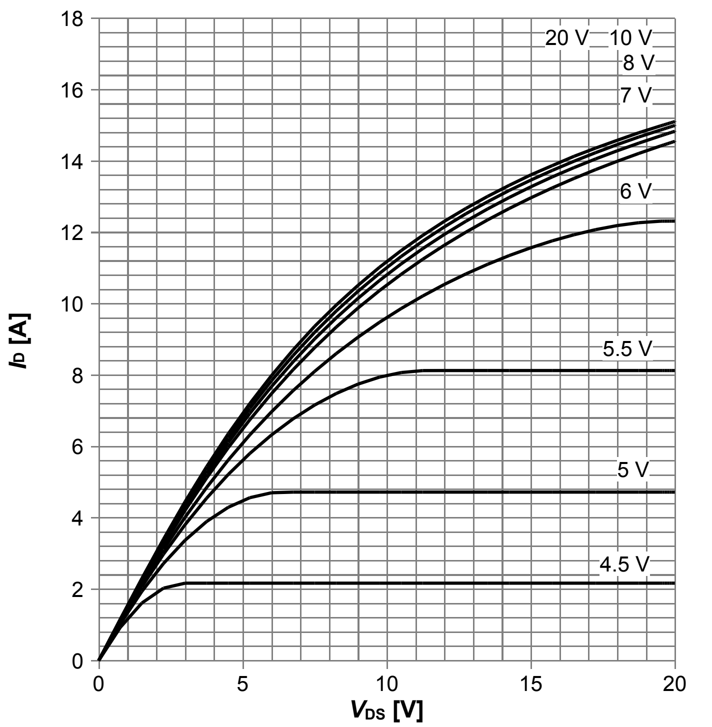
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



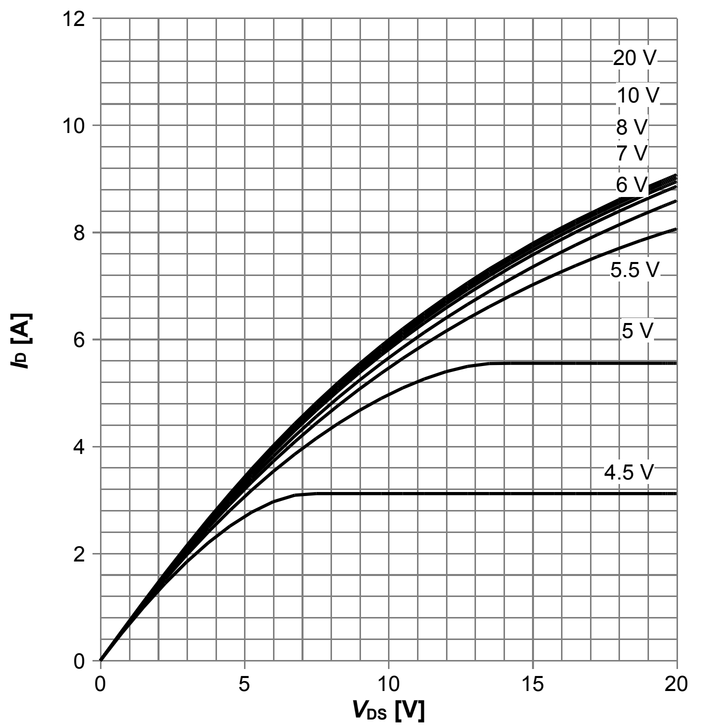
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



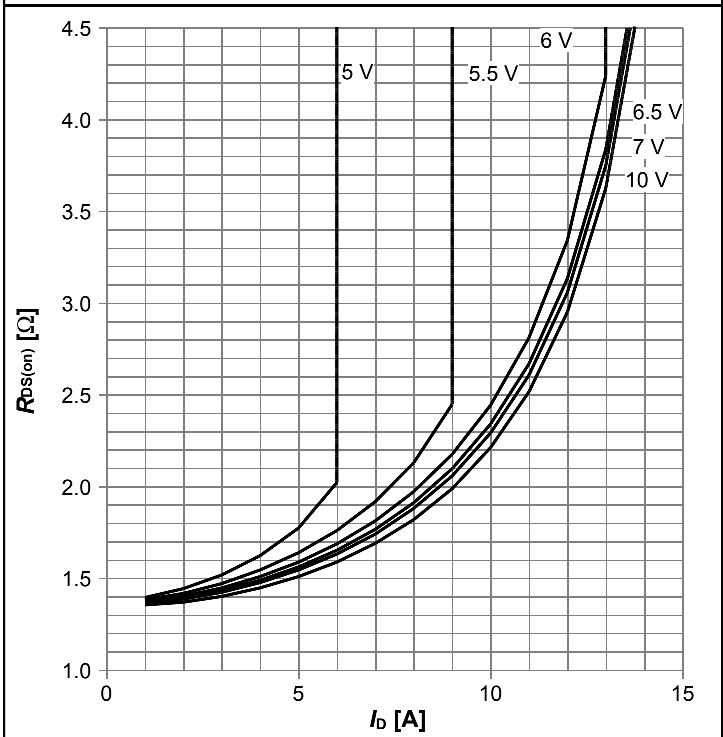
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



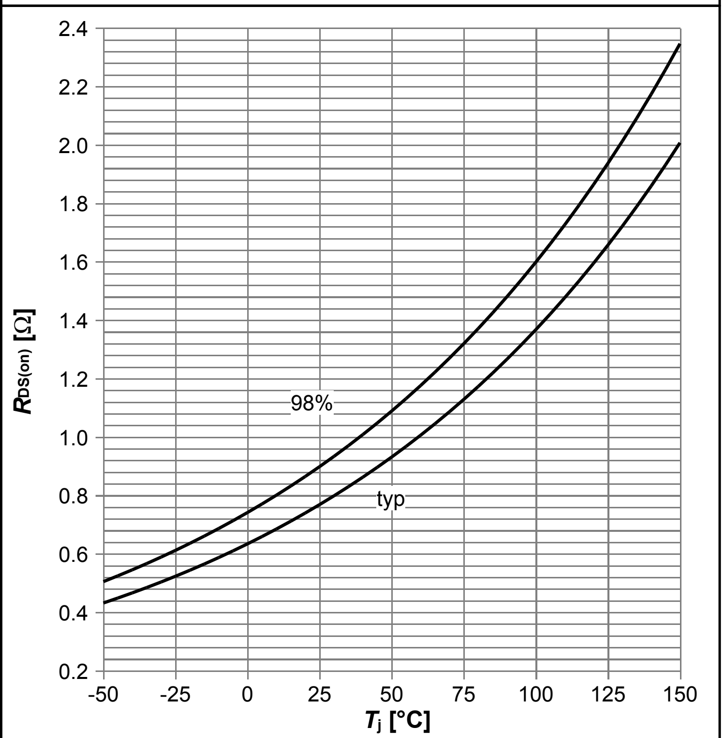
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



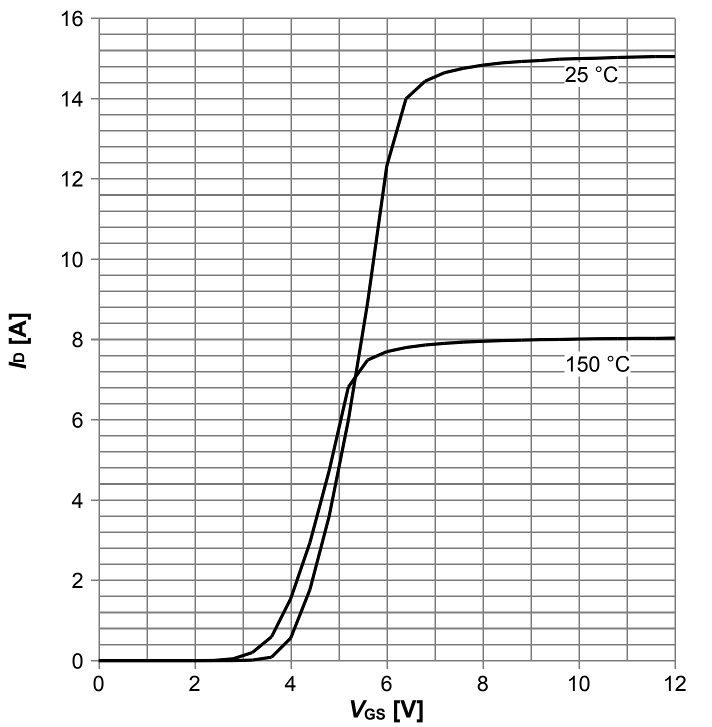
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



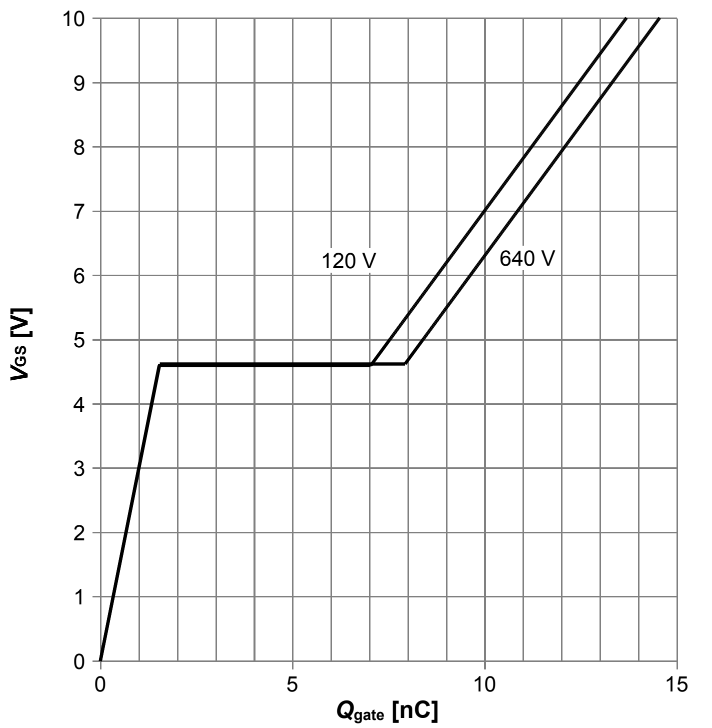
$R_{DS(on)}$=f(T_j); I_D=2.2 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



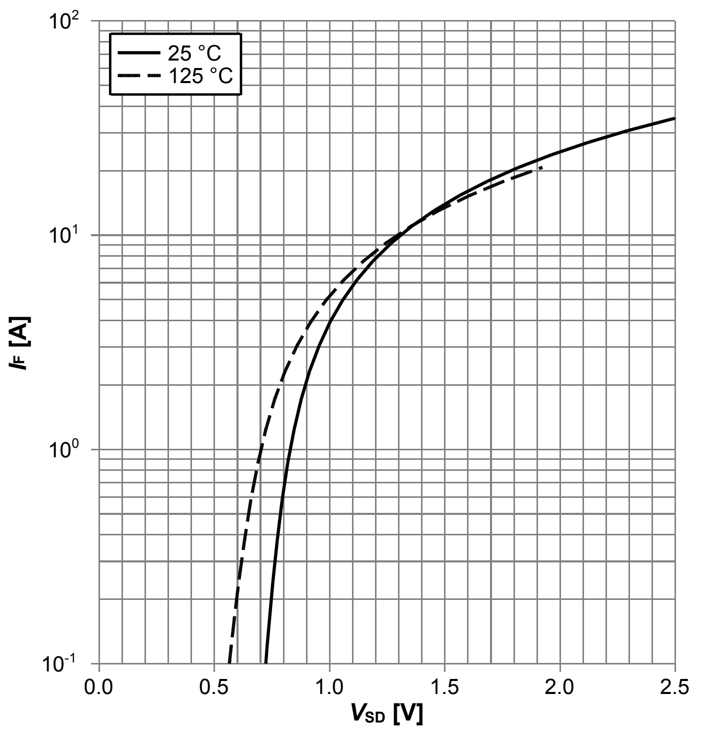
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



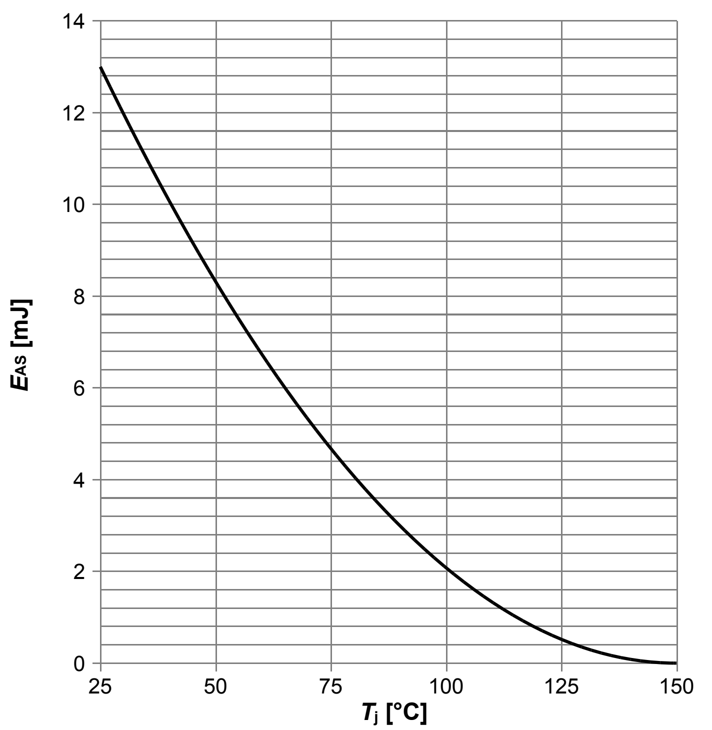
V_{GS}=f(Q_{gate}); I_D=2.2 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



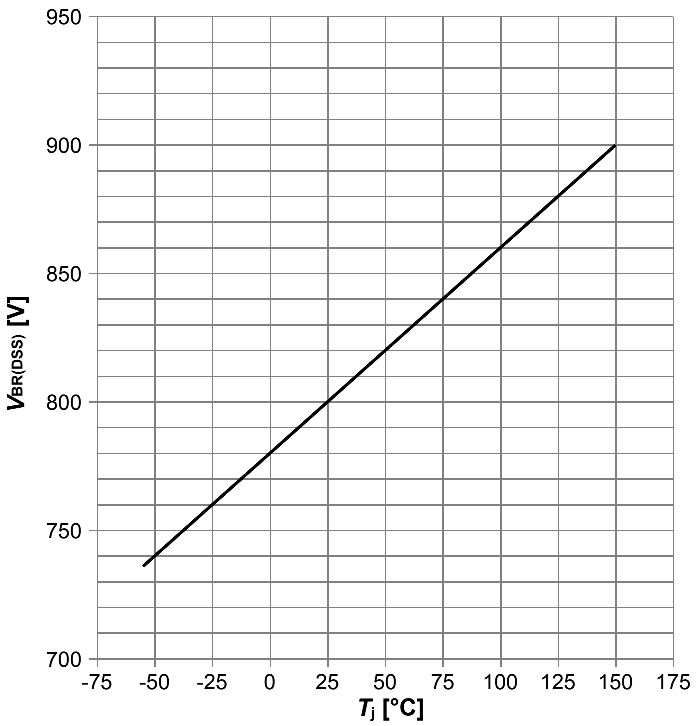
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



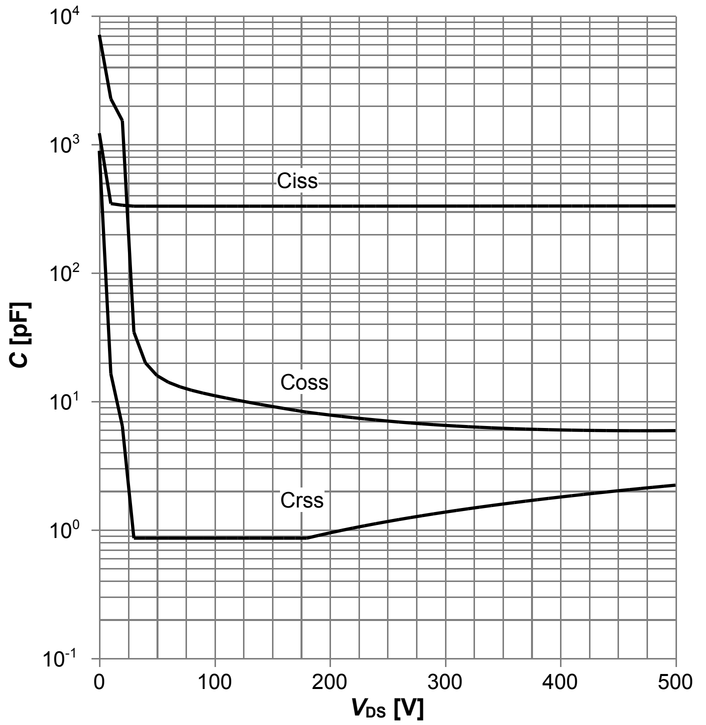
E_{AS}=f(T_j); I_D=0.9 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



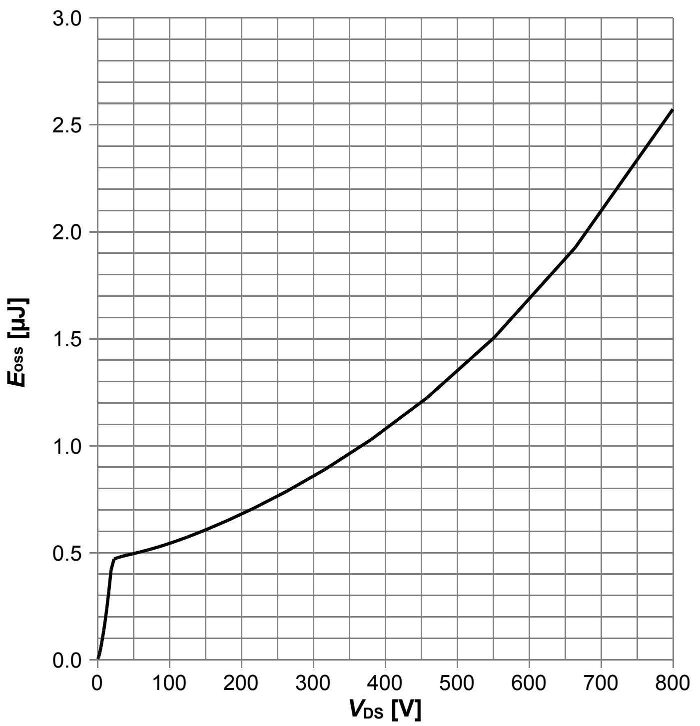
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

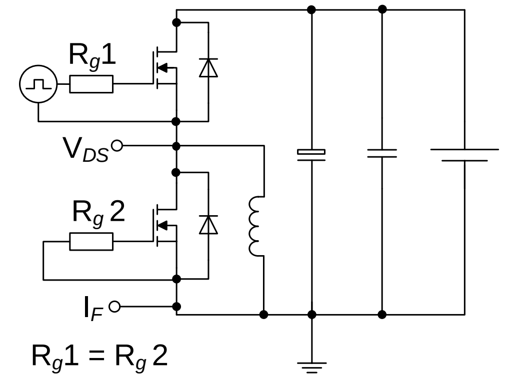
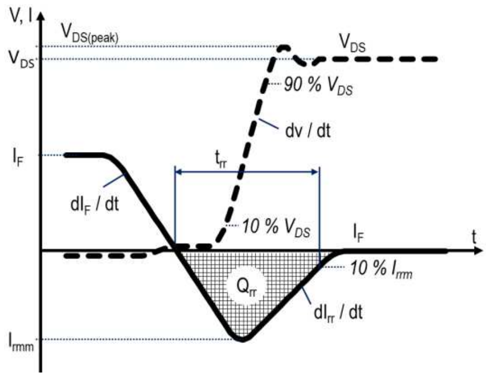
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

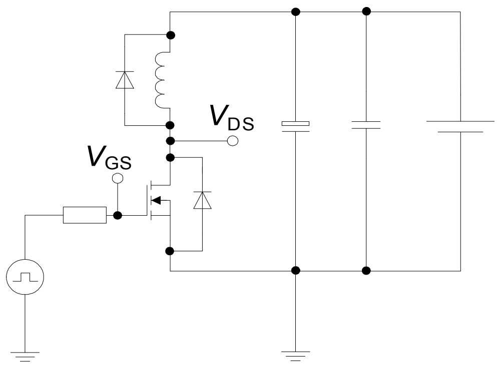
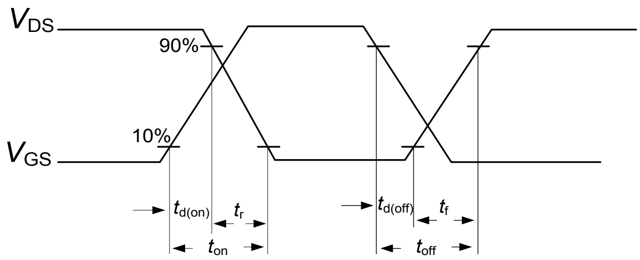
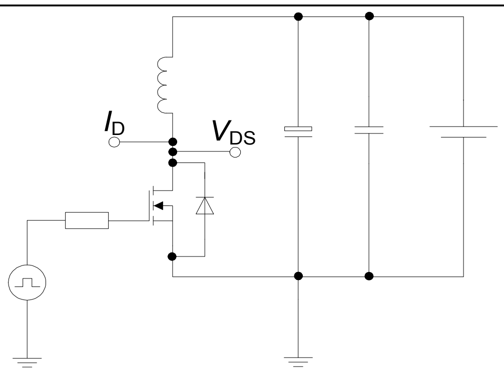
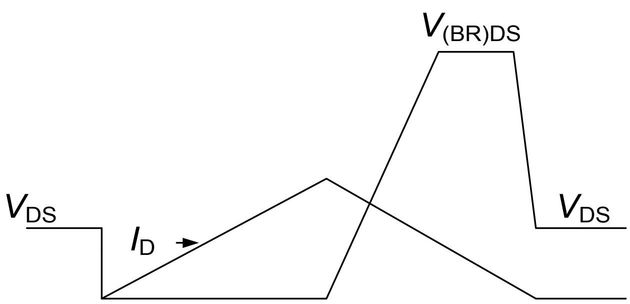
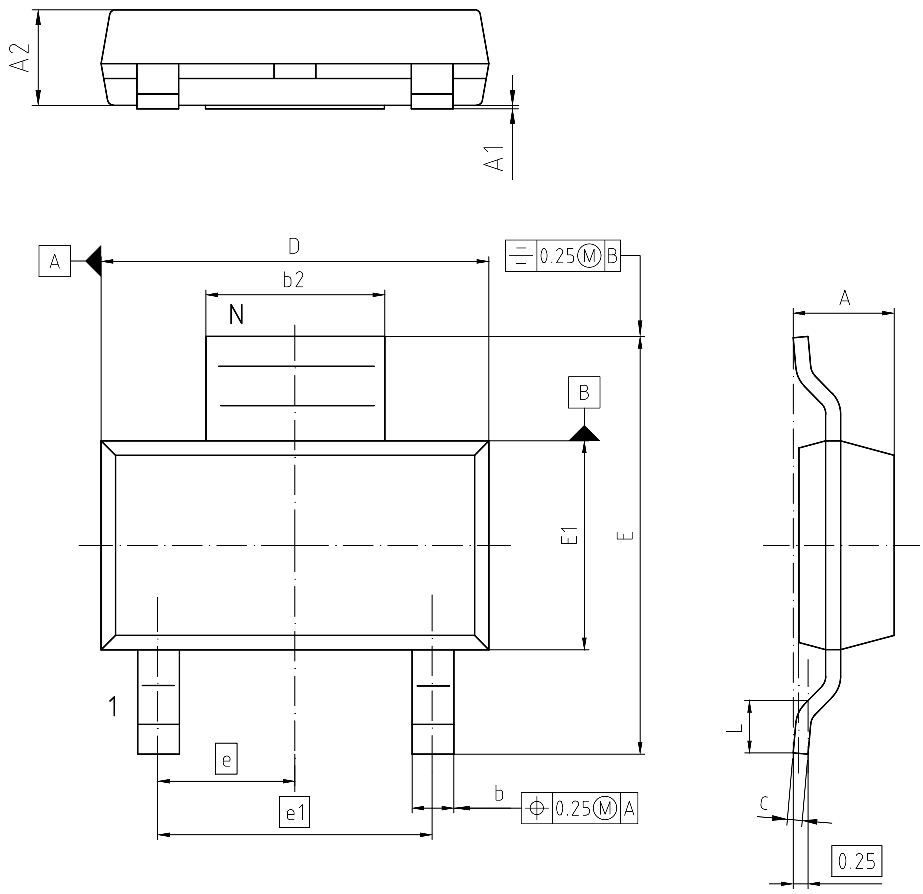
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS	
	MIN	MAX
A	1.52	1.80
A1	-	0.10
A2	1,50	1.70
b	0.60	0.80
b2	2.95	3.10
c	0.24	0.32
D	6.30	6.70
E	6.70	7.30
E1	3.30	3.70
e	2.3 BASIC	
e1	4.6 BASIC	
L	0.75	1.10
N	3	
O	0°	10°

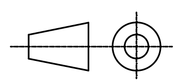
NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DOCUMENT NO.
Z8B00180553

SCALE 0 2.5 5mm

EUROPEAN PROJECTION



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01

Figure 1 Outline PG-SOT223, dimensions in mm - Industrial Grade

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPN80R900P7

Revision: 2018-02-09, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-06-23	Release of final version
2.1	2018-02-09	Corrected front page text

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