

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CFD2 650V

650V CoolMOS™ CFD2 Power Transistor
IPW65R080CFD

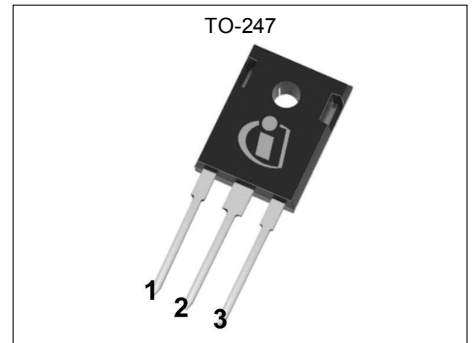
Data Sheet

Rev. 2.4
Final

Industrial & Multimarket

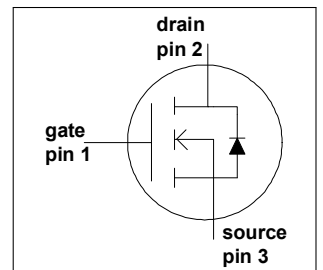
1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.



Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)



Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server, Telecom and Solar.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j \max}$	700	V
$R_{DS(on),max}$	0.08	Ω
Q_g,typ	167	nC
$I_D,pulse$	137	A
$E_{oss} @ 400V$	12.5	μJ
Body diode di/dt	900	A/ μs
Q_{rr}	1	μC
t_{rr}	180	ns
I_{rrm}	10	A

Type / Ordering Code	Package	Marking	Related Links
IPW65R080CFD	PG-TO 247	65F6080	see Appendix A



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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			43.3	A	$T_C = 25^\circ\text{C}$
				27.4		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			137	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			1160	mJ	$I_b = 8.7\text{A}$, $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}			1.76	mJ	$I_b = 8.7\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			8.7	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{Hz}$)
Power dissipation (non FullPAK) TO-247	P_{tot}			391.0	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Mounting torque (non FullPAK) TO-247				60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S			43.3	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			140	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_b$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed	di_f/dt			900	A/ μs	

¹⁾ Limited by $T_{j\text{ max}}$.

²⁾ Pulse width t_p limited by $T_{j\text{ max}}$

³⁾ $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j\text{ max}}$, identical low and high side switch with same R_g

3 Thermal characteristics

Table 3 Thermal characteristics TO-247

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			0.32	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}, I_D = 1.8mA$
Zero gate voltage drain current	I_{DSS}			2	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			500			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.072	0.08	Ω	$V_{GS} = 10V, I_D = 17.6A, T_j = 25^\circ C$
			0.187			$V_{GS} = 10V, I_D = 17.6A, T_j = 150^\circ C$
Gate resistance	R_G		0.7		Ω	$f = 1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		5030		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	C_{oss}		215		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		158		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		794		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		20		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 26.3A, R_G = 1.8\Omega$
Rise time	t_r		18		ns	
Turn-off delay time	$t_{d(off)}$		85		ns	
Fall time	t_f		6		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		32		nC	$V_{DD} = 480V, I_D = 26.3A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		87		nC	
Gate charge total	Q_g		167		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 26.3A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		180		ns	$V_R = 400V, I_F = 26.3A, dI/dt = 100A/\mu s$
Reverse recovery charge	Q_{rr}		1		μC	
Peak reverse recovery current	I_{rrm}		10		A	

5 Electrical characteristics diagrams

Table 8

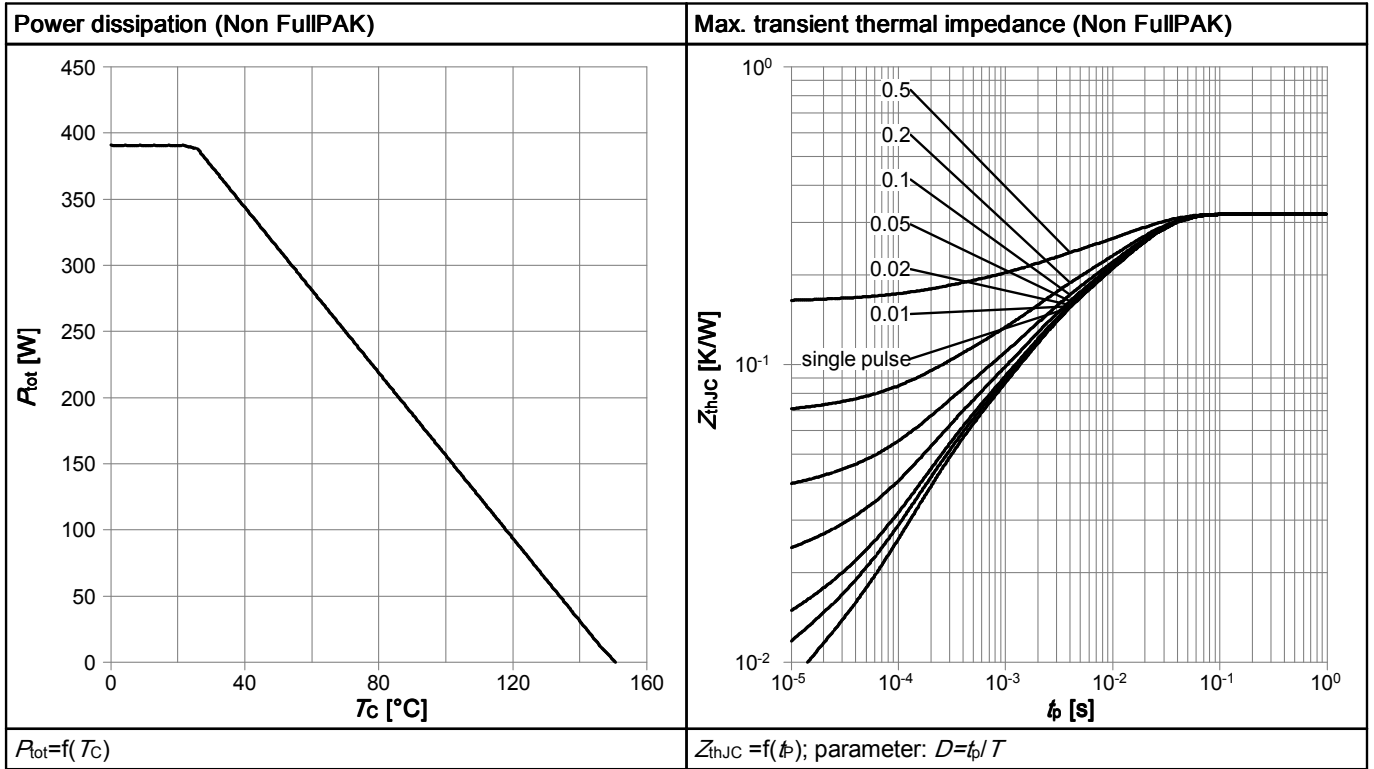


Table 9

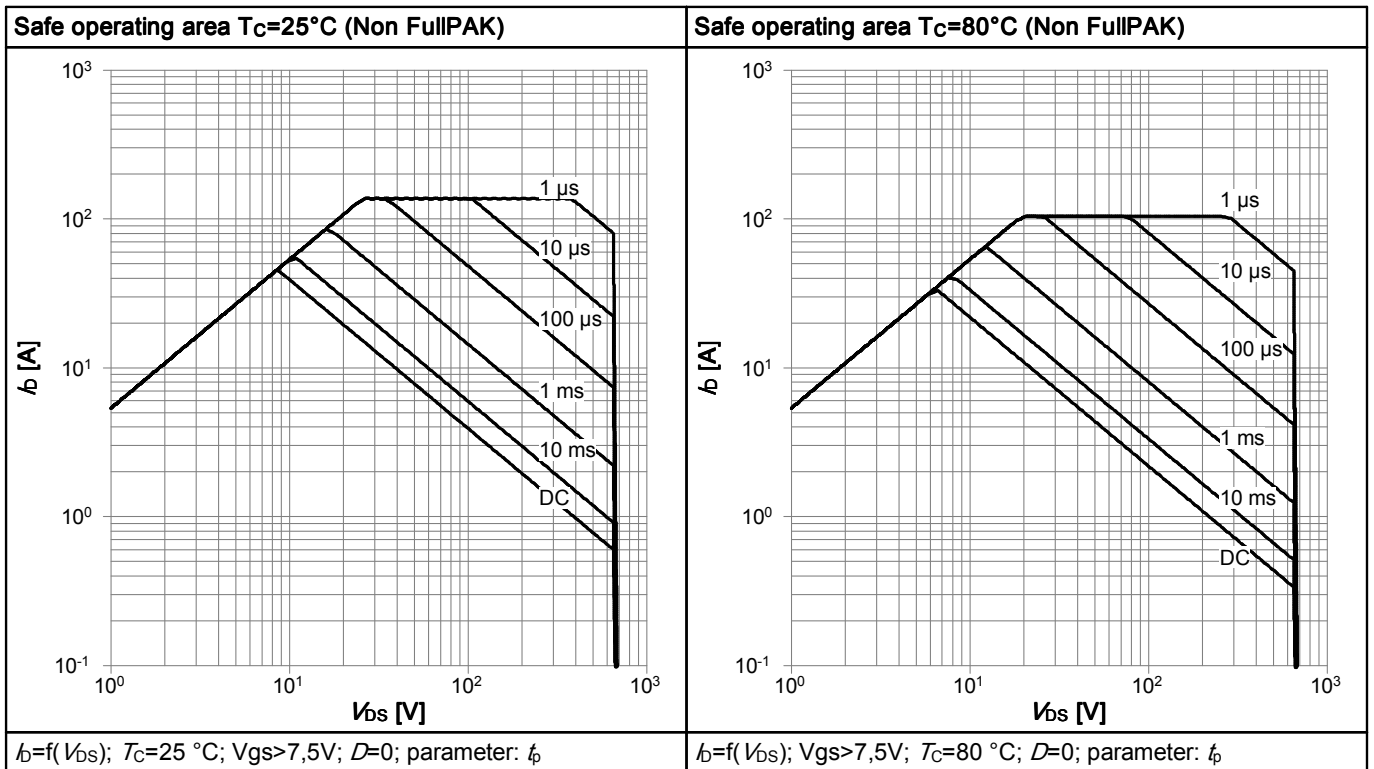


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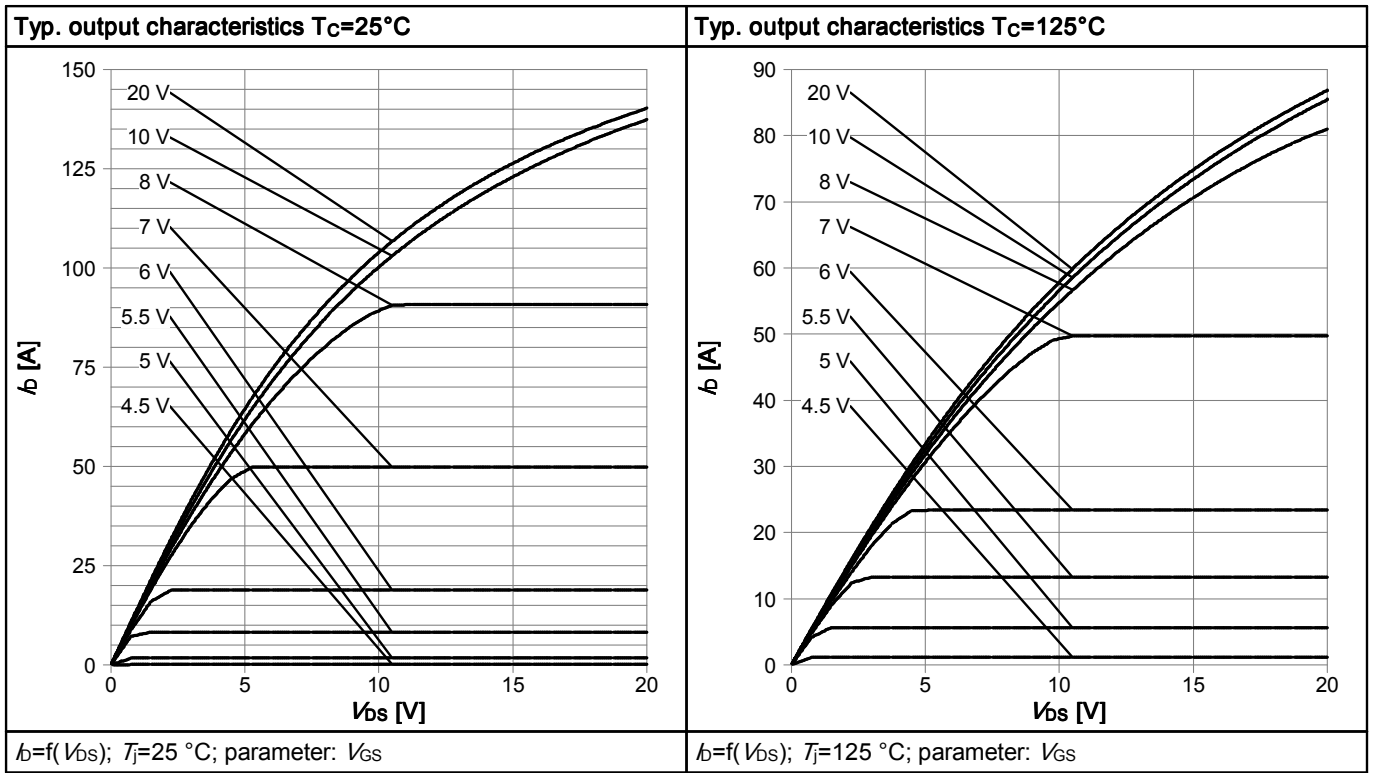


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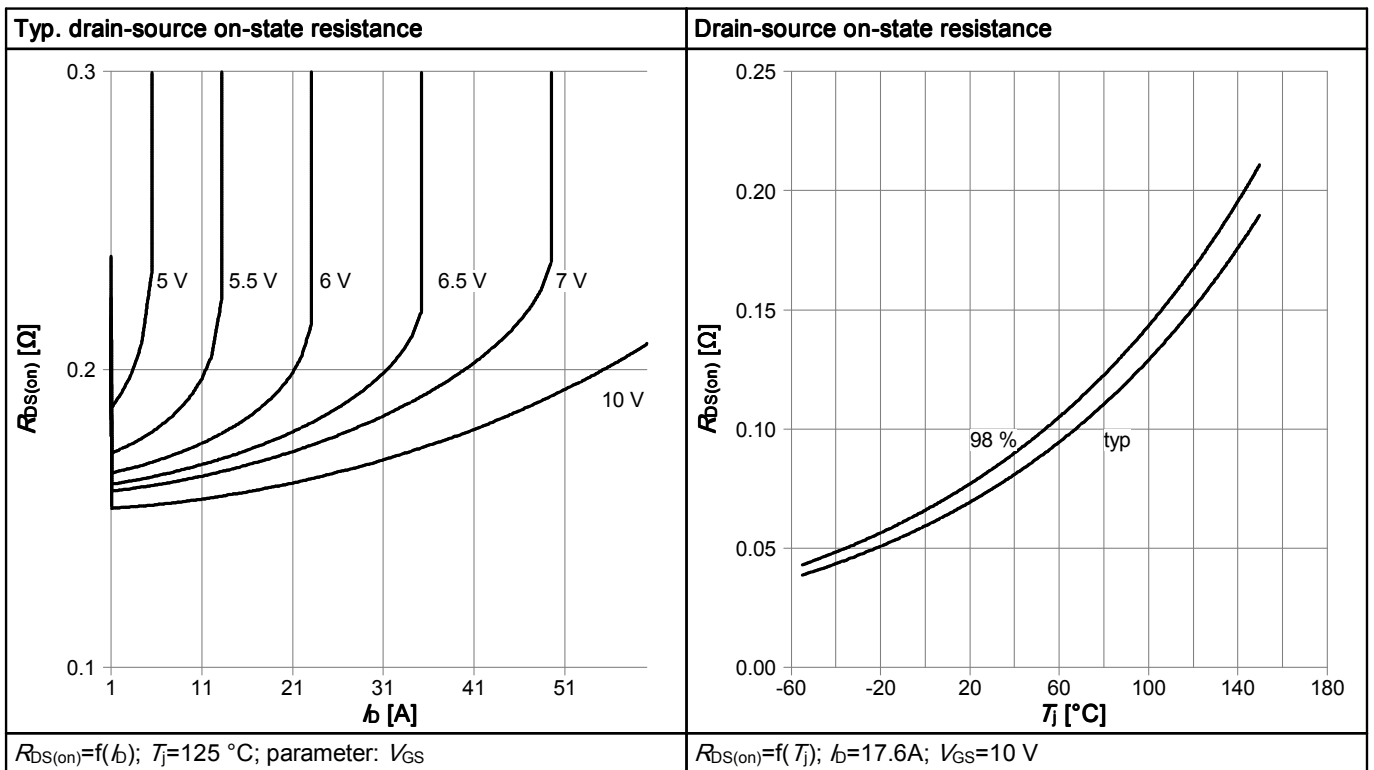


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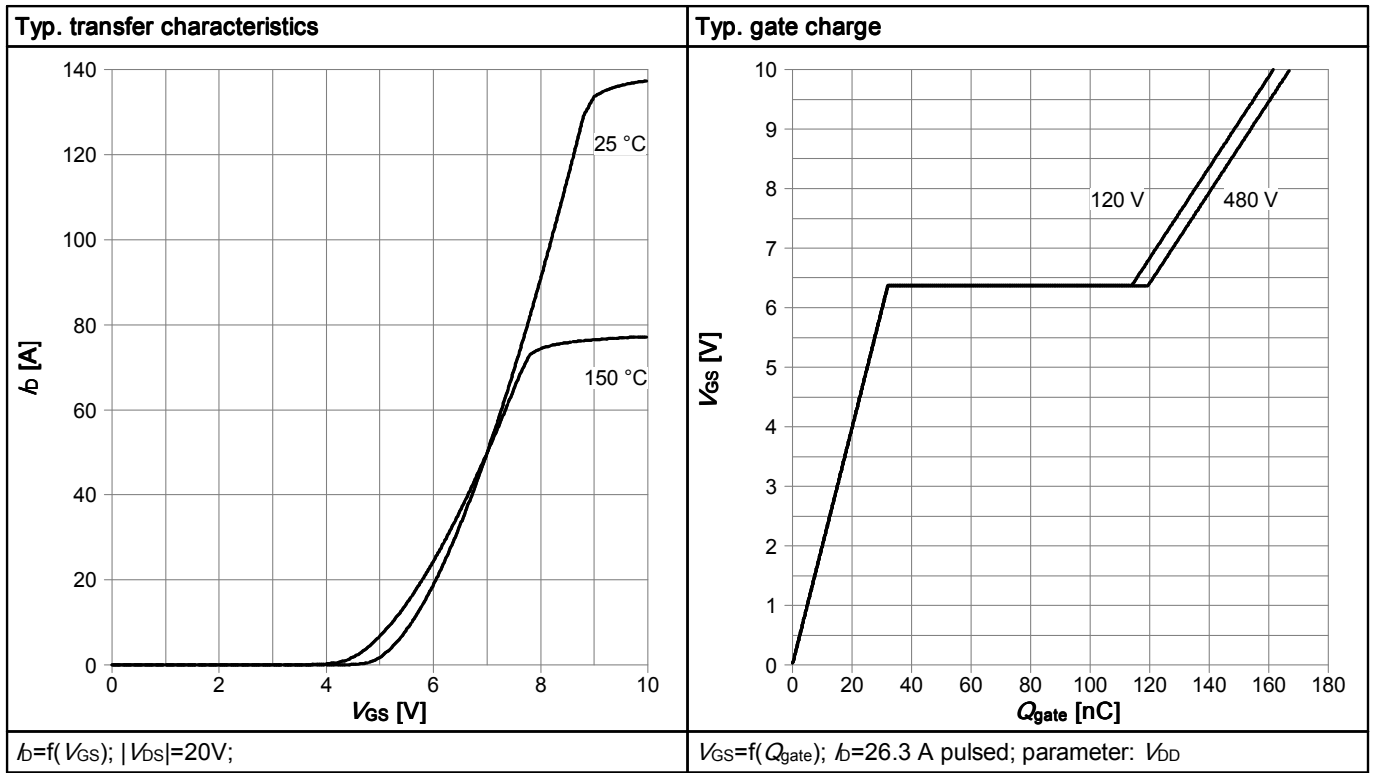


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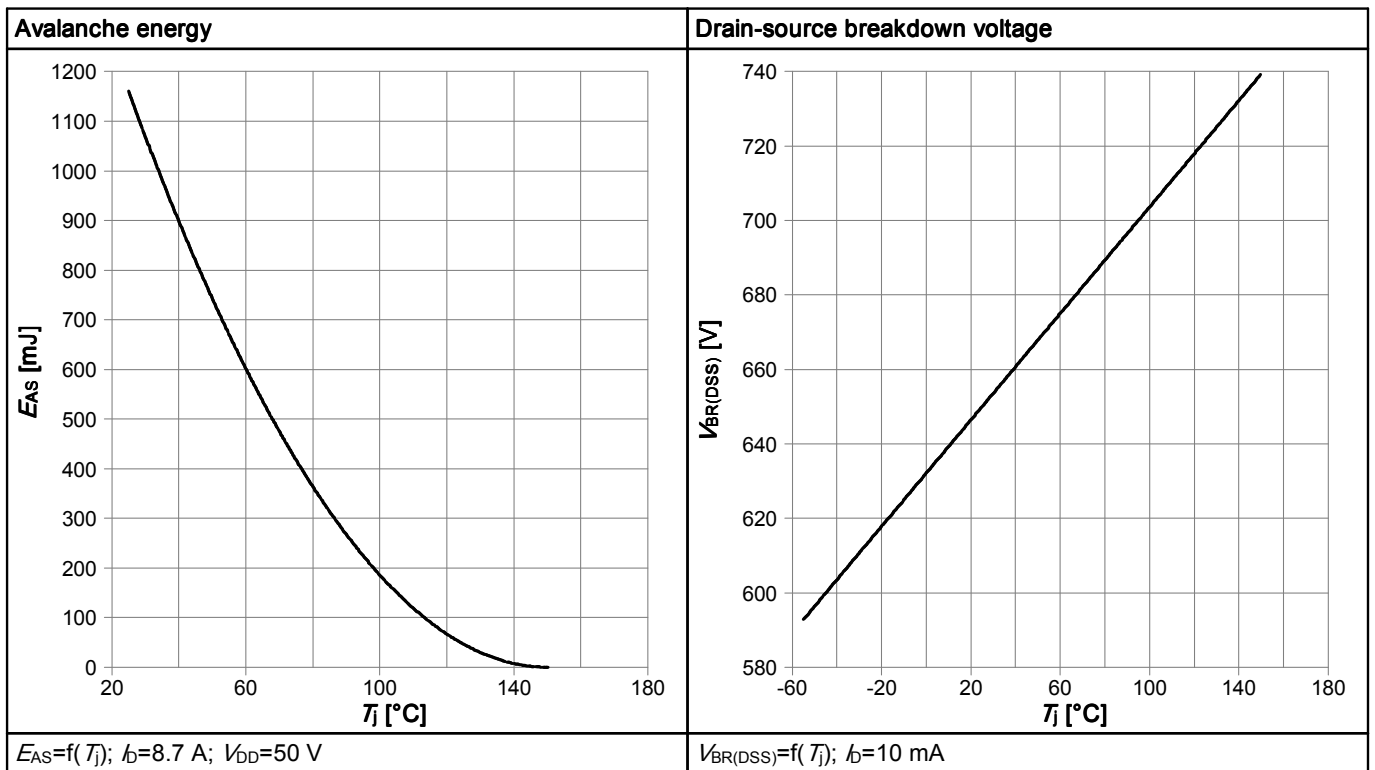


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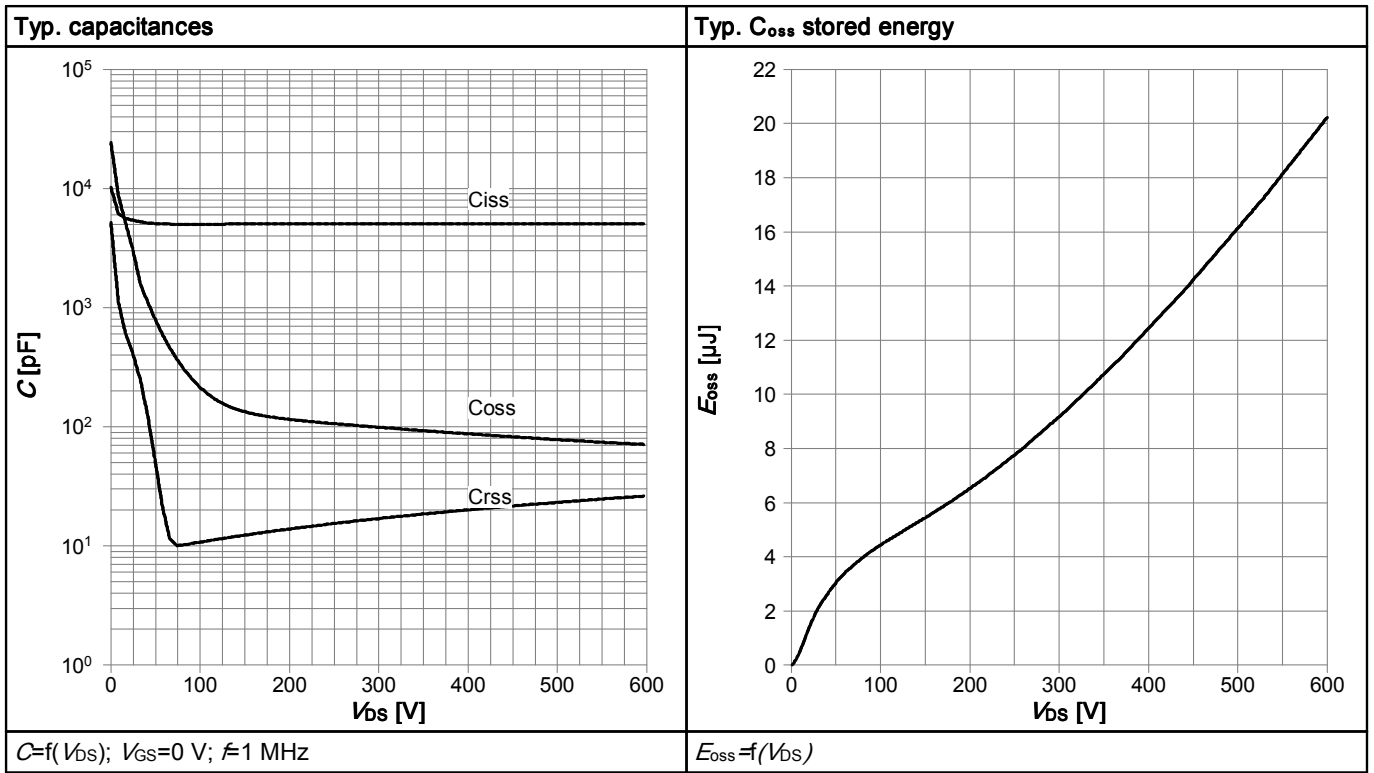
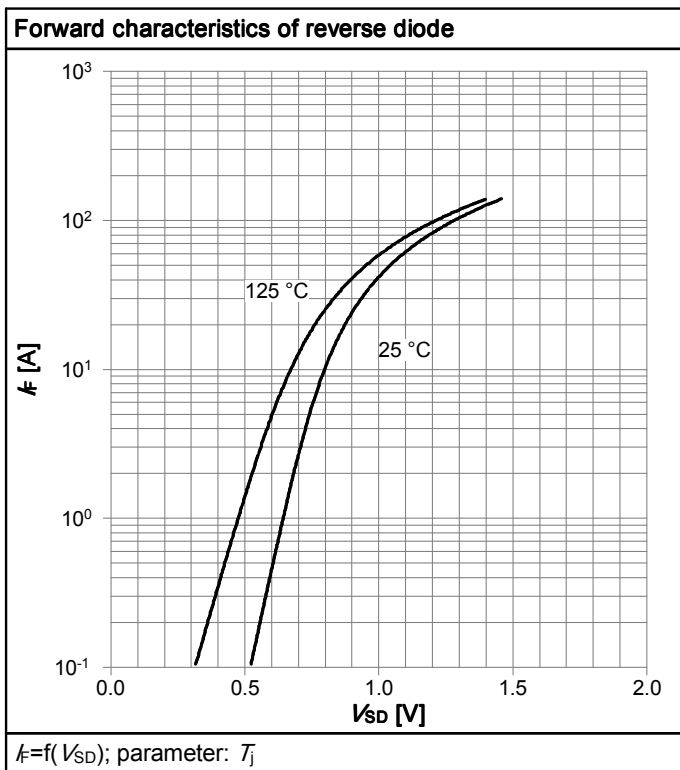


Table 15



6 Test Circuits

Table 16 Diode_characteristics

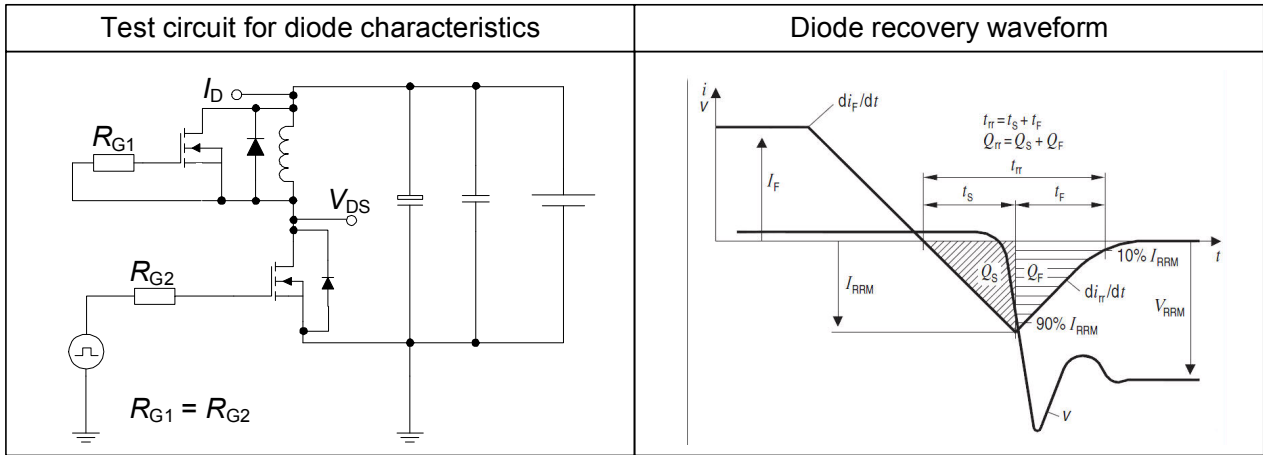


Table 17 Switching_times

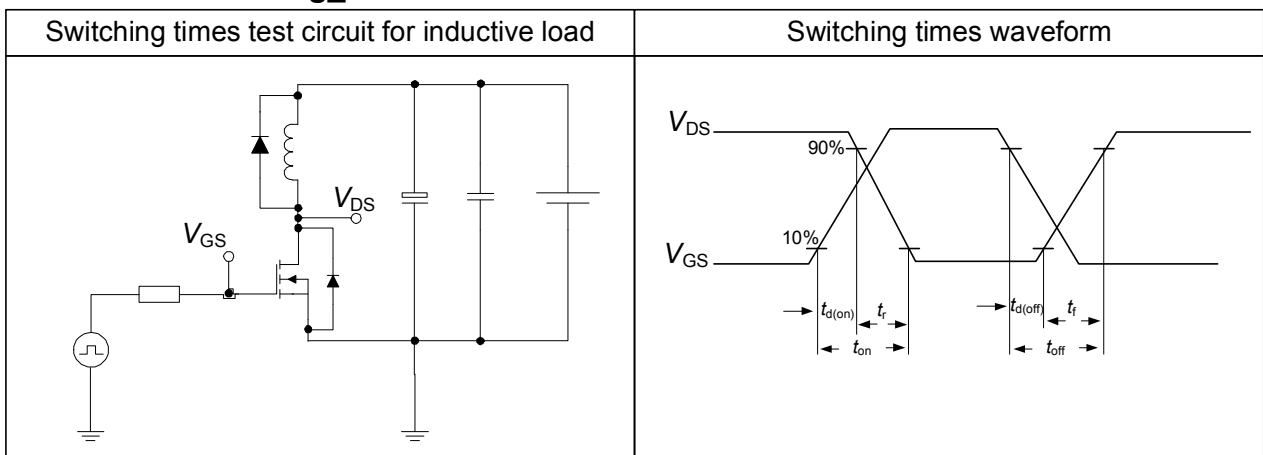
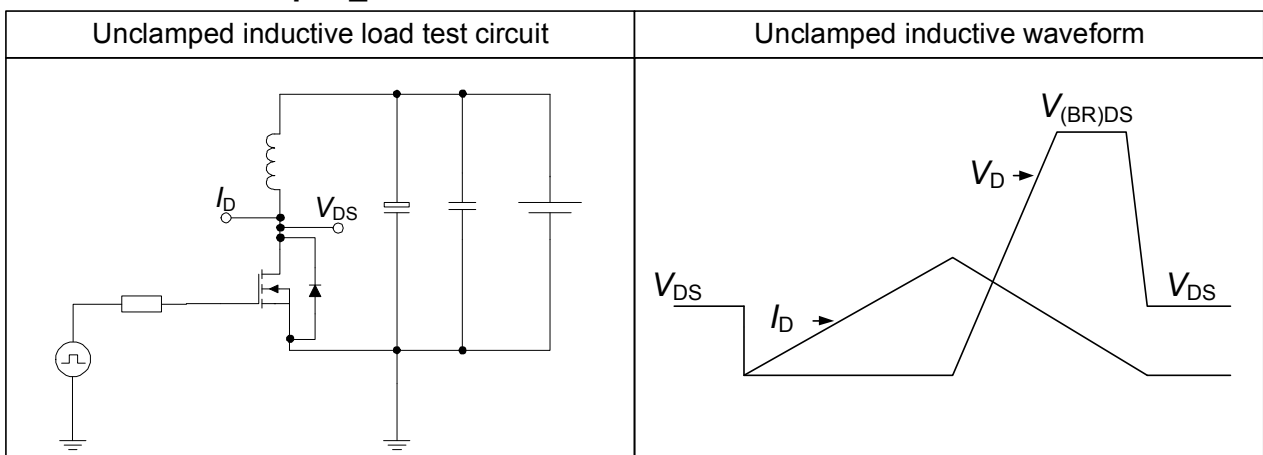


Table 18 Unclamped_inductive



7 Package Outlines

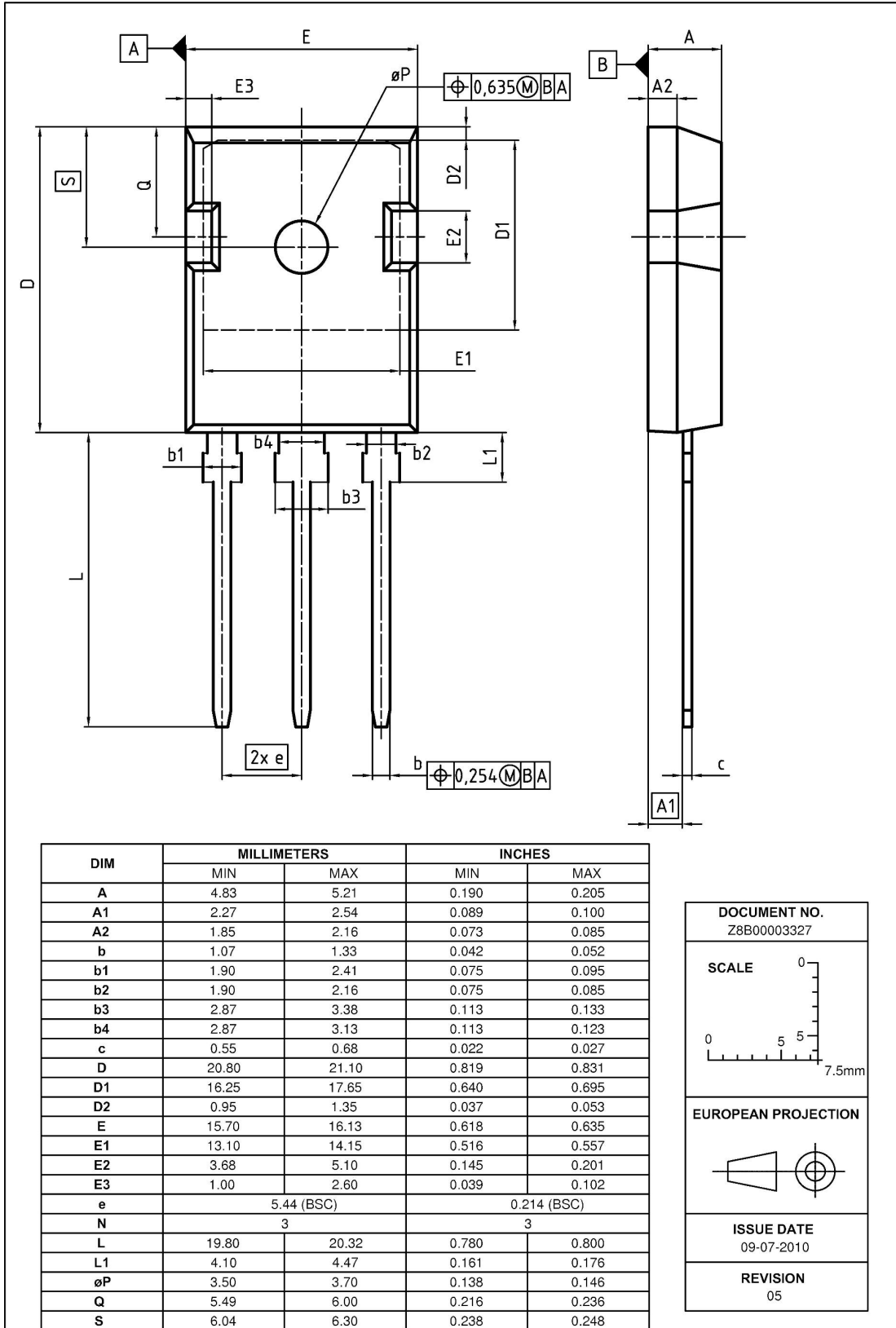


Figure 1 Outline PG-TO 247, dimensions in mm/inches

8 Appendix A

Table 19 Related Links

- **IFX Design Tools:**
<http://www.infineon.com/cms/en/product/promopages/designtools/index.html>
- **IFX CoolMOS Webpage:**
<http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8>

Revision History

IPW65R080CFD

Revision: 2011-09-27, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2011-08-29	update to CFD2 standard
2.2	2011-09-15	update pin naming
2.3	2011-09-16	release of new pin naming
2.4	2011-09-27	update the Igss test condition

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

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