

**Dual Low Side Driver**

**Features**

- Gate drive supply range from 6V to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs in phase with inputs

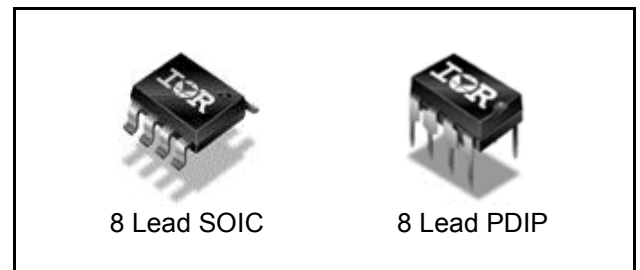
**Product Summary**

$I_{O+/-}$	1.5A / 1.5A
$V_{OUT}$	6V – 20V
Ton/off (typ.)	85 & 65 ns

**Description**

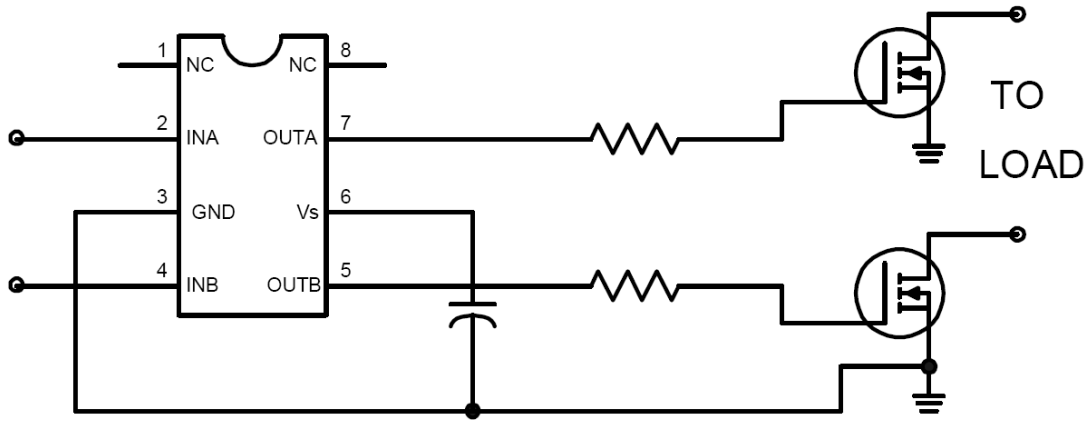
The IR25600(S) is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

**Package Options**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR25600SPBF	SO8N	Tube	95	IR25600SPBF
IR25600SPBF	SO8N	Tape and Reel	2500	IR25600STRPBF
IR25600PBF	PDIP8	Tube	50	IR25600PBF

**Typical Connection Diagram**


### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
$V_S$	Fixed supply voltage		-0.3	25	V
$V_O$	Output voltage		-0.3	$V_S + 0.3$	
$V_{IN}$	Logic input voltage		-0.3	$V_S + 0.3$	
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	8 lead PDIP	—	1	W
		8 lead SOIC	—	0.625	
$R_{thJA}$	Thermal resistance, junction to ambient	8 lead PDIP	—	125	$^\circ\text{C/W}$
		8 lead SOIC	—	200	
$T_J$	Junction temperature		—	150	$^\circ\text{C}$
$T_S$	Storage temperature		-55	150	
$T_L$	Lead temperature (soldering, 10 seconds)		—	300	

### Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages references to GND.

Symbol	Definition		Min.	Max.	Units
$V_S$	Fixed supply voltage		6	20	V
$V_O$	Output voltage		0	$V_S$	
$V_{IN}$	Logic input voltage (IN & SD)		0	$V_S$	
$T_A$	Ambient temperature		-40	125	$^\circ\text{C}$

### Dynamic Electrical Characteristics

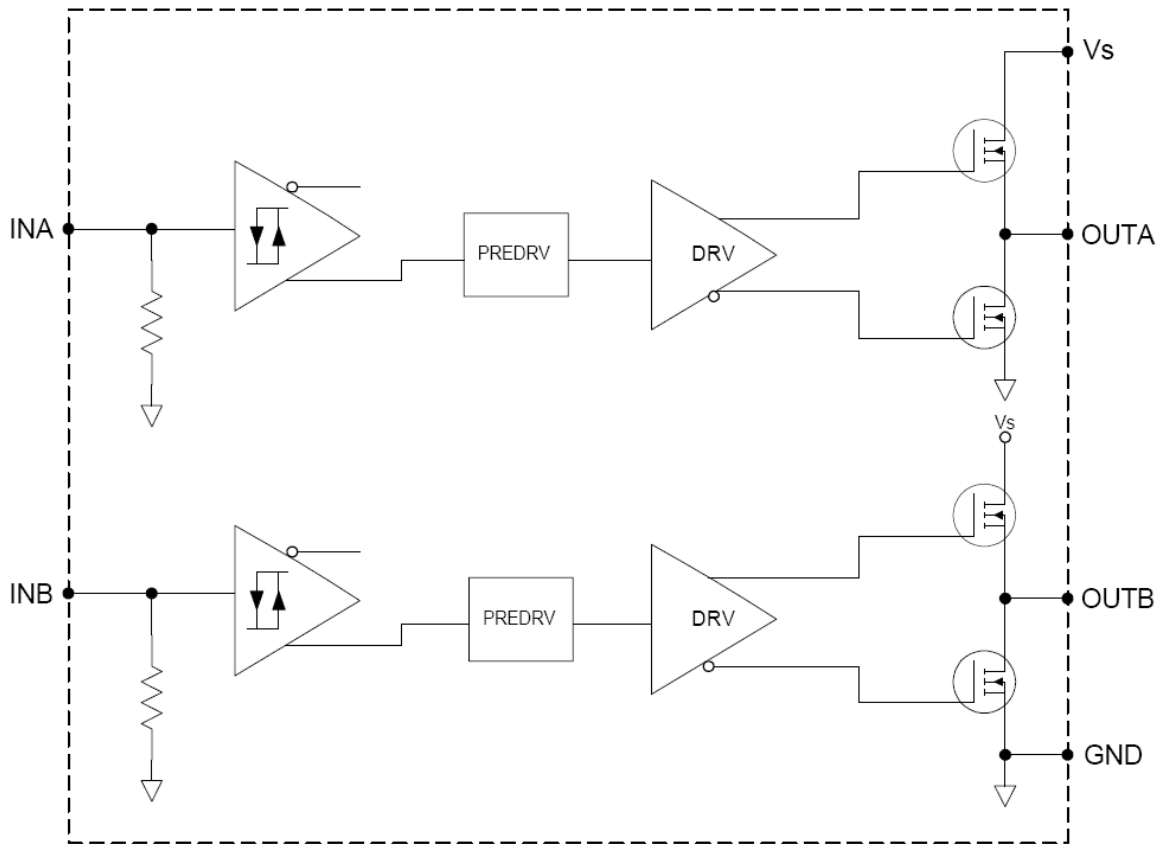
$V_{BIAS} (V_S) = 15V$ ,  $CL = 1000 \text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	85	160	ns	Figure 2
$t_{off}$	Turn-off propagation delay	—	65	150		
$t_r$	Turn-on rise time	—	15	35		
$t_f$	Turn-off fall time	—	10	25		

### Static Electrical Characteristics

$V_{BIAS} (V_S) = 15V$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to GND and are applicable to input leads INA and INB. The  $V_O$  and  $I_O$  parameters are referenced to GND and are applicable to the respective output leads: OUTA and OUTB.

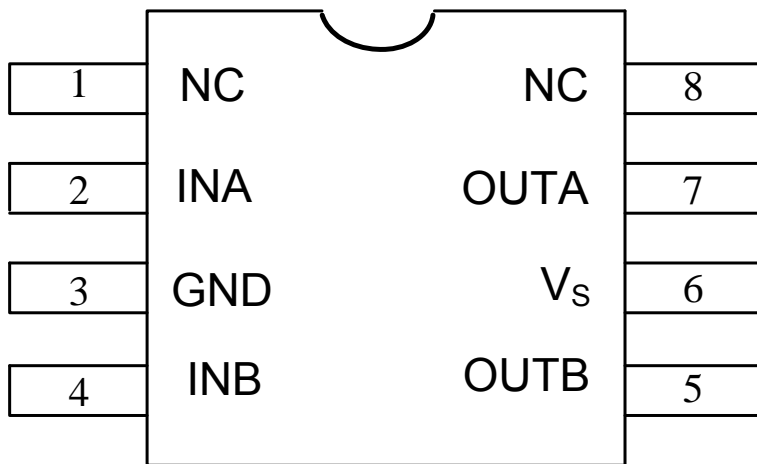
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage (OUTA = HI and OUTB = HI)	2.7	—	—	V	
$V_{IL}$	Logic "0" input voltage (OUTA = LO and OUTB = LO)	—	—	0.8		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.2		$I_O = 0A$
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.1		$I_O = 0A$
$I_{QS}$	Quiescent $V_S$ supply current	—	100	200	$\mu A$	$V_{IN} = 0V$ or $V_S$
$I_{IN+}$	Logic "1" input bias current (OUT = HI)	—	5	15		$V_{IN} = V_S$
$I_{IN-}$	Logic "0" input bias current (OUT = LO)	—	-10	-30		$V_{IN} = 0V$
$I_{O+}$	Output high short circuit pulsed current	1.5	2.3	—	A	$V_O = 0V$ , $V_{IN} = V_S$ $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	1.5	3.3	—		$V_O = 15V$ , $V_{IN} = 0V$ $PW \leq 10 \mu s$

**Functional Block Diagram**


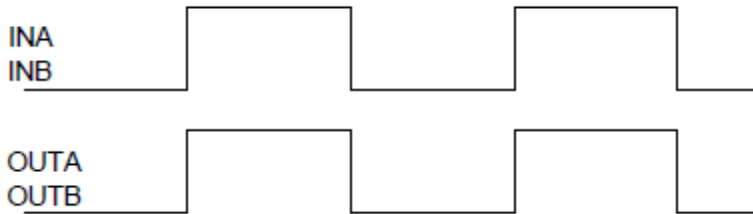
### Lead Definitions

Symbol	Description
INA	Logic input gate driver output (OUTA), in phase
INB	Logic input gate driver output (OUTB), in phase
OUTA	Gate drive output A
OUTB	Gate drive output B
V <sub>S</sub>	Supply Voltage
GND	Ground

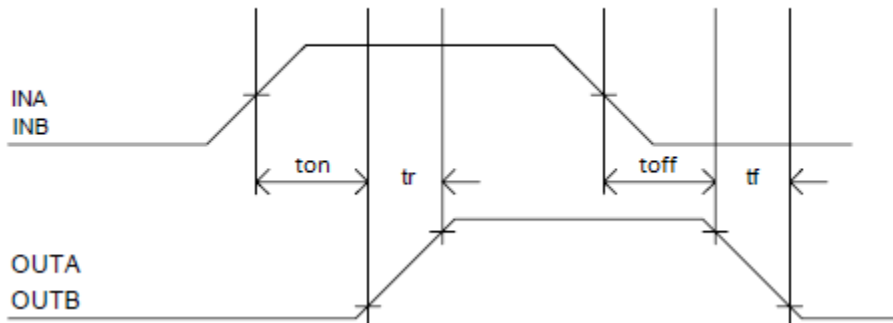
### Lead Assignments



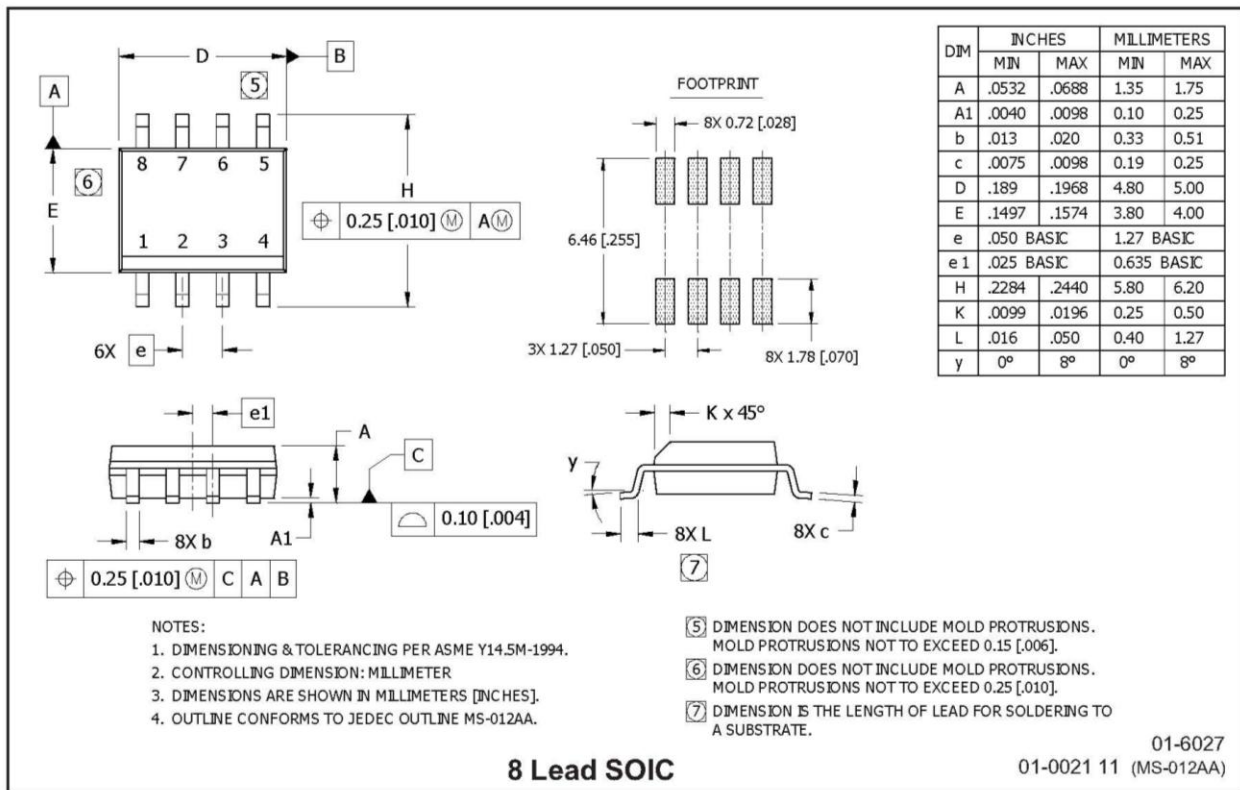
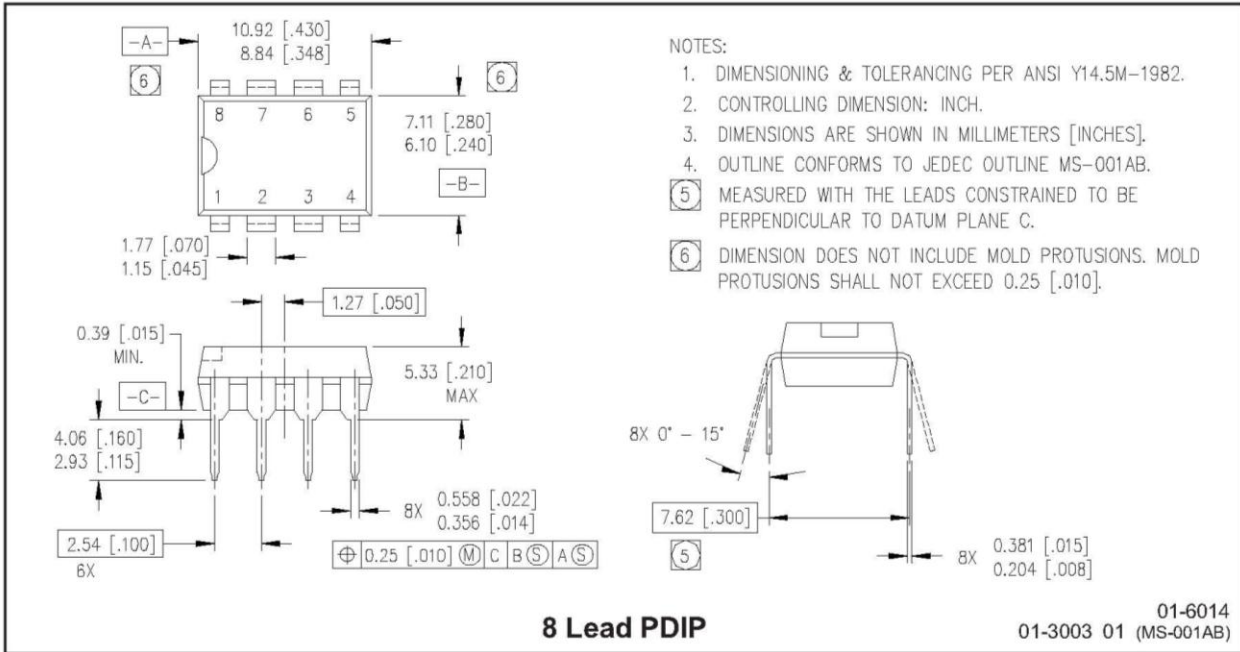
### Application Information and Additional Information



**Figure 1. Input/Output Timing Diagram**

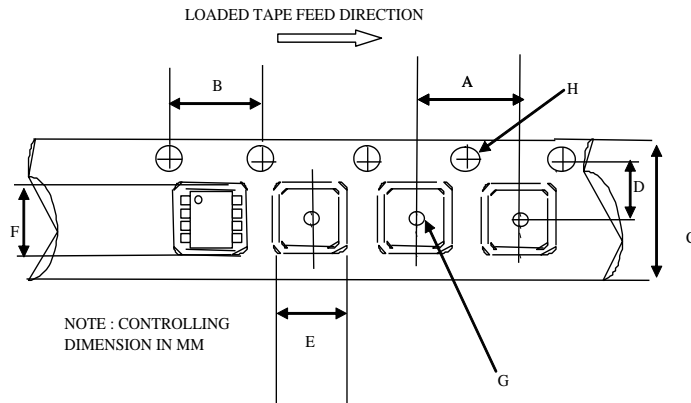


**Figure 2. Switching Time Waveform Definitions**

**Package Details**


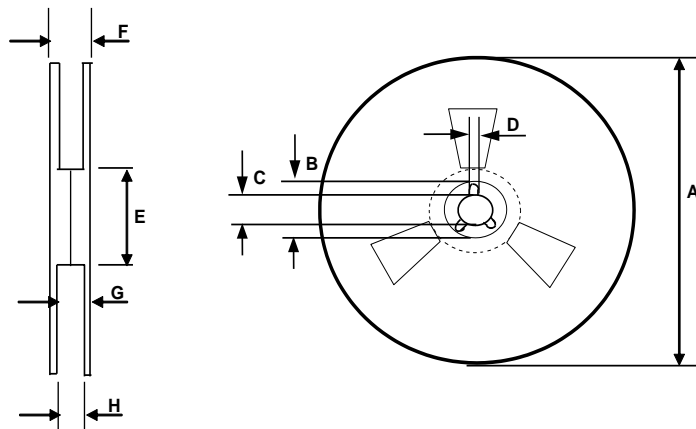


### Tape and Reel Details, SO8N



CARRIER TAPE DIMENSION FOR 8SOICN

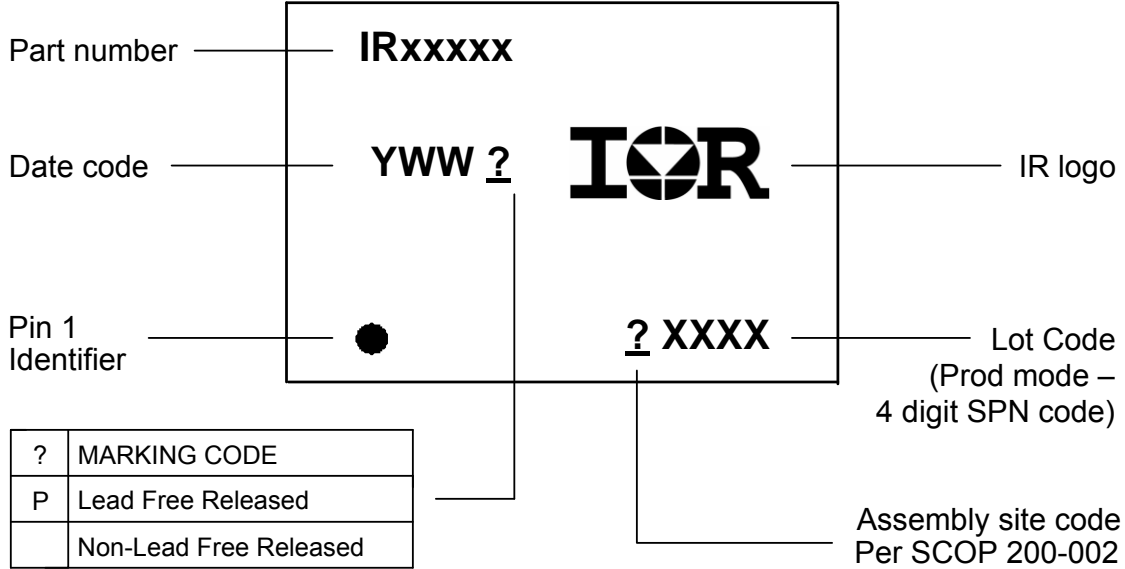
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial <sup>††</sup> (per JEDEC JESD 47)	
	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>	SOIC8N	MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD 020)
	PDIP8	Not applicable (non-surface mount package style)
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

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