International
IOR Rectifier

**PD97401**

# IR3640MPBF

## HIGH FREQUENCY SYNCHRONOUS PWM BUCK CONTROLLER

### Features

- 4.5V to 5.5V external supply
- Wide Input voltage from 1.5V to 24V
- Output voltage range: 0.7V to 0.9*Vin
- Programmable switching frequency up to 1.5MHz
- Programmable Soft-start
- Hiccup mode over current protection using Rds(on) sensing
- Programmable OCP
- Reference voltage 0.7V (+/-1%, 0ºC <Tj<125ºC)
- Enhanced Pre-bias start up
- Output voltage tracking
- Integrated MOSFET drivers and bootstrap diode
- Operating temp: -40ºC <Tj<125ºC
- External synchronization
- Power Good output
- Thermal shut down
- Over voltage protection
- Enable Input with voltage monitoring capability
- Pb-Free & Halogen-Free (RoHS Compliant)
- 20 -Lead MLPQ package (3mmx4mm)

### Applications

- Point of Load Power Architectures
- Server & Netcom Applications
- Game Consoles
- General DC/DC Converters

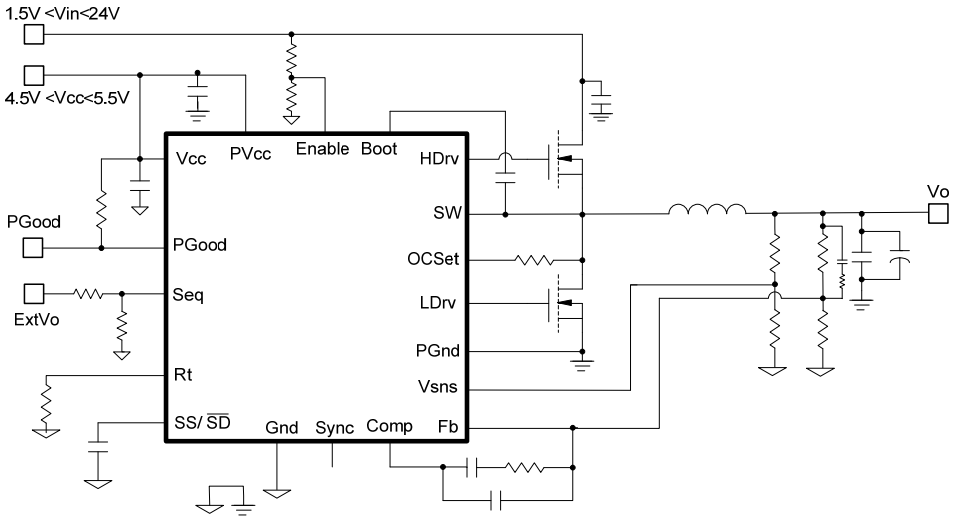
### Description

The IR3640M is a synchronous Buck PWM controller designed for performance demanding DC/DC applications. The single loop voltage mode architecture simplifies design while delivery precise output voltage regulation and fast transient response. Because of its wide input and output voltage range it can be used in a large variety of point of load applications within a system and across different markets.

The part is designed to drive a pair of N-Channel MOSFETs from 250kHz to 1.5Mhz switching frequency giving designers the flexibility to optimize the solution for best efficiency or smallest footprint. The output voltage can be precisely regulated from as low as 0.7V within a tolerance of +/-1% over temperature, line and load variations.

The device also integrates a diversity of features including; programmable soft start, pre-bias start up, voltage tracking, external synchronization, enable input and Power Good output. Fault protection features include thermal shutdown, over voltage and over current shutdown and under voltage lock out.

### Typical Application



## ABSOLUTE MAXIMUM RATINGS

*(Voltages referenced to GND unless otherwise specified)*

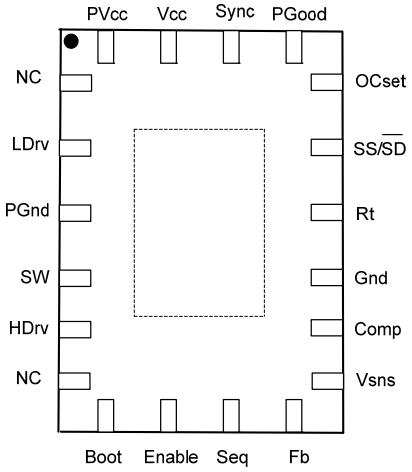
- Vcc and PVcc ..... -0.3V to 8V *(Note2)*
- Boot ..... -0.3V to 40V
- SW ..... -4V (100ns), -0.3V(DC) to 31V
- Boot to SW ..... -0.3V to Vcc+0.3V *(Note1)*
- LDrv to PGND ..... -0.3V to Vcc+0.3V *(Note1)*
- HDrv to SW ..... -0.3V to BOOT+0.3V *(Note1)*
- OCSet ..... -0.3V to 30V, 30mA
- Input / output Pins ..... -0.3V to Vcc+0.3V *(Note1)*
- PGND to GND ..... -0.3V to +0.3V
- Storage Temperature Range ..... -55°C To 150°C
- Junction Temperature Range ..... -40°C To 150°C *(Note2)*
- ESD Classification ..... JEDEC Class 1C
- Moisture sensitivity level..... JEDEC Level 2@260 °C

***Note1:***
*Must not exceed 8V*
***Note2:***
*Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C*

***Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

## Package Information

***20-Lead MLPQ***
***(3x4)mm***




$\Theta_{JA}$ = 36° C/W *
$\Theta_{JC}$ = 4° C/W

**Exposed pad on underside is connected to a copper pad through vias for 4-layer PCB board design*

## Ordering Information

| PKG DESIG | PACKAGE DESCRIPTION | PIN COUNT | PARTS PER REEL |
|---|---|---|---|
| M | IR3640MTRPbF | 20 | 3000 |

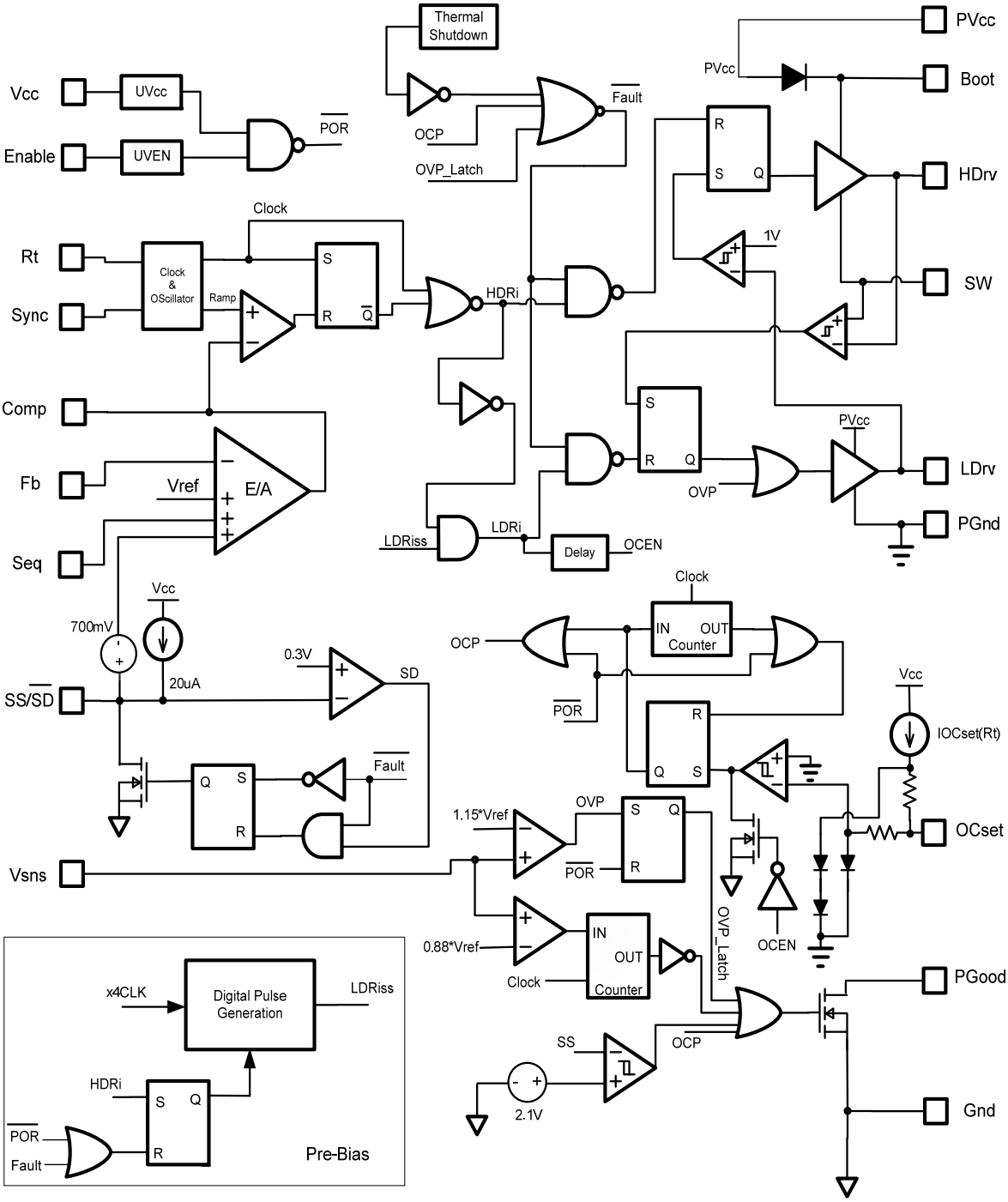



Fig. 2. Simplified block diagram of the IR3640

## Pin Description

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | NC | No Connect |
| 2 | LDrv | Output driver for Low-side MOSFET |
| 3 | PGnd | Power Ground |
| 4 | SW | Switch Node |
| 5 | HDrv | Output driver for High-side MOSFET |
| 6 | NC | No Connect |
| 7 | Boot | Supply Voltage for High-side Driver |
| 8 | Enable | User programmable Enable |
| 9 | Seq | Sequence. If it is not used connect to Vcc |
| 10 | Fb | Inverting Pin of E/A |
| 11 | Vsns | OVP / PGood Sense |
| 12 | Comp | Output of Error Amplifier |
| 13 | Gnd | IC Ground |
| 14 | Rt | Set the Switching Frequency |
| 15 | SS/$\overline{SD}$ | Soft Start/Shutdown |
| 16 | OCset | External Resistor connection to set the **Over Current Limit** |
| 17 | PGood | Power Good Output. Open Drain |
| 18 | Sync | External Synchronization |
| 19 | Vcc | Supply Voltage for IC Bias |
| 20 | PVcc | Supply Voltage for Driver section |

## Recommended Operating Conditions

| Symbol | Definition | Min | Max | Units |
|---|---|---|---|---|
| Vcc and PVcc | Supply voltages | 4.5 | 5.5 | V |
| Fs | Operating frequency | 225 | 1650 | kHz |
| Tj | Junction temperature | -40 | 125 | °C |

## Electrical Specifications

Unless otherwise specified, these specification apply over 4.5V<$V_{cc}$<5.5V, 0°C<$T_j$<125°C
Typical values are specified at 25°C

| Parameter | SYM | Test Condition | Min | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **Voltage Accuracy** | | | | | | |
| Regulated voltage at Fb | VFb | | | 0.7 | | V |
| Accuracy | | 0°C<Tj<125°C | -1.0 | | +1.0 | % |
| | | -40°C<Tj<125°C, *Note3* | -2 | | +2 | |
| **Supply Current** | | | | | | |
| $V_{cc}$ Supply Current (Standby) | $I_{cc}$ (Standby) | No Switching, Enable low | | | 500 | µA |
| $V_{cc}$ Supply Current (Dyn) | $I_{cc}$ (Dynamic) | Vcc=5V, Freq=600kHz, Enable high, $C_{LOAD\_H}$=2.2nF $C_{LOAD\_L}$=4.4nF | | | 40 | mA |
| $V_{cc}$ Supply current | $I_{bias}$ | Vcc=5V, Freq=600kHz, Enable high, Cload=Open | | | 6 | |
| **Under Voltage Lockout / Enable** | | | | | | |
| Vcc-Threshold-Start | Vcc_UVLO_Start | Vcc Rising Trip Level | 4.06 | 4.26 | 4.46 | V |
| Vcc-Threshold-Stop | Vcc_UVLO_Stop | Vcc Falling Trip Level | 3.76 | 3.96 | 4.16 | |
| Vcc-Hysteresis | Vcc-Hys | | 0.25 | 0.3 | 0.38 | |
| Enable Threshold-Start | En_UVLO_Start | Enable Rising Trip Level | 1.14 | 1.2 | 1.36 | |
| Enable Threshold-Stop | En_UVLO_Stop | Enable Falling Trip Level | 0.9 | 1.0 | 1.06 | |
| Enable-Hysteresis | En_Hys | | 0.16 | 0.20 | 0.25 | |
| Enable Leakage Current | Ien | Enable=3.3V | | | 18 | µA |
| **Oscillator** | | | | | | |
| Rt Voltage | | | 0.665 | 0.7 | 0.735 | V |
| Frequency | $F_S$ | Rt=59K | 225 | 250 | 275 | kHz |
| | | Rt=28.7K | 450 | 500 | 550 | |
| | | Rt=9.31K | 1350 | 1500 | 1650 | |
| Ramp Amplitude | Vramp | *Note4* | | 1.8 | | Vp-p |
| Ramp Offset | Ramp (os) | *Note4* | | 0.6 | | V |

## Electrical Specifications

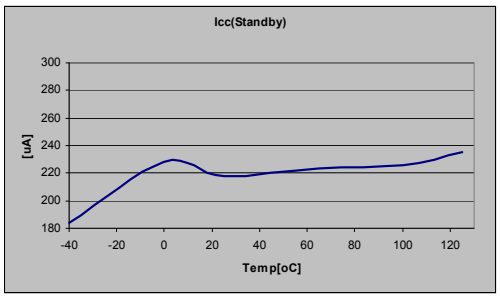
| Parameter | SYM | Test Condition | Min | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **Oscillator (cont.)** | | | | | | |
| Min Pulse Width | Dmin(ctrl) | Note4 | | 50 | | ns |
| Max Duty Cycle | Dmax | Fs=250kHz | 92 | | | % |
| Fixed Off Time | Hdrv(off) | Note4 | | 130 | 200 | ns |
| Sync Frequency Range | | 20% above free running frequency | 225 | | 1650 | kHz |
| Sync Pulse Duration | | | 100 | 200 | | ns |
| Sync Level Threshold | High | | 2 | | | V |
| | Low | | | | 0.6 | |
| **Error Amplifier** | | | | | | |
| Input Offset Voltage | Vos | Vfb-Vseq Vseq=0.8V | -10 | 0 | +10 | mV |
| Input Bias Current | IFb(E/A) | | -1 | | +1 | µA |
| Input Bias Current | IVp(E/A) | | -1 | | +1 | |
| Sink Current | Isink(E/A) | | 0.40 | 0.85 | 1.2 | mA |
| Source Current | Isource(E/A) | | 8 | 10 | 13 | |
| Slew Rate | SR | *Note4* | 7 | 12 | 20 | V/µs |
| Gain-Bandwidth Product | GBWP | *Note4* | 20 | 30 | 40 | MHz |
| DC Gain | Gain | *Note4* | 100 | 110 | 120 | dB |
| Maximum Voltage | Vmax(E/A) | Vcc=4.5V | 3.4 | 3.5 | 3.7 | V |
| Minimum Voltage | Vmin(E/A) | | | 120 | 220 | mV |
| Seq Common Mode Voltage | Seq | *Note4* | 0 | | 1 | V |
| **Soft Start/SD** | | | | | | |
| Soft Start Current | ISS | Source | 14 | 20 | 26 | µA |
| Soft Start Clamp Voltage | Vss(clamp) | | 2.7 | 3.0 | 3.3 | V |
| Shutdown Output Threshold | SD | | | | 0.3 | |
| **Over Current Protection** | | | | | | |
| OCSET Current | $I_{OCSET}$ | Fs=250kHz | 20.8 | 23.6 | 26.4 | µA |
| | | Fs=500kHz | 43 | 48.8 | 54.6 | |
| | | Fs=1500kHz | 136 | 154 | 172 | |
| OC Comp Offset Voltage | $V_{OFFSET}$ | *Note4* | -10 | 0 | +10 | mV |
| SS off time | SS_Hiccup | | | 4096 | | Cycles |

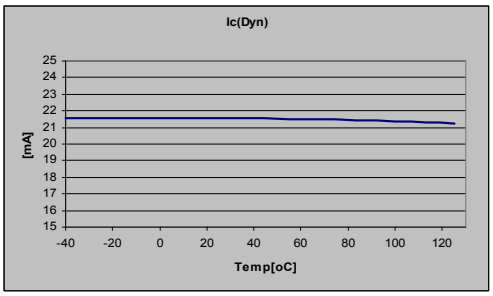
## Electrical Specifications

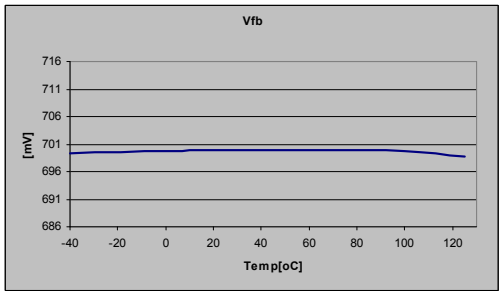
| Parameter | SYM | Test Condition | Min | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown | | *Note4* | | 140 | | °C |
| Hysteresis | | | | 20 | | |
| **Power Good** | | | | | | |
| Power Good Threshold | VPG | Vsns Rising | 83 | 88 | 93 | %Vref |
| Delay Comparator Threshold | SS(Delay) | Relative to charge voltage, SS rising | 2.0 | 2.1 | 2.2 | V |
| Delay Comparator Hysteresis | Delay(SShys) | *Note4* | 260 | 300 | 340 | mV |
| PGood Voltage Low | PG(voltage) | $I_{PGood}$=-5mA | | | 0.5 | V |
| PGood Comparator Delay | PG(Delay) | | | 256/Fs | | s |
| Leakage Current | $I_{leakage}$ | | | 0 | 10 | uA |
| **High Side Driver** | | | | | | |
| Source Impedance | $R_{source}$(Hdrv) | $V_{Boot}$-$V_{SW}$=5V, *Note4* | | 2.0 | 5.0 | Ω |
| Sink Impedance | $R_{sink}$(Hdrv) | $V_{Boot}$-$V_{SW}$=5V , *Note4* | | 1.0 | 2.5 | |
| Rise Time | THdrv(Rise) | $V_{Boot}$-$V_{SW}$=5V, $C_{load}$=2.2nF 1V to 4V | | | 40 | ns |
| Fall Time | THdrv(Fall) | $V_{Boot}$-$V_{SW}$=5V, $C_{load}$=2.2nF 4V to 1V | | | 27 | |
| Deadband Time | Tdead(L to H) | Ldrv going Low to Hdrv going High, 1V to 1V | 10 | 20 | 45 | |
| SW Bias Current | Isw | SW=0V, Enable=0V | | | 6 | µA |
| **Low Side Driver** | | | | | | |
| Source Impedance | $R_{source}$(Ldrv) | Vcc=5V, *Note4* | | 1.0 | 2.5 | Ω |
| Sink Impedance | $R_{source}$(Ldrv) | Vcc=5V, *Note4* | | 0.4 | 1.0 | |
| Rise Time | TLdrv(Rise) | Vcc=5V $C_{load}$=4.4nF 1V to 4V | | | 40 | ns |
| Fall Time | TLdrv(Fall) | Vcc=5V $C_{load}$=4.4nF 4V to 1V | | | 40 | |
| Deadband Time | Tdead(H to L) | Hdrv going Low to Ldrv going High, 1V to 1V | 10 | 20 | 45 | |
| **Over Voltage Protection** | | | | | | |
| OVP Trip Threshold | OVP(trip)_Vref | | 110 | 115 | 120 | %Vref |
| OVP Fault Prop Delay | OVP(delay) | | | | 150 | ns |
| **Bootstrap Diode** | | | | | | |
| Forward Voltage | | I(Boot)=30mA | 180 | 260 | 470 | mV |

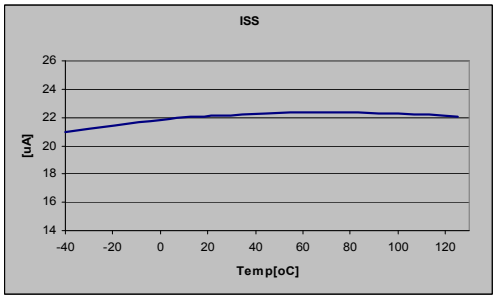
*Note3: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production*
*Note4: Guaranteed by Design, but not tested in production*

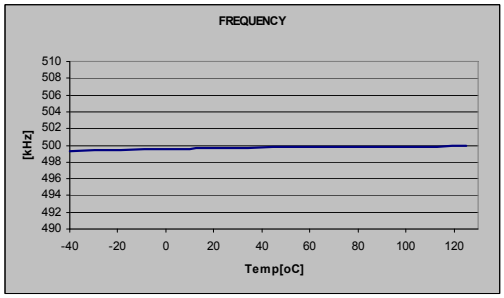
## TYPICAL OPERATING CHARACTERISTICS: (-40ºC - 125ºC) $F_s$= 500 kHz

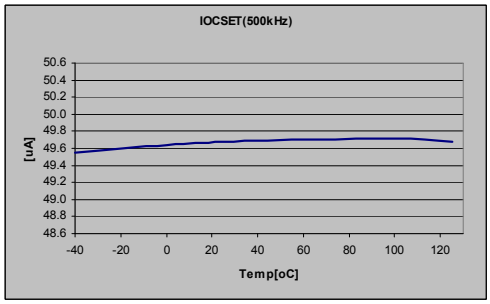


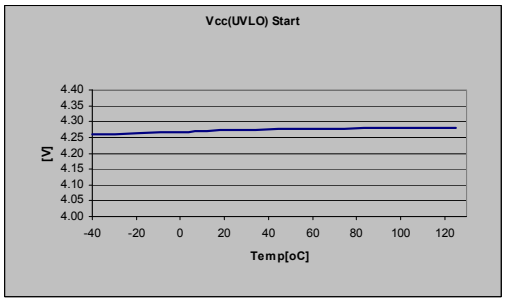



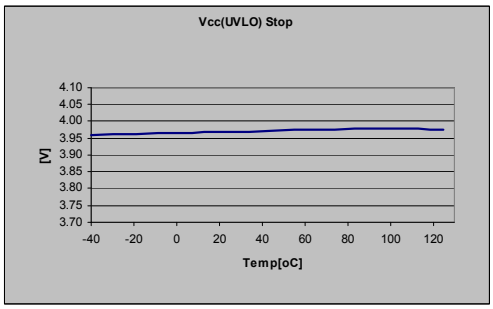



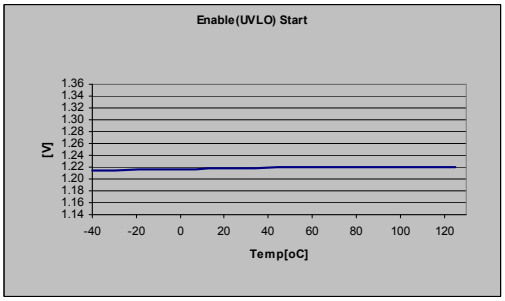



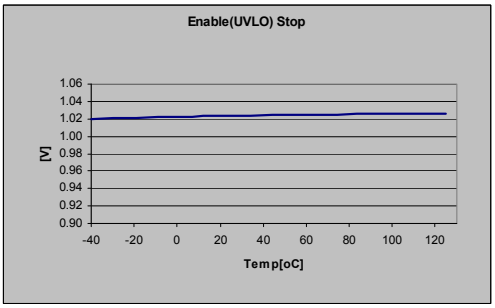



# Circuit Description

## THEORY OF OPERATION

### Introduction

The IR3640 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 250kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3640 provides precisely regulated output voltage programmed via two external resistors from 0.7V to 0.9*Vin.

The IR3640 operates with an external bias supply from 4.5V to 5.5V, allowing an extended operating input voltage range from 1.5V to 24V.

The device utilizes the on-resistance of the low side MOSFET as current sense element, this method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

### Under-Voltage Lockout and POR

The under-voltage lockout circuit monitors the input supply Vcc and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

### Enable

The Enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3640 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3640 does not turn on until the bus voltage reaches the desired level. Only after the bus voltage reaches or exceeds this level will the voltage at Enable pin exceed its threshold, thus enabling the IR3640. Therefore, in addition to being a logic input pin to enable the IR3640, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage $V_{in}$. This is desirable particularly for high output voltage applications, where we might want the IR3640 to be disabled at least until $V_{in}$ exceeds the desired output voltage level.

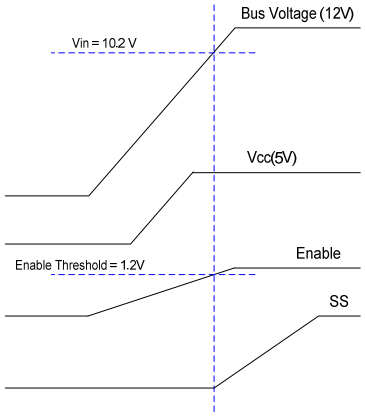



Fig. 3a: Normal Start up, Device turns on when the Bus voltage reaches 10.2V

Figure 3b shows the recommended start-up sequence for the non-sequenced operation of IR3640, when Enable is used as a logic input.

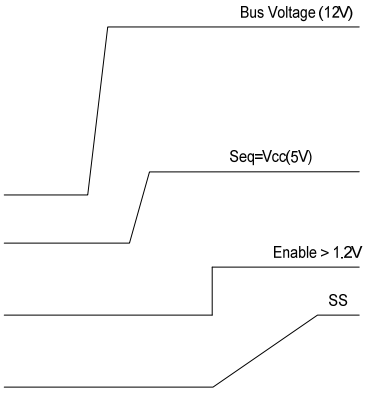



Fig. 3b: Recommended startup sequence, Non-Sequenced operation

Figure 3c shows the recommended startup sequence for sequenced operation of IR3640 with Enable used as logic input.

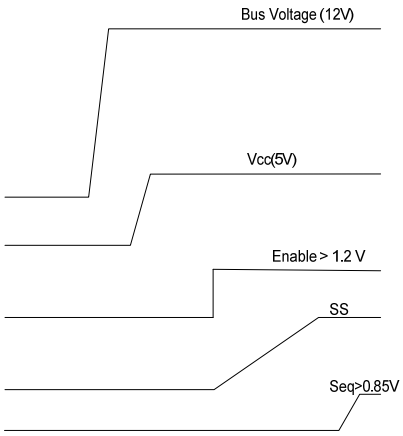



Fig. 3c. Recommended startup sequence, Sequenced operation

**Pre-Bias Startup**

IR3640 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Figure 4 shows a typical Pre-Bias condition at start up.

The synchronous MOSFET always starts with a narrow pulse width and gradually increases its duty cycle with a step of 25%, 50%, 75% and 100% until it reaches the steady state value. The number of these startup pulses for the synchronous MOSFET is internally programmed. Figure 5 shows a series of 32, 16, 8 startup pulses.

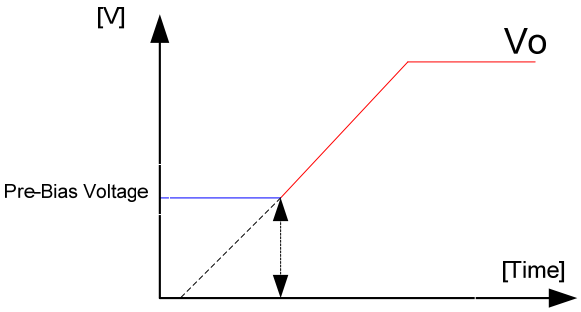



Fig. 4. Pre-Bias startup

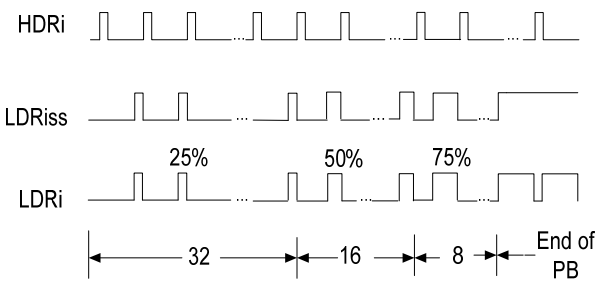



Fig. 5. Pre-Bias startup pulses

**Soft-Start**

The IR3640 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal current source (typically 20uA) charges the external capacitor $C_{ss}$ linearly from 0V to 3V. Figure 6 shows the waveforms during the soft start.

The start up time can be estimated by:

$$T_{start} = \frac{(1.4 - 0.7) * C_{SS}}{20\mu A} \quad --(1)$$

During the soft start the OCP is enabled to protect the device for any short circuit and over current condition.

The SS pin can be used as shutdown signal, pulling low this pin will result to turning off the high side driver and turning on the low side driver.

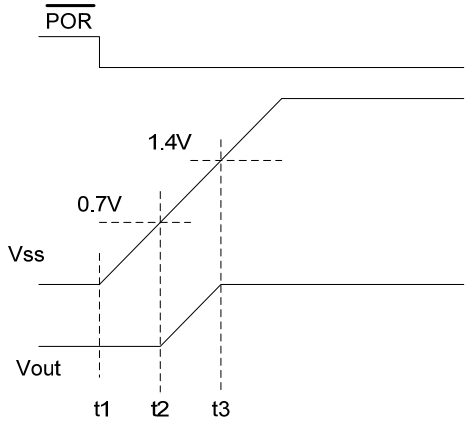



Fig. 6. Theoretical operation waveforms during soft-start

### Operating Frequency

The switching frequency can be programmed between 250kHz – 1500kHz by using an external resistor from $R_t$ to Gnd. Table 1 tabulates the oscillator frequency versus $R_t$. Trailing edge modulation is used for generating PWM signal(Fig.7) .

Table 1. Switching Frequency and $I_{OCSet}$ vs. External Resistor ($R_t$)

| $R_t$ (kΩ) | $F_s$ (kHz) | $I_{ocset}$ (µA) |
|---|---|---|
| 47.5 | 300 | 29.4 |
| 35.7 | 400 | 39.2 |
| 28.7 | 500 | 48.7 |
| 23.7 | 600 | 59.07 |
| 20.5 | 700 | 68.2 |
| 17.8 | 800 | 78.6 |
| 15.8 | 900 | 88.6 |
| 14.3 | 1000 | 97.9 |
| 12.7 | 1100 | 110.2 |
| 11.5 | 1200 | 121.7 |
| 10.7 | 1300 | 130.8 |
| 9.76 | 1400 | 143.4 |
| 9.31 | 1500 | 150.3 |

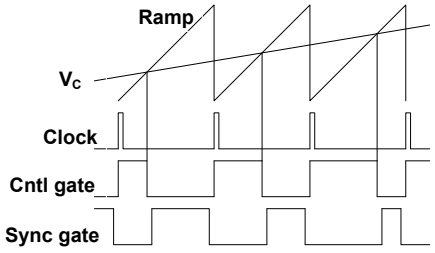



Fig. 7: Trailing-edge Modulation

### Frequency Synchronization

The IR3640 is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge at an external clock. The switching frequency is set by external resistor ($R_t$). During synchronization, $R_t$ is selected such that the free running frequency is 20% below the synchronization frequency. When unused, the sync pin will remain floating and is noise immune.

### Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduce cost by eliminating a current sense resistor. As shown in Fig. 8, an external resistor ($R_{OCset}$ is connected between OCSet pin and the drain of low side MOSFET (Q2) which sets the current limit set point.

The internal current source develops a voltage across $R_{SET}$. An internal current source sources current ($I_{OCSet}$ ) out of the *OCSet* pin. This current is a function of the switching frequency and hence, of $R_t$. Table 1. shows $I_{OCSet}$ at different switching frequencies.

$$I_{OCSet}(\mu A) = \frac{1400}{R_t(k\Omega)} \qquad --(2)$$

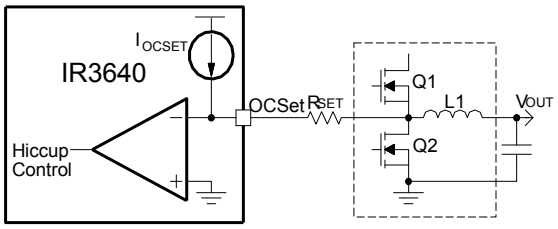



Fig. 8: Connection of over current sensing resistor

When the low side MOSFET is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \qquad --(3)$$

An over current is detected if the OCSet pin goes below ground. Hence, at the current limit threshold, $V_{OCset}$=0. Then, for a current limit setting $I_{Limit}$, $R_{OCSet}$ is calculated as follows:

$$R_{OCSet} = \frac{R_{DS(on)} * I_{Limit}}{I_{OCSet}} \qquad --(4)$$

An over-current detection trips the OCP comparator, latches OCP signal and cycles the soft start function in hiccup mode.

The hiccup is performed by shorting the soft-start capacitor to ground and counting the number of switching cycles. The soft start pin is held low until 4096 cycles have been completed. The OCP signal resets and the converter recovers. After every soft start cycle, the converter stays in this mode until the overload or short circuit is removed.

The OCP circuit starts sampling current typically 160 ns after the low gate drive rises to about 3V. This delay functions to filter out switching noise.

The value of $R_{OCSet}$ should be checked in an actual circuit to ensure that the over current protection circuit activates as expected.

### Shutdown

The IR3640 can be shutdown by pulling the Enable pin below its 1 V threshold. This will tri-state both, the high side driver as well as the low side driver. Alternatively, the output can be shutdown by pulling the soft-start pin below 0.3V. In shutdown by this method, the high side driver is turned off, and the low side driver is turned on. Thus, in this method, the output voltage can be actively discharged through the synchronous FET. Normal operation is resumed by cycling the voltage at the Soft Start pin.

### Output Voltage Sequencing

The IR3640 can accommodate a full spectrum of user programmable sequencing option using Seq, Enable and Power Good pins.

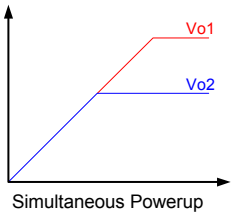



Fig. 9a: Simultaneous Power-up of the slave with respect to the master.

Through these pins, voltage sequencing such as simultaneous, sequential, etc. can be implemented. Figure 9b shows simultaneous sequencing configurations. In simultaneous powerup, the voltage at the Seq pin of the slave reaches 0.7V before the Fb pin of the master. For $R_E/R_F = R_C/R_D$, therefore, the output voltage of the slave follows that of the master until the voltage at the Seq pin of the slave reaches 0.7 V. After the voltage at the Seq pin of the slave exceeds 0.85V, the internal 0.7V reference of the slave dictates its output voltage.

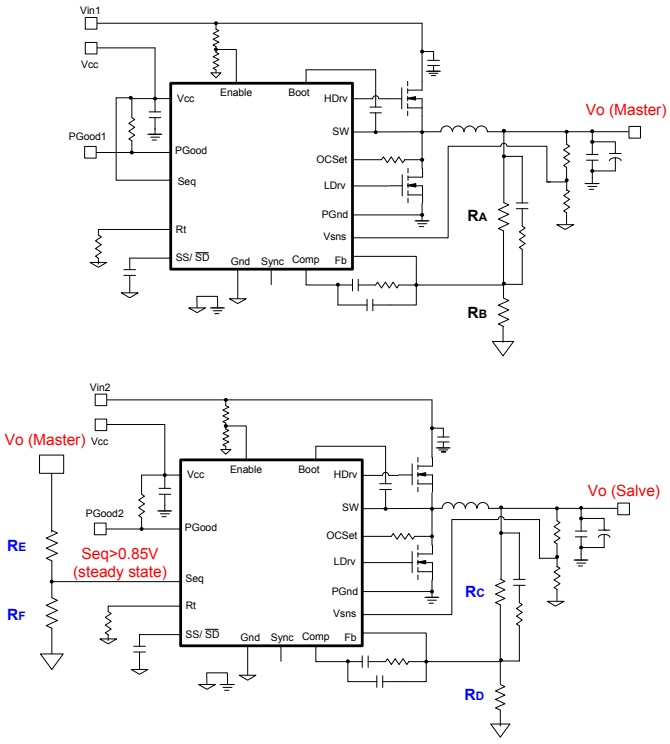



Fig. 9b: Application Circuit for Simultaneous Sequencing

### Thermal Shutdown

Temperature sensing is provided inside IR3640. The trip threshold is typically set to 140°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and discharges the soft start capacitor. Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

### Power Good and Over-voltage Protection

The IC continually monitors the output voltage via sense pin. The Vsns voltage compares to a fixed voltage. As soon as the sensed voltage reaches 0.88*Vref, the Power Good signal flags. Power Good pin needs to be externally pulled high. High state indicates that output is in regulation. Figure 10a and 10b shows the timing diagrams of Power Good function.

If the output voltage exceeds the over voltage threshold, an over voltage trip signal asserts, this will result to turn off the high side driver and turn on the low side driver until the Vsns voltage drops below 1.15*Vref threshold. Both drivers are latched off until a reset performed by cycling either Vcc or Enable.

The OVP threshold can be externally programmed to user defined value. Figure 10c shows the response in over-voltage condition.

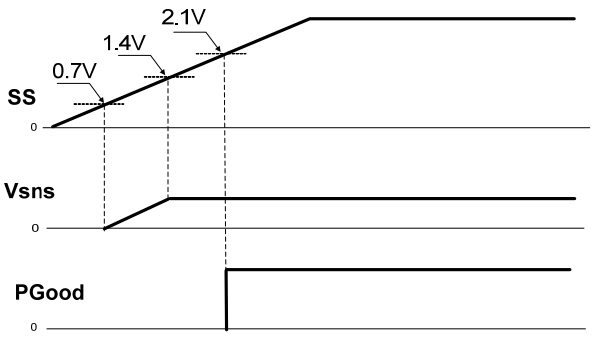



Fig.10a: IR3640 Non-Sequencing Power Up (Seq=Vcc)

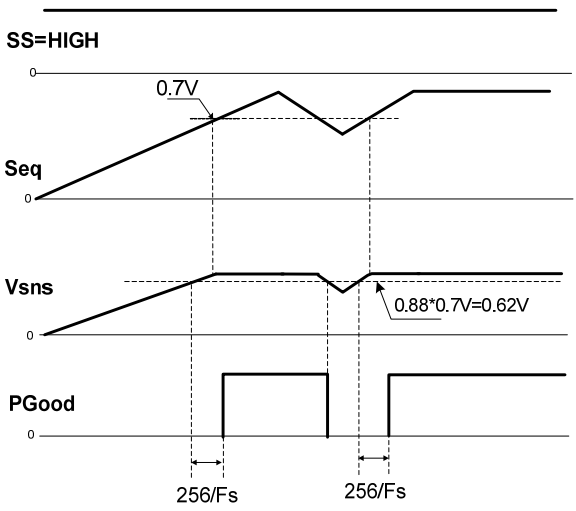



Fig.10b: IR3640 Sequencing Power Up

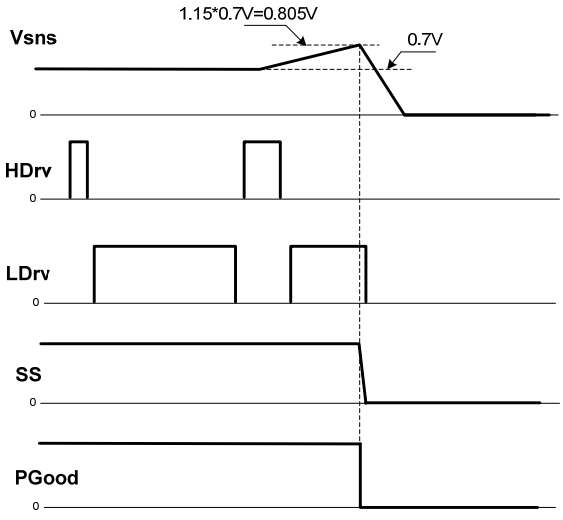



Fig.10c: IR3640 Timing Diagram of Over-voltage Protection

### Minimum on time Considerations

The minimum ON time is the shortest amount of time for which the Control FET may be reliably turned on, and this depends on the internal timing delays. For the IR3640, the typical minimum on-time is specified as 50 ns.
Any design or application using the IR3640 must ensure operation with a pulse width that is higher than this minimum on-time and preferably higher than 100 ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses the IR3640, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on}$$

$$\therefore t_{on(\min)} \le \frac{V_{out}}{V_{in} \times F_s}$$

$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.7 V. Therefore, for $V_{out(min)}$ = 0.7 V,

$$\therefore V_{in} \times F_s \le \frac{V_{out(\min)}}{t_{on(\min)}}$$

$$\therefore V_{in} \times F_s \le \frac{0.7\ \text{V}}{100\ \text{ns}} = 7 \times 10^6\ \text{V/s}$$

Therefore, at the maximum recommended input voltage 24V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 292 kHz. Conversely, for operation at the maximum recommended operating frequency 1.65 MHz and minimum output voltage, any voltage above 4.2 V may not be stepped down without pulse-skipping.

### Maximum Duty Ratio Considerations

A fixed off-time of 200 ns maximum is specified for the IR3640. This provides an upper limit on the operating duty ratio at any given switching frequency. It is clear, that higher the switching frequency, the lower is the maximum duty ratio at which the IR3640 can operate. To allow some margin, the maximum operating duty ratio in any application using the IR3640 should still accommodate about 250 ns off-time. Figure 11 shows a plot of the maximum duty ratio vs. the switching frequency, with 250 ns off-time.

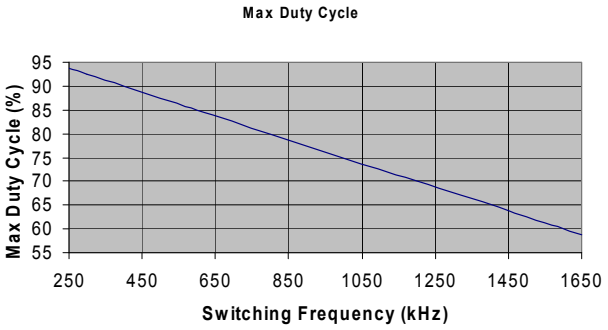



Fig. 11: Maximum duty cycle vs. switching frequency

## Application Information

### Design Example:

The following example is a typical application for IR3640. The application circuit is shown on page 23.

$V_{in}$=12V,(13.2V,max )
$V_o$=1.8V
$I_o$=25A
$\Delta V_o \leq$ 54mV
$F_s$=600kHz

### Enabling the IR3640

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage.

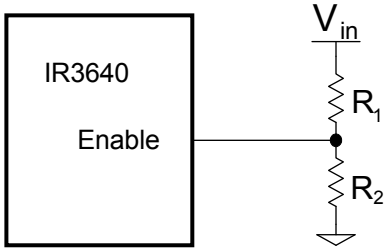



Fig. 12: Typical application of the IR3640 for programming the Enable threshold

For a typical Enable threshold of $V_{EN}$ = 1.2 V

$$V_{in(\min)} * \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad --(5)$$

$$R_2 = R_1 \frac{V_{EN}}{V_{in(\min)} - V_{EN}} \quad --(6)$$

For a $V_{in\ (min)}$=10.1V, $R_1$=4.99K and $R_2$=681 ohm is a good choice.

### Programming the frequency

For $F_s$ = 600 kHz, select $R_t$ = 23.7 kΩ, using Table. 1.

### Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.7V. The divider is ratioed to provide 0.7V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad --(7)$$

When an external resistor divider is connected to the output as shown in figure 11.

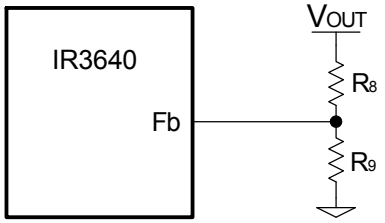



Fig. 13: Typical application of the IR3640 for programming the output voltage

Equation (7) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_O - V_{ref}}\right) \quad --(8)$$

For the calculated values of $R_8$ and $R_9$ see feedback compensation section.

### Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} = \frac{\text{Tstart} * 20\text{uA}}{(1.4 - 0.7)V} \quad --(9)$$

Where $T_{start}$ is the desired start-up time (ms).
For a start-up time of 3.5ms, the soft-start capacitor will be 0.099uF. Choose a ceramic capacitor at 0.1uF.

### Bootstrap Capacitor Selection

To drive the high side switch, it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external capacitor (C6). The operation of the circuit is as follows: When the lower MOSFET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards $PV_{cc}$ through the internal bootstrap diode, which has a forward voltage drop $V_D$. The voltage $V_C$ across the bootstrap capacitor C6 is approximately given as

$$V_C \cong PV_{CC} - V_D \quad \text{--(10)}$$

When the upper MOSFET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage $V_{in}$. However, if the value of C6 is appropriately chosen, the voltage $V_C$ across C6 remains approximately unchanged and the voltage at the Boot pin becomes

$$V_{Boot} \cong V_{in} + PV_{cc} - V_D \quad \text{--(11)}$$

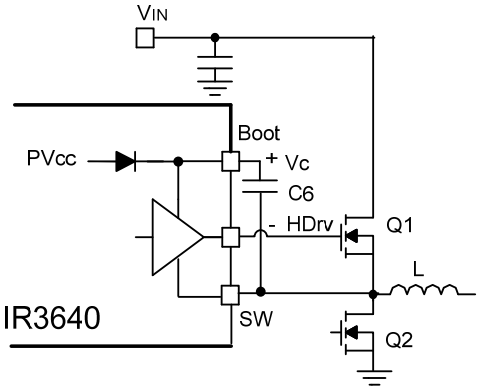



Fig. 14: Bootstrap circuit to generate Vc voltage

A capacitor in the range of 0.1uF is generally adequate for most applications.

### Input Capacitor Selection

The ripple current generated during the on time of upper the MOSFET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{--(12)}$$

$$D = \frac{V_o}{V_{in}} \quad \text{--(13)}$$

Where:

D is the Duty Cycle

$I_{RMS}$ is the RMS value of the input capacitor current.

Io is the output current.

For Io=25A and D=0.15, the $I_{RMS}$=8.9A.

Ceramic capacitors are recommended due to their peak current capabilities, they also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 4x10uF 25V ceramic capacitors GRM31CR61E106KA12L from Murata Electronics. In addition to these, although not mandatory, a 2X330uF, 25V SMD capacitor EEV-FK1E331P may also be used as a bulk capacitor.

### Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor $(\Delta i)$ . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\quad \Delta t = D * \frac{1}{F_s}$$
$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \qquad --(14)$$

Where:

$V_{in}$ = *Maximum input voltage*
$V_o$ = *Output Voltage*
$\Delta i$ = *Inductor ripple current*
$F_s$ = *Switching frequency*
$\Delta t$ = *Turn on time*
$D$ = *Duty cycle*

If $\Delta i \approx 35\%(I_o)$ , then the output inductor is calculated to be 0.29uH. Select L=0.33uH

The MPL104-R33 from Delta provides a compact, low profile inductor suitable for this application.

**Output Capacitor Selection**

The voltage ripple and transient requirements determine the output capacitors type and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

$\Delta V_o$ = Output vdtage ripple

$\Delta I_L$ = Inductor ripple current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3840 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Ten of the Murata GRM21BR60G476ME15L (47uF/4V) capacitors is a good choice.

**Power MOSFET Selection**

The IR3640 uses two N-Channel MOSFETs per channel. The selection criteria to meet power transfer requirements are based on maximum drain-source voltage ($V_{DSS}$), gate-source drive voltage ($V_{gs}$), maximum output current, On-resistance $R_{DS(on)}$, and thermal management.

The MOSFET must have a maximum operating voltage ($V_{DSS}$) exceeding the maximum input voltage ($V_{in}$).

The gate drive requirement is almost the same for both MOSFETs. A logic-level transistor can be used and caution should be taken with devices at very low gate threshold voltage ($V_{gs}$) to prevent undesired turn-on of the complementary MOSFET, which results in a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{cond}(\text{upperswitch}) = I_{load}^2 * R_{ds(on)} * D * \vartheta$$
$$P_{cond}(\text{lowerswitch}) = I_{load}^2 * R_{ds(on)} * (1-D) * \vartheta$$
$\vartheta = R_{ds(on)}$ temperature dependency

The $R_{DS(on)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET datasheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, the IRF6710 is selected for control FET and IRF6795 is selected for the synchronous FET. These devices provide low on resistance in a DirectFET package.

The MOSFETs have the following data:

| ControlFET(IRF6710) | SyncFET(IRF6795) |
|---|---|
| $V_{ds} = 25V, Q_g = 8.8nC$ | $V_{ds} = 25V, Q_g = 35nC$ |
| $R_{ds(on)} = 9.0m\Omega @ V_{gs} = 4.5V$ | $R_{ds(on)} = 2.4m\Omega @ V_{gs} = 4.5V$ |

The conduction losses will be: $P_{cond}$*=2.12W at Io=25A.* The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times, such as turn-on / turn-off delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in a synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{sw} = \frac{V_{ds(off)}}{2} * \frac{t_r + t_f}{T} * I_{load} \quad \text{--(15)}$$

Where:

$V_{ds(off)}$ = Drain to source voltage at the off time

$t_r$ = Rise time

$t_f$ = Fall time

T = Switching period

$I_{load}$ = Load current

The switching time waveforms is shown in Fig. 15.

From IRF6710 data sheet:

tr = 20ns

tf = 6ns

These values are taken under a certain test condition. For more details please refer to the IRF6710 data sheet.

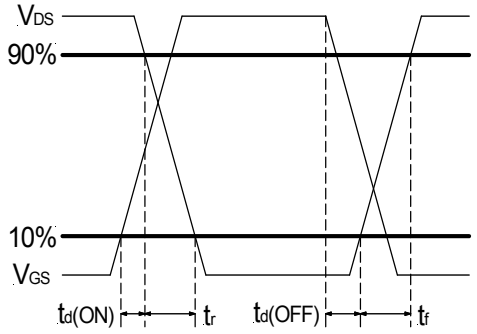



Fig. 15: Switching time waveforms

By using equation (15), we can calculate the switching losses. $P_{sw}$*=2.34W at Io=25A.*

The reverse recovery loss is also another contributing factor in control FET switching losses. This is equivalent to extra current required to remove the minority charges from the synchronous FET. The reverse recovery loss can be expressed as:

$$P_{Qrr} = Q_{rr} * V_{in} * F_s$$

$Q_{rr}$: Reverse Recovery Charge

$V_{in}$: Input Bus Voltage

$F_s$: Switching Frequency

The gate driving loss is the power consumption to drive both the control and synchronous FETs. The gate driving loss can be estimated as:

$$P_{Driver} = Q_g * V_g * F_s$$

$Q_g$: Total Gate Charge

$V_g$: Gate Driving Voltage

$F_s$: Switching Frequency

**Feedback Compensation**

The IR3640 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Fig. 16). The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2*\pi\sqrt{L_o * C_o}} \quad \text{--(16)}$$

Figure 16 shows gain and phase of the LC filter. Since we already have 180° phase shift from the output filter alone , the system risks being unstable.

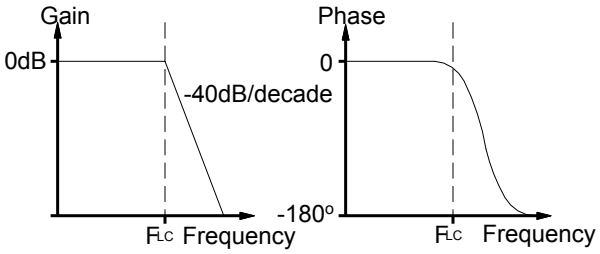



Fig. 16: Gain and Phase of LC filter

The IR3640 uses a voltage-type error amplifier with high-gain (110dB) and wide-bandwidth. The output of it is available for DC gain control or AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation. When it is used in type II compensation, a series RC circuit from Comp pin to ground as shown in figure 16 is used.

This method requires the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \quad \text{--(17)}$$

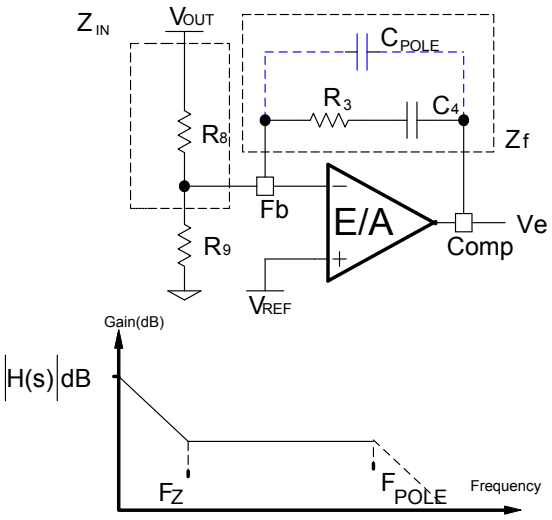



Fig. 17: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$\frac{V_e}{V_o} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_4}{sR_8C_4} \quad \text{--(18)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = \frac{R_3}{R_8} \quad \text{--(19)}$$

$$F_z = \frac{1}{2\pi*R_3*C_4} \quad \text{--(20)}$$

First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * R_8}{V_{in} * F_{LC}^2} \quad \text{--(21)}$$

Where:
$V_{in}$ = Maximum Input Voltage
$V_{osc}$ = Oscillator Ramp Voltage
$F_o$ = Crossover Frequency
$F_{ESR}$ = Zero Frequency of the Output Capacitor
$F_{LC}$ = Resonant Frequency of the Output Filter
$R_8$ = Feedback Resistor

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad \text{--(22)}$$

Using equations (15) and (16) to calculate C4.
One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}}$$

The pole sets to one half of the switching frequency which results in the capacitor $C_{POLE}$:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s}$$

For a general solution for unconditional stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network (type III). The typically used compensation network for voltage-mode controller is shown in Fig. 17.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = -\frac{Z_f}{Z_{IN}}$$

By replacing $Z_{in}$ and $Z_f$ according to Fig. 17, the transfer function can be expressed as:

$$H(s) = \frac{-1}{sR_8(C_4 + C_3)} * \frac{(1 + sR_3C_4) * [1 + sC_7(R_8 + R_{10})]}{\left[1 + sR_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)\right] * (1 + sR_{10}C_7)}$$

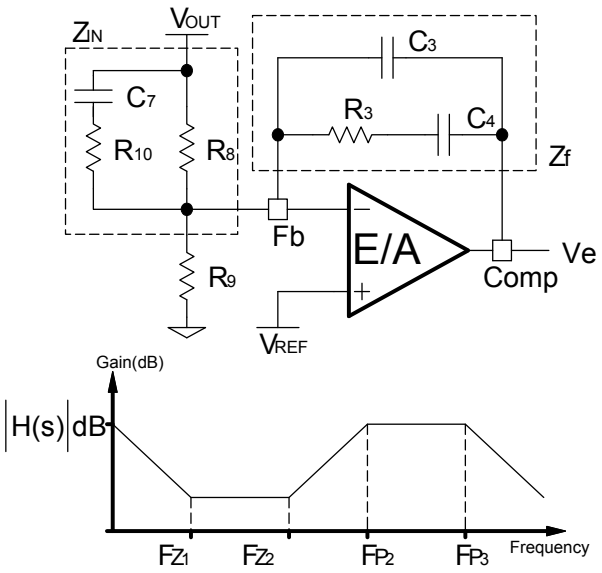



Fig.18: Compensation network with local feedback and its asymptotic gain plot

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7}$$

$$F_{P3} = \frac{1}{2\pi * R_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)} \cong \frac{1}{2\pi * R_3 * C_3}$$

$$F_{z1} = \frac{1}{2\pi * R_3 * C_4}$$

$$F_{z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8}$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by the output capacitor and its ESR versus crossover frequency, the compensation type can be different. Table 2 below shows the compensation types and location of the crossover frequency.

Table 2 The compensation type and location of $F_{ESR}$ versus $F_o$

| Compensator Type | $F_{ESR}$ vs $F_o$ | Output Capacitor |
|---|---|---|
| Type II | $F_{LC}<F_{ESR}<F_o<F_s/2$ | Electrolytic Tantalum |
| Type III | $F_{LC}<F_o<F_{ESR}$ | Tantalum Ceramic |

The higher the crossover frequency, the potentially faster the load transient response. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency is selected such that

$$F_o \le (1/5 \sim 1/10) * F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45º for overall stability.

For this design we have:
$V_{in}$=12V
$V_o$=1.8V
$V_{osc}$=1.8V
$V_{ref}$=0.7V
$L_o$=0.33uH
$C_o$=10x47uF(ceramic)

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 47uF capacitor used in this design is 23uF at 1.8 V DC bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency $F_{LC}$ and using equation (16) to compute the small signal $C_o$.

These result to:

**$F_{LC}$=18.3kHz**
**$F_{ESR}$=2306kHz**
**$F_{s/2}$=300kHz**

Select crossover frequency:

**Fo=100kHz**

Since: $F_{LC}<F_o<F_{S/2}<F_{ESR}$, TypeIII is selected to place the pole and zeros. Detailed calculation of compensation TypeIII:

Desired Phase Margin $\Theta = 70^{\circ}$

$$F_{Z2} = F_o \sqrt{\frac{1-\sin\Theta}{1+\sin\Theta}} = 17.63\text{kHz}$$

$$F_{P2} = F_o \sqrt{\frac{1+\sin\Theta}{1-\sin\Theta}} = 567.1\text{kHz}$$

Select $F_{Z1} = 0.5 * F_{Z2} = 8.82\,\text{kHz}$ and

$$F_{P3} = 0.5 * F_s = 300\ \text{kHz}$$

Select $C_7 = 2.2\text{nF}$

Calculate $R_3$, $C_3$ and $C_4$:

$$R_3 = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{C_7 * V_{in}};\ R_3 = 3.25\ \text{k}\Omega$$

Select $R_3 = 3.24\,\text{k}\Omega$

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3};\ C_4 = 5.57\ \text{nF},\ \text{Select}\ C_4 = 5.6\ \text{nF}$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3};\ C_3 = 16374\ \text{pF},\ \text{Select}\ C_3 = 160\,\text{pF}$$

Calculate $R_{10}$, $R_8$ and $R_9$:

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}};\ R_{10} = 130\,\Omega,\ \text{Select}\ R_{10} = 130\,\Omega$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10};\ R_8 = 3.98\text{k}\Omega$$

$$\text{Select}\ R_8 = 4.02\text{k}\Omega$$

$$R_9 = \frac{V_{ref}}{V_o - V_{ref}} * R_8;\ R_9 = 2.56\text{k}\Omega\ \ \text{Select}\ R_9 = 2.55\text{k}\Omega$$

### Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor ($R_{OCSET}$) from the drain of the low-side MOSFET to the OCSet pin. The resistor can be calculated by using equation (3). The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worst case operation. This resistor must be placed close to the IC. This IC doesn't require a small ceramic capacitor from OCset pin to ground.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad --(23)$$

$$R_{DS(on)} = 2.4m\Omega * 1.5 = 3.6m\Omega$$
$$I_{SET} \cong I_{o(LIM)} = 25A * 1.5 = 37.5A$$
$$(50\%\ \text{over nominal output current})$$
$$I_{OCSet} = 59.1uA\ \ (\text{at Fs} = 600\text{kHz})$$
$$R_{OCSet} = 2.29K\Omega\ \ \text{Select}\ \ R_7 = 2.26K\Omega$$

### Setting the Power Good Threshold

Power Good threshold can be programmed by using two external resistors (R6, R7 in Page 23).

The following formula can be used to set the threshold:

$$R_6 = \left(\frac{0.9 * V_{out}}{0.88 * V_{ref}} - 1\right) * R_7 \quad --(24)$$

Where: $0.88*V_{ref}$ is reference of the internal comparator, for IR3640, it is 0.62V
0.9*Vout is selectable threshold for power good, for this design it is 1.62V.

Select $R_7$=2.55KOhm

Using (24): $R_6$=4.16KOhm

Select $R_6$=4.12KOhm

Use a pull up resistor (4.99K) from PGood pin to Vcc.

### Layout Consideration

The layout is very important when designing high frequency switching converters. Poor layout will affect noise pickup and can cause a good design to perform with less than expected results.
Start to place the power components, making all the connection in the top layer with wide, copper filled areas. The inductor, output capacitors and the MOSFETS should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor very close to the drain of the high-side MOSFET.
The feedback part of the system should be kept away from the inductor and other noise sources.
The critical bypass components such as capacitors for Vcc and PVcc should be close to the respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.
Place the Rocset resistor close to Ocset pin and connect this with a short trace to SW pin.
In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.
The MLPQ is a thermally enhanced package. Based on thermal performance it is recommended to use 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to ground plane using vias.

## Application Diagram:

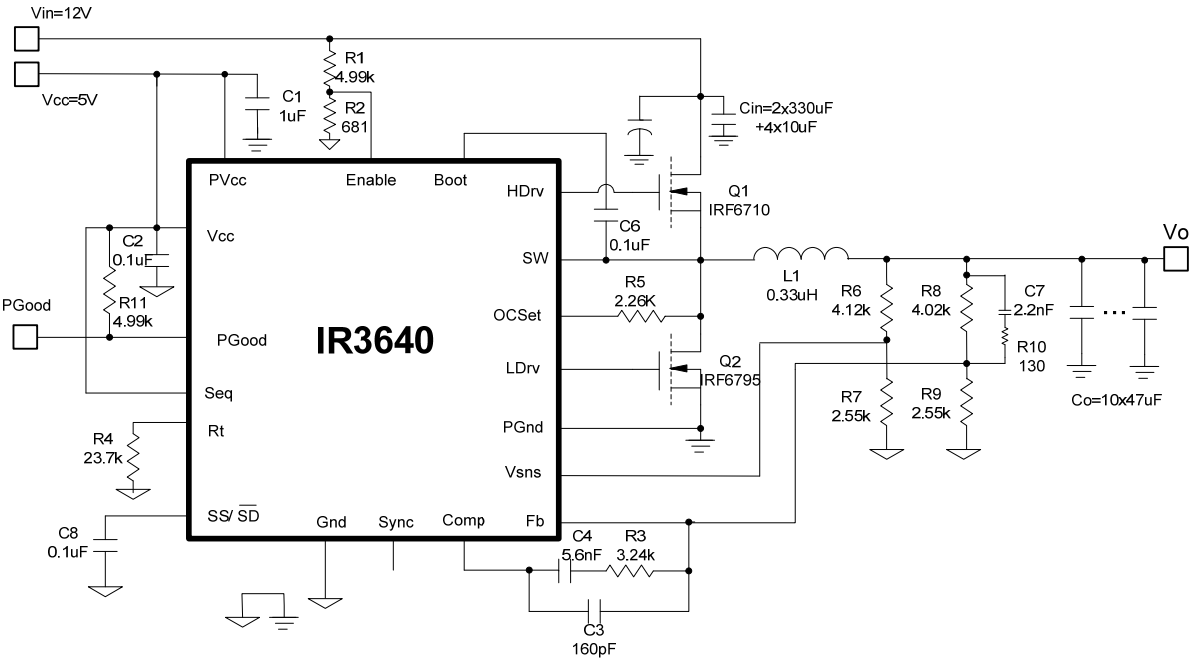



Fig. 19: Typical Application Circuit for Non-Sequencing
12V to 1.8V, 25A Point of Load Converter

## Suggested Bill of Materials for the application circuit:

| Reference | Value | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| Cin | 330uF | SMD Elecrolytic, 25V,F-size,20% | Panasonic | EEE-FK1E331P |
| Cin | 10uF | Ceramic,25V,1210,X5R,10% | Taiyo-Yuden | TMK325BJ106MN-T |
| Co | 47uF | Ceramic,4V,0805,X5R,10% | Murata Electronics | GRM21BR60G476ME15L |
| C1 | 1.0uF | Ceramic,25V,0603,X5R,10% | Murata Electronics | GRM188R61E105KA12D |
| C2 C6 C8 | 0.1uF | Ceramic,50V,0603,X7R,10% | Panasonic | ECJ-1VB1H104K |
| C3 | 160pF | Ceramic,50V,0603,C0G,5% | Murata Electronics | GRM1885C1H161JA01D |
| C4 | 5.6nF | Ceramic,25V,0603,C0G,5% | Panasonic-ECG | C1608C0G1E562J |
| C7 | 2200pF | Ceramic,50V,0603,C0G,5% | TDK Corporation | C1608C0G1H222J |
| L1 | 0.33uH | SMT-Inductor,1.5mOhms,10x11mm,20% | Delta | MPL104-R33IR |
| Q1 | IRF6710S2TRPbF | IRF6710 SQ 25V | International Rectifier | IRF6710S2TRPbF |
| Q2 | IRF6795MPbF | IRF6795 MX 25V | International Rectifier | IRF6795MPbF |
| R1 R11 | 4.99K | Thick-film,0603,1/10W,1% | Rohm | MCR03EZPFX4991 |
| R2 | 681 | Thick-film,0603,1/10 W,1% | Vishey/Dale | CRCW0603681RFKEA |
| R3 | 3.24K | Thick-film,0603,1/10W,1% | Rohm | MCR03EZPFX3241 |
| R4 | 23.7K | Thick-film,0603,1/10W,1% | Rohm | MCR03EZPFX2372 |
| R5 | 2.26K | Thick-film,0603,1/10W,1% | Rohm | MCR03EZPFX2261 |
| R6 | 4.12K | Thick-film,0603,1/10 W,1% | Rohm | MCR03EZPFX4121 |
| R7 R9 | 2.55K | Thick-film,0603,1/10 W,1% | Rohm | MCR03EZPFX2551 |
| R8 | 4.02K | Thick-film,0603,1/10 W,1% | Rohm | MCR03EZPFX4021 |
| R10 | 130 | Thick-film,0603,1/10 W,1% | Rohm | MCR03EZPFX1300 |

**Application Diagram:**

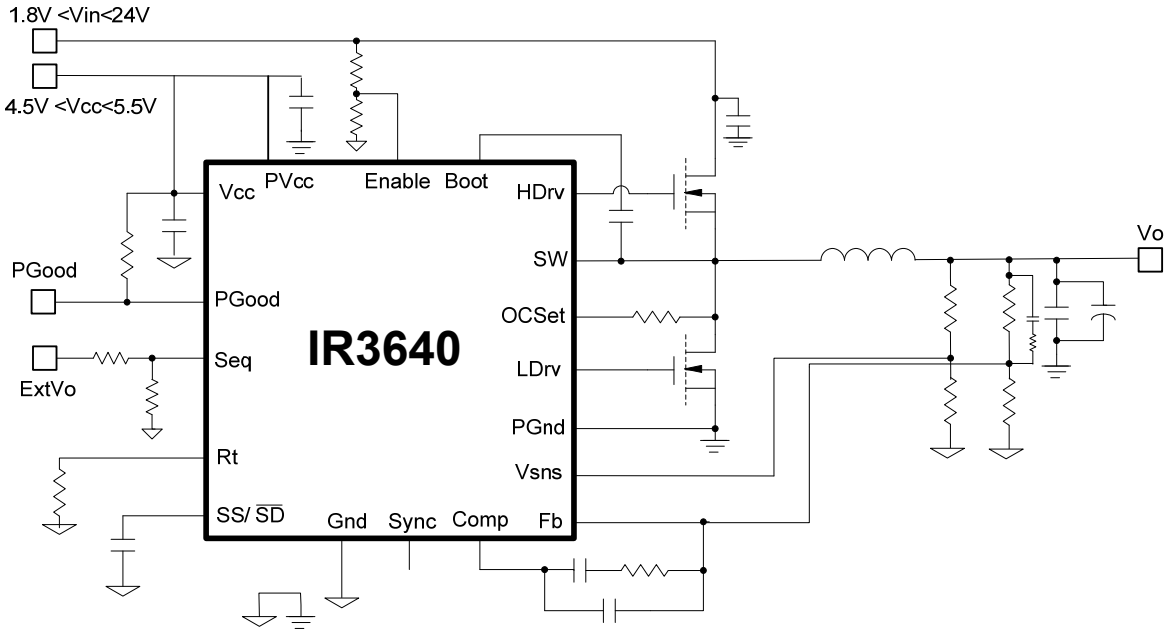



Fig. 20: Typical Circuit for Sequencing Application

## TYPICAL OPERATING WAVEFORMS

(Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0- 25A, Room Temperature, No Air Flow, Fig.19)

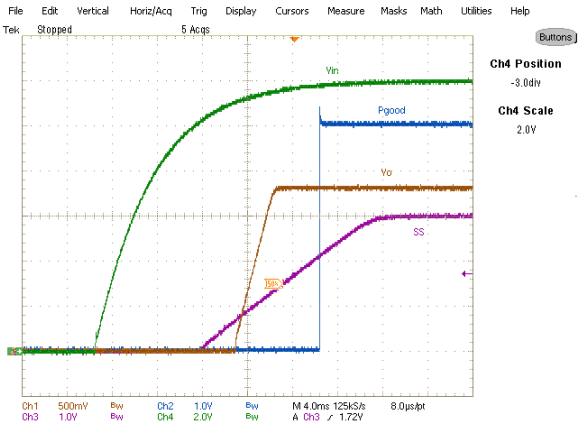



Fig. 21: Start up at 0A Load
$Ch_1$:$V_o$, $Ch_2$:PGood $Ch_3$:$V_{SS}$ $Ch_4$: $V_{in}$

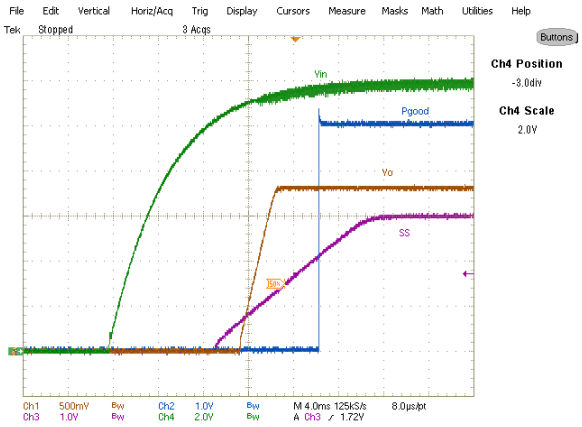



Fig. 22: Start up at 25A Load
$Ch_1$:$V_o$, $Ch_2$:PGood $Ch_3$:$V_{SS}$ $Ch_4$: $V_{in}$

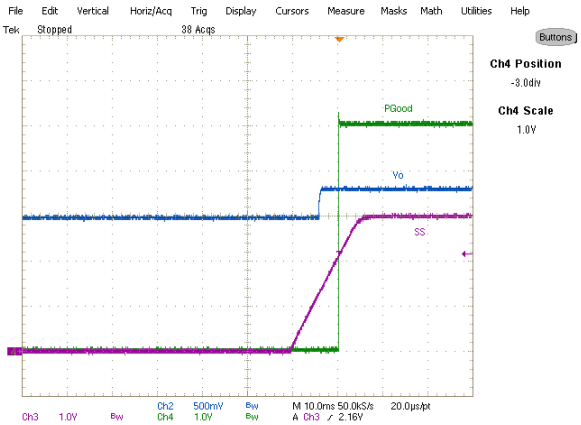



Fig. 23: Start up with 1.5V Prebias,
0A Load, $Ch_2$:$V_{out}$ $Ch_3$:$V_{SS}$ $Ch_4$: PGood

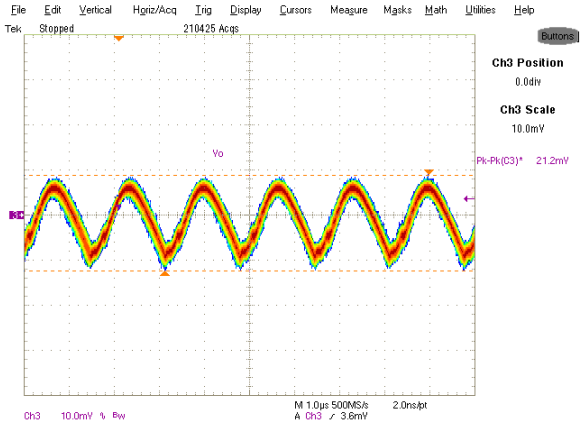



Fig. 24: Output Voltage Ripple, 25A load
$Ch_3$: $V_{out}$

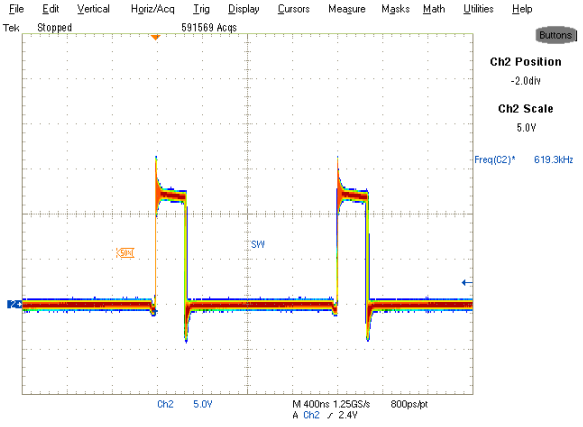



Fig. 25: Inductor node at 25A load
$Ch_2$:SW

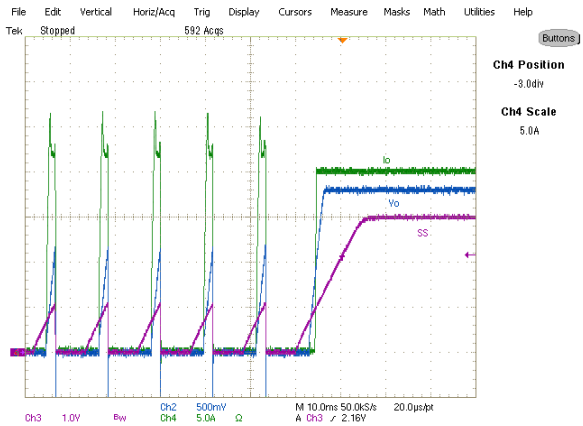



Fig. 26: Short (Hiccup) Recovery
$Ch_2$:$V_{out}$, $Ch_3$:$V_{SS}$ , $Ch_4$:Io

## TYPICAL OPERATING WAVEFORMS

(Vin=12V, Vcc=5V, Vo=1.8V, Room Temperature, No Air Flow, Fig.19)

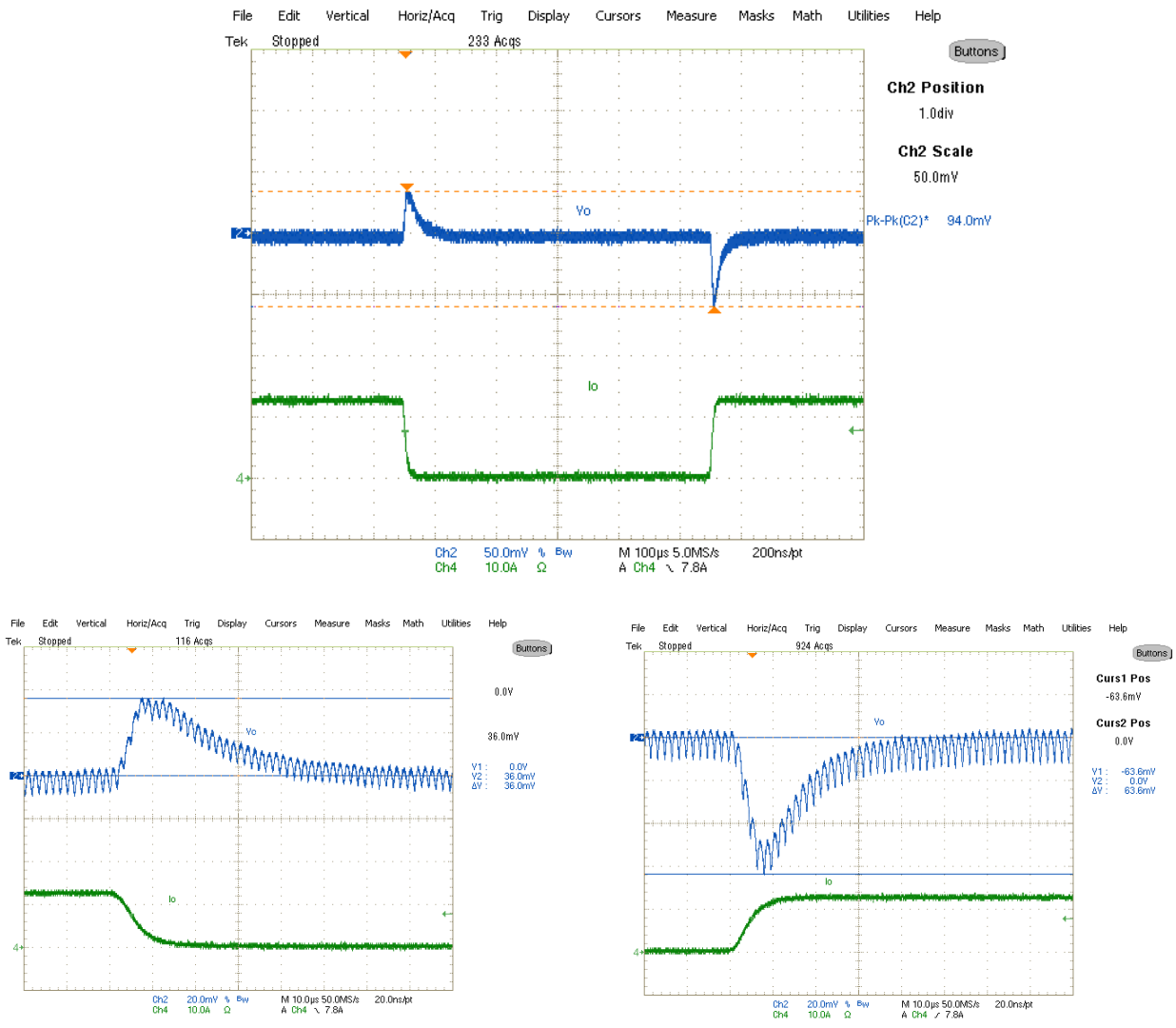



Fig. 27: Transient Response
0A-12.5A load $Ch_2$:$V_{out}$, $Ch_4$:$I_o$

## TYPICAL OPERATING WAVEFORMS

(Vin=12V, Vcc=5V, Vo=1.8V, Io=0-25A, Room Temperature, No Air Flow, Fig.19)

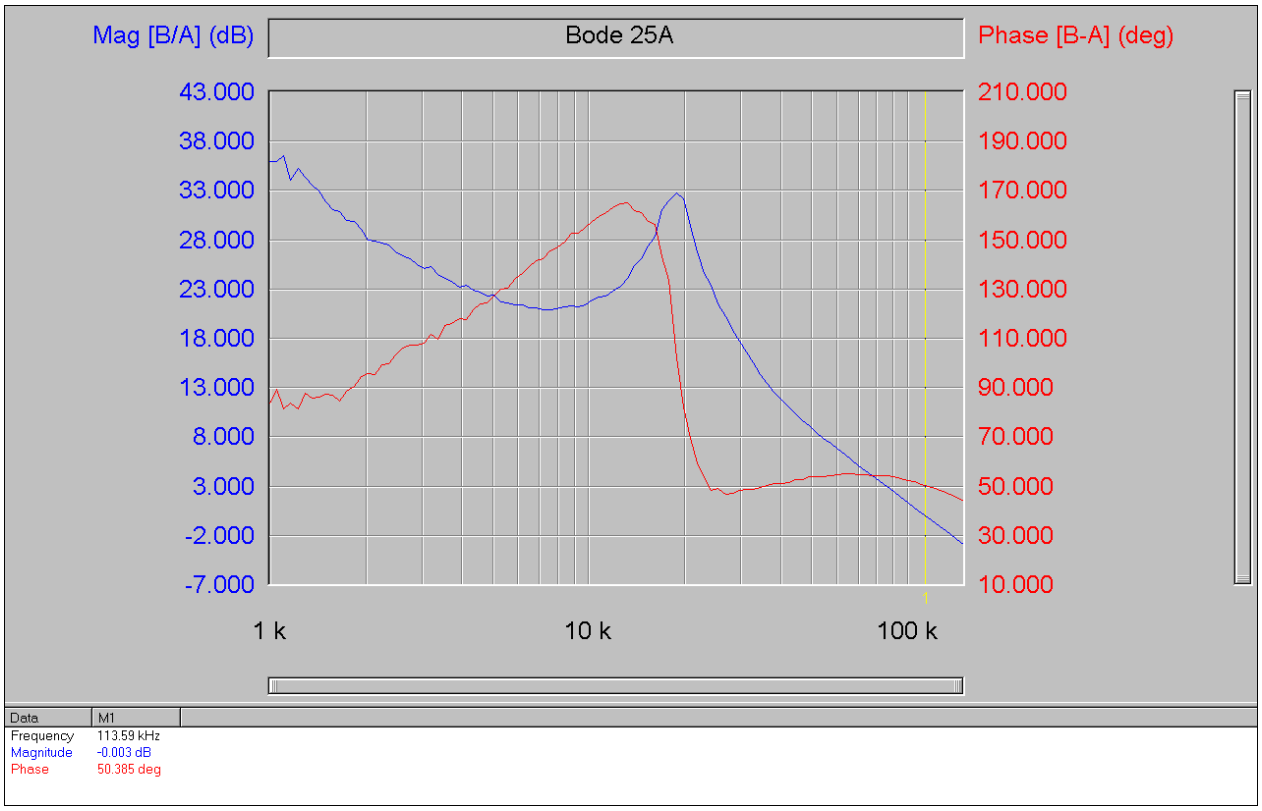
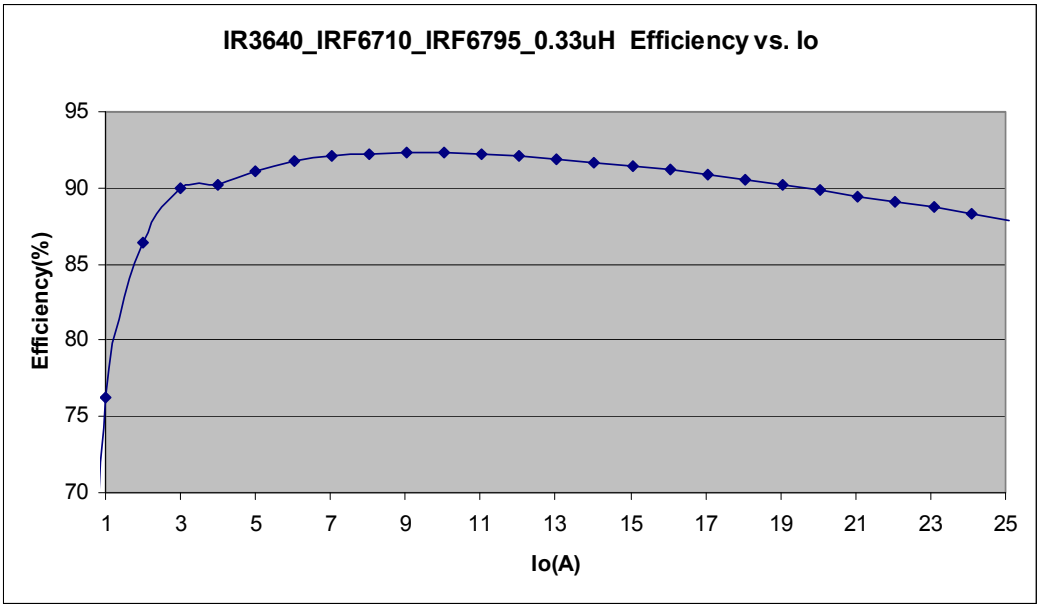



Fig.28: Bode Plot at 25A load shows a bandwidth of 113.6kHz and phase margin of 50.4 degrees

## TYPICAL OPERATING WAVEFORMS

(Vin=12V, Vo=1.8V, Io=0-25A, Room Temperature, No Air Flow, Fig.19)



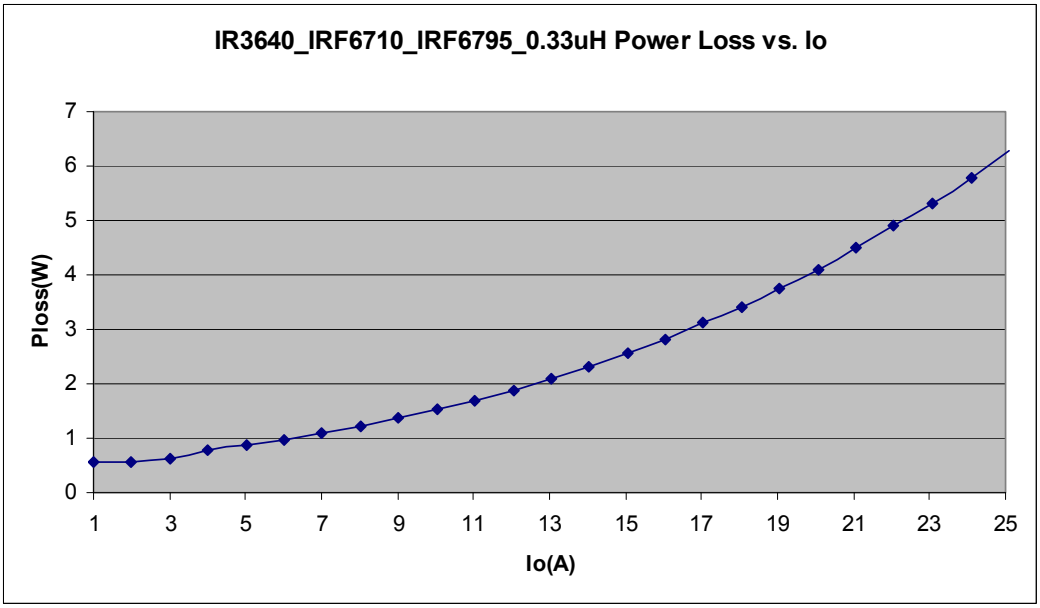
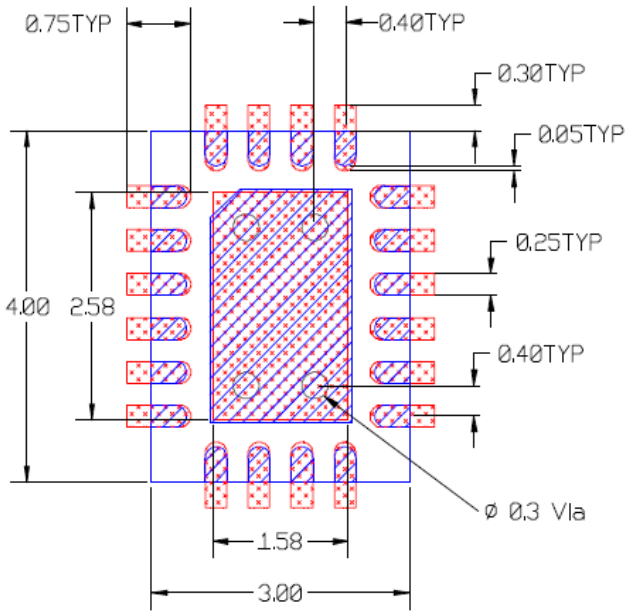




Fig.29: Efficiency and power loss vs. load current

## PCB Metal and Components Placement

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension +0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper).
- Four 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



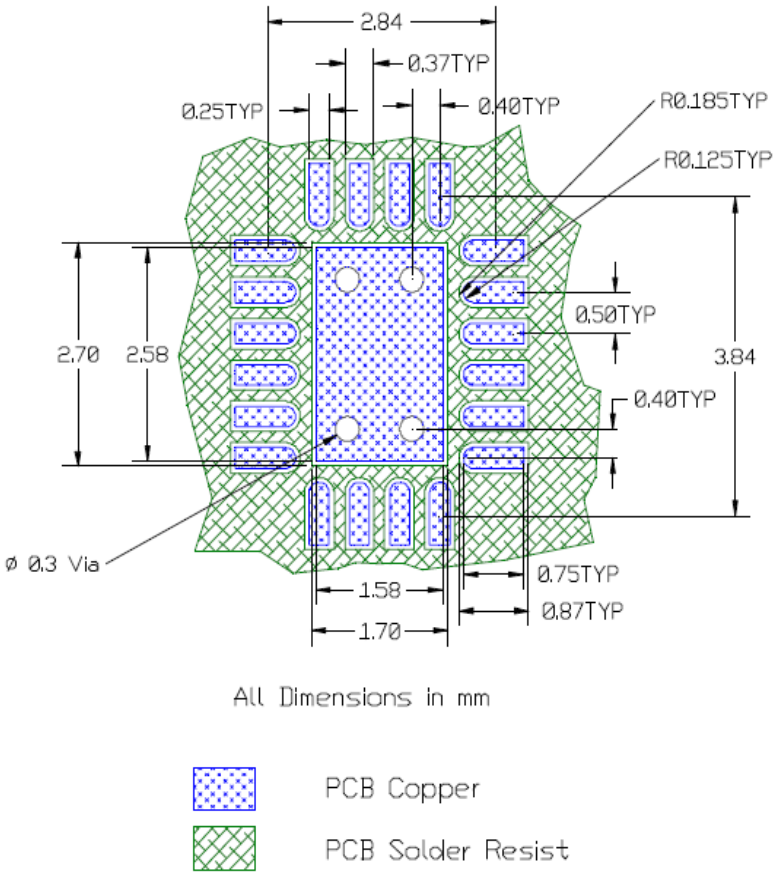

All Dimensions In mm

PCB Copper

Component

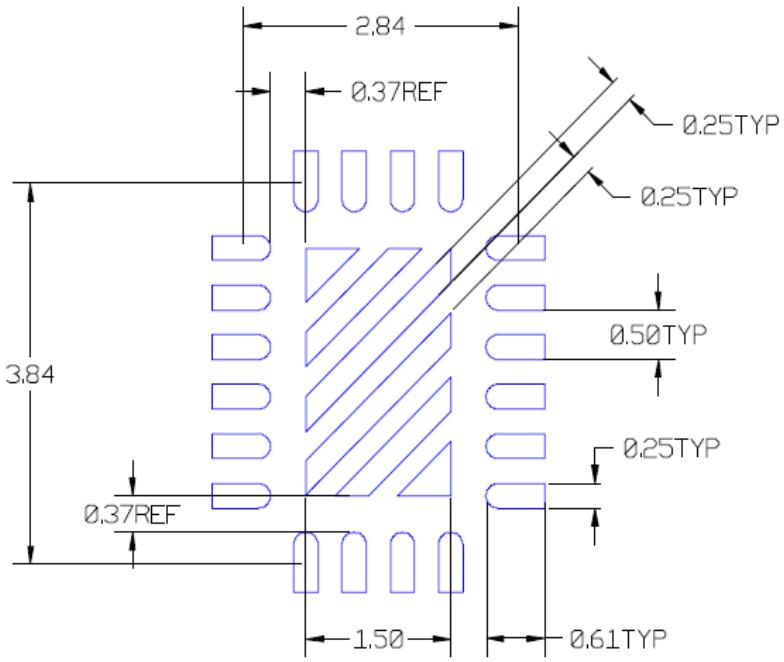
## Solder Resist

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm. At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Non Solder Mask Defined (NSMD), with a minimum pullback of the solder resist off the copper of 0.06mm to accommodate solder resist mis-alignment.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- Each via in the land pad should be tented or plugged from bottom boardside with solder resist.



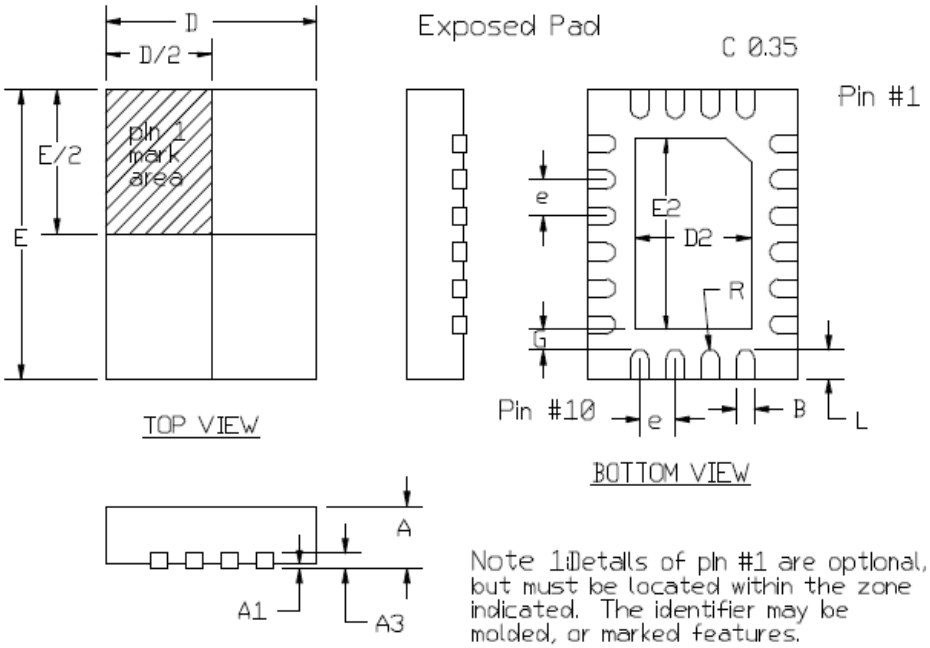
## Stencil Design

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mmpitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.




Stencil Aperture

All Dimensions in mm




| 20L 3x4 (unit: MM) | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.8 | 0.85 | 0.9 |
| A1 | 0.00 | | 0.05 |
| A3 | 0.20 REF | | |
| B | 0.20 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 1.55 | 1.65 | 1.75 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.55 | 2.65 | 2.75 |
| e | 0.5 REF | | |
| G | 0.275 REF | | |
| L | 0.30 | 0.40 | 0.50 |
| R | 0.125 TYP | | |

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