IR3651SPBF

HIGH VOLTAGE SYNCHRONOUS PWM BUCK CONTROLLER

Features

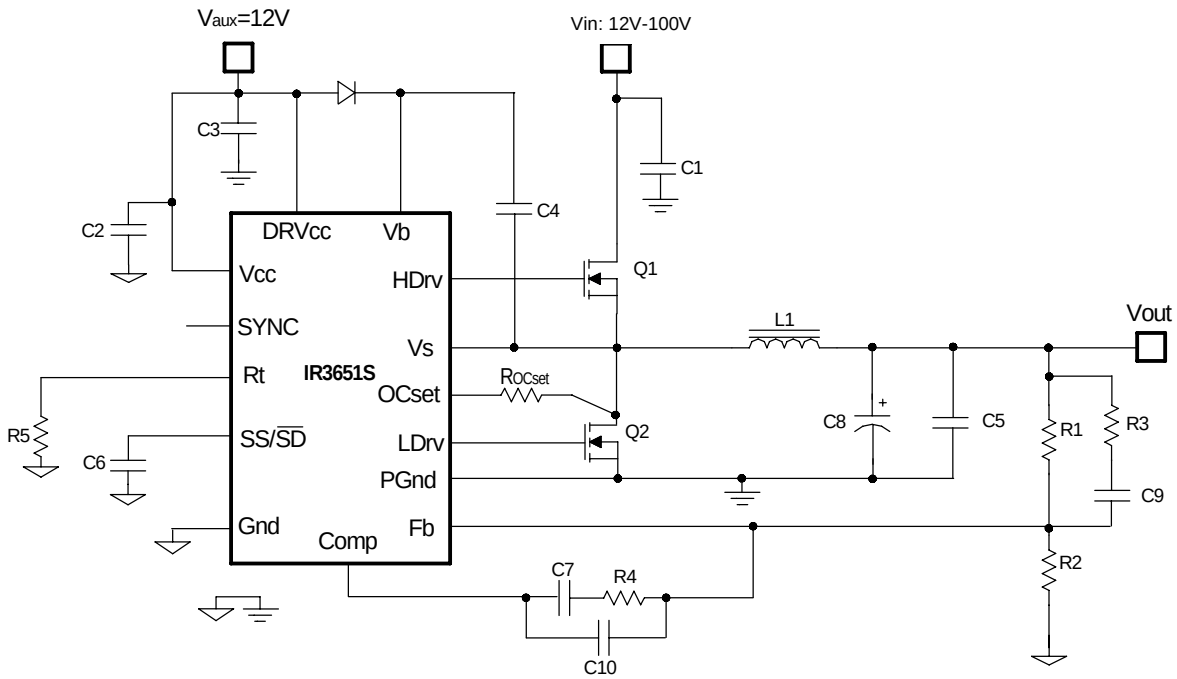
- High Voltage Operating up to 100V
- Programmable Switching Frequency up to 400kHz
- 1A Output Drive Capability
- Precision Reference Voltage (1.25V)
- Programmable Soft-Start
- Programmable Over Current Protection
- Hiccup Current Limit Using MOSFET $R_{DS(on)}$ sensing
- External Frequency Synchronization
- 14-pin SOIC Package

Applications

- 48V non-isolated DC to DC Converter
- Embedded Telecom Systems
- Networking and Computing Voltage Regulator
- Distributed Point of Load Power Architectures
- General high voltage DC/DC Converters

Description

The IR3651 is a high voltage PWM controller designed for high performance synchronous Buck DC/DC applications. The IR3651 drives a pair of external N-MOSFETs using a programmable switching frequency up to 400kHz allows flexibility to tune the operation of the IC to meet system level requirements, and synchronization allows the simplification of system level filter design. The output voltage can be precisely regulated using the internal 1.25V reference voltage for low voltage applications. Protection such as under voltage lockout and hiccup current limit are provided to give required system level security in the event of fault conditions.



Typical application Circuit

ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T&R ORIANTAION
S	IR3651SPBF	14	55	-------	Fig A
S	IR3651STRPBF	14	--------	2500	

ABSOLUTE MAXIMUM RATINGS

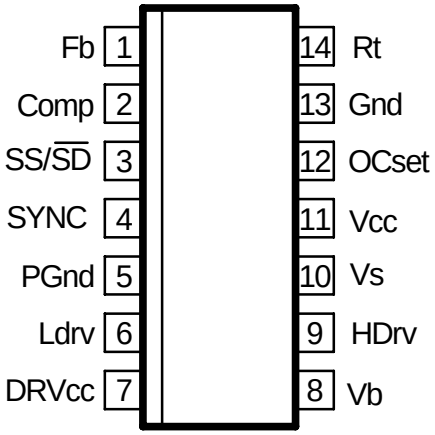
(Voltages referenced to GND)

- Vcc, DRVcc Supply Voltage ..... -0.3V to 20V
- Vs Supply Voltage ..... -0.3V to 150V
- Vb Supply Voltage ..... -0.3V to Vs+20V
- OCset 10mA
- Storage Temperature Range ..... -65°C To 150°C
- Operating Junction Temperature Range ..... -40°C To 150°C
- ESD Classification ..... JEDEC, JESD22-A114 (1K)
- Moisture Sensitivity Level ..... JEDEC Level 2 @ 260°C

***CAUTION:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.*

Package Information

14-Pin SOIC NB (S)



Θ_{JA} = 88.2° C/W
Θ_{JC} = 37° C/W

Block Diagram

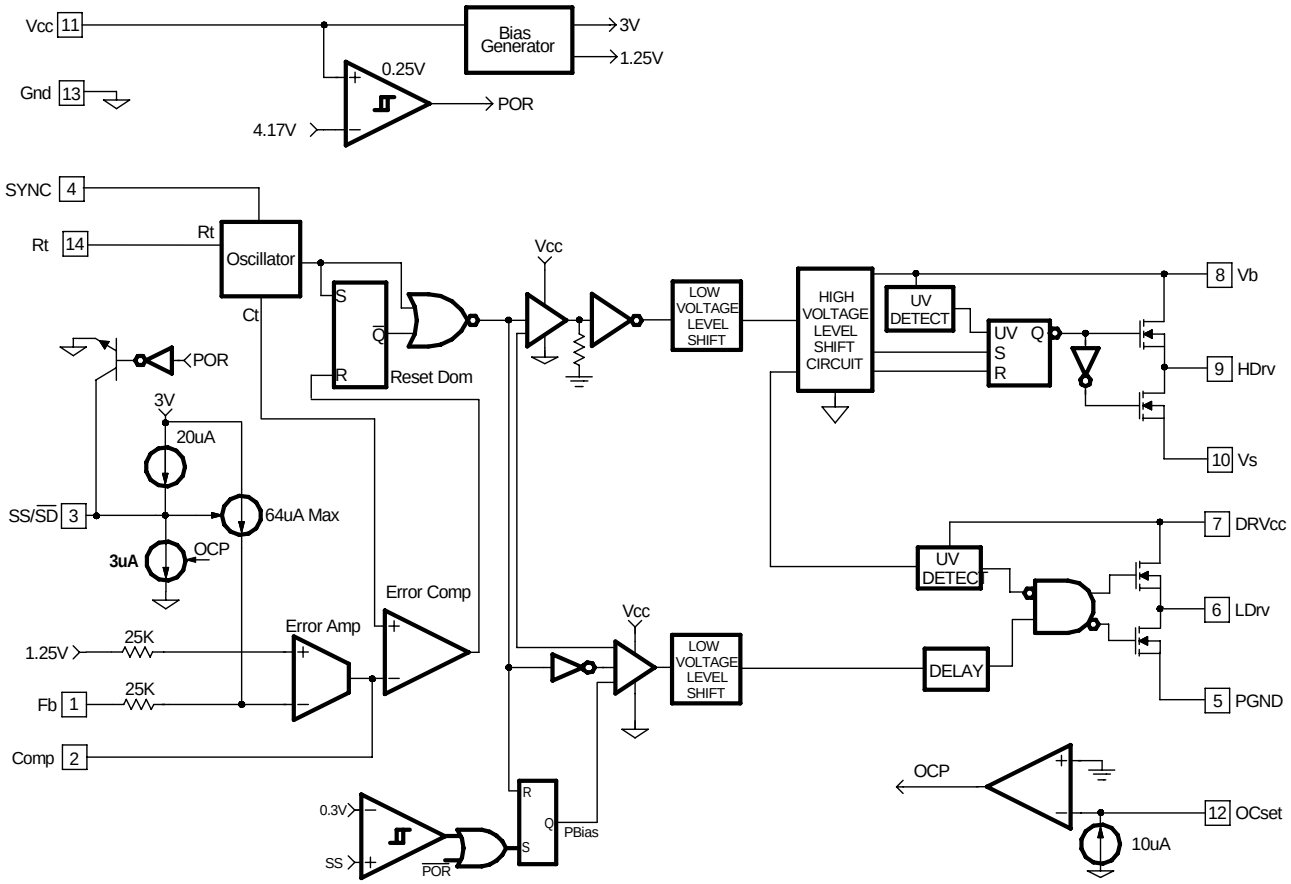


Fig. 1: Simplified block diagram of the IR3651

Pin Description

Pin	Name	Description
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
3	SS/SD	Soft start / shutdown. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to ground to set the start up time of the output voltage. The converter can be shutdown by pulling this pin below 0.3V.
4	SYNC	The internal oscillator can be synchronized to an external clock via this pin.
5	PGnd	Power Ground. This pin serves as a separate ground for the MOSFET driver and should be connected to the system's power ground plane.
6	LDrv	Output driver for low side MOSFET.
7	DRVcc	This pin provides biasing for the internal low side driver. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to power ground.
8	Vb	This pin powers the high side driver and must be connected to a voltage higher than bus voltage. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to switch node.
9	HDrv	Output driver for high side MOSFET
10	Vs	Switch node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is return path for the upper gate driver.
11	Vcc	This pin provides power for the internal blocks of the IC. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to ground.
12	OCSet	Current limit set point. A resistor from this pin to drain of low side MOSFET will set the current limit threshold.
13	Gnd	Signal ground for internal reference and control circuitry.
14	Rt	Connecting a resistor from this pin to ground sets the oscillator frequency.

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{bus}	Converting Voltage	12	100	V
V_{cc}	Supply Voltage	4.5	13.2	V
DRV_{cc}	Supply Voltage	10	16	V
V_b to V_s	Supply Voltage	10	16	V
F_s	Operating Frequency	100	400	kHz
T_j	Junction Temperature	-40	125	^oC

Electrical Specifications

Unless otherwise specified, these specifications apply over V_{cc}=5V; DRV_{cc}=Vb=12V, 0ºC<T_j< 125ºC

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Feedback Voltage	V_{FB}			1.25		V
Accuracy		$0^oC<Tj<125^oC$	-1.5		+1.5	%
		$-40^oC<Tj<125^oC$, *Note1*	-3		+1.5	%
Fb Voltage Line Regulation	LREG	5V<Vcc<12V			2.0	mV
Supply Current						
V_{CC} Supply Current (Stat)	$I_{CC(Static)}$	SS=0V, No Switching		6	7	mA
V_{CC} Supply Current (Dyn)	$I_{CC(Dynamic)}$	F_s=200kHz, C_{LOAD}=1.5nF		6	7	mA
DRV_{cc} Supply Current (Stat)	$I_{C(Static)}$	SS=0V, No Switching		0.3	0.5	mA
DRV_{cc} Supply Current (Dyn)	$I_{C(Dynamic)}$	F_s=200kHz, C_{LOAD}=1.5nF		4	5	mA
Vb Supply Current (Stat)	$I_{b(Static)}$	SS=0V, No Switching		0.3	0.5	mA
Vb Supply Current (Dyn)	$I_{b(Dynamic)}$	F_s=200kHz, C_{LOAD}=1.5nF		4.5	5.5	mA
Under Voltage Lockout						
V_{CC}-Start-Threshold	V_{CC}_UVLO(R)	Supply ramping up	4.0	4.17	4.35	V
V_{CC}-Stop-Threshold	V_{CC}_UVLO(F)	Supply ramping down	3.75		4.1	V
V_{CC}-Hysteresis		Supply ramping up and down	0.15	0.25	0.3	V
DRV_{cc}-Start-Threshold	DR_{cc}_UVLO(R)	Supply ramping up	8.3	9	9.7	V
DRV_{cc}-Stop-Threshold	DRV_{cc}_UVLO(F)	Supply ramping down	7.5	8.2	8.9	V
DRV_{Cc}-Hysteresis		Supply ramping up and down	0.6		0.9	V
V_b-Start-Threshold	V_b_UVLO(R)	Supply ramping up	8.3	9	9.7	V
V_b-Stop-Threshold	V_b_UVLO(F)	Supply ramping down	7.5	8.2	8.9	V
V_b-Hysteresis		Supply ramping up and down	0.6		0.9	V
Oscillator						
Frequency	F_S	Rt=120K Rt=51K	170 340	200 400	230 460	kHz
Ramp Amplitude	V_{ramp}	*Note2*		1.25		V
Min Duty Cycle	D_{min}	Fb=2V			0	%
Min Pulse Width	$D_{min(ctrl)}$	F_s=200kHz, *Note2*			200	ns
Max Duty Cycle	D_{max}	F_s=200kHz, Fb=1.2V F_s=400kHz, Fb=1.2V	80 70			%
Sync Frequency Range	Sync(Fs)	20% above free running freq			480	kHz
Sync Pulse Duratin	Sync(puls)		200			ns
Sync high Level Threshold	Sync(H)		2			V
Sync Low Level Threshold	Sync(L)				0.8	V

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Error Amplifier						
Input Bias Current	I_{FB}	SS=3V, Fb=1V		-0.1	-0.4	µA
Source/Sink Current	I(source/Sink)		50	85	120	µA
Transconductance	gm		1500	2400	3000	µmho
Soft Start/SD						
Soft Start Current	I_{SS}	SS=0V	15	20	25	µA
Shutdown Output Threshold	SD				0.25	V
Over Current Protection						
OCSET Current	I_{OCSET}		7.5	10	12.5	µA
Hiccup Current	I_{Hiccup}	*Note2*		3		µA
Hiccup Duty Cycle	Hiccup(duty)	I_{Hiccup} / I_{SS} , *Note2*			5	%
Output Drivers						
LO, Drive Rise Time	Tr(Lo)	CL=1.5nF See Fig 2, *Note2*		10	20	ns
HI Drive Rise Time	Tr(Hi)	CL=1.5nF, See Fig 2, *Note2*		10	20	ns
LO Drive Fall Time	Tf(Lo)	CL=1.5nF See Fig 2,*Note2*		10	20	ns
HI Drive Fall Time	Tf(Hi)	CL=1.5nF, See Fig 2,*Note2*		10	20	ns
Dead Band Time	Tdead	See Fig 2	30	45	100	ns
Upper Driver Source Current	$I_{upper(source)}$	HDrv short circuit pulsed current. PW<10us		1.0		A
Upper Driver Sink Curret	$I_{upper(sink)}$	HDrv short circuit pulsed current. PW<10us		1.0		A
Lower Driver Source Current	$I_{lower(source)}$	LDrv short circuit pulsed current. PW<10us		1.0		A
Lower Driver Sink Current	$I_{lower(sink)}$	LDrv short circuit pulsed current. PW<10us		1.0		A

Note1: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

Note2: Guaranteed by Design but not tested in production.

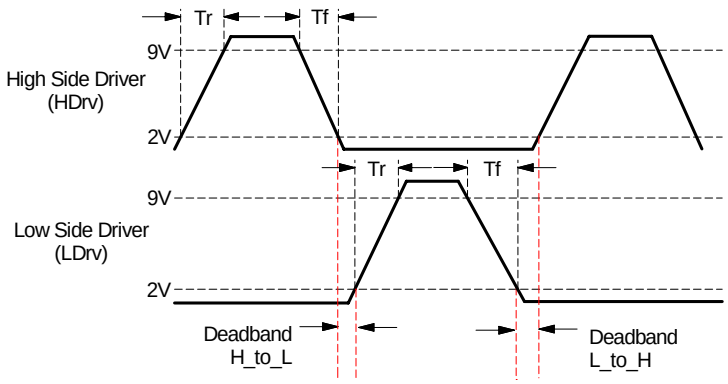
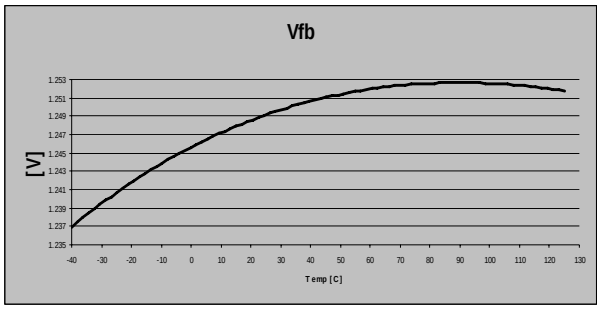
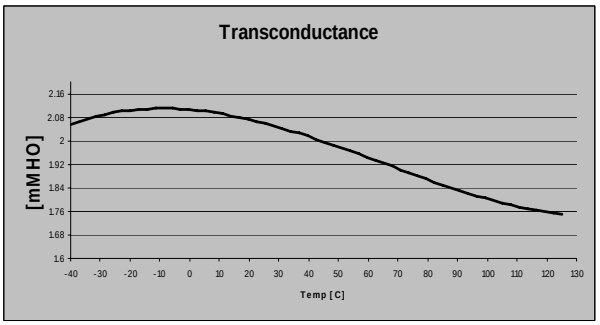
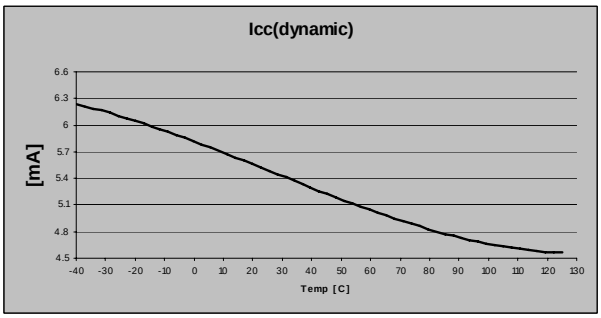


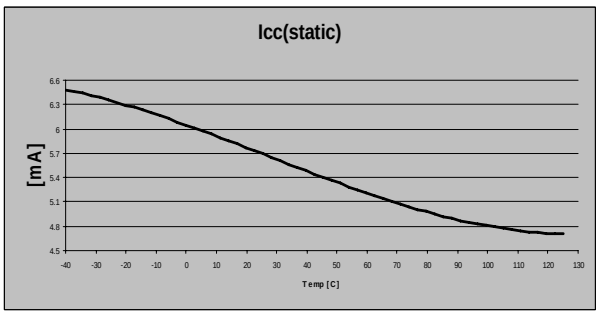
Fig. 2: Definition of Rise/Fall time and Deadband Time

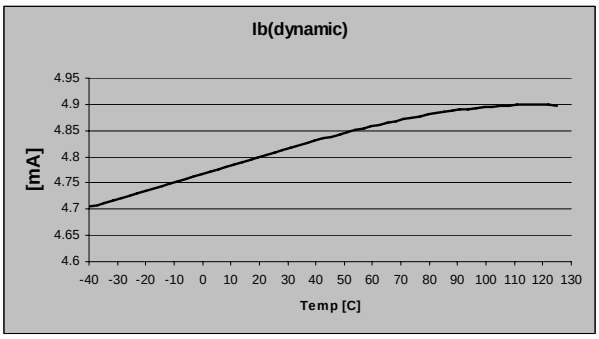
TYPICAL OPERATING CHRACTERISTICS (-40ºC TO +125ºC)

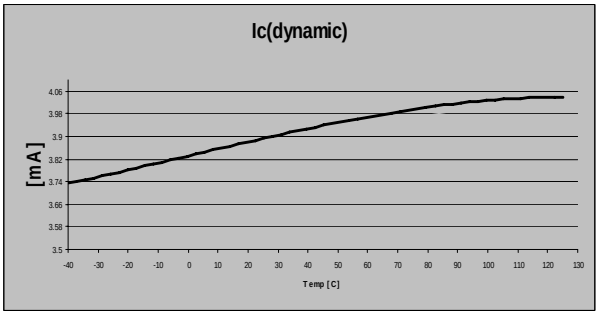


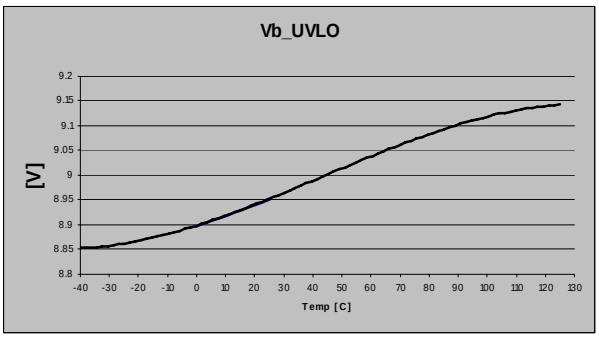


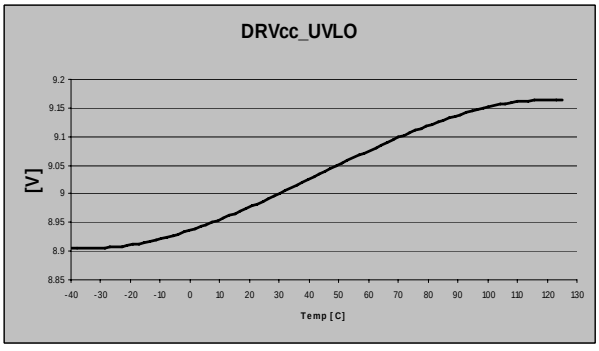












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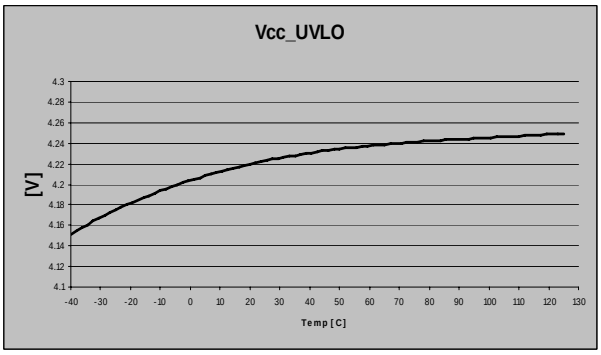
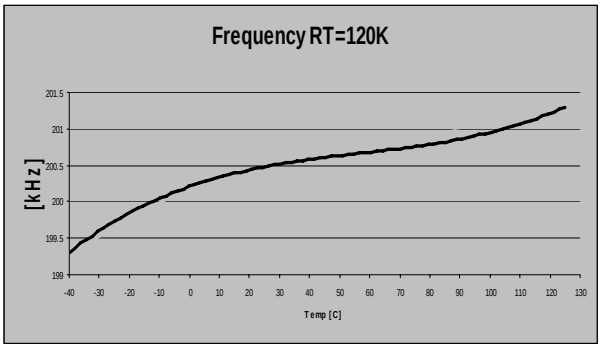
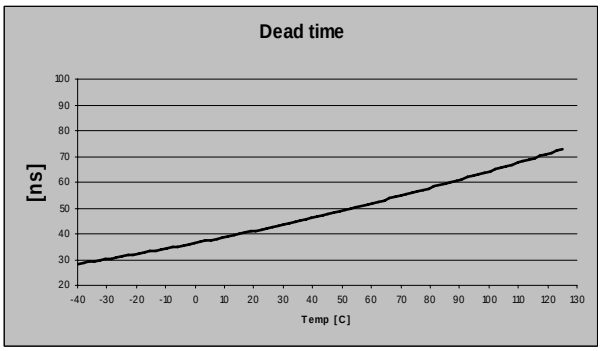
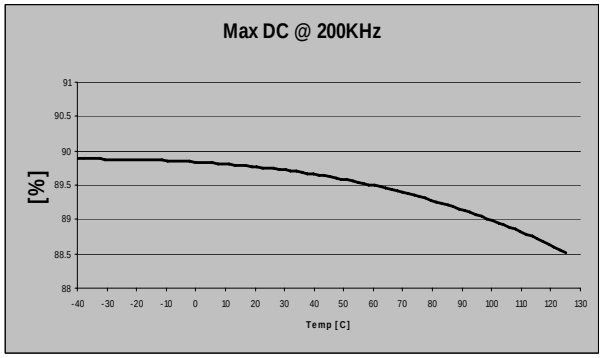
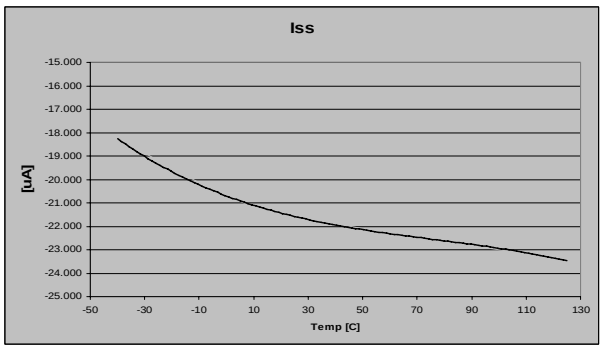
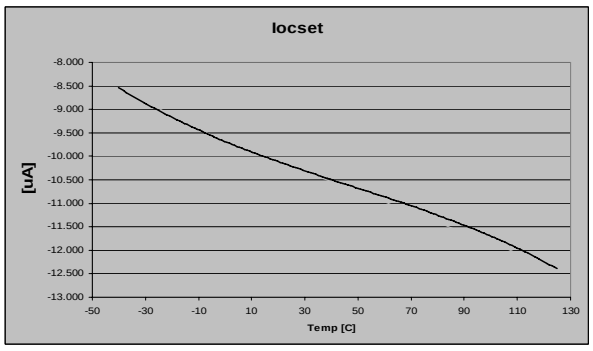












Circuit Description

THEORY OF OPERATION

Introduction

The IR3651 is a voltage mode PWM synchronous controller. The output voltage is set by feedback pin (Fb) and the internal reference voltage (1.25V). These are two inputs to error amplifier. The error signal between these two inputs is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle (D) which drivers N-channel external MOSFETs.

The timing of the IC is controlled by an internal oscillator circuit that can be externally programmed up to 400kHz.

The IR3651 operates with a wide input voltage from 12V to 100V allowing an extended operating input voltage range.

The current limit is programmable and uses on-resistance of the low-side MOSFET, eliminating the need for an external current sense resistor.

Under-Voltage Lockout

The under-voltage lockout circuit monitors the Vcc supply and assures that the IC doesn't starts until the Vcc reaches the set threshold. Lockout occurs if Vcc falls below 4.1V. Normal operation resumes once Vcc rises above the set value.

Shutdown

The output can be shutdown by pulling the soft-start pin below 0.3V. This can be easily done by using an external small signal transistor. During shutdown both MOSFET drivers will be turned off. Normal operation will resume by cycling soft start pin.

Error Amplifier

The IR3651 is a voltage mode controller. The error amplifier is of transconductance type. The amplifier is capable of operating with Type III compensation control scheme using low ESR output capacitance.

Operating Frequency Selection

The switching frequency is determined by connecting an external resistor (Rt) to ground. Figure 3 provides a graph of oscillator frequency versus Rt.

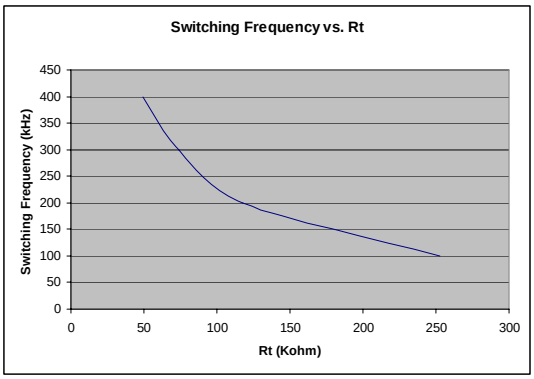


Fig. 3: Switching Frequency vs. Rt

Frequency Synchronization

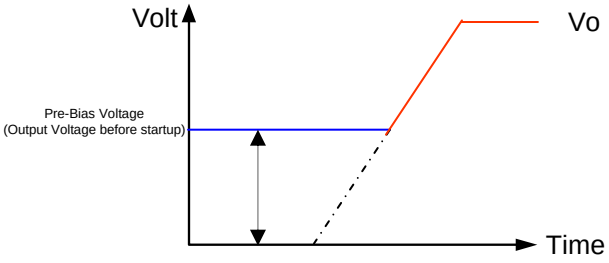
The IR3651 is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge at an external clock. Switching frequency is set by external resistor (Rt). During synchronization, Rt is selected such that the free running frequency is 20% below the synchronization frequency. When unused, the sync pin will remain floating and is noise immune.

Pre-Bias Startup

IR3651 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Below figure shows a typical Pre-Bias condition at start up.

Depends on system configuration, specific amount of output capacitors may be required to prevent discharging the output voltage



Soft-Start

The IR3651 has programmable soft-start to control the output voltage rise and limit the inrush current during start-up.

To ensure correct start-up, the soft-start sequence initiates when Vcc rises above its threshold and generate the Power On Ready (POR) signal. The soft-start function operates by sourcing current to charge an external capacitor to about 3V.

Initially, the soft-start function clamps the output of error amplifier by injecting a current (64uA) into the Fb pin and generates a voltage about 1.6V (64ux25K) across the negative input of error amplifier (see figure 4).

The magnitude of the injected current is inversely proportional to the voltage at the soft-start pin. As the soft-start voltage ramps up, the injected current decreases linearly and so does the voltage at negative input of error amplifier.

When the soft-start capacitor is around 1V, the voltage at the positive input of the error amplifier is approximately 1.25V.

The output of error amplifier will start increasing and generating the first PWM signal. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing.

The feedback voltage increases linearly as the soft start voltage ramps up. When soft-start voltage is around 2V the output voltage is reached the steady state and the injected current is zero.

Figure 5 shows the theoretical operational waveforms during soft-start.

The output voltage start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V.

The start-up time will be dependent on the size of the external soft-start capacitor and can be estimate by:

$$20\mu A * \frac{T_{start}}{C_{ss}} = 2V - 1V$$

For a given start-up time, the soft-start capacitor (nF) can be estimated as:

$$C_{SS} \cong 20\mu A * T_{start}(ms) \quad \text{--(1)}$$

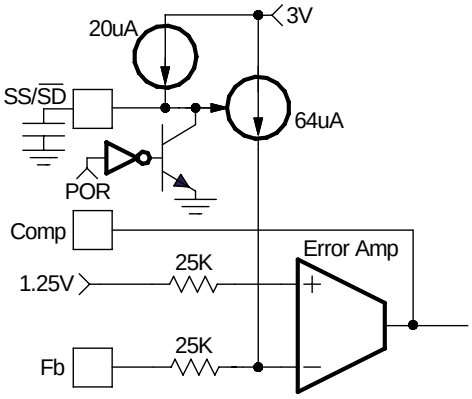


Fig. 4: Soft-Start circuit for IR3651

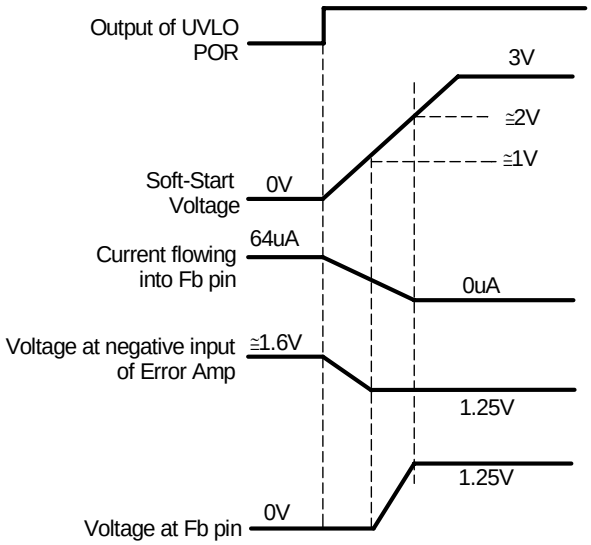


Fig. 5: Theoretical operation waveforms during soft-start

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduce cost by eliminating a current sense resistor. As shown in figure 6, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) which sets the current limit set point.

The internal current source develops a voltage across R_{SET}. When the low side MOSFET is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \qquad --(2)$$

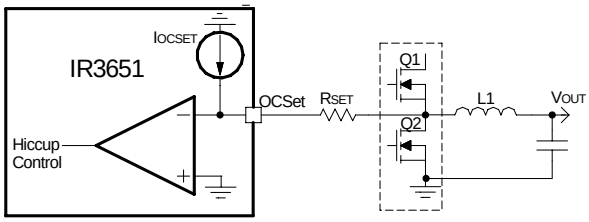


Fig. 6: Connection of over current sensing resistor

The critical inductor current can be calculated by setting:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) = 0$$

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \qquad --(3)$$

$$I_{SET} = I_{L(critical)} = 1.5 * I_o + \frac{\Delta i_L}{2}$$

An over current is detected if the OCSet pin goes below ground. This trips the OCP comparator and cycles the soft start function in hiccup mode.

The hiccup is performed by charging and discharging the soft-start capacitor in certain slope rate. As shown in figure 7 a 3uA current source is used to discharge the soft-start capacitor.

The OCP comparator resets after every soft start cycles, the converter stays in this mode until the overload or short circuit is removed. The converter will automatically recover.

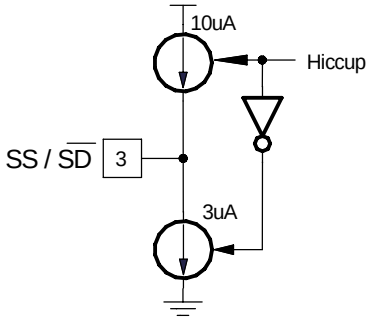


Fig. 7: 3uA current source for discharging soft-start capacitor during hiccup

The OCP circuit starts sampling current approximately 200ns before the low gate drive turns off. The OCSet pin is internally clamped to about 1.5V during deadtime to prevent false trigging, figure 8 shows the OCSet pin during one switching cycle.

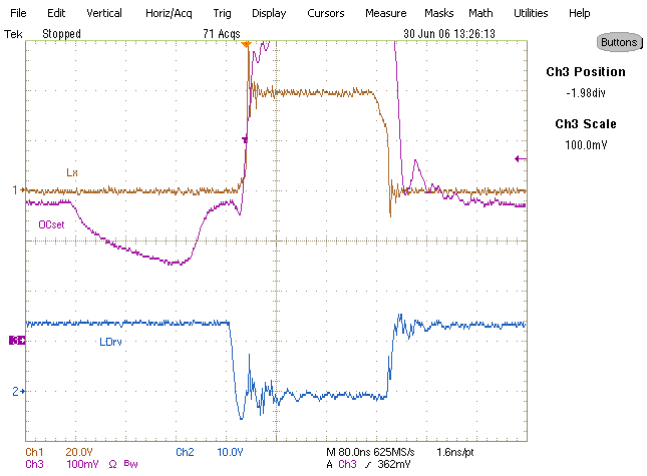


Fig. 8: OCset pin during normal condition
Ch1: Inductor point, Ch2:Ldrv, Ch3:OCSet

The value of R_{SET} should be checked in an actual circuit to ensure that the over current protection circuit activates as expected. The IR3651 current limit is designed primarily as disaster preventing, "no blow up" circuit, and doesn't operate as a precision current regulator.

Application Information

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

When an external resistor divider is connected to the output as shown in figure 9.

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad --(4)$$

Equation (4) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_O - V_{ref}}\right) \quad --(5)$$

For the calculated values of R_8 and R_9 see feedback compensation section.

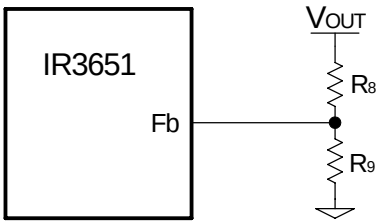


Fig. 9: Typical application of the IR3651 for programming the output voltage

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 20\mu A * T_{start} \quad --(1)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 5ms, the soft-start capacitor will be 0.1uF. Choose a ceramic capacitor at 0.1uF.

Input Capacitor Selection

The input filter capacitor should be selected based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{--(7)} \qquad D = \frac{V_o}{V_{in}}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For applications with input supplies above 30V, choice of input capacitor type is limited to ceramics or aluminum electrolytics. Ceramic capacitors offer high peak current capabilities, they also feature low ESR and ESL at higher frequency which enhance better efficiency, however high voltage ceramic capacitors are available with only in low value capacitance. A combination of ceramic capacitors and electrolytic capacitors are recommended.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t}; \quad \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{--(8)}$$

Where:

V_{in} = Maximum input voltage

V_o = Output Voltage

Δi = Inductor ripple current

F_s = Switching frequency

Δt = Turn on time

D = Duty cycle

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors types and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components, these components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \quad \text{--(9)}$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = Output voltage ripple

ΔI_L = Inductor ripple current

Since the output capacitor has major role in overall performance of converter and determines the result of transient response, selection of capacitor is critical. The IR3651 can perform well with all types of capacitors.

As a rule the capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements.

The goal for this design is to meet the voltage ripple requirement in smallest possible capacitor size. Therefore ceramic capacitor is selected due to low ESR and small size.

In the case of tantalum or low ESR electrolytic capacitors, the ESR dominates the output voltage ripple, equation (9) can be used to calculate the required ESR for the specific voltage ripple.

Power MOSFET Selection

The IR3651 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{gs}), maximum output current, On-resistance $R_{DS(on)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{in}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{gs} to prevent undesired turn-on of the complementary MOSFET, which results in shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{cond} = (upper switch) = I_{load}^2 * R_{ds(on)} * D * \vartheta$$

$$P_{cond} = (lower switch) = I_{load}^2 * R_{ds(on)} * (1-D) * \vartheta$$

$$\vartheta = R_{ds(on)}\ temperature\ \ dependency$$

The $R_{DS(on)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turn-off delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{sw} = \frac{V_{ds(off)}}{2} * \frac{t_r + t_f}{T} * I_{load} \quad --(10)$$

Where:

$V_{ds(off)}$ = Drain to source voltage at the off time

t_r = Rise time

t_f = Fall time

T = Switching period

I_{load} = Load current

The switching time waveforms is shown in figure10.

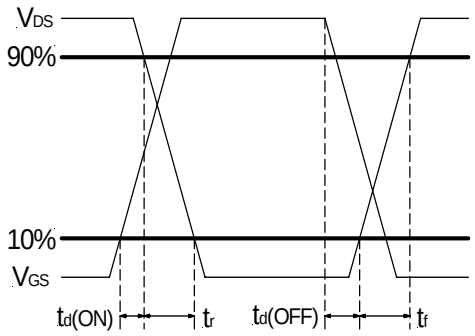


Fig. 10: switching time waveforms

Feedback Compensation

The IR3651 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 11). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2 * \pi \sqrt{L_o * C_o}} \quad \text{--(11)}$$

Figure 11 shows gain and phase of the LC filter. Since we already have 180º phase shift just from the output filter, the system risks being unstable.

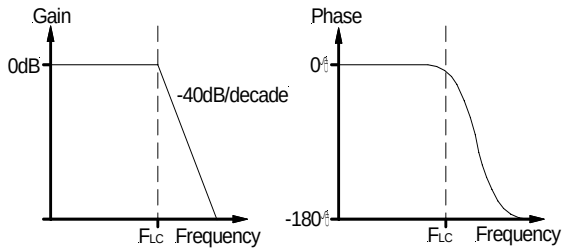


Fig. 11: Gain and Phase of LC filter

The IR3651's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The error amplifier can be compensated either in typeII or typeIII compensation. When it is used in typeII compensation the transconductance properties of the error amplifier become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in figure 12.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2 * \pi * ESR * C_o} \quad \text{--(12)}$$

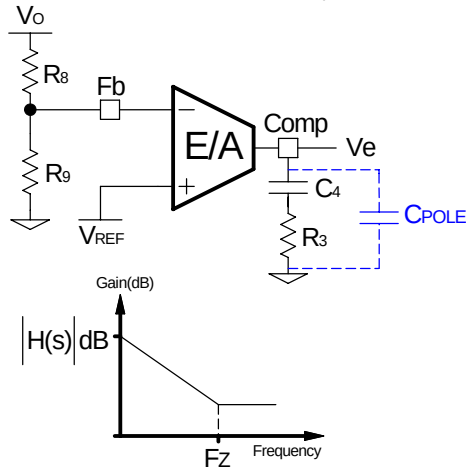


Fig. 12: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = \left(g_m * \frac{R_9}{R_9 + R_8} \right) * \frac{1 + sR_3C_4}{sC_4} \quad \text{--(13)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_9}{R_9 + R_8} \right) * R_3$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad \text{--(14)}$$

The gain is determined by the voltage divider and error amplifier's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \; and \; F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R4:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * (R_8 + R_9)}{V_{in} * F_{LC}^2 * R_9 * g_m} \quad \text{--(15)}$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 and R_9 = Feedback Resistor Dividers
g_m = Error Amplifier Transconductance

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad --(16)$$

Using equations (15) and (16) to calculate C_4.

One more capacitor is sometimes added in parallel with C_4 and R_3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s}$$

$$For\ F_P << \frac{F_s}{2}$$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network (typeIII). The typically used compensation network for voltage-mode controller is shown in figure 15.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m * Z_f >> 1 \ and \ \ g_m * Z_{in} >> 1 \quad --(17)$$

By replacing Z_{in} and Z_f according to figure 15, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_8(C_4 + C_3)} * \frac{(1 + sR_3C_4) * [1 + sC_7(R_8 + R_{10})]}{\left[1 + sR_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)\right] * (1 + sR_{10}C_7)}$$

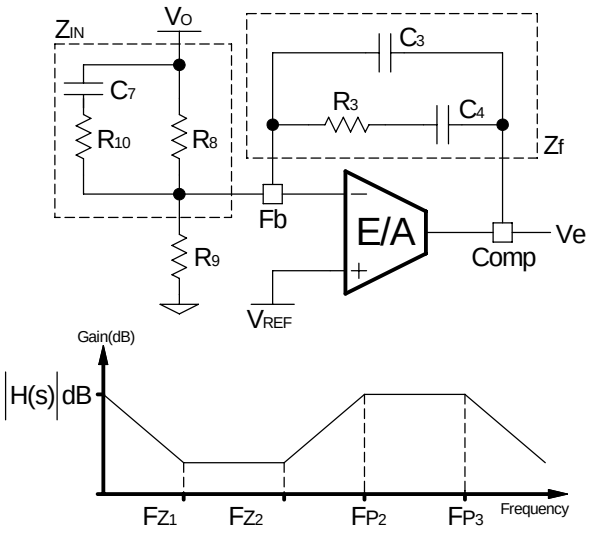


Fig.15: Compensation network with local feedback and its asymptotic gain plot

As known, transconductance amplifier has high impedance (current source) output, therefore, consideration should be taken when loading the error amplifier output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7}$$

$$F_{P3} = \frac{1}{2\pi * R_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)} \cong \frac{1}{2\pi * R_3 * C_3}$$

$$F_{z1} = \frac{1}{2\pi * R_3 * C_4}$$

$$F_{z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8}$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
TypII(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
TypeIII(PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
TypeIII(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from IR Web-Site.

For $F_{LC}<F_o<F_{s/2}<F_{ESR}$

typeIII method B is selected to place the pole and zeros.

$$F_o < F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

$$F_{Z2} = F_o * \sqrt{\frac{1-Sin\Theta}{1+Sin\Theta}}$$

$$F_{P2} = F_o * \sqrt{\frac{1+Sin\Theta}{1-Sin\Theta}}$$

Select: $F_{Z1} = 0.5 * F_{Z2}$ and $F_{P3} = 0.5 * F_s$

$$R_3 \ge \frac{2}{g_m};$$

The following design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient response. The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45º for overall stability.

Desired Phase Margin: $\Theta_{max} = \frac{\pi}{3}$

Calculate C_4, C_3 *and* C_7 *:*

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3};$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3};$$

$$C_7 = \frac{2\pi * F_o * L_o * C_o * V_{osc.}}{R_3 * V_{in}};$$

Calculate R_{10}, R_8 *and* R_9 :

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}};$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10};$$

$$R_9 = \frac{V_{ref}}{V_o - V_{ref}} * R_8;$$

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (3).

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worse case operation. This resistor must be placed close to the IC, place a small ceramic capacitor from this pin to ground for noise rejection purposes.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad \text{--(3)}$$

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas.

The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units

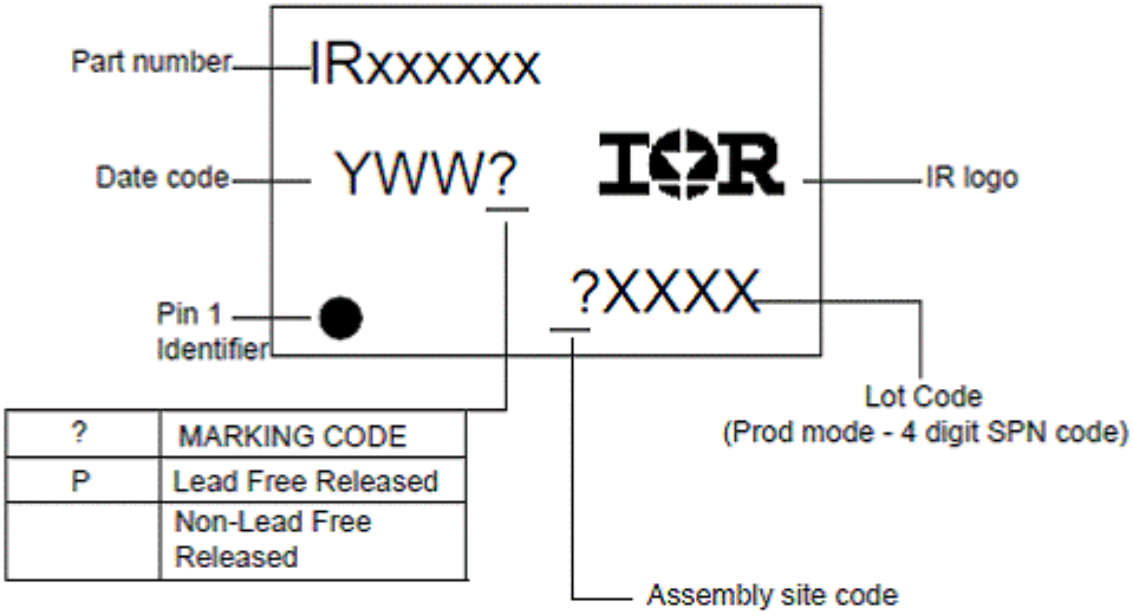
.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vcc, DRVc and Vb should be close to respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

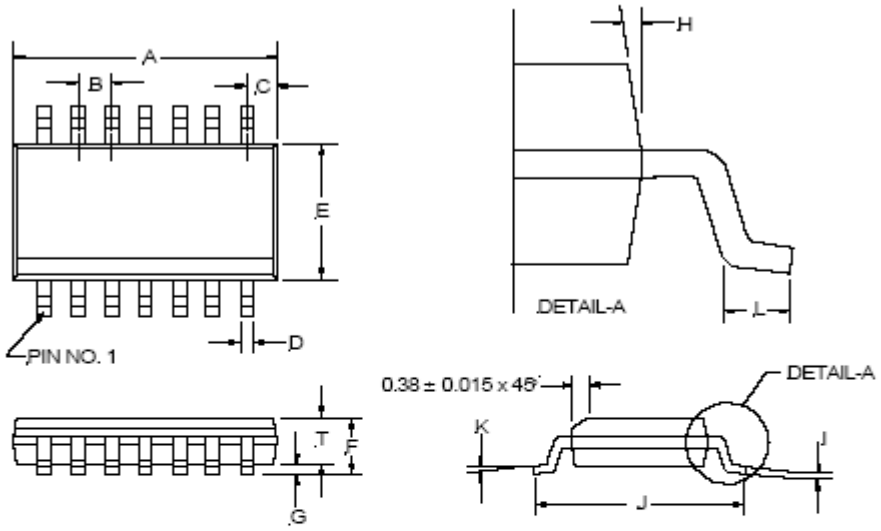
In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

(S) SOIC Package
14-Pin Surface Mount, Narrow Body



14-PIN		
SYMBOL	MIN	MAX
A	8.56	8.74
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

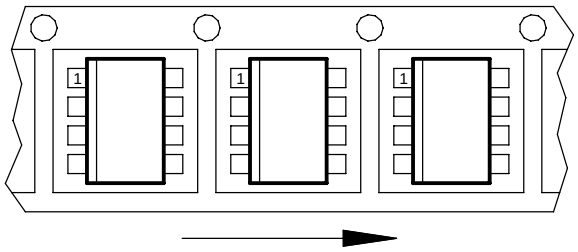


Figure A

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