IR38164 OptiMOS™ iPOL

30A Single-voltage Synchronous Buck Regulator with SVID

Features

- Internal LDO allows single 16 V operation
- Output Voltage Range: 0.5 V to 0.875*PVin
- 0.5% accurate Reference Voltage
- Intel VR12.5 (Rev 1.5), SVID (Rev 1.7) and VR13 (Rev 1.1) compliant
- Enhanced line/load regulation with Feedforward
- Frequency programmable by PMBus™ up to 1.5 MHz
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- Fast mode I2C and 400 kHz PMBus™ interface for programming, sequencing and margining output voltage, and for monitoring input voltage, output voltage, output current and temperature.
- PMBus™ configurable fault thresholds for input UVLO, output OVP, OCP and thermal shutdown.
- Thermally compensated pulse-by-pulse current limit and Hiccup Mode Over Current Protection
- Dedicated output voltage sensing for power good indication and over-voltage protection which remains active even when Enable is low.
- Enhanced Pre-Bias Start up
- Integrated MOSFET drivers and Bootstrap diode
- Operating junction temp: -40 °C<Tj<125°C
- Thermal Shut Down
- PMBus™ Programmable Power Good Output
- Small Size 5 mmx 7 mm PQFN
- Pb-Free (RoHS Compliant)
- External resistor allows setting up to 16 PMBus™ addresses

Applications

- Designed for Intel® single phase power rails requiring SVID communication such as VCCIO and VCMP on platforms such as VR13HC, VR13 and VR12.5.
- Servers and High End Desktop CPU VRs for non-core applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The IR38164 OptiMOS™ IPOL is an easy to use, fully integrated and highly efficient dc-dc regulator with Intel SVID and I2C/PMBus™ interfaces. The on-chip PWM controller and co-packaged low duty cycle optimized MOSFETs make the device a space-efficient solution, providing accurate power delivery for low output voltage and high current applications that require an Intel SVID interface.
The IR38164 offers programmability of switching frequency, output voltage, and fault/warning thresholds and fault responses while operating over a wide input range. Providing flexibility as well as system level security in the event of fault conditions.
The switching frequency is programmable from 500 kHz to 1.5 MHz for an optimum solution.
The on-chip sensors and ADC along with the SVID, I2C and PMBus™ make it easy to monitor and report input voltage, output voltage, output current and temperature.

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1 Ordering information

Table 1 Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
IR38164	QFN 5 mm x 7 mm	Tape and Reel	4000	IR38164MTRPbF

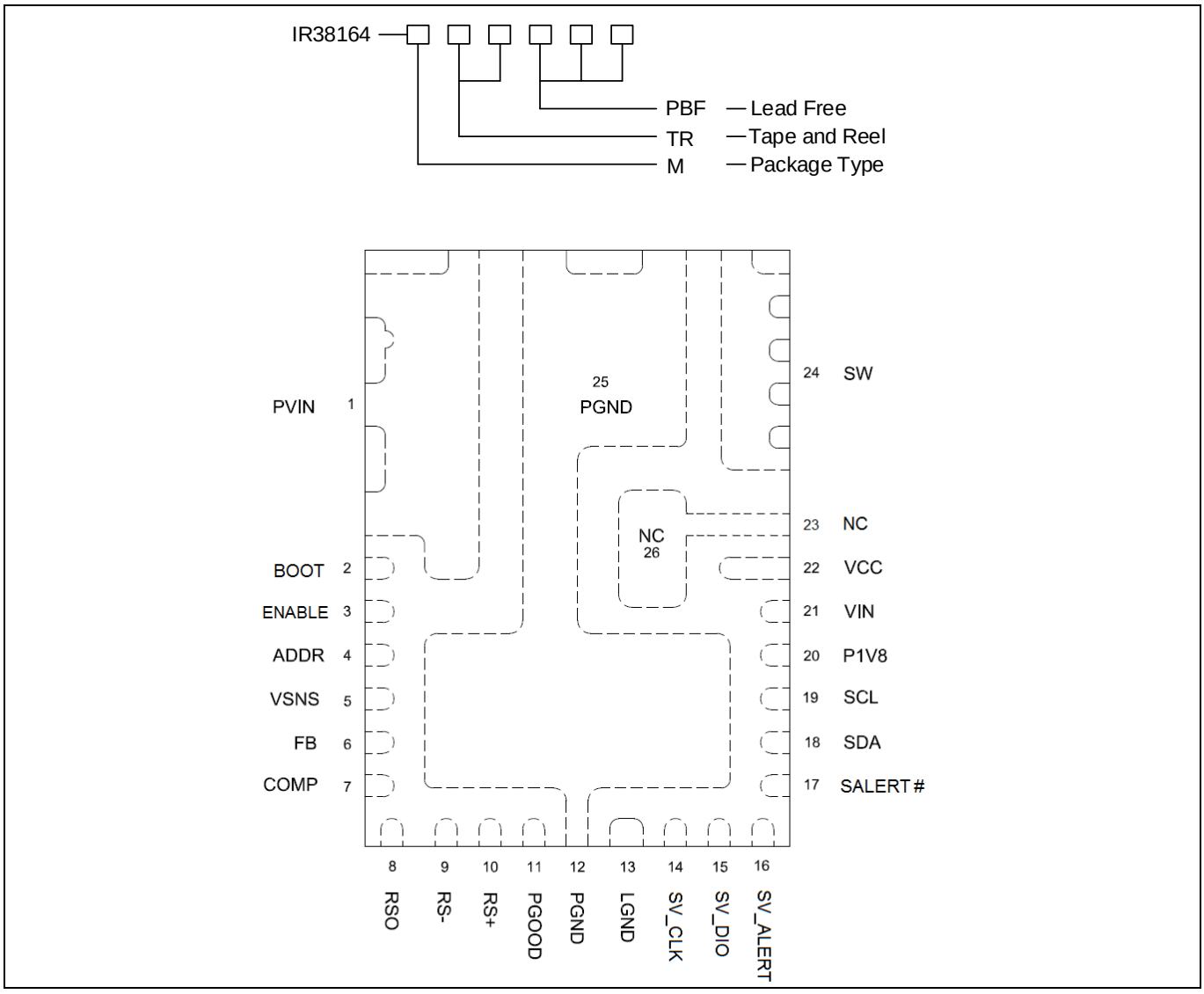


Figure 1 Package Top View

2 Functional block diagram

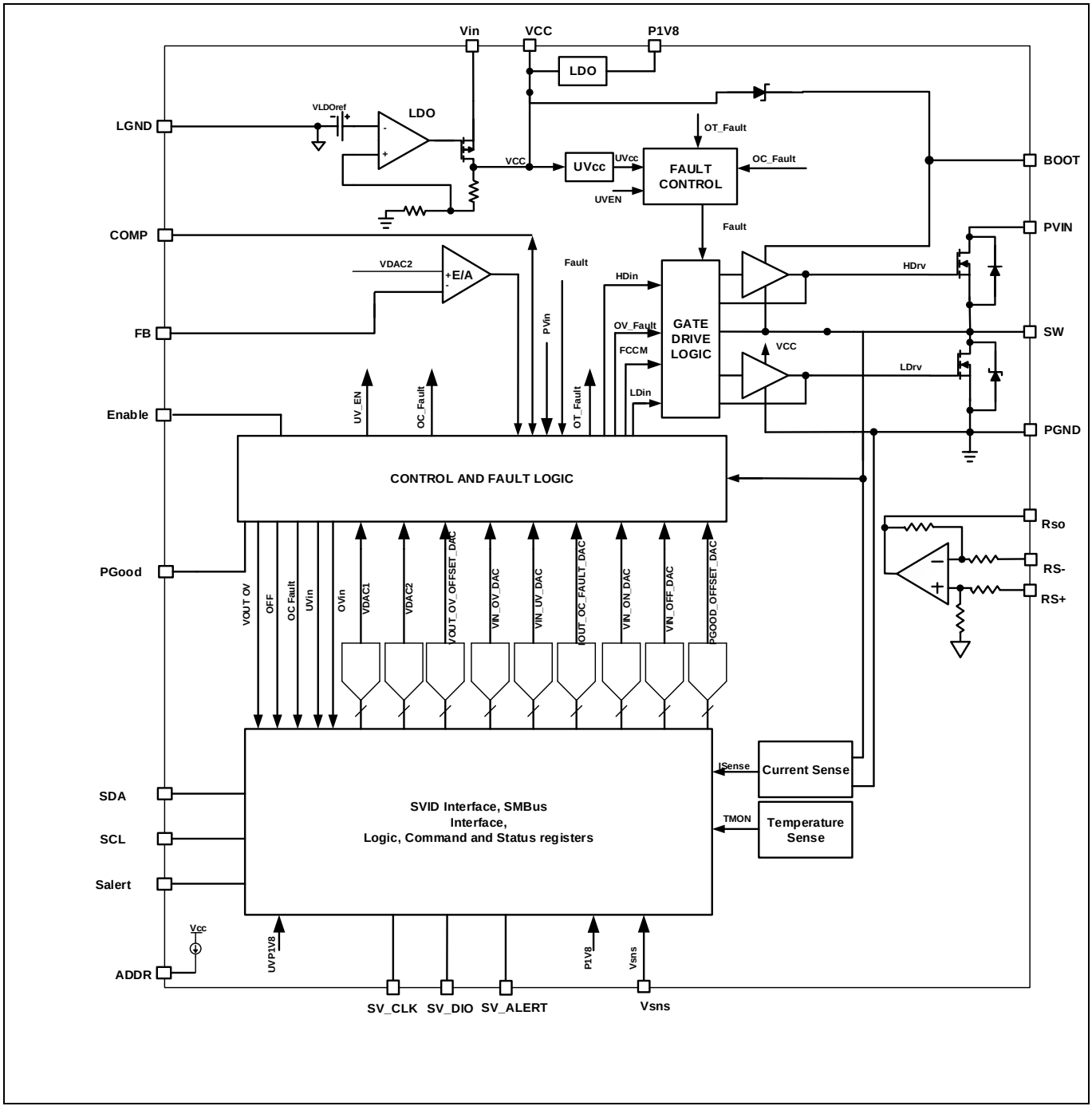


Figure 2 Block diagram

3 Typical application diagram

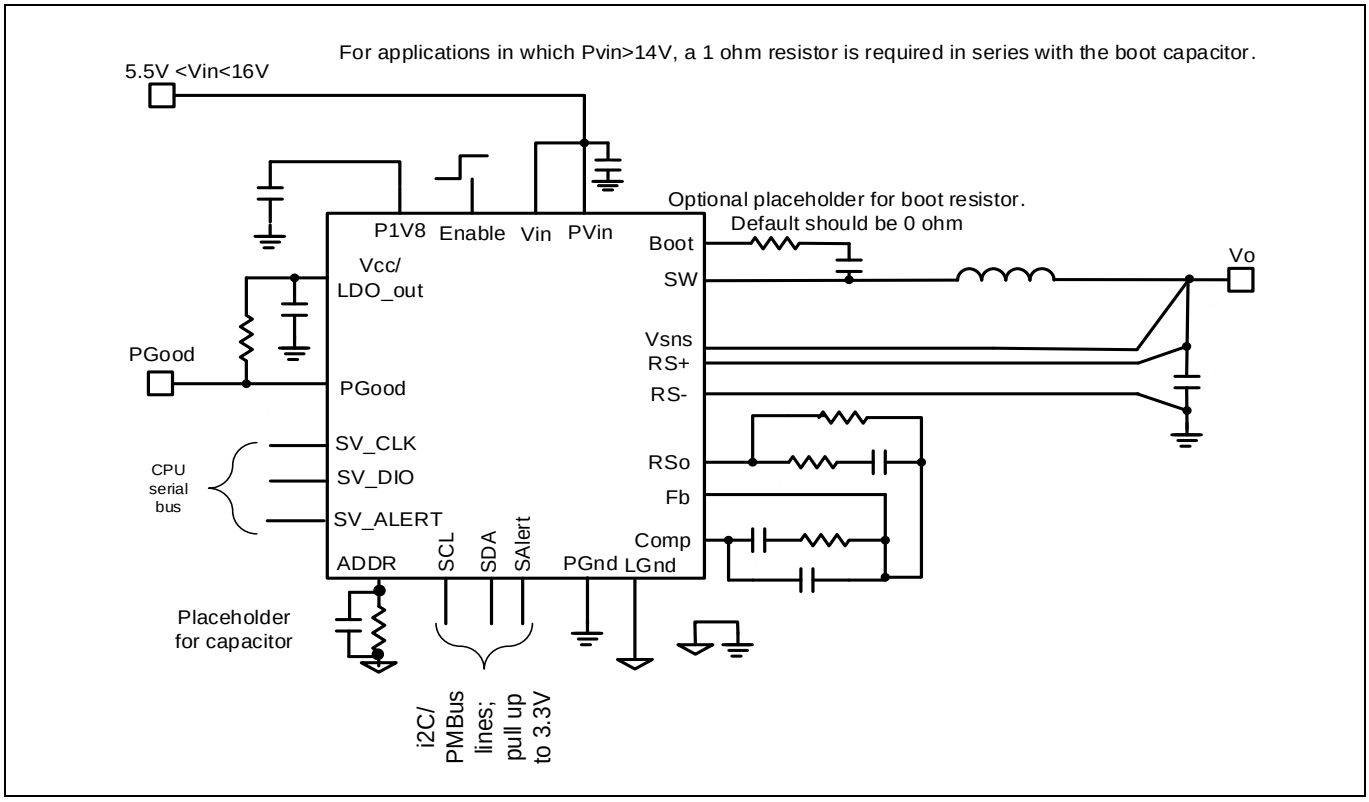


Figure 3 IR38164 basic application circuit

4 Pin descriptions

Table 2 Pin descriptions

Pin#	Pin name	Pin description
1	PVIN	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND. Typical applications use four 22 µF input capacitors and a low ESR, low ESL 0.1 µF decoupling capacitor in a 0603/0402 case size. A 3.3 nF capacitor may also be used in parallel with these input capacitors to reduce ringing on the SW node.
2	Boot	Supply voltage for high side driver. A 0.1 µF capacitor should be connected from this pin to the SW pin. It is recommended to provide a placement for a 0 ohm resistor in series with the capacitor. For applications in which PVin>14 V, a 1 ohm resistor is required in series with the boot capacitor.
3	ENABLE	Enable pin to turn the IC on and off.
4	ADDR	A resistor should be connected from this pin to LGnd to set the PMBus™ address offset for the device. It is recommended to provide a placement for a 10 nF capacitor in parallel with the offset resistor.
5	Vsns	Sense pin for OVP and PGood. Typically connected to a local Vout capacitor at the output of the inductor.
6	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
7	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
8	RSo	Remote Sense Amplifier Output. When the remote sense amplifier is used, this is connected to the feedback compensation network
9	RS-	Remote Sense Amplifier input. Connect to ground at the load.
10	RS+	Remote Sense Amplifier input. Connect to output at the load.
11	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC. If the power good voltage needs to be limited to < 500 mV prior power supply ramps above the VCC UVLO, use a 49.9 kΩ pullup. After VCC UVLO a 4.99 kΩ pullup will suffice.
12,25	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to PVIN pin (pin 1) and this pin.
13	LGND	Signal ground for internal reference and control circuitry. This should be connected to the PGnd plane at a quiet location using a single point connection.
14	SV_CLK	SVID CLK line. This is pulled up to VDDIO/VCCIO voltage. It is recommended to provide a placement for a 0603 resistor between the pin and the pullup resistor.
15	SV_DIO	SVID Data line. This is pulled up to VDDIO/VCCIO voltage. It is recommended to provide a placement for a 0603 resistor between the pin and the pullup resistor.
16	SV_ALERT	SVID Alert line. This is pulled up to VDDIO/VCCIO voltage through a resistor.
17	SAlert#	SMBus Alert line; open drain SMBALERT# pin. This should be pulled up to 3.3 V-5 V with a 1 kΩ - 5 kΩ resistor.
18	SDA	SMBus data serial input/output line. This should be pulled up to 3.3 V-5 V with a 1 kΩ - 5 kΩ resistor.
19	SCL	SMBus clock line. This should be pulled up to 3.3 V-5 V with a 1 kΩ - 5 kΩ resistor.

Pin descriptions

Pin#	Pin name	Pin description
20	P1V8	This is the supply for the digital circuits; bypass with a 10 µF capacitor to PGnd.
21	Vin	Input Voltage for LDO. A 1 µF capacitor is placed from this pin to PGnd. If the internal bias LDO is used, tie this pin to PVin. If an external bias voltage (typically 5 V) is available for Vcc, tie the Vin pin to Vcc.
22	VCC	Bias Voltage for IC and driver section, output of LDO. Add 10 µF bypass cap from this pin to PGnd.
23,26	NC	Do not connect to this pin.
24	SW	Switch node. This pin is connected to the output inductor.

5 Absolute maximum ratings

Table 3 Absolute maximum ratings

PVin, Vin	-0.3 V to 25 V
Vcc/LDO_Out	-0.3 V to 6 V
P1V8	-0.3 V to 2 V
SW	-0.3 V to 25 V (dc), -4 V to 25 V (ac, 100 ns)
Boot	-0.3 V to 31 V
Boot to SW	-0.3 V to 6 V (dc) (Note 1), -0.3 V to 6.5 V (ac, 100 ns)
PGood, other Input/Output Pins	-0.3 V to 6 V (Note 1)
PGnd to Gnd	-0.3 V to + 0.3 V
Thermal information	
Junction to ambient thermal resistance θ_{JA}	11.1 C/W (Note 2)
Junction to board thermal resistance θ_{JB}	4.16 C/W (Note 3)
Junction to case top thermal resistance $\theta_{JC(top)}$	18.9 C/W (Note 4)
Junction to case top thermal parameter $\Psi_{JT\ (top)}$	0.32 C/W (Note 2)
Storage Temperature Range	-55 °C to 150 °C
Junction Temperature Range	-40 °C to 150 °C

(Voltage referenced to GND unless otherwise specified)

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and not functional operation ratings of the device.***

Note: [1] Must not exceed 6 V

[2] Value obtained via thermal simulation under natural convection on an IR38164 demo board. 10 layer, 7" x 5.5"x0.072" PCB with 1.5 oz copper at the top and bottom layer. Inner layers 2, 3, 8 and 9 have 1 oz copper and layers 4,5,6,7 have 2 oz copper. T_a = 25 °C was used for the simulation.

[3] PCB from note 2 and package is considered in thermal simulation with Ta=25 °C. Pin 12 is considered.

[4] Only package is considered. Simulation is used with a cold plate that fixes top of package at Ta=25 °C.

6 Electrical specifications

Table 4 Recommended operating conditions for reliable operation with margin

Input Voltage Range, PVin (Note 4)	1.5 V to 16 V
Input Voltage Range, Vin	5.3 V to 16 V
Supply Voltage Range, Vcc	4.5 V to 5.5 V
Supply Voltage Range, Boot to SW	4.5 V to 5.5 V
Output Voltage Range	0.5 V to 0.875 x Vin
Output Current Range	0 to 30 A
Switching Frequency	500 kHz to 1500 kHz
Operating Junction Temperature	-40 °C to 125 °C

(Voltages referenced to GND unless otherwise specified)

Note: *[4] Maximum absolute SW node voltage should not exceed 25 V. A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage does not exceed 25 V.*

7 Electrical characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{DS(ON)\_Top}$	VBoot – Vsw= 5 V, I_O = 30 A, Tj =25 °C		2.2		mΩ
Bottom Switch	$R_{DS(ON)\_Bot}$	Vcc = 5 V, I_O = 30 A, Tj =25°C		0.78		
Bootstrap Diode Forward Voltage		I(Boot) = 40 mA	150	300	450	mV
SW Leakage Current	I_{SW}	SW = 0 V, Enable = 0 V			1	µA
	I_{SW_EN}	SW=0; Enable= 2 V		18		
Supply Voltage						
PVin range (using external Vcc=5 V)				1.5-16		V
Vin range (using internal LDO)		Fsw=600 kHz		5.3-16		V
		Fsw=1.5 MHz		5.5-16		
Vin range (when Vin=Vcc)			4.5	5.0	5.5	V
Supply Current						
Vin Supply Current (standby) (internal Vcc)	$I_{in(Standby)}$	Enable low, No Switching, Vin=16 V, low power mode enabled		2.7	4	mA
Vin Supply Current (dynamic) (internal Vcc)	$I_{in(Dyn)}$	Enable high, Fs = 600 kHz, Vin=16 V		39	50	mA
VCC Supply Current (Standby)(external Vcc)	$I_{cc(Standby)}$	Enable low, No Switching, Vcc=5.5 V, low power mode enabled		2.7	5	mA
VCC Supply Current (Dyn)(external Vcc)	$I_{cc(Dyn)}$	Enable high, Fs = 600 kHz, Vcc=5.5 V		39	50	mA
Internal Regulator VCC\LDO)						
Output Voltage	VCC	Vin(min) = 5.5 V, Io=0 mA, Cload = 10 µF	4.8	5.15	5.4	V
		Vin(min) = 5.5 V, Io=70 mA, Cload = 10 µF	4.5	4.99	5.2	
VCC Dropout	VCC_{drop}	Io=0-70 mA, Cload =10µF, Vin=5.1 V			0.7	V
Short Circuit Current	I_{short}			110		mA
Internal Regulator (P1V8)						
Output Voltage	P1V8	Vin(min) = 4.5 V, Io = 0-1mA , Cload = 10 µF	1.795	1.83	1.905	V
1.8V UVLO Start	P1V8_UVLO_Start	1.8 V Rising Trip Level	1.66	1.72	1.78	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.8V UVLO Stop	P1V8_UVLO_Stop	1.8 V Falling Trip Level	1.59	1.63	1.68	V
Oscillator						
Ramp Amplitude	Vramp	PVin=5 V, D=Dmax, Note 2		0.71		Vp-p
		PVin=12 V, D=Dmax,Note 2		1.84		
		PVin=16 V, D=Dmax,Note 2		2.46		
Ramp Offset	Ramp(os)	Note 2		0.22		V
Min Pulse Width	Tmin(ctrl)	Note 2		35	50	ns
Fixed Off Time	Toff	Note 2 Fs=1.5 MHz		100	150	ns
Max Duty Cycle	Dmax	Fs=400 kHz	86	87.5	89	%
Error Amplifier						
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Sink Current	Isink(E/A)		0.6	1.1	1.8	mA
Source Current	Isource(E/A)		8	13	25	mA
Slew Rate	SR	Note 2	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 2	20	30	40	MHz
DC Gain	Gain	Note 2	100	110	120	dB
Maximum output Voltage	Vmax(E/A)		2.8	3.9	4.3	V
Minimum output Voltage	Vmin(E/A)				100	mV
Reference Voltage						
Accuracy $0^0C<Tj<85^0C$		1.25 V<V_{FB}<2.555 V VOUT_SCALE_LOOP=1;	-1		+1	%
		0.75 V<VFB<1.25 V VOUT_SCALE_LOOP=1;	-0.75		+0.75	
		0.45 V<V_{FB}<0.75 V VOUT_SCALE_LOOP=1;	-0.5		+0.5	
Accuracy $-40^0C<Tj<125^0C$		1.25 V<V_{FB}<2.555 V VOUT_SCALE_LOOP=1;	-1.6		+1.6	%
		0.75 V<VFB<1.25 V VOUT_SCALE_LOOP=1;	-1.0		+1.0	
		0.45 V<V_{FB}<0.75 V VOUT_SCALE_LOOP=1;	-2.0		+2.0	
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 2	3	6.4		MHz
DC Gain	Gain_RS	Note 2		110		dB
Offset Voltage	Offset_RS	0.5 V<RS+<2.555 V, 4 kΩ load 27 °C<Tj<85 °C	-1.6	0	1.6	mV
		0.5 V<RS+<2.555 V, 4kΩ load -40 °C<Tj<125 °C	-3		3	
Source Current	Isource_RS	V_RSO=1.5 V, V_RSP=4 V	11		16	mA
Sink Current	Isink_RS		0.4	1	2	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Slew Rate	Slew_RS	Note 2, Cload = 100 pF	2	4	8	V/µs
Source Current	Isource_RS	V_RSO=1.5 V, V_RSP=4 V	11		16	mA
RS+ input impedance	Rin_RS+		36	55	74	Kohm
RS- input impedance	Rin_RS-	Note 2	36	55	74	Kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RS+)	0.5	1	1.5	V
Minimum Voltage	Min_RS			4	20	mV
Power Good						
Power Good High threshold	Power_Good_High	Vsns rising, VOUT_SCALE_LOOP=1, Vout=0.5 V, PMBus™ mode		0.45		V
Power Good Low Threshold	Power_Good_Low	Vsns falling, VOUT_SCALE_LOOP=1, Vout=0.5 V, PMBus™ mode		0.43		V
Power Good High Threshold Rising Delay	TPDLY	Vsns rising, Vsns > Power_Good_High		0		ms
Power Good Low Threshold Falling delay	VPG_low_Dly	Vsns falling, Vsns < Power_Good_Low	150	175	200	µs
Pgood Voltage Low	PG(voltage)	Ipgood = -5 mA			0.5	V
Under-Voltage Lockout						
Vcc-Start Threshold	VCC_UVLO_Start	Vcc Rising Trip Level	4.0	4.2	4.4	V
Vcc-Stop Threshold	VCC_UVLO_Stop	Vcc Falling Trip Level	3.7	3.9	4.1	
Enable-Start-Threshold	Enable_UVLO_Start	EN supply ramping up	0.55	0.6	0.65	V
Enable-Stop-Threshold	Enable_UVLO_Stop	EN supply ramping down	0.35	0.4	0.45	
Enable Leakage Current	Ien	Enable = 5.5 V			1	µA
Over-Voltage Protection						
OVP Trip Threshold	OVP (trip)	Vsns rising, VOUT_SCALE_LOOP=1, Vout=0.5V	0.57	0.605	0.63	V
OVP Comparator Delay	OVP (hyst)	Vsns falling, VOUT_SCALE_LOOP=1, Vout=0.5 V	20	30	40	mV
OVP Fault Prop Delay	OVP (delay)	Vsns rising, Vsns-OVP(trip)>200 mV		200		ns
Over-Curent Protection						
OC Trip Current	I_{TRIP}	OC limit=40, VCC = 5.05 V, T_j=25 °C	34.5	40	44	A
OCset Current Temperature coefficient	OCSET(temp)	-40 °C to 125 °C, VCC=5.05 V, Note 2		5900		ppm/°C
Hiccup blanking time	Tblk_Hiccup	Note 2		20		ms
Over-Temperature Protection						
Thermal Shutdown		Note 2		145		°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis		Note 2		25		
Input Over-Voltage Protection						
PVin over-voltage threshold	$PVin_{OV}$		22	23.7	25	V
PVin over-voltage Hysteresis	$PVin_{ov\ hyst}$			2.4		V
Output Voltage Reporting						
Resolution	N_{Vout}	Note 2		1/256		V
Vout update rate				31.25		kHz
Lowest reported Vout	Vomon_low	Vsns=0V		0		V
Highest reported Vout	Vomon_high	VOUT_SCALE_LOOP=1, Vsns=3.3 V		3.3		V
		VOUT_SCALE_LOOP=0.5, Vsns=3.3 V		6.6		V
		VOUT_SCALE_LOOP=0.25, Vsns=3.3 V		13.2		V
		VOUT_SCALE_LOOP=0.125, Vsns=3.3 V		26.4		V
Vout reporting accuracy		0 °C to 85 °C, 4.5 V<Vcc<5.5 V, 1 V<Vsns≤ 1.5 V VOUT_SCALE_LOOP=1		+/-0.6		%
		0 °C to 85 °C, 4.5 V<Vcc<5.5 V, Vsns> 1.5 V VOUT_SCALE_LOOP=1		+/-1		
		0 °C to 125 °C, 4.5 V<Vcc<5.5 V, Vsns>0.9 V VOUT_SCALE_LOOP=1		+/-1.5		
		0°C to 125°C, 4.5V<Vcc<5.5V, 0.5V<Vsns<0.9V VOUT_SCALE_LOOP=1		+/-3		
Iout Reporting						
Resolution	N_{Iout}	Note 2		1/16		A
Iout update rate				31.25		kHz
Iout (digital) monitoring Range			0		40	A
Iout_dig Accuracy	I2C/PMBus™ mode	0 °C to 125 °C, 4.5 V<Vcc<5.5 V, 5 A < Iout <30 A		+/-5		%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		Note 3				
Temperature Reporting						
Resolution	N_{Tmon}	Note 2		1		°C
Temperature update rate				31.25		kHz
Temperature Monitoring Range	Tmon_dig		-40		150	°C
Thermal shutdown hysteresis		Note 2		25		°C
Input Voltage Reporting						
Resolution	N_{PVin}	Note 2		1/32		V
Monitoring Range	PMBVinmon		0		21	V
PVin update rate				31.25		kHz
Monitoring accuracy		0 °C to 85 °C 4.5 V<Vcc<5.5V, PVin>10 V	-1.5		1.5	%
		-40°C to 125°C 4.5 V<Vcc<5.5 V, PVin>14 V	-1.5		1.5	
		-40 °C to 125 °C, 4.5 V<Vcc<5.5 V, 7V<PVin<14 V	-4		4	
PMBus™ Interface Timing Specifications						
SMBus Operating frequency	F_{SMB}				400	kHz
Bus Free time between Start and Stop condition	T_{BUF}		1.3			µs
Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$		0.6			µs
Repeated start condition setup time	$T_{SU:STA}$		0.6			µs
Stop condition setup time	$T_{SU:STO}$		0.6			µs
Data Rising Threshold			1.339		1.766	V
Data Falling Threshold			1.048		1.495	V
Data Rising Threshold LVT			0.45		0.65	V
Clock Rising Threshold LVT			0.7		0.9	V
Clock Falling Threshold LVT			0.45		0.65	V
Data Hold Time	$T_{HD:DAT}$		300		900	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Setup Time	$T_{SU:DAT}$		100			ns
Data pulldown resistance			8	11	16	Ω
SALERT# pulldown resistance			9	12	17	Ω
Clock low time out	$T_{TIMEOUT}$		25		35	ms
Clock low period	T_{LOW}		1.3			µs
Clock High Period	T_{HIGH}		0.6		50	µs

Note: *[2] Guaranteed by design and not tested in production.*

Note: *[3] Guaranteed by statistical correlation, but not tested in production.*

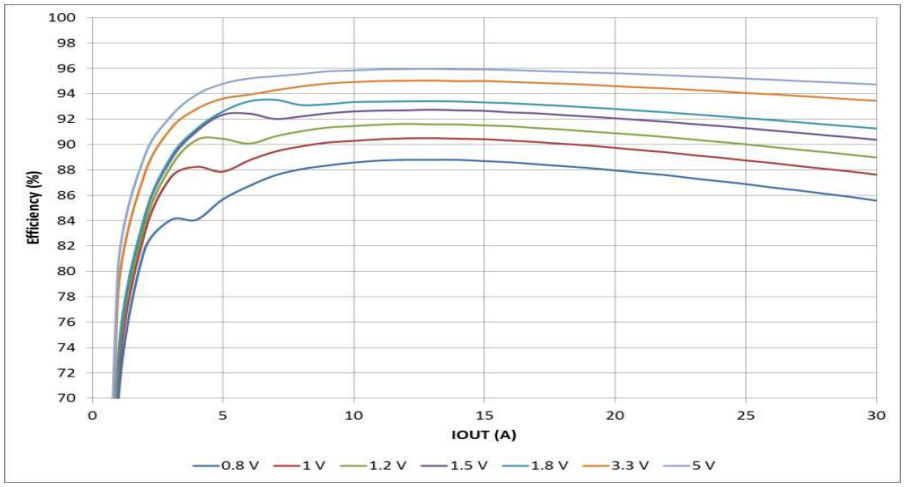
8 Typical efficiency and power loss curves

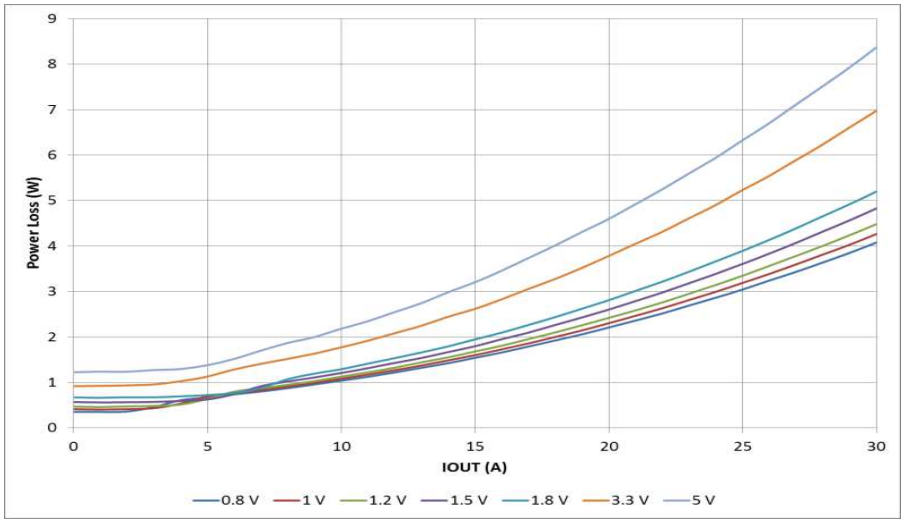
8.1 $PV_{in} = V_{in} = 12$ V, VCC=5 V, $F_s = 600$ kHz

$PV_{in} = V_{in} = 12$ V, VCC=5 V (external), Io=0-30 A, Fs= 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR38164, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 5 Inductors for $PV_{in}=V_{in}=12$ V, VCC, $F_s = 600$ kHz

Vout (V)	Lout (µH)	P/N	DCR (mΩ)	Size (mm)
0.8	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.0	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.2	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.5	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.8	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
3.3	0.32	FP1308R3-R32-R (Cooper)	0.32	12.7 x 13.4 x 8
5	0.32	FP1308R3-R32-R (Cooper)	0.32	12.7 x 13.4 x 8



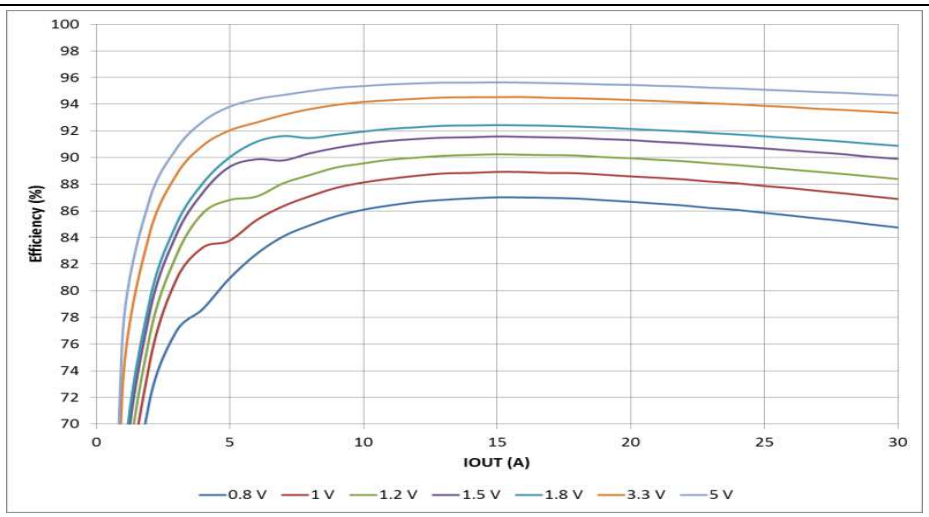


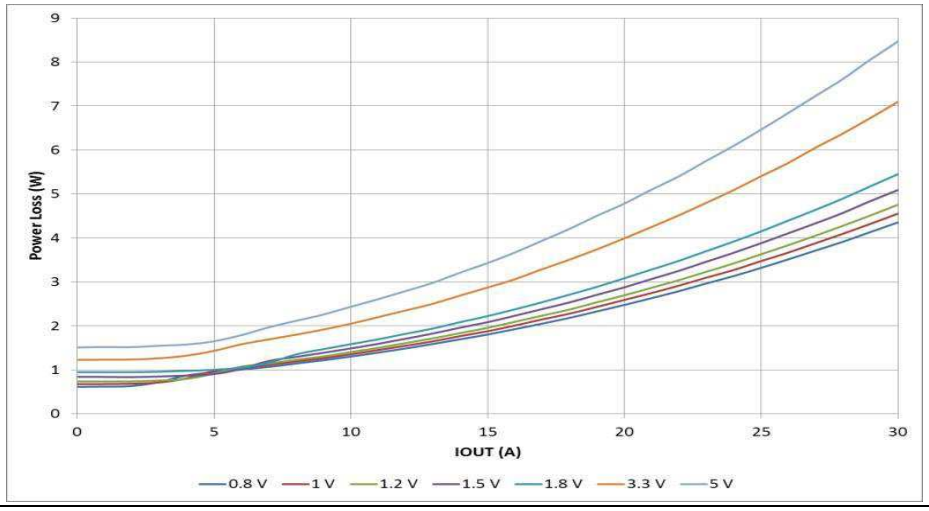
8.2 $PV_{in} = V_{in} = 12$ V, VCC (Internal LDO), $F_s = 600$ kHz

PVin = Vin = 12 V, Internal LDO, Io=0-30 A, Fs= 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR38164, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 6 Inductors for $PV_{in}=V_{in}=12$ V, Internal LDO, $F_s = 600$ kHz

Vout (V)	Lout (µH)	P/N	DCR (mΩ)	Size (mm)
0.8	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.0	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.2	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.5	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.8	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
3.3	0.32	FP1308R3-R32-R (Cooper)	0.32	12.7 x 13.4 x 8
5	0.32	FP1308R3-R32-R (Cooper)	0.32	12.7 x 13.4 x 8



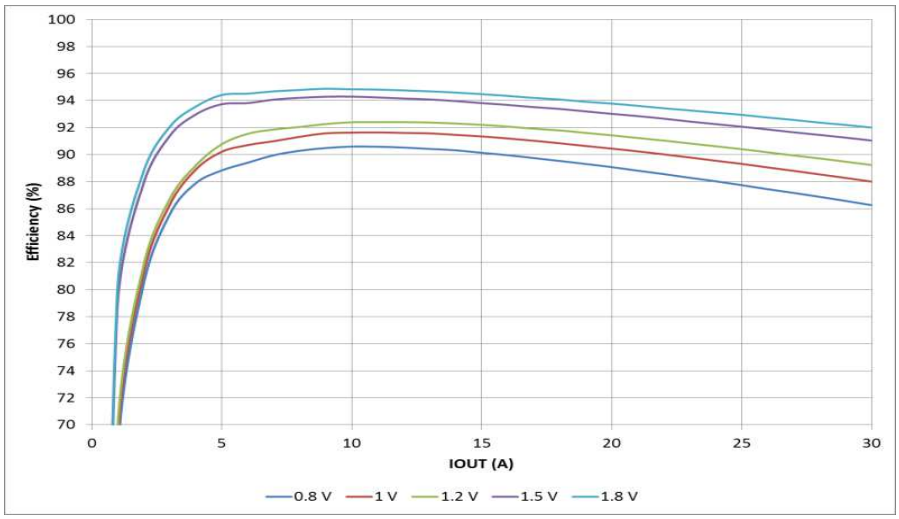


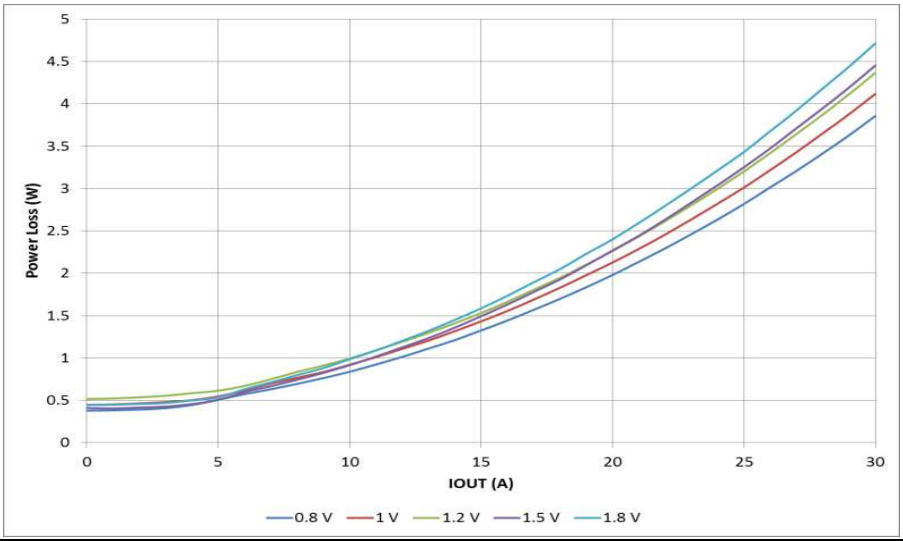
8.3 $PV_{in} = V_{in} = Vcc = 5\ V, F_s = 600\ kHz$

PVin = Vin = VCC = 5 V, Io=0-30 A, Fs= 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR38164, the inductor losses, the losses of the input and output capacitors and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 7 Inductors for $PV_{in}=V_{in}=Vcc=5\ V, F_s = 600\ kHz$

Vout (V)	Lout (µH)	P/N	DCR (mΩ)	Size (mm)
0.8	0.1	HCB138380D-101 (Delta)	0.15	12.4 x 8.3 x 8
1.0	0.1	HCB138380D-101 (Delta)	0.15	12.4 x 8.3 x 8
1.2	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.5	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.8	0.15	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8





9 Iout reporting curves (SVID)

An Intel VRTT tool was used on a 38164 demo board running at 978 kHz to collect SVID Iout reporting data. This is shown on Figure 4 and Figure 5.

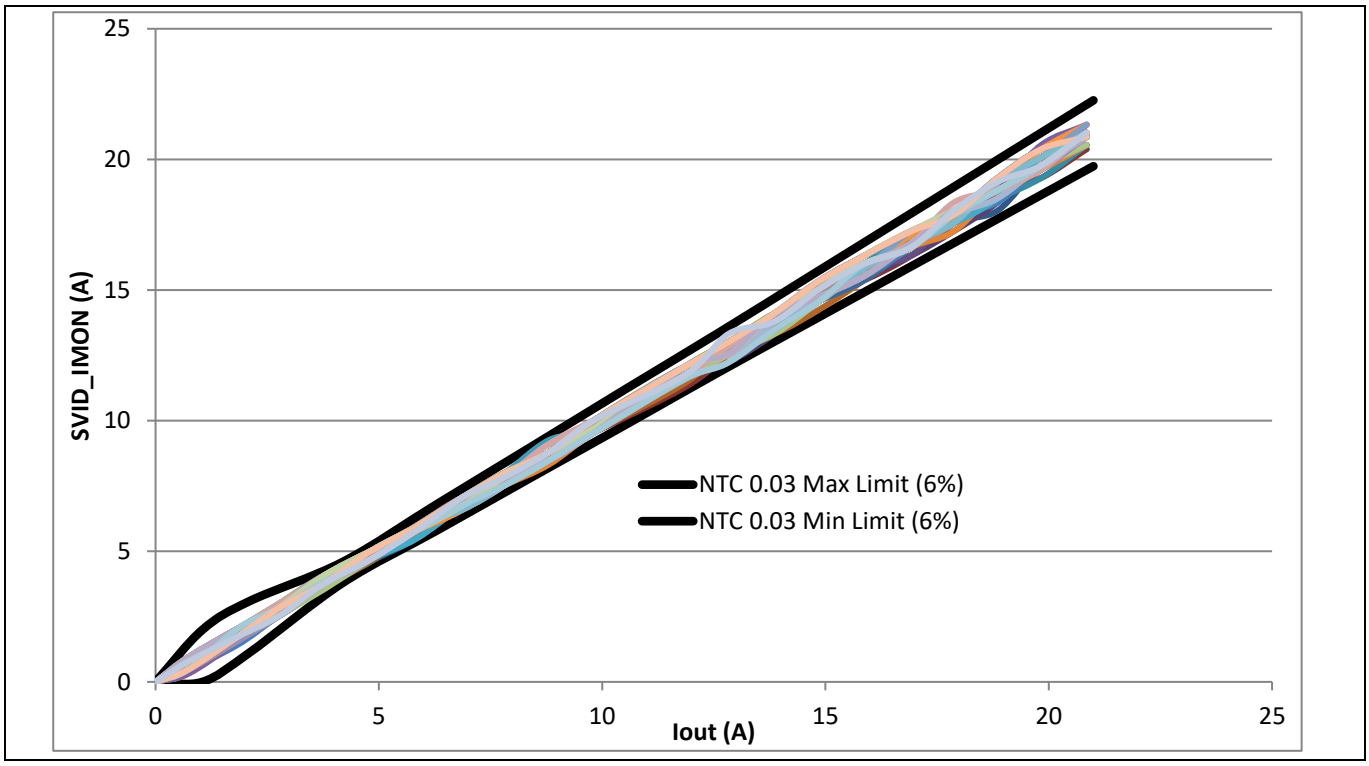


Figure 4 SVID readings from 37 units. Intel DCR 7%, NTC 3% spec.

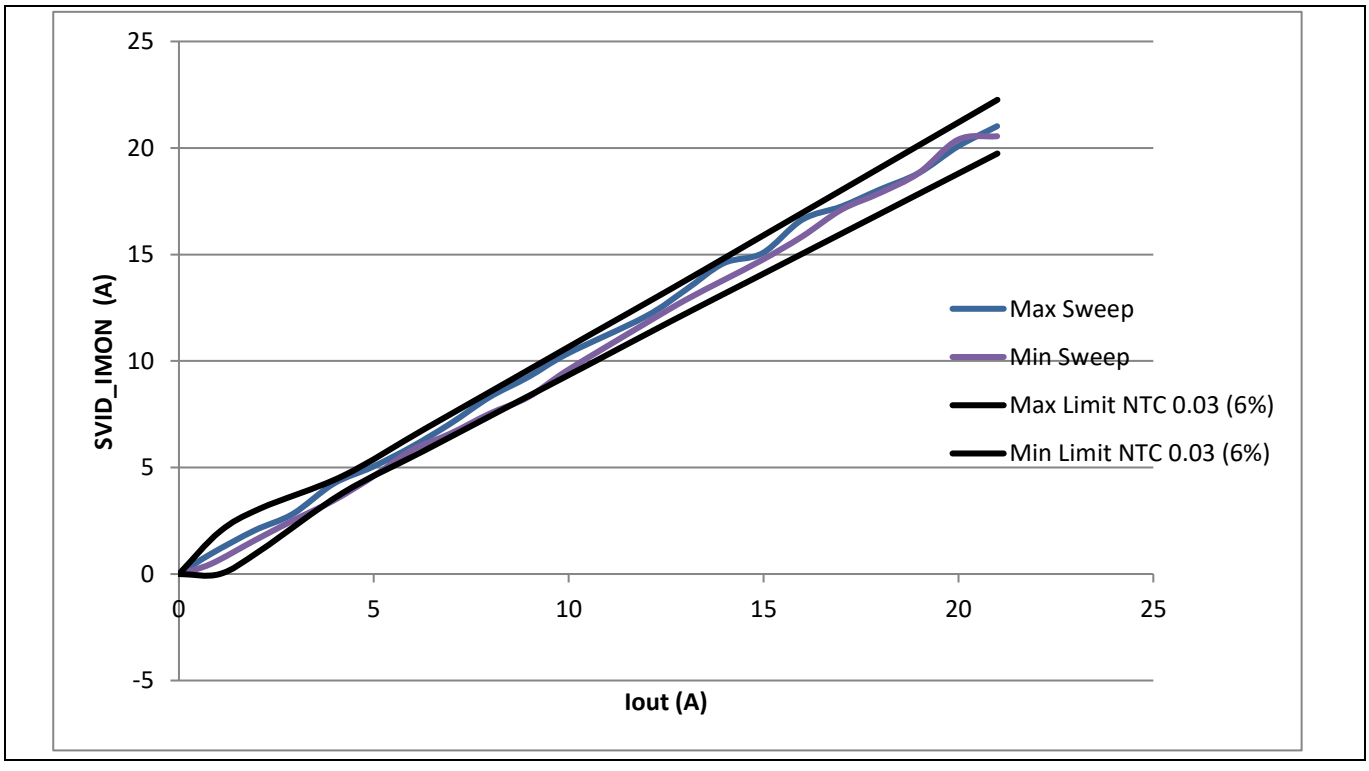


Figure 5 SVID readings for the min and max gain. Intel DCR 7%, NTC 3% spec.

10 Thermal Derating curves

The measurements were done on an IR38164 demo board. The PCB is 7.0” x 5.5” x 0.072” with 10-layers, FR4 material and 2 oz. copper.

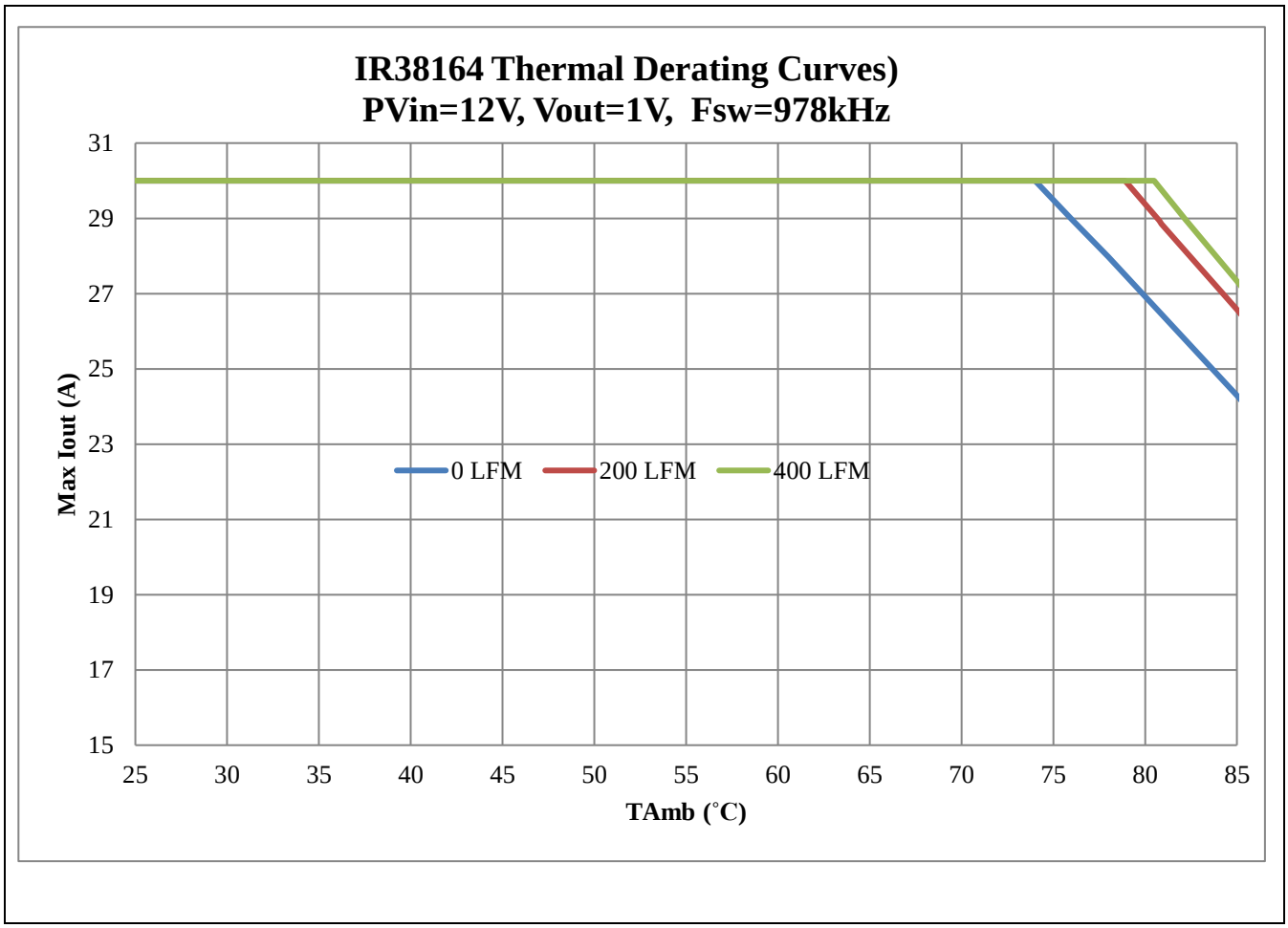


Figure 6 PV_{in} = 12 V, V_{out}=1 V, Vcc = Internal LDO, F_s = 978 kHz

11 Typical application configurations

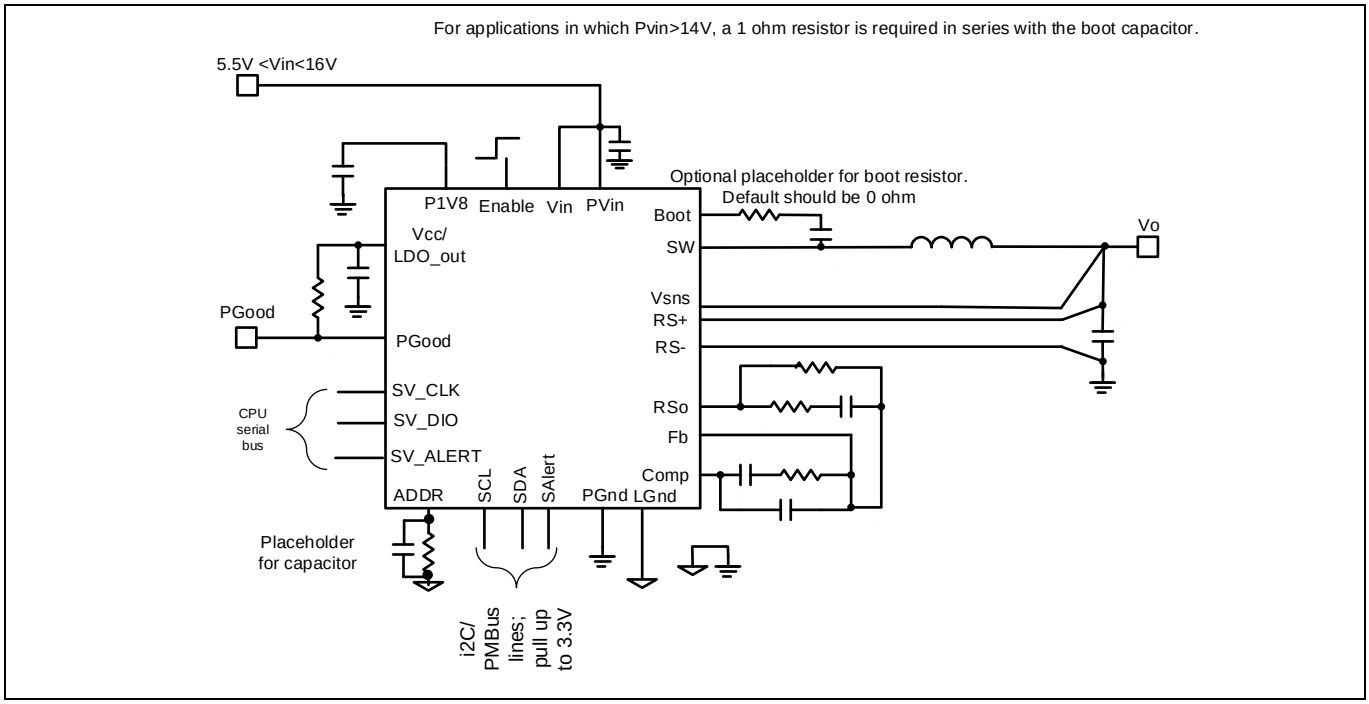


Figure 7 Using the internal LDO, Vo < 2.555 V

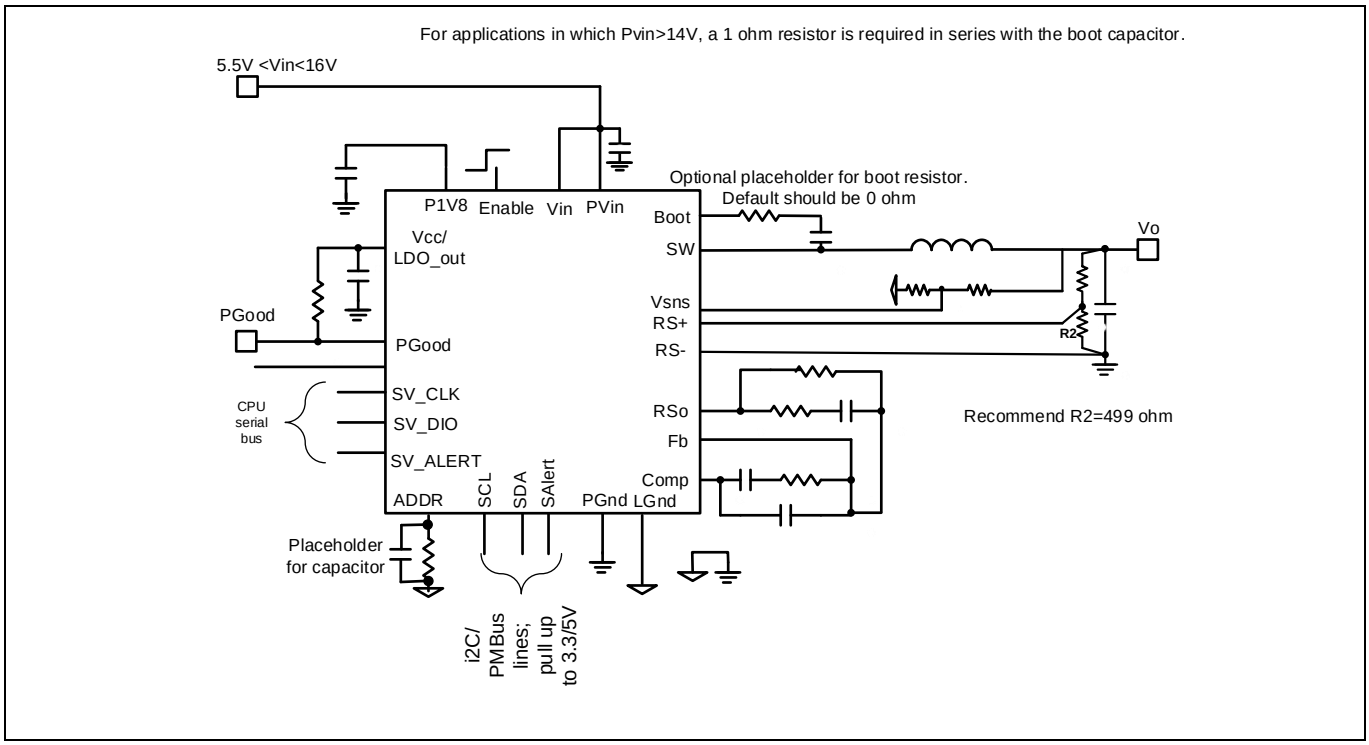


Figure 8 Using the internal LDO, Vo > 2.555 V

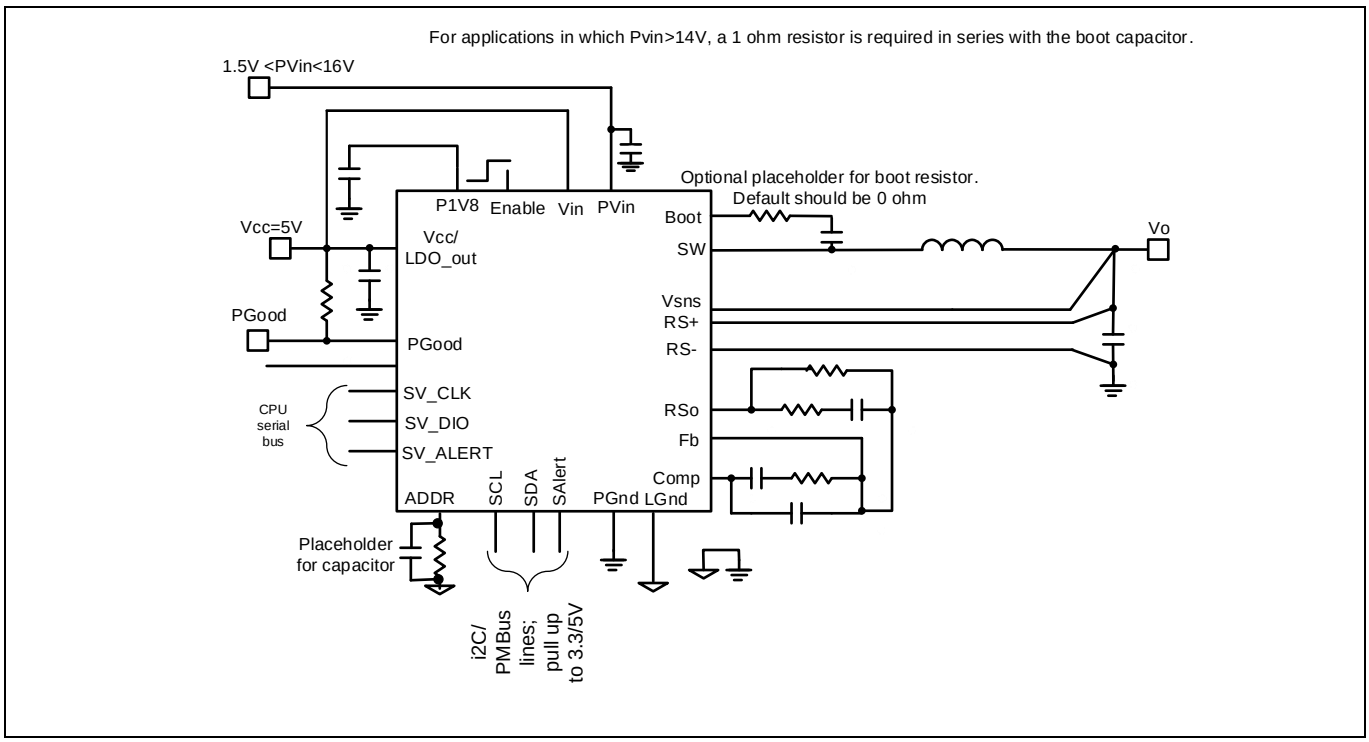


Figure 9 Using external Vcc, Vo<2.555 V

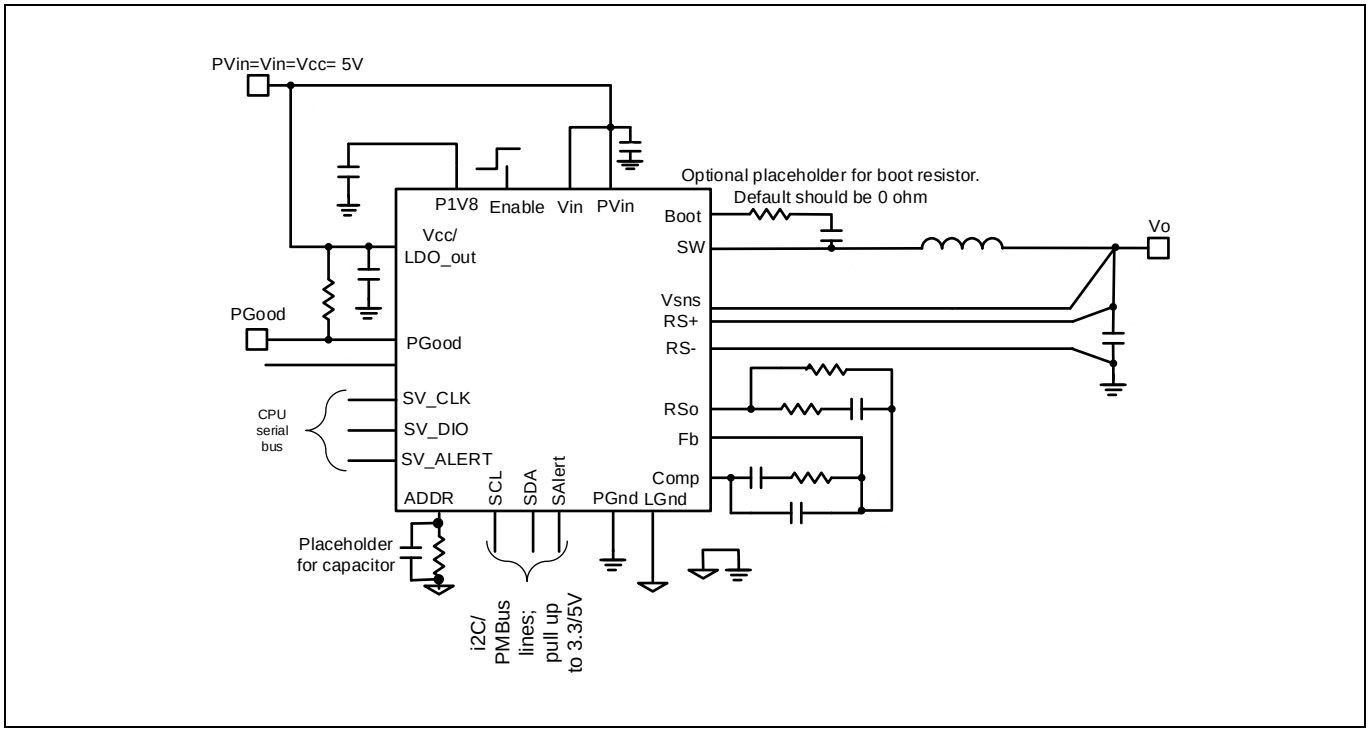


Figure 10 Single 5 V application, Vo<2.555 V

12 $R_{DS(ON)}$ of MOSFETs Over Temperature

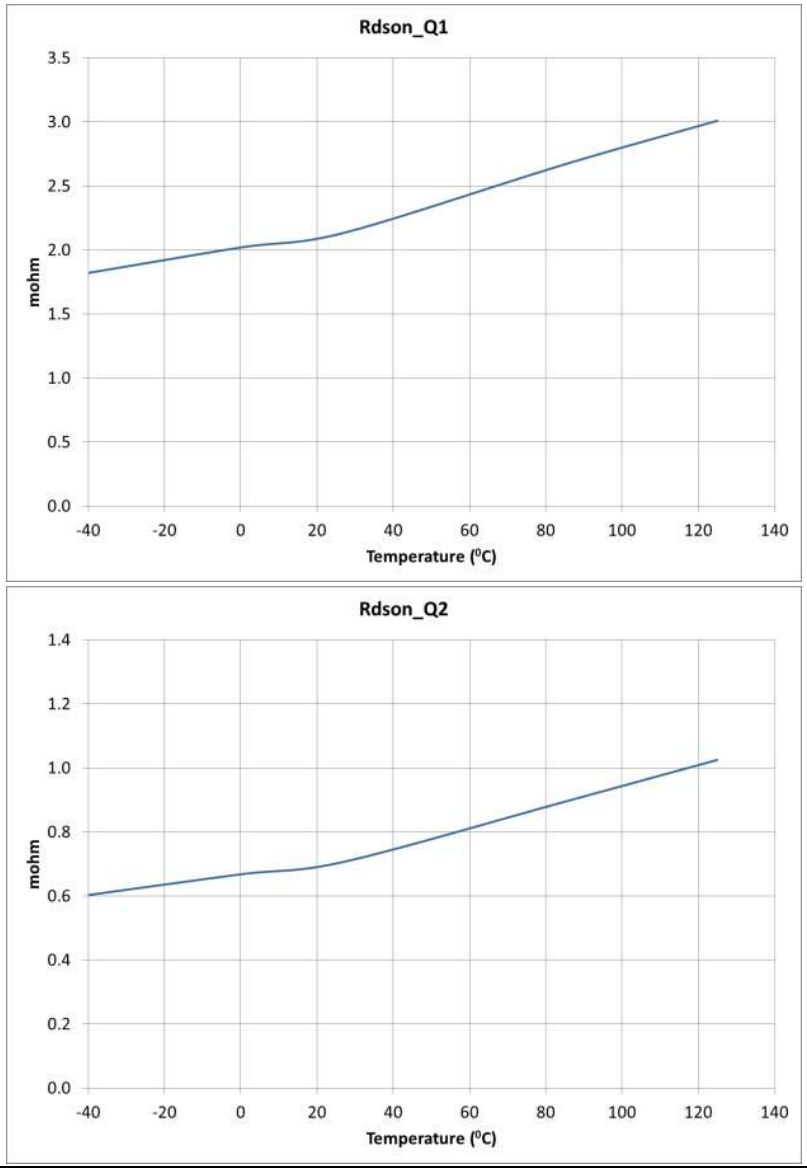


Figure 11 $R_{DS(on)}$ of MOSFETs over Temperature

13 Typical operating characteristics (-40 °C to +125 °C)

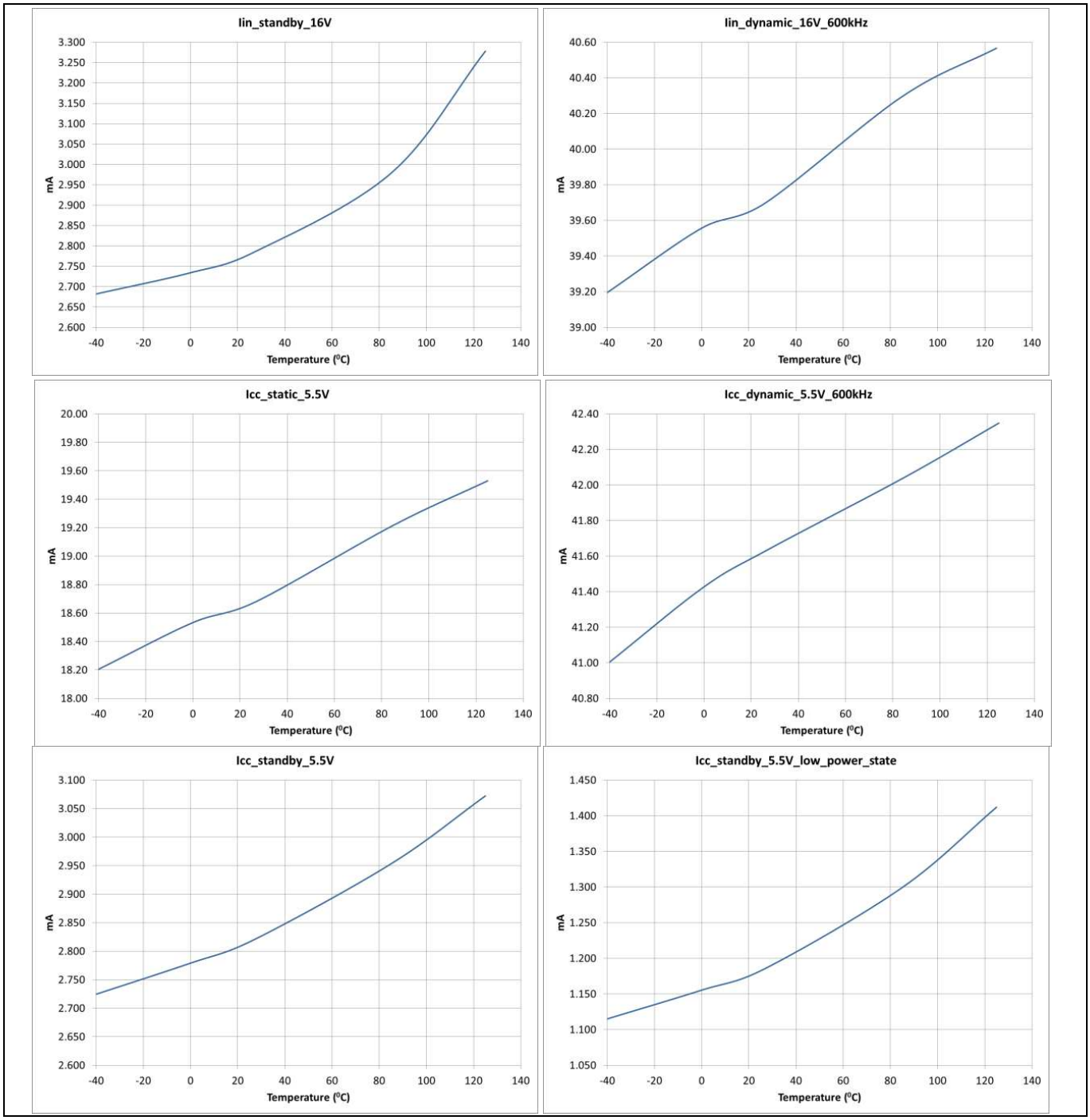


Figure 12 Typical operating characteristics (set 1 of 2)

Typical operating characteristics (-40 C to +125 C)

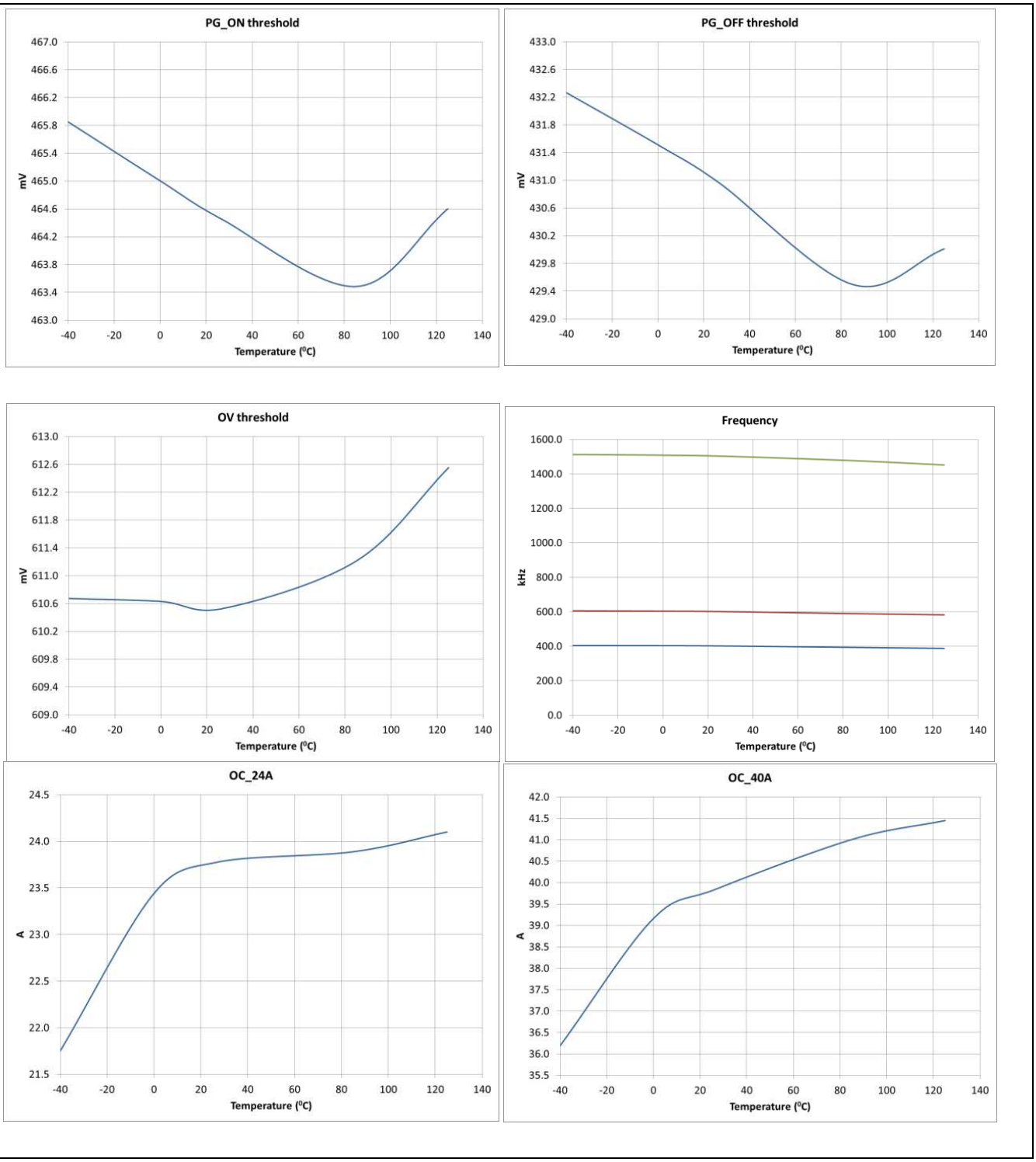


Figure 13 Typical operating characteristics (set 2of 2)

14 Theory of operation

14.1 Description

The IR38164 is a 30 A rated synchronous buck converter that supports PMBus™ and I2C digital interfaces respectively. This device is Intel SVID compliant and can support VR12.5 as well as VR13. It uses an externally compensated fast, analog, PWM voltage mode control scheme to provide good noise immunity as well as fast dynamic response in a wide variety of applications. At the same time, the digital communication interfaces allow complete configurability of output setting and fault functions, as well as telemetry.

The switching frequency is programmable from 500 kHz to 1.5 MHz and provides the capability of optimizing the design in terms of size and performance.

The IR38164 provides precisely regulated output voltages from 0.5 V to 0.875*PVin programmed via two external resistors or through the communication interfaces. They operate with an internal bias supply (LDO), typically 5.2 V. This allows operation with a single supply. The output of this LDO is brought out at the Vcc pin and must be bypassed to the system power ground with a 10 µF decoupling capacitor. The Vcc pin may also be connected to the Vin pin, and an external Vcc supply between 4.5 V and 5.5 V may be used, allowing an extended operating bus voltage (PVin) range from 1.5 V to 16 V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as the current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense components.

The IR38164 includes two low $R_{DS(ON)}$ MOSFETs using Infineon's OptiMOS™ technology. These are specifically designed for low duty cycle, high efficiency applications.

14.2 Device Power-up and Initialization

During the power-up sequence, when Vin is brought up, the internal LDO converts it to a regulated 5.2 V at Vcc. There is another LDO which further converts this down to 1.8 V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of VCC pin and the P1V8 pin, and holds the Power-on-reset (POR) low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes a multiple times programmable (MTP) memory load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use PMBus™ commands to re-configure the various parameters to suit the specific VR design requirements if desired, irrespective of the status of Enable.

The typical default configuration utilizes the internal LDO to supply the VCC rail when PVin is brought up. For this configuration power conversion is enabled only when the Enable pin voltage exceeds its under-voltage threshold, the PVin bus voltage exceeds its under-voltage threshold, the contents of the MTP have been fully loaded into the working registers and the device address has been read. The initialization sequence is shown in Figure 14. Another common default configuration uses an external power supply for the VCC rail. While in this configuration it is recommended to ensure the VCC rail reaches its target voltage prior the enable signal goes high.

Additional options are available to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface or PMBus™. For further details, see the UN0075 IR3816x PMBus™ commandset user note.

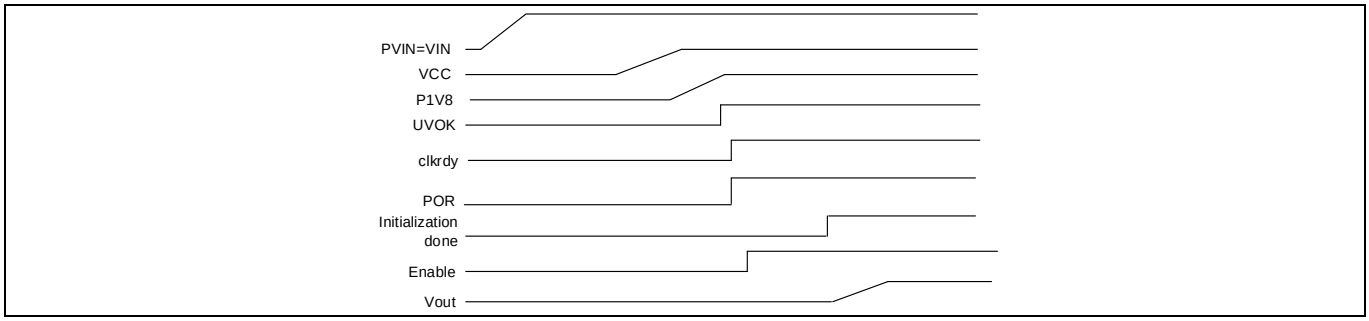


Figure 14 Initialization sequence showing PVin, Vin, Vcc, 1.8V, Enable and Vout signals as well as the internal logic signals

14.3 I2C and PMBUS™ Communication

All the devices in this family have two 7-bit registers that are used to set the base I2C address and base PMBus™ address of the device, as shown below in Table 8 .

Table 8 Registers used to set device base address

Register	Description
I2c_address[6:0]	The chip I2C address. An address of 0 will disable I2C communication. Note that disabling I2C does not disable PMBus™.
PMBus™_address[6:0]	The chip PMBus™ address. An address of 0 will disable PMBus™ communication. Note that disabling PMBus™ does not disable I2C.

In addition, a resistor may be connected between the ADDR and LGND pins to set an offset from the default preconfigured I2C address (0x10) /PMBus™ address (0x40) in the MTP. Up to 16 different offsets can be set, allowing 16 devices with unique addresses in a single system. This offset, and hence, the device address, is read by the internal 10-bit ADC during the initialization sequence.

Table 9 below provides the resistor values needed to set the 16 offsets from the base address.

***Do not use these values for applications with ambient temperatures <0°C.**

Table 9 Address offset vs External Resistor(R_{ADDR})

ADDR Resistor (Ohm)	Address Offset
499	+0
1050	+1
1540	+2
2050	+3
2610	+4
3240	+5
3830	+6

ADDR Resistor (Ohm)	Address Offset
4530	+7
5230	+8
6040	+9
6980	+10
7870	+11
8870	+12
9760	+13
10700	+14
>11800	+15

The device will then respond to I2C/PMBus™ commands sent to this address. There is also a register bit i2c_disable_addr_offset that may be set in order to instruct the device to ignore the resistor offset for both I2C and PMBus™. If this bit is set, the device will always respond to commands sent to the base address. For applications with junction temperatures below 0°C, offsets +0, +1, and +2 are not available.

14.4 Modes for Setting Output Voltages

These devices provide a configuration bit that allows the user to choose between PMBus™ and SVID modes. When this bit is set, SVID mode, the output voltage will ramp to the configured boot voltage and subsequently, respond to voltage set commands issued by the CPU on the Serial VID (SVID) interface. The VID tables for 5 mV and 10 mV VID steps are shown in the tables below. A VID code of 0 corresponds to 0 V as well as the regulator shutdown code in SVID mode. Vboot which is utilized in the SVID mode should not be set to 0 V as this will shutdown the regulator. When this bit is zero, the regulation is determined by the output voltage set by the PMBus™ commands. It should be noted that irrespective of the mode used to set the output voltage, telemetry information always remains available on both the communications busses.

Table 10 Intel 5 mV VID table

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
FF	1.52	C5	1.23	91	0.97	57	0.68	2F	0.48
FE	1.515	C4	1.225	90	0.965	56	0.675	2E	0.475
FD	1.51	C3	1.22	8F	0.96	55	0.67	2D	0.47
FC	1.505	C2	1.215	8E	0.955	54	0.665	2C	0.465
FB	1.5	C1	1.21	8D	0.95	53	0.66	2B	0.46
FA	1.495	C0	1.205	8C	0.945	52	0.655	2A	0.455
F9	1.49	BF	1.2	8B	0.94	51	0.65	29	0.45
F8	1.485	BE	1.195	8A	0.935	50	0.645	28	0.445
F7	1.48	BD	1.19	89	0.93	4F	0.64	27	0.44
F6	1.475	BC	1.185	88	0.925	4E	0.635	26	0.435
F5	1.47	BB	1.18	87	0.92	4D	0.63	25	0.43
F4	1.465	BA	1.175	86	0.915	4C	0.625	24	0.425
F3	1.46	B9	1.17	85	0.91	4B	0.62	23	0.42
F2	1.455	B8	1.165	84	0.905	4A	0.615	22	0.415
F1	1.45	B7	1.16	83	0.9	49	0.61	21	0.41
F0	1.445	B6	1.155	82	0.895	48	0.605	20	0.405
EF	1.44	BB	1.18	81	0.89	47	0.6	1F	0.4
EE	1.435	BA	1.175	80	0.885	58	0.685	1E	N/A
ED	1.43	B9	1.17	7F	0.88	57	0.68	1D	N/A
EC	1.425	B8	1.165	7E	0.875	56	0.675	1C	N/A
EB	1.42	B7	1.16	7D	0.87	55	0.67	1B	N/A
EA	1.415	B6	1.155	7C	0.865	54	0.665	1A	N/A
E9	1.41	B5	1.15	7B	0.86	53	0.66	19	N/A
E8	1.405	B4	1.145	7A	0.855	52	0.655	18	N/A
E7	1.4	B3	1.14	79	0.85	51	0.65	17	N/A
E6	1.395	B2	1.135	78	0.845	50	0.645	16	N/A
E5	1.39	B1	1.13	77	0.84	4F	0.64	15	N/A
E4	1.385	B0	1.125	76	0.835	4E	0.635	14	N/A
E3	1.38	AF	1.12	75	0.83	4D	0.63	13	N/A
E2	1.375	AE	1.115	74	0.825	4C	0.625	12	N/A
E1	1.37	AD	1.11	73	0.82	4B	0.62	11	N/A
E0	1.365	AC	1.105	72	0.815	4A	0.615	10	N/A
DF	1.36	AB	1.1	71	0.81	49	0.61	0F	N/A
DE	1.355	AA	1.095	70	0.805	48	0.605	0E	N/A
DD	1.35	A9	1.09	6F	0.8	47	0.6	0D	N/A
DC	1.345	A8	1.085	6E	0.795	46	0.595	0C	N/A
DB	1.34	A7	1.08	6D	0.79	45	0.59	0B	N/A
DA	1.335	A6	1.075	6C	0.785	44	0.585	0A	N/A
D9	1.33	A5	1.07	6B	0.78	43	0.58	09	N/A
D8	1.325	A4	1.065	6A	0.775	42	0.575	08	N/A
D7	1.32	A3	1.06	69	0.77	41	0.57	07	N/A
D6	1.315	A2	1.055	68	0.765	40	0.565	06	N/A
D5	1.31	A1	1.05	67	0.76	3F	0.56	05	N/A
D4	1.305	A0	1.045	66	0.755	3E	0.555	04	N/A
D3	1.3	9F	1.04	65	0.75	3D	0.55	03	N/A
D2	1.295	9E	1.035	64	0.745	3C	0.545	02	N/A
D1	1.29	9D	1.03	63	0.74	3B	0.54	01	N/A
D0	1.285	9C	1.025	62	0.735	3A	0.535	00	N/A
CF	1.28	9B	1.02	61	0.73	39	0.53		
CE	1.275	9A	1.015	60	0.725	38	0.525		
CD	1.27	99	1.01	5F	0.72	37	0.52		
CC	1.265	98	1.005	5E	0.715	36	0.515		
CB	1.26	97	1	5D	0.71	35	0.51		
CA	1.255	96	0.995	5C	0.705	34	0.505		
C9	1.25	95	0.99	5B	0.7	33	0.5		
C8	1.245	94	0.985	5A	0.695	32	0.495		
C7	1.24	93	0.98	59	0.69	31	0.49		
C6	1.235	92	0.975	58	0.685	30	0.485		

Table 11 Intel 10 mV VID table

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
FF	3.04	C5	2.46	8B	1.88	51	1.30	17	0.72
FE	3.03	C4	2.45	8A	1.87	50	1.29	16	0.71
FD	3.02	C3	2.44	89	1.86	4F	1.28	15	0.70
FC	3.01	C2	2.43	88	1.85	4E	1.27	14	0.69
FB	3.00	C1	2.42	87	1.84	4D	1.26	13	0.68
FA	2.99	C0	2.41	86	1.83	4C	1.25	12	0.67
F9	2.98	BF	2.40	85	1.82	4B	1.24	11	0.66
F8	2.97	BE	2.39	84	1.81	4A	1.23	10	0.65
F7	2.96	BD	2.38	83	1.80	49	1.22	0F	0.64
F6	2.95	BC	2.37	82	1.79	48	1.21	0E	0.63
F5	2.94	BB	2.36	81	1.78	47	1.20	0D	0.62
F4	2.93	BA	2.35	80	1.77	46	1.19	0C	0.61
F3	2.92	B9	2.34	7F	1.76	45	1.18	0B	0.60
F2	2.91	B8	2.33	7E	1.75	44	1.17	0A	0.59
F1	2.90	B7	2.32	7D	1.74	43	1.16	09	0.58
F0	2.89	B6	2.31	7C	1.73	42	1.15	08	0.57
EF	2.88	B5	2.30	7B	1.72	41	1.14	07	0.56
EE	2.87	B4	2.29	7A	1.71	40	1.13	06	0.55
ED	2.86	B3	2.28	79	1.70	3F	1.12	05	0.54
EC	2.85	B2	2.27	78	1.69	3E	1.11	04	0.53
EB	2.84	B1	2.26	77	1.68	3D	1.10	03	0.52
EA	2.83	B0	2.25	76	1.67	3C	1.09	02	0.51
E9	2.82	AF	2.24	75	1.66	3B	1.08	01	0.50
E8	2.81	AE	2.23	74	1.65	3A	1.07		
E7	2.80	AD	2.22	73	1.64	39	1.06		
E6	2.79	AC	2.21	72	1.63	38	1.05		
E5	2.78	AB	2.20	71	1.62	37	1.04		
E4	2.77	AA	2.19	70	1.61	36	1.03		
E3	2.76	A9	2.18	6F	1.60	35	1.02		
E2	2.75	A8	2.17	6E	1.59	34	1.01		
E1	2.74	A7	2.16	6D	1.58	33	1.00		
E0	2.73	A6	2.15	6C	1.57	32	0.99		
DF	2.72	A5	2.14	6B	1.56	31	0.98		
DE	2.71	A4	2.13	6A	1.55	30	0.97		
DD	2.70	A3	2.12	69	1.54	2F	0.96		
DC	2.69	A2	2.11	68	1.53	2E	0.95		
DB	2.68	A1	2.10	67	1.52	2D	0.94		
DA	2.67	A0	2.09	66	1.51	2C	0.93		
D9	2.66	9F	2.08	65	1.50	2B	0.92		
D8	2.65	9E	2.07	64	1.49	2A	0.91		
D7	2.64	9D	2.06	63	1.48	29	0.90		
D6	2.63	9C	2.05	62	1.47	28	0.89		
D5	2.62	9B	2.04	61	1.46	27	0.88		
D4	2.61	9A	2.03	60	1.45	26	0.87		
D3	2.60	99	2.02	5F	1.44	25	0.86		
D2	2.59	98	2.01	5E	1.43	24	0.85		
D1	2.58	97	2.00	5D	1.42	23	0.84		
D0	2.57	96	1.99	5C	1.41	22	0.83		
CF	2.56	95	1.98	5B	1.40	21	0.82		
CE	2.55	94	1.97	5A	1.39	20	0.81		
CD	2.54	93	1.96	59	1.38	1F	0.80		
CC	2.53	92	1.95	58	1.37	1E	0.79		
CB	2.52	91	1.94	57	1.36	1D	0.78		
CA	2.51	90	1.93	56	1.35	1C	0.77		
C9	2.50	8F	1.92	55	1.34	1B	0.76		
C8	2.49	8E	1.91	54	1.33	1A	0.75		
C7	2.48	8D	1.90	53	1.32	19	0.74		
C6	2.47	8C	1.89	52	1.31	18	0.73		

14.5 Bus Voltage UVLO

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the device does not turn on until the bus voltage reaches the desired level as shown in Figure 15. Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold (typically 0.6 V) will the device be enabled. Therefore, in addition to being logic input pin to enable the converter, the Enable feature, with its precise threshold, also allows the user to override the default 8 V under-voltage lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the device to be disabled at least until PVin exceeds the desired output voltage level. Alternatively, the default 8 V PVin UVLO threshold may be reconfigured/overridden using the VIN_ON and VIN_OFF PMBus™ commands or the corresponding registers. It should be noted that the input voltage is also fed to an ADC through a 21:1 internal resistive divider. However, the digitized input voltage is used only for the purposes of reporting the input voltage through the READ_VIN PMBus™ command. It has no impact on the bus voltage UVLO, input over-voltage faults and input under-voltage warnings, all of which are implemented by using analog comparators to compare the input voltage to the corresponding thresholds programmed by the PMBus™ commands VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT and VIN_UV_WARN_LIMIT respectively. The bus voltage reading as reported by READ_VIN has no effect on the input feedforward function either.

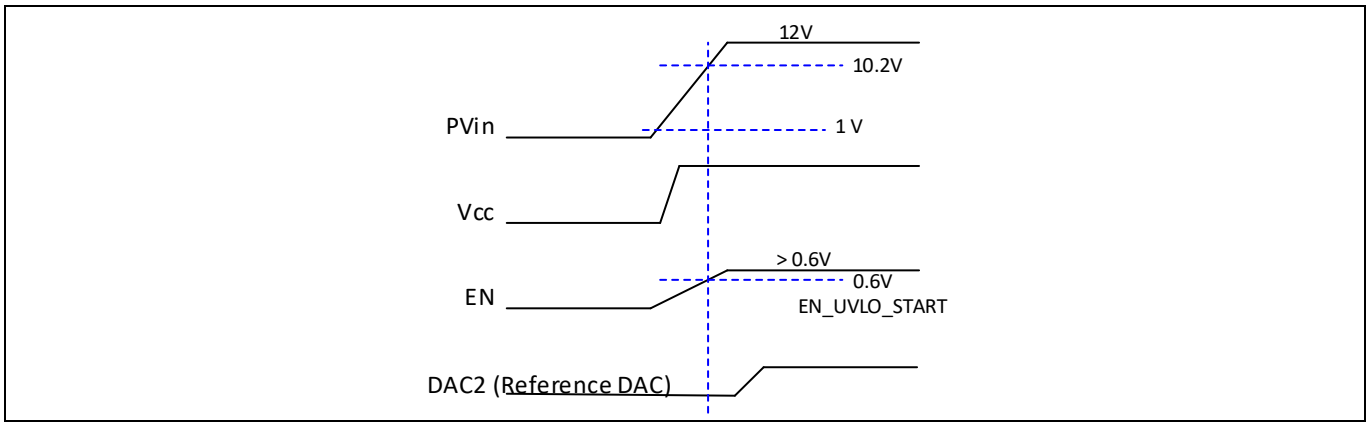


Figure 15 Normal Start up, device turns on when the bus voltage reaches 10.2 V. A resistor divider is used at EN pin from PVin to turn on the device at 10.2 V.

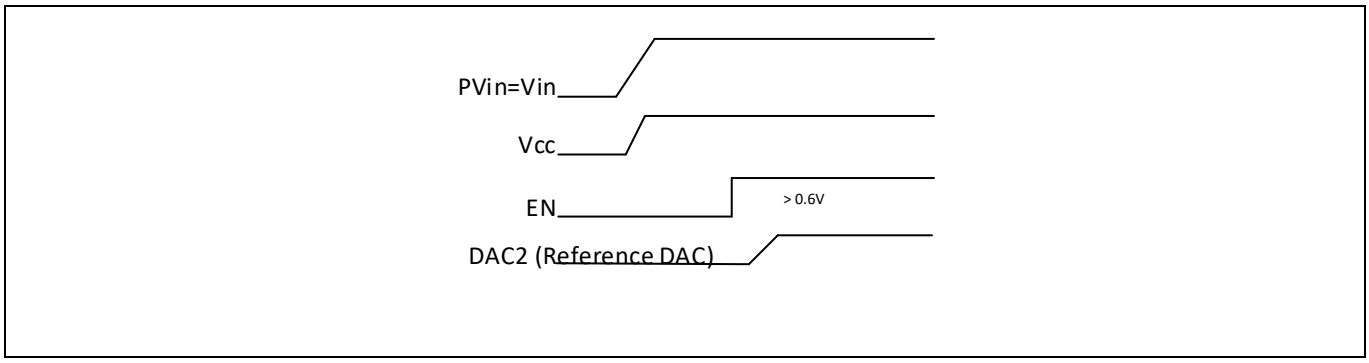


Figure 16 Recommended startup for Normal operation

Figure 16 shows the recommended startup sequence for the normal operation of the device, when Enable is used as logic input.

14.6 Pre-Bias startup

The IR38164 is able to start up into pre-charged output, without oscillations or other disturbance of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (sync FET) off until the first gate signal for the control MOSFET (ctrl FET) is generated. Figure 17 shows a typical pre-bias condition at start up.

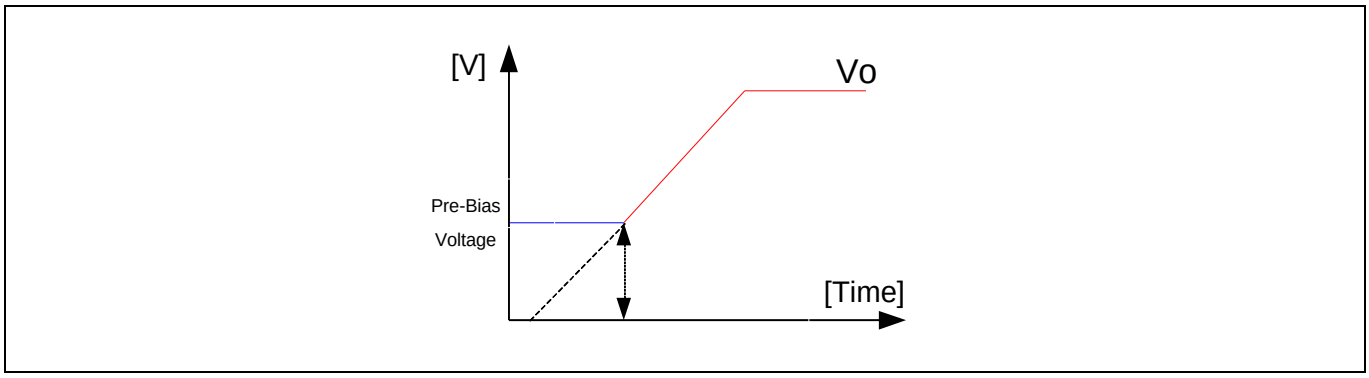


Figure 17 Pre-Bias startup

The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. There are 16 pulses in each step. This value is internally programmed. Figure 18 shows the series of 16x8 startup pulses.

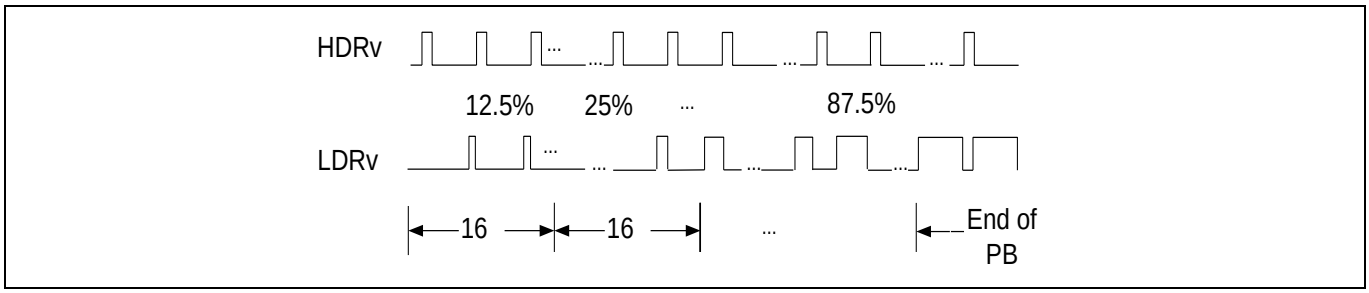


Figure 18 Pre-bias startup pulses

14.7 Soft-Start (Reference DAC ramp)

This device has an internal soft starting DAC to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the DAC sequence initiates only after power conversion is enabled when the Enable pin voltage exceeds its under-voltage threshold, the PVin bus voltage exceeds its under-voltage threshold and the contents of the MTP have been fully loaded into the working registers. Figure 19 shows the waveforms during soft start. It should be noted that the part may also be configured to require software Enable (set through the PMBus™ or the corresponding MTP register) instead of or in addition to a "hardware" signal at the Enable pin. In PMBus™ mode, the reference DAC soft-start may be delayed from the time power conversion is enabled. The range for this programmable delay is 0 ms to 127 ms, and the resolution is 1 ms. Further, in this mode, the soft start time may be configured from 1 ms to 127 ms with 1 ms resolution.

In SVID mode, the rise time is determined by the slow slew rate specified by Intel, and may be programmed to one of four values: 0.625 mV/µs, 1.25 mV/µs, 2.5 mV/µs and 5 mV/µs. In this mode, the device uses 2.5 mV/µs by default. It should be noted, however, that if Vboot is 0, the output voltage does not ramp until the CPU issues a voltage setting command at either the fast slew rate or slow slew rate specified by the CPU.

For more details on the PMBus™ commands TON_DELAY and TON_RISE used to program the startup sequence, please see the UN0075 IR3816x PMBus™ commandset user note.

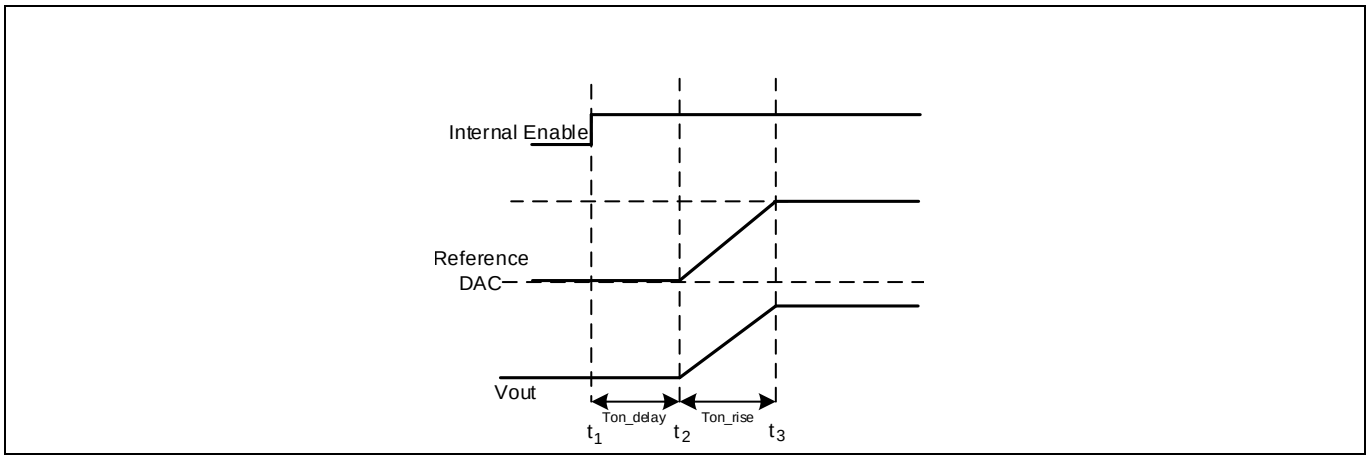


Figure 19 DAC2 (VREF) Soft start

During the startup sequence the over-current protection (OCP) and over-voltage protection (OVP) are active to protect the device against any short circuit or over voltage conditions.

14.8 Operating frequency

Using the FREQUENCY_SWITCH PMBus™ command, or the corresponding registers, the switching frequency may be programmed between 500 kHz and 1.5 MHz. For best telemetry accuracy, it is recommended that the following switching frequencies be avoided: 500 kHz, 600 kHz, 750 kHz, 800 kHz, 1 MHz, 1.2 MHz and 1.5 MHz. Instead the following values are recommended, 505 kHz, 607 kHz, 762 kHz, 813 kHz, 978 kHz, 1171 kHz and 1454 kHz respectively.

14.9 Shutdown

In the default configuration, the device can be shutdown by pulling the Enable pin below its 0.4 V threshold. During shutdown the high side and the low side drivers are turned off. By default, the device exhibits an immediate shutdown with no delay and no soft stop.

Alternatively, the part may be configured to allow shutdown using the OPERATION PMBus™ command or the corresponding register. It may also be configured to allow a soft or controlled turned off. In PMBus™ mode, if the soft-off option is used, the turn off may be delayed from the time the power conversion is disabled. The range for this programmable delay is 0 ms to 127 ms, and the resolution is 1 ms. Further, in this mode, the soft stop time may be configured from 1ms to 127 ms with 1 ms resolution. The programmable turn off delay only applies in PMBus™ mode.

If VCC voltage supply is used to shutdown the system, a continuous ramp from 5V to 0V should be utilized. Shutdown via the Enable pin is the recommended shutdown method.

14.10 Current Sensing, Telemetry and Over-Current Protection

Current sensing for both telemetry as well as over-current protection is done by sensing the voltage across the sync FET $R_{DS(ON)}$. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any minimizes sensitivity to layout related noise issues. A novel, patented scheme allows reconstruction of the average inductor current from the voltage sensed across the Sync FET $R_{DS(ON)}$. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting as well as for over-current warning, the threshold for which may be set using the IOUT_OC_WARN_LIMIT command. The current is reported in 1/16 A resolution using the READ_IOUT PMBus™ command. The current information may also be read back using I2C, through the 8-bit register *output_current_byte,* which reports the current in 1/4 A resolution.

The Over current (OC) fault protection circuit also uses the voltage sensed across the $R_{DS(ON)}$ of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the over-current threshold and does not depend on the ADC or reported current. The current limit scheme uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(ON)}$ of the Synchronous MOSFET. As a result, the over-current trip threshold remains almost constant over temperature.

Over Current Protection circuitry senses the inductor current flowing through the Synchronous FET closer to the valley point. The OCP circuit samples this current for 75 ns typically after the rising edge of the PWM set pulse which is an internal signal that has a width of 12.5% of the switching period. The PWM pulse that turns on the high side FET starts at the falling edge of the PWM set pulse. This makes valley current sense more robust as current is sensed close to the bottom of the inductor downward slope where transient and switching noise is low. This helps to prevent false tripping due to noise and transients.

The actual DC output current limit point will be greater than the valley point by an amount equal to approximately half of the peak to peak inductor ripple current. The current limit point will be a function of the inductor value, input voltage, output voltage and the frequency of operation. On equation 1, I_{Limit} is the value set when configuring the 38164 OCP value. The user should account for the inductor ripple to obtain the actual DC output current limit.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2} \qquad (1)$$

I_{OCP} = DC current limit hiccup point
I_{LIMIT} = Current Limit Valley Point
Δi = Inductor ripple current

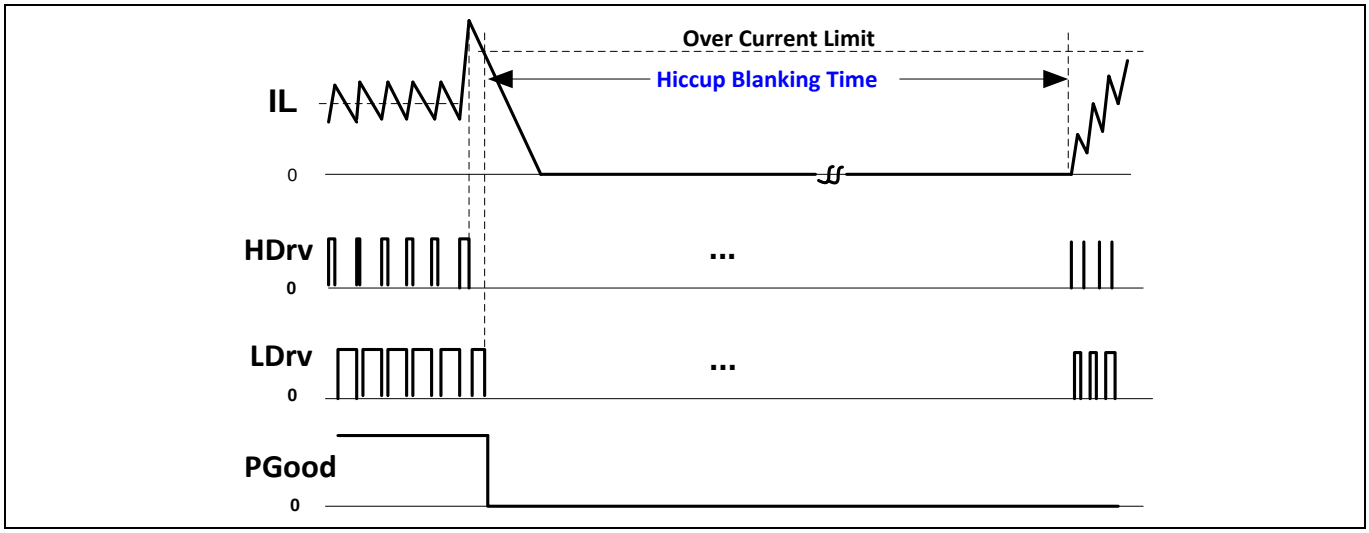


Figure 20 Timing diagram for current limit hiccup

In the default configuration, if the over-current detection trips the OCP comparator for a total of 8 cycles, the device goes into a hiccup mode. The hiccup is performed by de-asserting the internal Enable signal to the analog and power conversion circuitry and holding it low for 20 ms.

Following this, the OCP signal resets and the converter recovers. After every hiccup cycle, the converter stays in this mode until the overload or short circuit is removed. This behavior is shown in Figure 20.

Note that the user can override the default over-current threshold using the PMBus™ command IOUT_OC_FAULT_LIMIT. This command can be used to program the over-current threshold from a minimum recommended 16 A setting to a maximum of 56 A, in 4 A steps. While the IR38164 will still offer over-current protection below 16 A and at magnitudes that are not multiples of 4, these thresholds will not be as accurate. Therefore it's recommended to keep the current limit setting from 16A to 56A with 4A increments. Systems with a high inductor current ripple will affect the accuracy, refer to (1).

Also, using the PMBus™ command IOUT_OC_FAULT_RESPONSE or the corresponding registers, the part may be configured to respond to an over-current fault in one of two ways:

1) Pulse by pulse current limiting for a programmed number of eight switching cycles followed by a latched shutdown.

2) Pulse by pulse current limiting for a programmed number of eight switching cycles followed by hiccup.

The pulse-by-pulse or constant current limiting mechanism is briefly explained below.

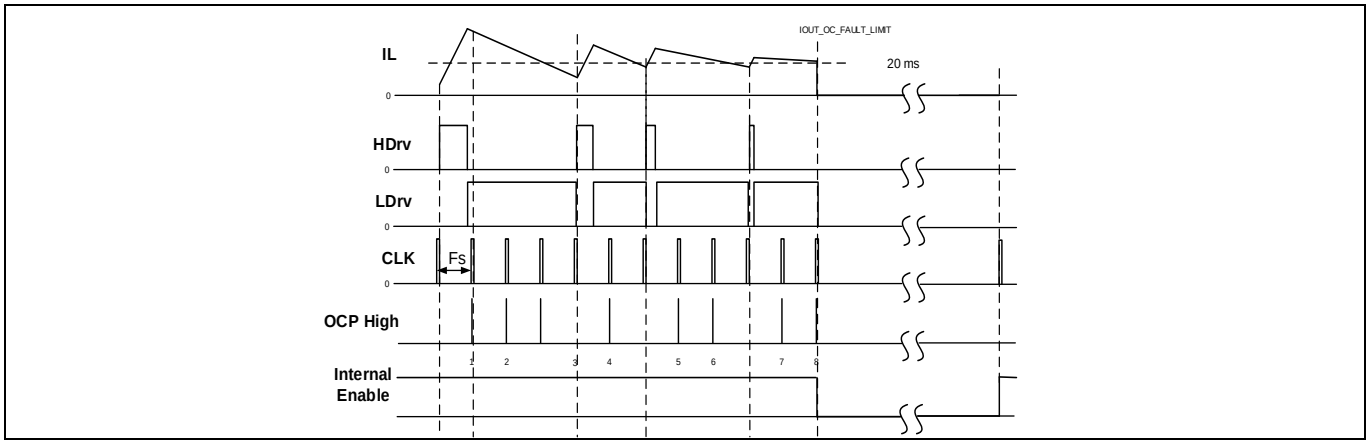


Figure 21 Pulse by pulse current limiting for 8 cycles, followed by hiccup

In Figure 21 above, with the over-current response set to pulse-by-pulse current limiting for 8 cycles followed by hiccup, the converter is operating at D<0.125 when the overcurrent condition occurs. In such a case, no duty cycle limiting is applied.

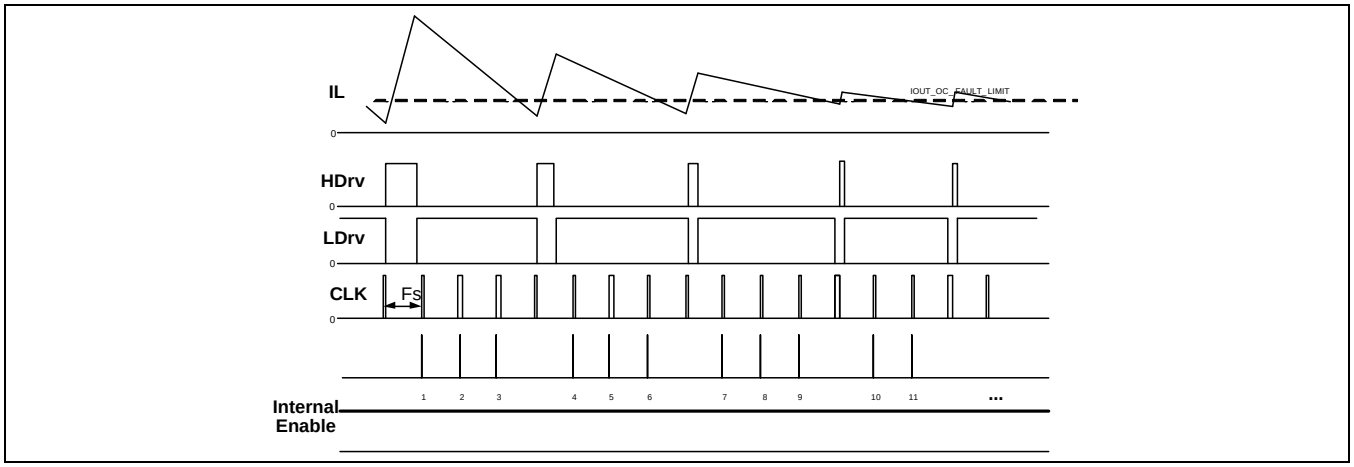


Figure 22 Constant current limiting

Figure 22 depicts a case where the over-current condition happens when the converter is operating at D>0.5 and the over-current response has been set to constant current operation through pulse by pulse current limiting. In such a case, after 3 consecutive over-current cycles are recognized, the pulse width is dropped such that D=0.5 and then after 3 more consecutive OCP cycles, to 0.25 and then finally to 0.125 at which it keeps running until the total OCP count reaches the programmed maximum following which the part enters hiccup mode. Conversely, when the over-current condition disappears, the pulse width is restored to its nominal value gradually, by a similar mechanism in reverse; every sequence of 4 consecutive cycles in which the current is below the over-current threshold doubles the duty cycle, so that D goes from 0.125 to 0.25, then to 0.5 and finally to its nominal value.

14.11 Current reporting limitation at high operating temperature

The IR38164 is designed to give the industry's highest accuracy output current reporting across a range of 0 to 30 Amps. To achieve the goal of highest possible accuracy particularly at Iout up to 30Amps, a high gain was used in the Rds_on current sensing circuit. As the operating temperature increases the Rds_on of the low side MOSFET increases and at the rated current of 30A with junction temperatures around 90 °C, the ADC saturates and no longer reads higher values of the MOSFET RDS_on. The result is that at a high operating junction temperature condition the maximum PMBus™ and SVID current reporting is clamped as shown in Figure 23 below.

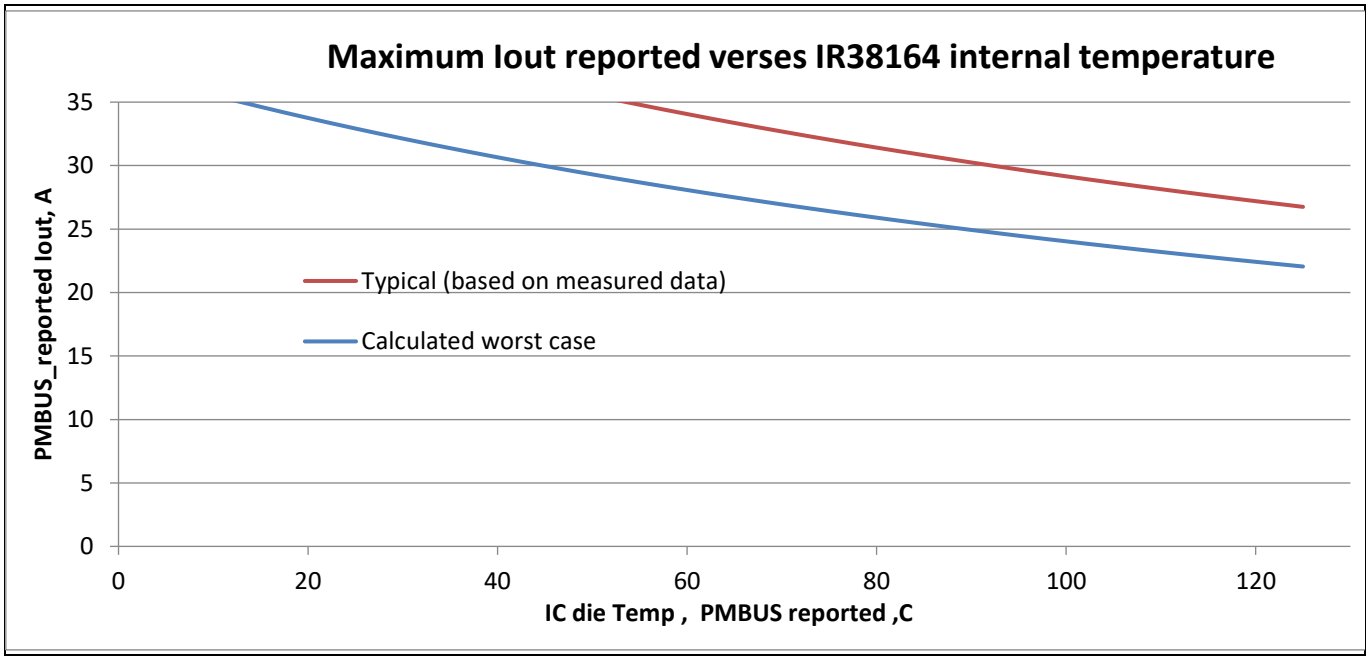


Figure 23 Maximum Iout reported versus IR38164 reported die temperature

Note that Infineon does not recommend operating the part with a reading of the ADC being clamped, because other readings of the ADC can be compromised. If higher Iout readings are needed, the IR38163 with a lower gain in the Rds_on detection circuit is recommended to be used. Lastly, please note that the current limit ability of the IR38164 is not affected by the ADC clamping. The IR38164 current limit function is performed by an analog circuit and does not use the ADC. The OCP warn function (PMBUS setting) is however based on the ADC output and will not function properly at a high temperature if the threshold is set higher than the maximum current reported shown above.

14.12 Die temperature sensing, telemetry and thermal shutdown

On die temperature sensing is used for accurate temperature reporting and over-temperature detection. The READ_TEMEPRATURE PMBus™ command reports this temperature in 10 ^{0}C resolution. The temperature may also be read back using I2C through the 8-bit register *temp_byte*, which reports the die temperature in 1 °C resolution, offset by 40 °C. Thus, the temperature is given by *temp_byte* +40 °C.

The trip threshold is set by default to 125 °C. The default over temperature response of the device is to inhibit power conversion while the fault is present, followed by automatic restart after the fault condition is cleared. Hence, in the default configuration, when the trip threshold is exceeded, the internal Enable signal to the power conversion circuitry is de-asserted, turning off both MOSFETs.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 25 °C hysteresis in the thermal shutdown threshold.

The default over-temperature threshold as well as over-temperature response may be re-configured or overridden using the OT_FAULT_LIMIT and OT_FAULT_RESPONSE PMBus™ commands respectively or the corresponding registers may be used. The devices support three types of responses to an over-temperature fault:

1) Ignore

2) Inhibit when the over-temperature condition exists and auto-restart when the over-temperature condition disappears

3) Latched shutdown.

14.13 Remote voltage sensing

True differential remote sensing in the feedback loop is critical to high current applications where the output voltage across the load may differ from the output voltage measured locally across an output capacitor at the output inductor, and to applications that require die voltage sensing.

The RS+ and RS- pins form the inputs to a remote sense differential amplifier with high speed, low input offset and low input bias current, which ensure accurate voltage sensing and fast transient response in such applications.

The input range for the differential amplifier is limited to 1.5 V below the VCC rail. Therefore, for applications in which the output voltage is more than 2.55 V, it is recommended to use local sensing, or if remote sensing is a must, then the voltage between the RS+ and RS-pins must be divided down to less than 2.55 V using a resistive voltage divider. It's recommended that the divider be placed at the input of the remote sense amplifier and that a low impedance such as 499 Ω be used between the RS+ and RS- nodes. A typical schematic for this setup is shown on Figure 8 Please note, however, that this modifies the open loop transfer function and requires a change in the compensation network to optimally stabilize the loop.

14.14 Feed-forward

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when PVin varies over a wide range. The PWM ramp amplitude (Vramp) is proportionally changed with PVin to maintain PVin/Vramp almost constant throughout PVin variation range (as shown in Figure 24). Thus, the control loop bandwidth and phase margin can be maintained constant. The feed-forward function can also minimize impact on output voltage from fast PVin changes. The feedforward is disabled for PVin<4.7 V. Hence, for PVin<4.7 V, a re-calculation of control loop parameters is needed for re-compensation.

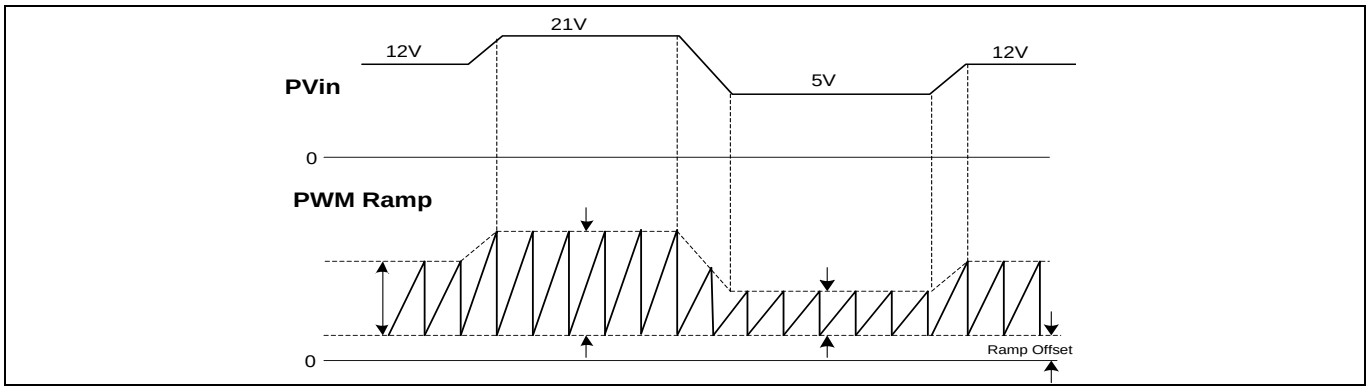


Figure 24 Timing diagram for feed-forward (F.F.) function

14.15 Output voltage sensing, telemetry and faults

For this family of devices, the voltage sense and regulation circuits are decoupled, enabling ease of testing as well as redundancy. In order to do this, the device uses the sense voltage at the dedicated Vsns pin for output voltage reporting (in 1/256 V resolution, using the READ_VOUT PMBus™ command) as well as for power good detection and output over-voltage protection.

Power good detection and output over-voltage detection rely on fast analog comparator circuits, whereas over-voltage warnings as well as under-voltage faults and warnings rely on comparing the digitized Vsns to the corresponding thresholds programmed using PMBus™ commands VOUT_OV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT respectively or the corresponding.

14.16 Power Good Output

The Vsns voltage is an input to the window comparator with programmable thresholds. The PGood signal is high whenever Vsns voltage is within the PGood comparator window thresholds. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. The Power Good thresholds may be changed through the POWER_GOOD_ON and POWER_GOOD_OFF commands, which set the rising and falling PGood thresholds respectively. The thresholds may also be programmed using the corresponding MTP registers. However, when no resistive divider is used, such as for output voltages lower than 2.555 V, the Power Good thresholds must be programmed to within 630 mV of the output voltage, otherwise, the effective power good threshold changes from an absolute threshold to one that tracks the output voltage with a 630 mV offset. By default, the PGood signal will assert as soon as the Vsns signal enters the regulation window. In digital mode, this delay is programmable from 0 to 10 ms with a 1 ms resolution, using the MFR_TPGDLY command.

The threshold is set differently in SVID mode. In this mode, the thresholds set by the POWER_GOOD_ON and POWER_GOOD_OFF commands (or the corresponding registers) are ignored. Power Good is asserted when the output voltage is within the tolerance band of the boot voltage. Following this, the Power Good signal remains asserted irrespective of any output voltage transitions and is de-asserted only in the event of a fault that shuts down power conversion, or, if so programmed, in the event of a command by the CPU to change the output voltage to 0 V.

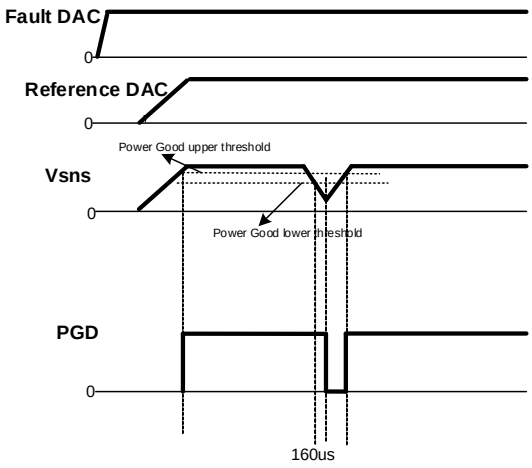


Figure 25 Power good in PMBus™ mode

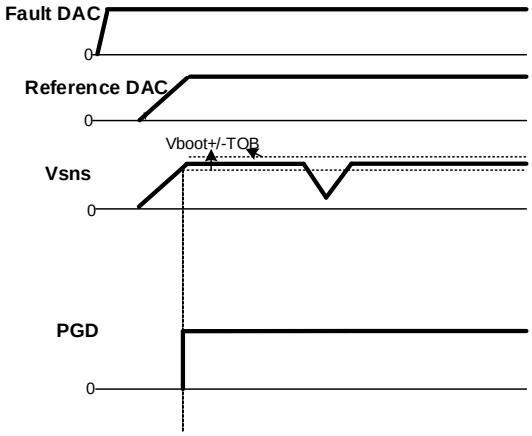


Figure 26 Power Good in SVID mode, Vboot>0 V

14.17 Over-Voltage Protection (OVP)

Over-voltage protection is achieved by comparing sense pin voltage Vsns to a configurable over-voltage threshold.

The OVP threshold may be reprogrammed to within 655 mV of the output voltage (for output voltages lower than 2.555 V, without any resistive divider on the Fb pin), using the VOUT_OV_FAULT_LIMIT PMBus™ command or the corresponding registers. For an OVP threshold programmed to be more than 655 mV greater than the output voltage, the effective OV threshold ceases to be an absolute value and instead tracks the output voltage with a 655 mV offset.

When Vsns exceeds the over-voltage threshold, an over-voltage trip signal asserts after 200 ns (typ.) delay. The default response is that the high side drive signal HDrv is latched off immediately and PGood flags are set low. The low side drive signal is kept on until the Vsns voltage drops below the threshold. HDrv remains latched off until a reset is performed by cycling either Vcc or Enable or the OPERATION command. The device allows the user to reconfigure this response by the use of the VOUT_OV_FAULT_RESPONSE PMBus™ command. In addition to the default response described above, this command can be used to configure the device such that Vout over-voltage faults are ignored and the converter remains enabled. (However, they will still be flagged in the STATUS_REGISTERS and by SAlert). For further details on the corresponding PMBus™ commands related to OVP, please refer to the UN0075 IR3816x PMBus™ commandset user note.

Vsns voltage is set by an external resistive voltage divider connected to the output. This divider ratio must match the divider used on the feedback pin or on the RS+ pin.

It should be noted that the over-voltage threshold applies in PMBus™ mode as well as SVID mode.

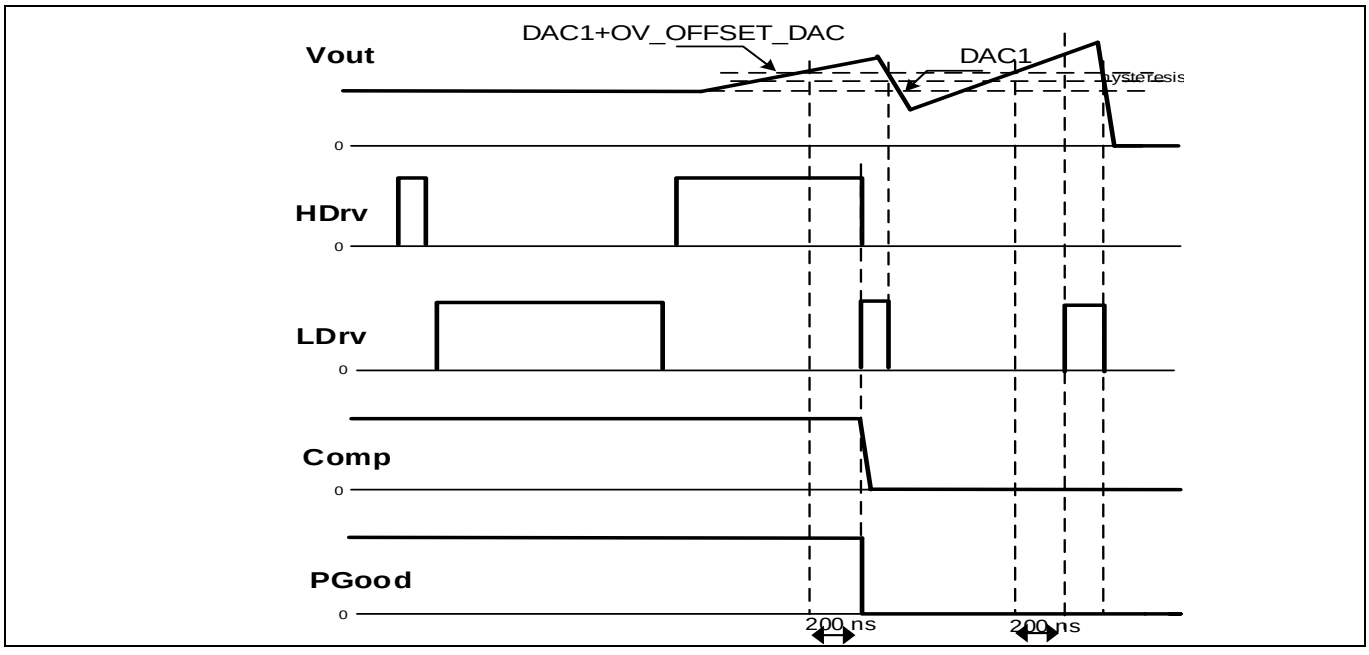


Figure 27 Timing diagram for OVP in non-tracking mode

14.18 Minimum On-Time Considerations

The minimum ON time is the shortest amount of time for the Control FET to be reliably turned on. This is a very critical parameter for low duty cycle, high frequency applications. In the conventional approach, when the error amplifier output is near the bottom of the ramp waveform with which it is compared to generate the PWM output, propagation delays can be high enough to cause pulse skipping, and hence limit the minimum pulse width that can be realized. Moreover, in the conventional approach, the bottom of the ramp often presents a high gain region to the error amplifier output, making the modulator more susceptible to noise and requiring the use of lower control loop bandwidth to prevent noise, jitter and pulse skipping.

Infineon has developed a proprietary scheme to improve and enhance the minimum pulse width which minimizes these delays and hence, allows stable operation with small pulse-widths. At the same time, this scheme also has greater noise immunity, thus allowing stable, jitter free operation down to very low pulse widths even with a high control loop bandwidth, thus reducing the required output capacitance.

Any design or application using this IC must ensure operation with a pulse width that is higher than the minimum on-time and at least 70 ns of on-time is recommended in the application. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{PV_{in} \times F_s} \quad (2)$$

In any application that uses this IC, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \quad (3)$$

$$t_{on(\min)} \le \frac{V_{out}}{PV_{in} \times F_s} \quad (4)$$

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (5)$$

The minimum output voltage is limited by the reference voltage and hence Vout(min) = 0.5 V. Therefore, for Vout(min) = 0.5 V,

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (6)$$

Therefore, at the maximum recommended input voltage of 16V with the minmum recommended frequency of 500 kHz the minimum output voltage should be => 0.56 V. Conversely for operation at a high frequency of 1 MHz and minimum output voltage (0.5 V), the input voltage (PVin) should not exceed 7.1 V, otherwise pulse skipping may happen. Pulse skipping is not an issue except that the ripple maybe slighty higher in this operating mode.

14.19 Maximum Duty Ratio

An upper limit on the operating duty ratio is imposed by the larger of a) fixed off time (dominant at high switching frequencies) b) blanking provided by the PWMSet or clock pulse, which has a pulse width that is 1/8 of the switching period. The latter mechanism is dominant at lower switching frequencies (typically below 1.25 MHz). This upper limit ensures that the Sync FET turns on for a long enough duration to allow recharging the bootstrap capacitor and also allows current sensing. Figure 28 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feed-forward mechanism.

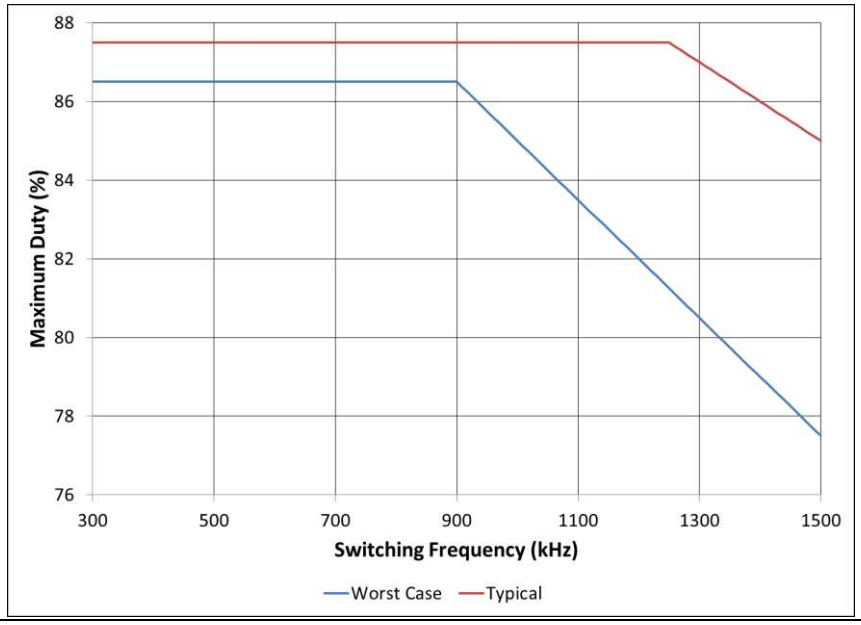


Figure 28 Maximum duty cycle vs. switching frequency with Vin feedforward

14.20 Bootstrap Capacitor

To drive the Control FET, it is necessary to supply a gate voltage at least 4 V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1) as shown in Figure 29. Typically a 0.1 µF capacitor is used. A layout placement for a 0 ohm resistor in series with the capacitor is also recommended. For applications where PVin>14 V, a 1 ohm resistor is required. The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \qquad (7)$$

When the Control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage PVin. However, if the value of C1 is appropriately chosen, the voltage Vc across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong PV_{in} + V_{cc} - V_D \qquad (8)$$

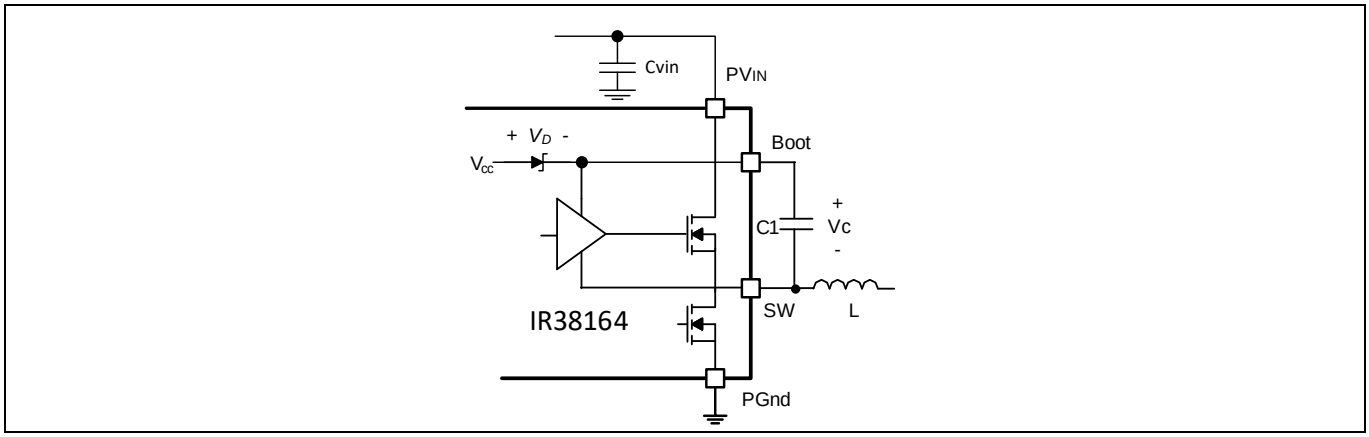


Figure 29 Bootstrap circuit to generate high side drive voltage

14.21 Intel SVID interface

The IR38164 implements a fully compliant Intel® VR 13, and VR 12.5 Serial VID (SVID) interface. This is a three-wire interface between an Intel processor and a VR that consists of clock, data and alert# signals.

The IR38164 implements all the required SVID registers and commands per Intel specifications. For the selected Intel mode, the IC also implements most of the optional commands and registers with very few exceptions.

The default SVID addresses of the devices is 02h. This address can be re-programmed in MTP or via GUI.

14.22 All Call support

All Call for the IR38164 can be configured in the following ways:

- 0E and 0F.
- 0E only.
- 0F only.
- No All Call

The devices can be configured to be used as VR for CPU which is All Call 0F or Memory which is All Call 0E.

14.23 VR12.5 operation

VR 12.5 mode is selectable via MTP bit. The boot voltage in VR 12.5 is also selectable and can be taken from the boot registers. The resolution is programmable via MTP bit to 10 mV to be compatible to VR12.5 mode.

14.24 VR13 operation

VR 13 mode is selectable via MTP bit. The boot voltage in VR13 mode is configured in the boot register. The resolution is programmable via MTP bit to 5 mV or 10 mV, to be compatible to VR13 mode.

14.25 Set Work Point

This family of devices supports SVID Set WP command to Set VID voltage for all rails through all call address. When the processor asserts a Set WP command, all the rails of the VR settle to the corresponding new set voltage encoded in WP registers. Slew rate and power state of all the rails are identical during a set work point operation.

14.26 Dynamic VID slew rate

The device provides the VR designer 16 fast slew rates that govern the rate of VID transitions. The slow slew rate is also programmable as a function of the fast slew rate, and 4 different options are available for each setting of the fast slew rate as shown below in Table 12.

Table 12 Slew Rates

Fast Rate mV/us	x 1/2 Factor	x 1/4 Factor	x 1/8 Factor	x 1/16 Factor
10	5.0	2.50	1.25	0.0625
15	7.5	3.75	1.875	0.94
20	10	5.00	2.50	1.25
25	12.5	6.25	3.125	1.56
30	15	7.5	3.75	1.88
35	17.5	8.75	4.375	2.19
40	20	10	5.0	2.5
45	22.5	11.25	5.625	2.81
50	25	12.5	6.25	3.125
55	27.5	13.75	6.875	3.4375
60	30	15	7.5	3.75
65	32.5	16.25	8.125	4.0625
70	35	17.5	8.75	4.375
80	40	20	10	5

14.27 Loop compensation

Feedback loop compensation is achieved using standard Type III techniques and the compensation values can be easily calculated using Infineon's design tool. The design tool can also be used to predict the control bandwidth and phase margin for the loop for any set of user defined compensation component values. For a theoretical understanding of the calculations used, please refer to Infineon's Application Note AN-1162 "Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier".

14.28 Dynamic VID compensation

This family of devices uses an analog control scheme with voltage mode control. In this scheme, the compensator acts on the Vout signal and not just on the error signal. For load and line transients, with a steady and unchanging reference voltage, this has the same dynamic characteristics as for a compensator that acts on only the error signal. However, for reference voltage changes, as in the case of Dynamic VID, the dynamics are altered. A proprietary dynamic VID compensation scheme allows the dynamic VID response to be tuned optimally to the feedback compensator values. Once properly optimized, the output voltage will follow the DAC more closely during a positive dynamic VID, and provide better dynamic VID alert timing, as required by Intel® processors. Infineon's SupIRBuck design tool will allow the user to quickly and conveniently calculate the dynamic VID compensation parameters for optimal dynamic VID response.

15 I2C and PMBus™ communication protocols

15.1 I2C Protocols

All registers may be accessed using either I2C or PMBus™ protocols. I2C allows the use of a simple format whereas PMBus™ provides error checking capability. Figure 30 shows the I2C format employed by IC.

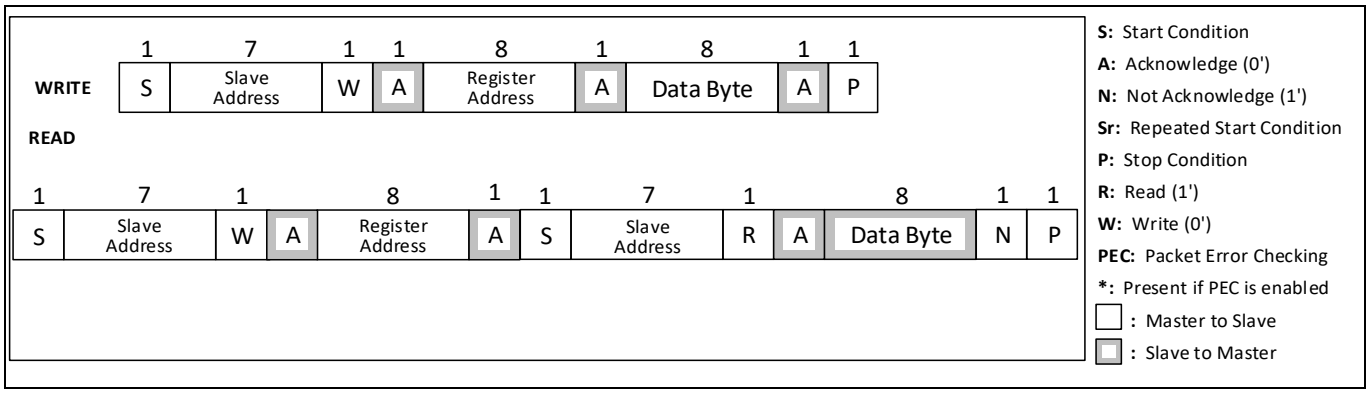


Figure 30 I2C format

15.2 SMBus/PMBus™ protocols

To access IR's configuration and monitoring registers, 4 different protocols are required:

- the SMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
- the SMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the SMBus Block Read protocol for accessing Model and Revision information
- the SMBus Process call (for accessing Configuration Registers)

In addition, IC supports:

- Alert Response Address (ARA)
- Bus timeout
- Group Command for writing to many VRs within one command

These various commands are illustrated in Figure 31 through Figure 37 below.

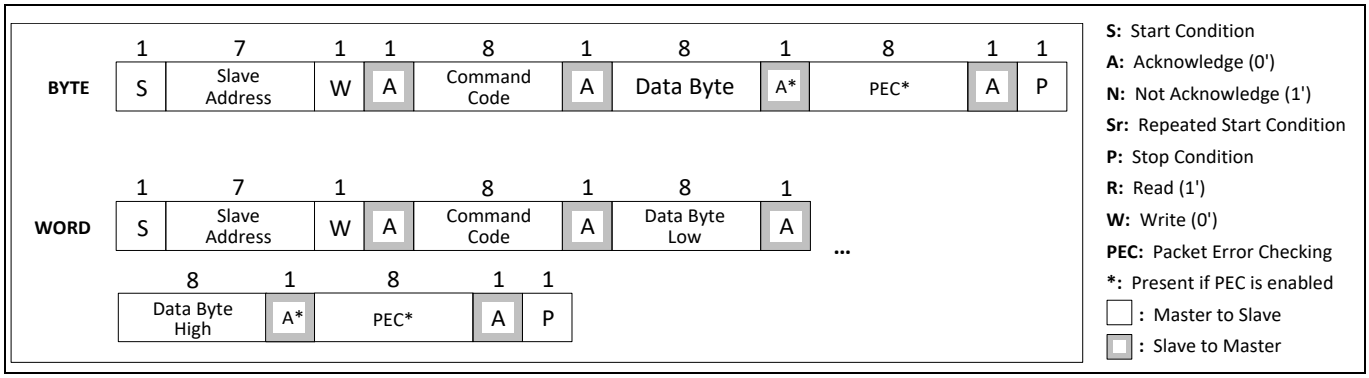


Figure 31 SMBus write byte/word

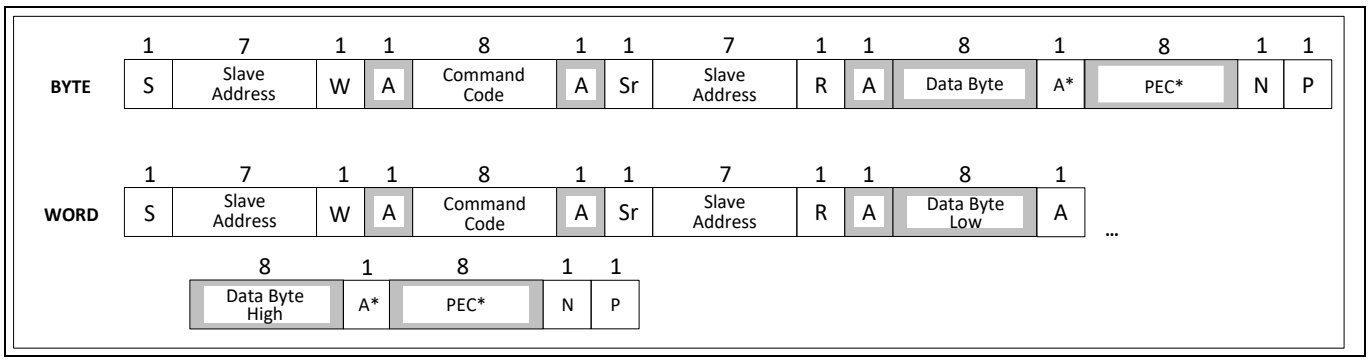


Figure 32 SMbus read byte/word

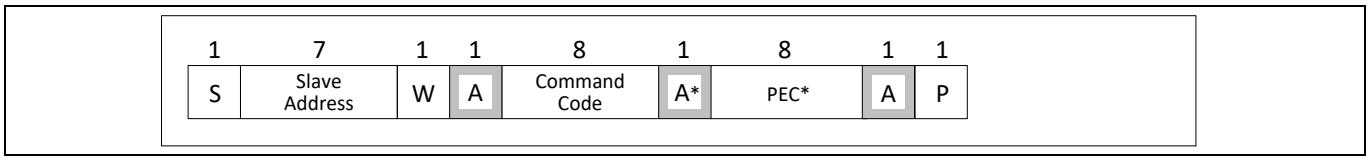


Figure 33 SMBus send byte

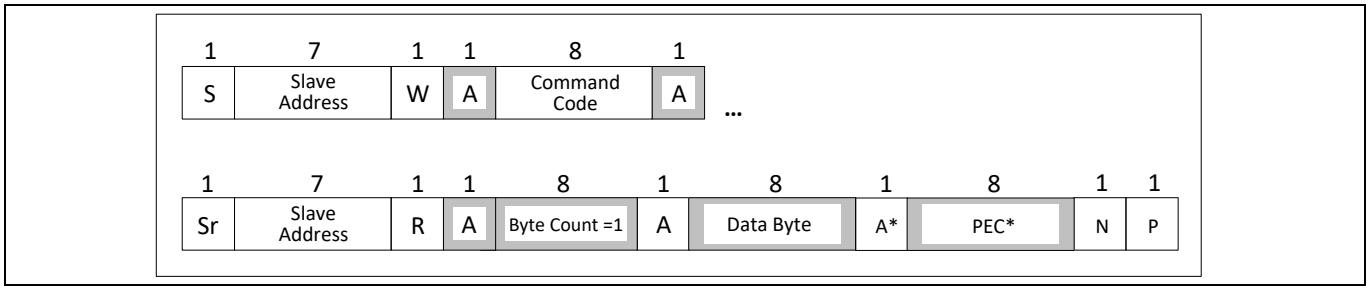


Figure 34 SMBus block read with byte count = 1

Figure 35 MFR specific command to write an internal register

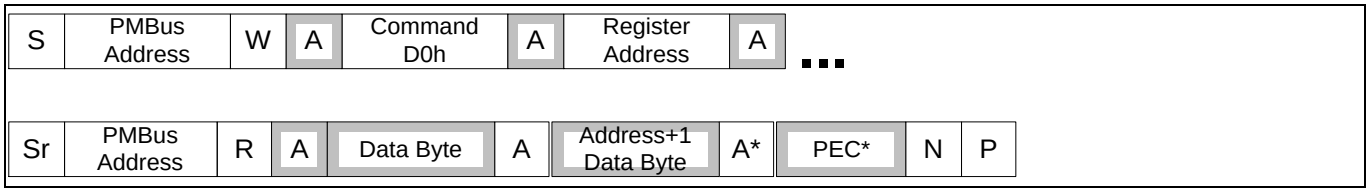


Figure 36 SMBus custom protocol call to read an internal register

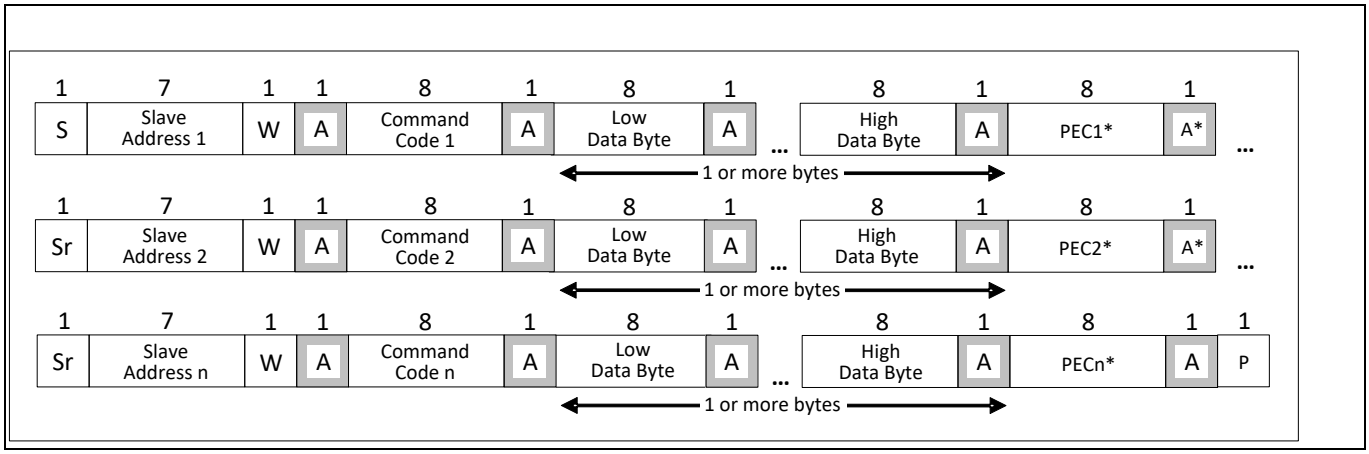


Figure 37 Group command

15.3 Supported PMBus™ commands

Table 13

Command Code	Command Name	SMBus transaction	No. of bytes	Range	Resolution	Default Value	Description
01h	OPERATION	R/W Byte	1				Enables or disables the device and controls margining
02h	ON_OFF_CONFIG	R/W Byte	1				Configures the combination of Enable pin input and serial bus commands needed to turn the unit on and off.
03h	CLEAR_FAULTS	Send Byte	0				Clear contents of Fault registers
10h	WRITE_PROTECT	R/W Byte	1				Used to control writing to the PMBus™ device. The intent of this command is to provide protection against accidental changes.
15h	STORE_USER_ALL	Send Byte	0				Burns the User section registers into OTP memory
16h	RESTORE_USER_ALL	Send Byte	0				Copies the OTP registers into User memory
19h	CAPABILITY	Read Byte	1				Returns 1011xxxx to indicate Packet Error Checking is supported, maximum bus speed is 400 kHz and SMBAlert# is supported.
1Bh	SMBALERT_MASK	Write word/Block read Process call	2				May be used to prevent a warning or fault condition from asserting the SMBALERT# signal.
21h	VOUT_COMMAND[16]	R/W Word	2	0-2.555V/V_S	5mV/V_S	1V	Causes the device to set its output voltage to the commanded value. V_S= VOUT_SCALE_LOOP
22h	VOUT_TRIM[16]	R/W Word	2	-128-+128V		0V	Available to the device user to trim the output voltage
24h	VOUT_MAX[16]	R/W Word	2			2V	Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations.
25h	VOUT_MARGIN_HIGH[16]	R/W Word	2	0-2.555V/V_S	5mV/V_S		Sets the MARGIN high voltage when commanded by OPERATION V_S= VOUT_SCALE_LOOP
26h	VOUT_MARGIN_LOW[16]	R/W Word	2	0-2.555V/V_S	5mV/V_S		Sets the MARGIN low voltage when commanded by OPERATION V_L= VOUT_SCALE_LOOP
27h	VOUT_TRANSITION_RATE[11]	R/W Word	2	0-63.9mV/us	0.0625mV/us	0.0625mV/us	Sets the rate in mV/µs at which the output should change voltage. Exponent 0 to -4 allowed.
29h	VOUT_SCALE_LOOP[11]	R/W Word	2	0.125-1		1	Compensates for external resistor divider in feedback path and in the sense path. Values 1, 0.5, 0.25, 0.125 allowed. Exponent -3 allowed.
33h	FREQUENCY_SWITCH[11]	R/W Word	2	504-1500kHz		978kHz	Sets the switching frequency, in kHz. Exponent 0 to 1 allowed.
35h	VIN_ON[11]	R/W Word	2	0-16.5V	0.5V	8.0V	Sets the value of the input voltage, in volts, at which the unit should start power conversion. Exponent -1 allowed.
36h	VIN_OFF[11]	R/W Word	2	0-16V	0.5V	7.0V	Sets the value of the input voltage, in volts, at which the unit, once operation has started, should stop power conversion. Exponent -1 allowed.
39h	IOUT_CAL_OFFSET[11]	R/W Word	2	-128A-+127.5A	0.25A	0A	Used to null out any offsets in the output current sensing circuit. Exponent -2 allowed.
40h	VOUT_OV_FAULT_LIMIT[16]	R/W Word	2	(25-655mV)/V_S	10mV/V_S	2.102V	Sets the value of the output voltage measured at the sense pin that causes an output over-voltage fault. V_S= VOUT_SCALE_LOOP
41h	VOUT_OV_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Shutdown	Instructs the device on what action to take in response to an output over-voltage fault. Ignore =0x00h, Shutdown = 0x80h.
42h	VOUT_OV_WARN_LIMIT[16]	R/W Word	2		3.9mV	1.902V	Sets the value of the output voltage at the sense pin that causes an output voltage high warning.
43h	VOUT_UV_WARN_LIMIT[16]	R/W Word	2		3.9mV	0.902V	Sets the value of the output voltage at the sense pin that causes an output voltage low warning.

Command Code	Command Name	SMBus transaction	No. of bytes	Range	Resolution	Default Value	Description
44h	VOUT_UV_FAULT_LIMIT[16]	R/W Word	2		3.9mV	0.898V	Sets the value of the output voltage at the sense pin that causes an output under-voltage fault.
45h	VOUT_UV_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Ignore	Instructs the device on what action to take in response to an output under-voltage fault.
46h	IOUT_OC_FAULT_LIMIT[11]	R/W Word	2	3-40A	0.5A	40A	Sets the value of I_{Limit} (valley), allowing user to set the output current in amperes, that causes the over-current detector to indicate an over-current fault. Exponent -1 allowed.
47h	IOUT_OC_FAULT_RESPONSE	R/W Byte	1			Pulse by pulse for 8 cycles followed by hiccup, retry after 20 ms	Instructs the device on what action to take in response to an output over-current fault.
4Ah	IOUT_OC_WARN_LIMIT[11]	R/W Word	2	0-63.5A	0.5A	35A	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. Exponent -1 allowed.
4Fh	OT_FAULT_LIMIT[11]	R/W Word	2	0-150°C	1°C	125°C	Set the temperature, in degrees Celsius, of the unit at which it should indicate an over-temperature fault. Exponent 0 allowed.
50h	OT_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown/ Auto-start		Auto-start	Instructs the device on what action to take in response to an over-temperature fault.
51h	OT_WARN_LIMIT[11]	R/W Word	2	0-150°C	1°C	100°C	Set the temperature, in degrees Celsius, of the unit at which it should indicate an over-temperature warning alarm. Exponent 0 allowed.
55h	VIN_OV_FAULT_LIMIT[11]	R/W Word	2	6.25V-24V	0.25V	15V	Sets the value of the input voltage that causes an input over-voltage fault. Exponent -2 allowed.
56h	VIN_OV_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Ignore	Instructs the device on what action to take in response to an input over-voltage fault.
58h	VIN_UV_WARN_LIMIT[11]	R/W Word	2	0-16V	0.5V	7.5V	Sets the value of the input voltage PVin, in volts, that causes an input over-voltage fault. Exponent -1 allowed.
5Eh	POWER_GOOD_ON[16]	R/W Word	2	(0-0.63V)/V_S	10mV/V_S	0.5V	Sets the output voltage at which an optional POWER_GOOD signal should be asserted. V_S=VOUT_SCALE_LOOP
5Fh	POWER_GOOD_OFF[16]	R/W Word	2	(0-0.63V)/V_S	10mV/V_S	0.25V	Sets the output voltage at which an optional POWER_GOOD signal should be negated. V_S=VOUT_SCALE_LOOP
60h	TON_DELAY[11]	R/W Word	2	0-127ms	1ms	0ms	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Exponent 0 allowed.
61h	TON_RISE[11]	R/W Word	2	0-127ms	1ms	1ms	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exponent 0 allowed.
62h	TON_MAX_FAULT_LIMIT[11]	R/W Word	2	0-127ms	1ms	0 (Disabled)	Sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output under-voltage fault limit. Exponent 0 allowed.
63h	TON_MAX_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Ignore	Instructs the device on what action to take in response to a TON_MAX fault.
64h	TOFF_DELAY	R/W Word	2	0-127ms	1ms	0ms	Sets the time, in milliseconds, from a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exponent 0 allowed.
65h	TOFF_FALL	R/W Word	2	0-127ms	1ms	1ms	Sets the time, in milliseconds, in which the reference voltage ramps down to zero (If a soft off is allowed by the configuration of the ON_OFF_CONFIG command). Exponent 0 allowed.
78h	STATUS BYTE	Read Byte	1				Returns 1 byte where the bit meanings are: Bit <7> device busy fault

Command Code	Command Name	SMBus transaction	No. of bytes	Range	Resolution	Default Value	Description
							Bit <6> output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input under-voltage fault Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: None of the above
79h	STATUS WORD	Read Word	2				Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> Reserved; hardcoded to 0 Bit <3> Output power not good Bit <2:0> Hardcoded to 0
7Ah	STATUS_VOUT	Read Byte	1				Reports types of VOUT related faults.
7Bh	STATUS_IOUT	Read Byte	1				Reports types of IOUT related faults.
7Ch	STATUS_INPUT	Read Byte	1				Reports types of INPUT related faults.
7Dh	STATUS_TEMPERATURE	Read Byte	1				Returns over- temperature warning and over-temperature fault (OTP level). Does not report under-temperature warning/fault. The bit meanings are: Bit <7> Over-Temperature Fault Bit <6> Over-Temperature Warning Bit <5> Under-Temperature Warning Bit <4> Under-Temperature Fault Bit <3:0> Reserved
7Eh	STATUS_CML	Read Byte	1				Returns 1 byte where the bit meanings are: Bit <7> Command not Supported Bit <6> Invalid data Bit <5> PEC fault Bit <4> OTP fault Bit <3:2> Reserved Bit<1> Other communication fault Bit<0> Other memory or logic fault; hardcoded to 0
88h	READ_VIN[11]	Read Word	2				Returns the input voltage in volts
8Bh	READ_VOUT[16]	Read Word	2				Returns the output voltage in volts
8Ch	READ_IOUT[11]	Read Word	2				Returns the output current in amperes
8Dh	READ_TEMPERATURE[11]	Read Word	2				Returns the device temperature in degrees Celsius
96h	READ_POUT[11]	Read Word	2				Returns the output power in watts
98h	PMBUS™_REVISION	Read Byte	1				Reports PMBus™ Part I rev 1.2 & PMBus™ Part II rev 1.2
99h	MFR_ID	Block Read/Write	2			IR	Returns 2 bytes used to read the manufacturer's ID. User can overwrite with any value.
9Ah	MFR_MODEL	Block Read/Write	3			Set 000000	If set to 000000h, returns a 1 byte code corresponding to IC_DEVICE_ID. Alternatively, user can set to any non-zero value
9Bh	MFR_REVISION	Block Read/Write	3			Set 000000	If set to 000000h, returns a 1 byte code corresponding to IC_DEVICE_REV. Alternatively, user can set to any non-zero value
ADh	IC_DEVICE_ID	Block Read	2				Used to read the type or part number of an IC. IR38164: 6Dh
AEh	IC_DEVICE_REV	Block Read	1				Used to read the revision of the IC

Command Code	Command Name	SMBus transaction	No. of bytes	Range	Resolution	Default Value	Description
D0h	MFR_READ_REG	Custom	2				Manufacturer Specific: Read from configuration registers
D1h	MFR_WRITE_REG	Write Word	2				Manufacturer Specific: Write to configuration & status registers
D8h	MFR_TPGDLY	R/W Word	2	0-10ms	1ms	0ms	Sets the delay in milliseconds, between the output voltage entering the regulation window and the assertion of the PGood signal. Exponent 0 allowed.
D9h	MFR_FCCM	R/W Byte	1	0-1		CCM	Allows the user to choose between forced continuous conduction mode and adaptive on-time operation at light load.
D6h	MFR_I2C_address	R/W Word	1	0-7Fh		10h	Sets and returns the device I2C base address
DBh	MFR_VOUT_PEAK[16]	Read Word	2				Continuously records and reports the highest value of Read Vout.
DCh	MFR_IOUT_PEAK[11]	Read Word	2				Continuously records and reports the highest value of Read Iout.
DDh	MFR_TEMPERATURE_PEAK[11]	Read Word	2				Continuously records and reports the highest value of Read_Temperature

Notes

[11] Uses LINEAR11 format

[16] Uses LINEAR16 format with exponent set to-8

16 PCB footprint and layout recommendations

16.1 Layout recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components on the top layer with wide, copper filled areas or shapes. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The input capacitors, inductor, output capacitors and the IR38164 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR38164. The feedback part of the system should be kept away from the inductor and other noise sources. The critical bypass components such as capacitors for Vin, Vcc, and 1.8 V should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB, use one layer as a power ground plane and have a control circuit ground (analog ground) to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control functions. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

IR38164 has three pins, SCL, SDA and SALERT# that are used for I2C/PMBus™ communication. It is recommended that the traces used for these communication lines be at least 10 mils wide with spacing between the SCL and SDA traces that is at least 2-3 times the trace width. Follow the Intel® recommended PCB routing techniques for the SVID interface.

The Power QFN is a thermally enhanced package. To effectively remove heat from the device, the exposed pad should be connected to the ground planes using multiple vias.

As shown in the PCB layout:

- Allow enough copper for PVin, GND and Vout
- All bypass capacitors are placed as close as possible to their connecting pins
- Components for loop compensation are placed as close as possible to the COMP pin
- AGND is connected to the inner PGND plane through via holes
- Resistor Rt is placed as close as possible to the Rt pin
- SW node copper should only be routed on the top layer to minimize switching noises
- Fb and Vsns trace routing are kept away from SW node
- Thermal via holes are placed on PVIN and PGND pads to aid thermal dissipation

16.2 PCB Metal and Component Placement

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to “SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.” (AN1132).

All dimensions in the following figures are in mm.

The PCB pads and component footprint are shown in Figure 38.

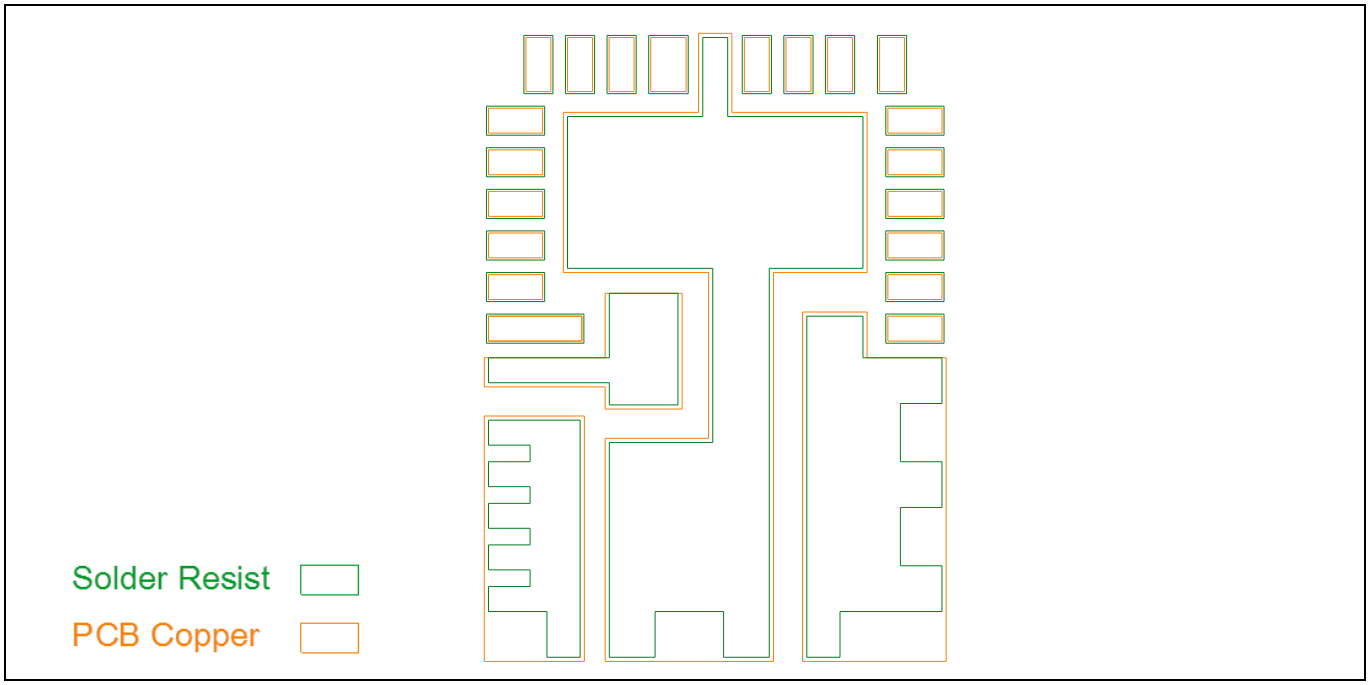


Figure 38 PCB pads and component

16.3 PCB copper and solder resist

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.

When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment (i.e. 0.1 mm in X & Y).

For smaller signal type leads around the edge of the device, Infineon recommends that these are Non Solder Mask Defined (NSMD) or Copper Defined.

When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025 mm on each edge, (i.e. 0.05 mm in X&Y,) in order to accommodate any layer to layer misalignment.

Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

Recommendations are shown in Figure 39 and Figure 40.

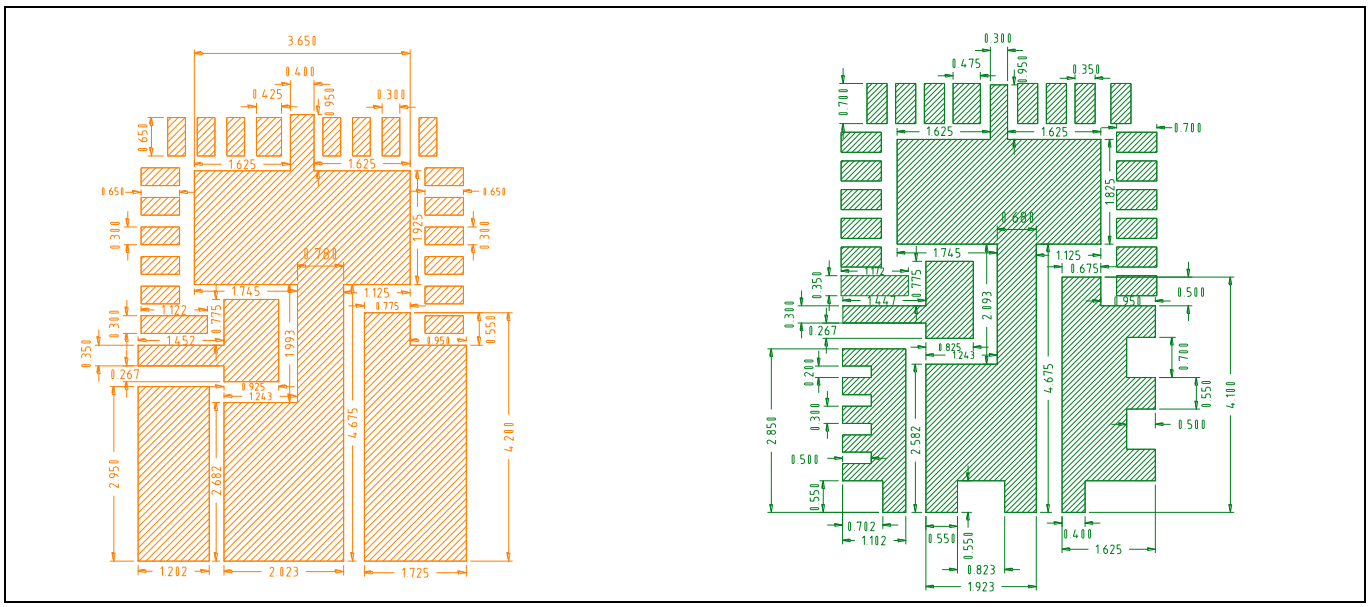


Figure 39 PCB copper and solder resist (pad sizes)

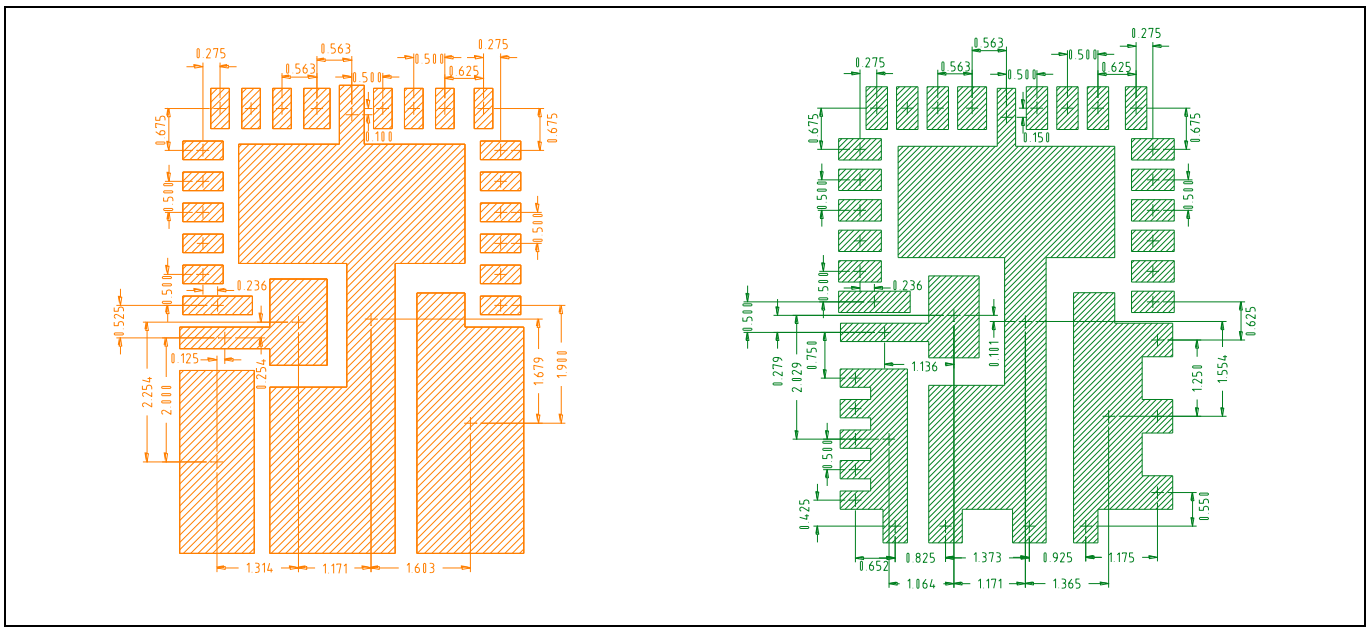


Figure 40 PCB copper and solder resist (pad spacing)

16.4 PCB solder paste stencil

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results.

A recommended stencil design is shown in Figure 41 and Figure 42. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

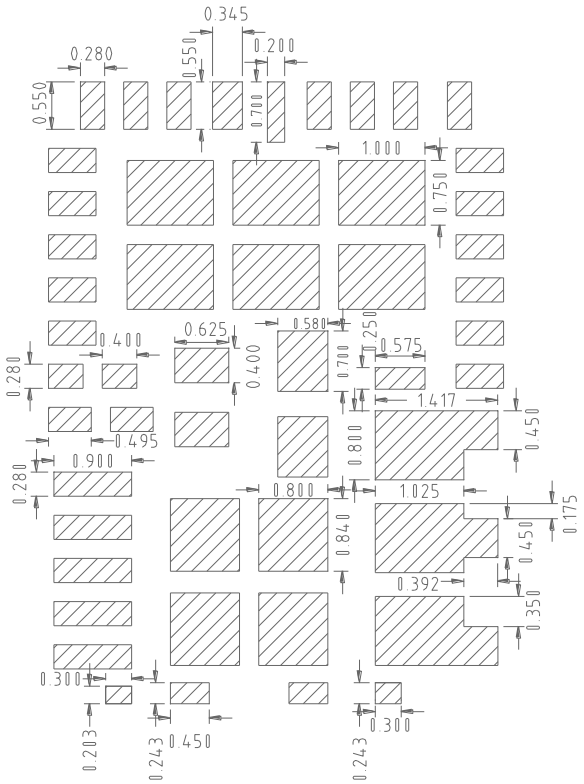


Figure 41 Solder paste stencil (pad sizes)

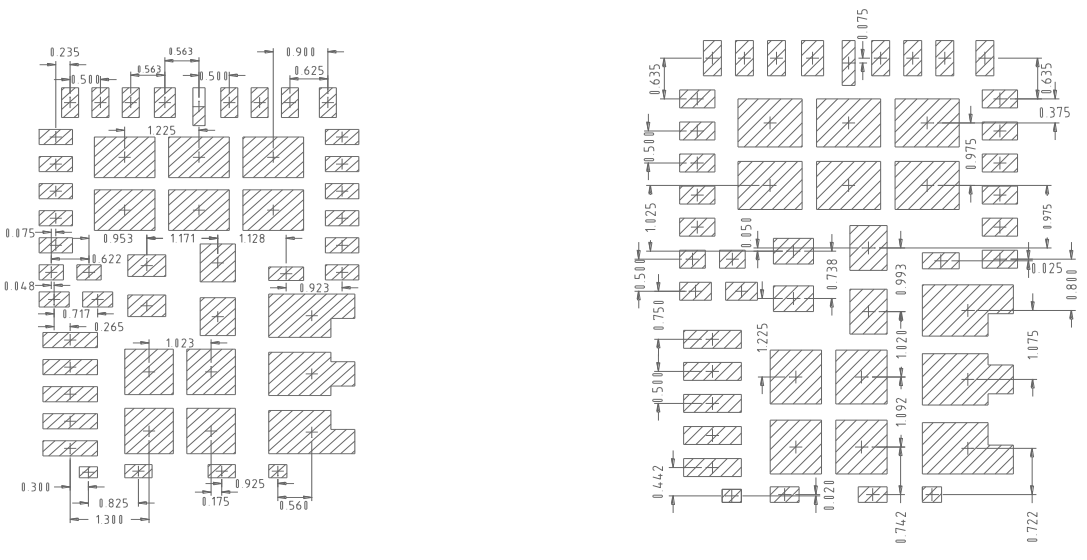


Figure 42 Solder paste stencil (pad spacing)

17 Marking and package information

17.1 Final production marking

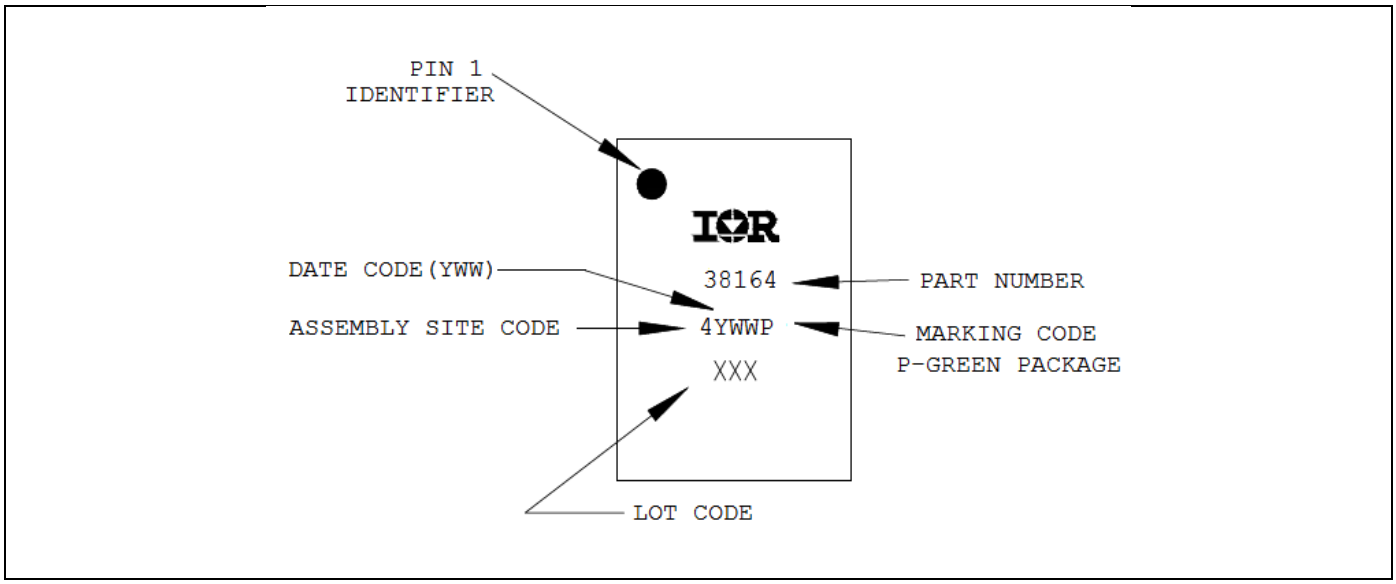


Figure 43 Package marking

17.2 Early production marking

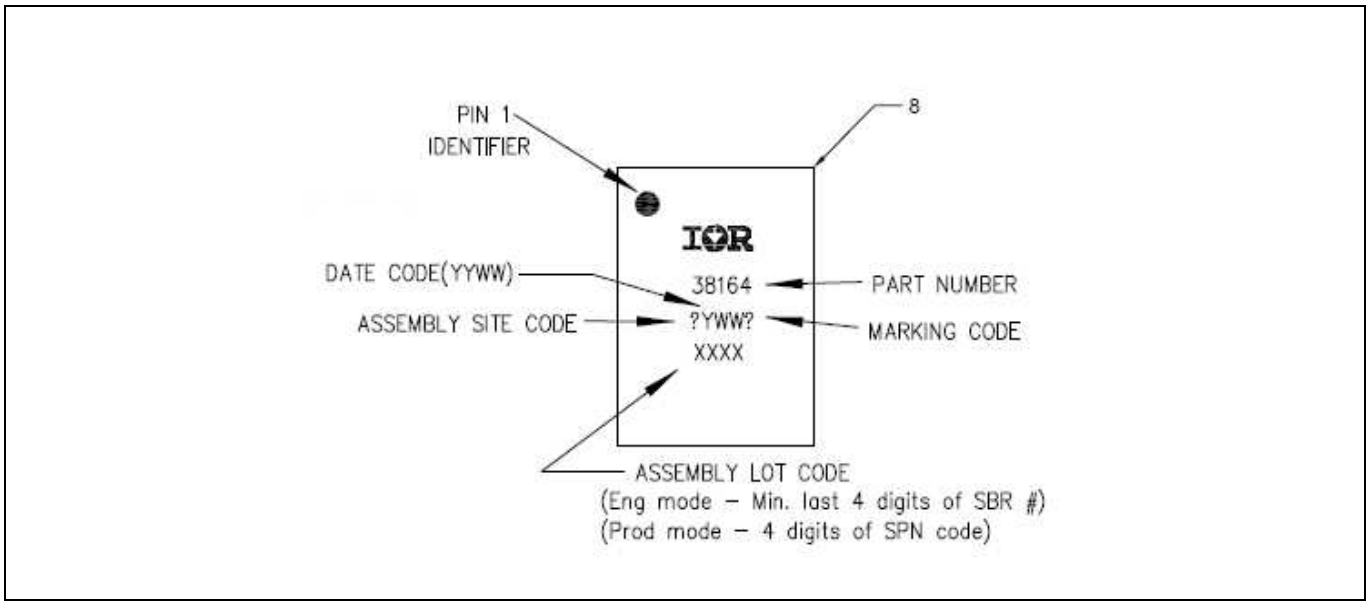


Figure 44 Package marking

17.3 Package dimensions

Package dimensions are shown in Figure 45 through Figure 47.

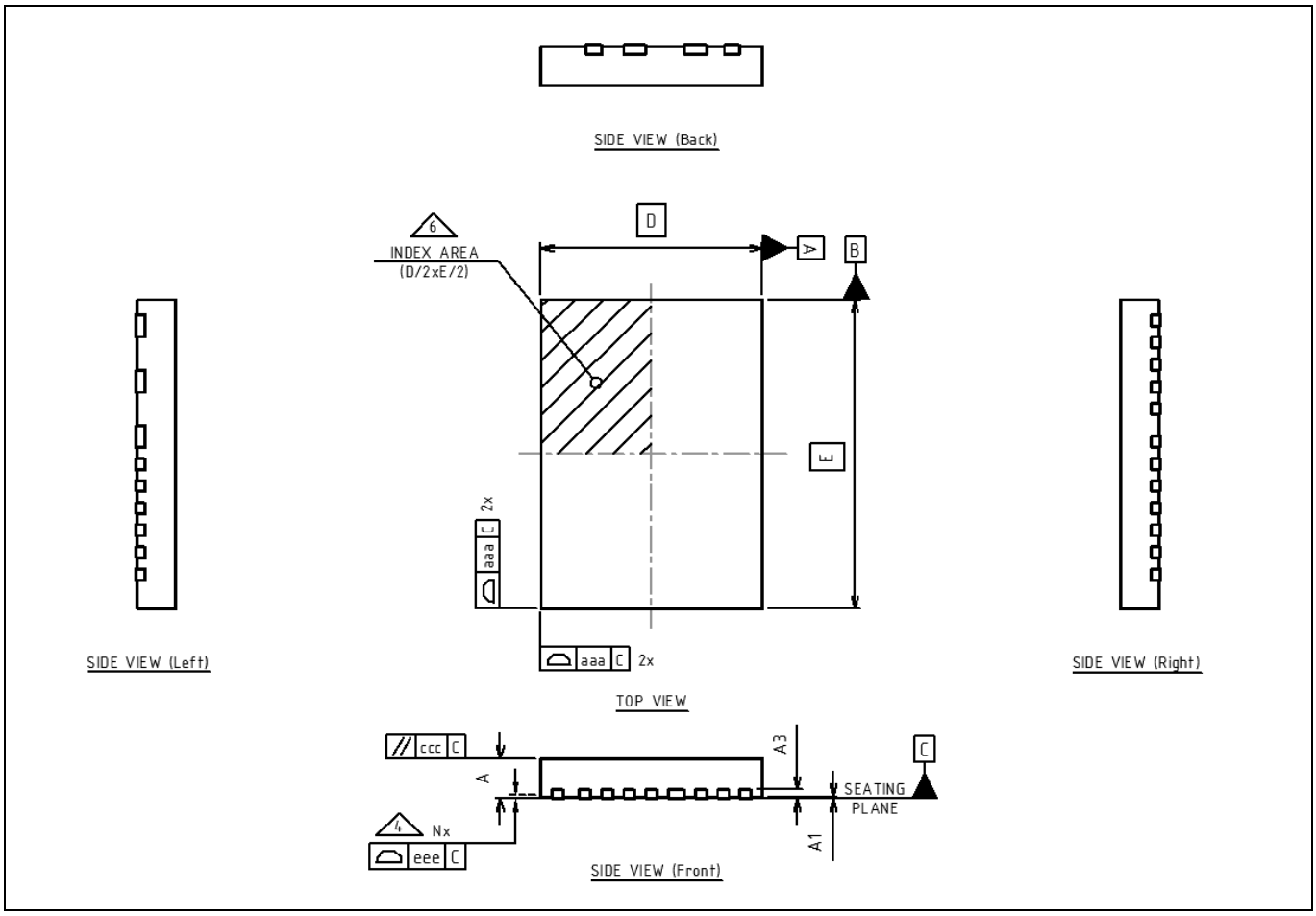
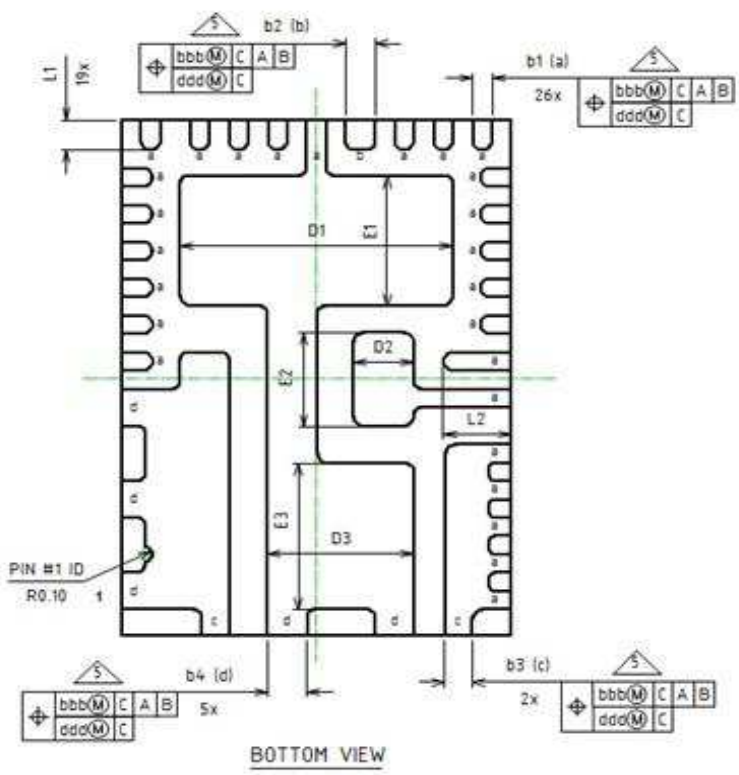


Figure 45 Package dimensions



Dimension Table				
Symbol \ Thickness	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b1	0.20	0.25	0.30	5
b2	0.325	0.375	0.425	5
b3	0.30	0.35	0.40	5
b4	0.45	0.50	0.55	5
D	5.00 BSC			
E	7.00 BSC			
D1	3.35	3.50	3.60	
E1	1.625	1.775	1.875	
D2	0.625	0.775	0.875	
E2	1.14	1.29	1.39	
D3	1.723	1.873	1.973	
E3	1.832	1.982	2.082	
L1	0.30	0.40	0.50	
L2	0.772	0.872	0.972	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	34			3
NOTES	1, 2			
LF PART NO	443297			

Figure 46 Package dimensions

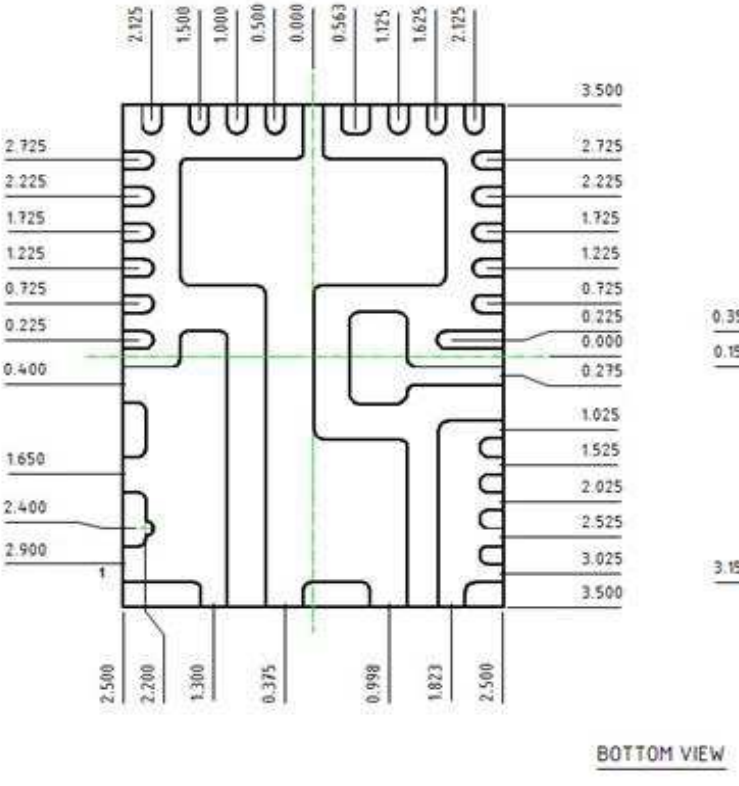


Figure 47 Package dimensions

18 Environmental Qualifications

Table 14

Qualification Level		**Industrial**	
Moisture Sensitivity		5mm x 7mm PQFN	MSL 2 260C
ESD	Human Body Model (JESD22-A114-F)	JEDEC Class 1C	
	Charged Device Model (JESD22-C101-F)	JEDEC Class 3	
RoHS Compliant		Yes (with Exemption 7a)	

19 References

[1] UN7005 IR3816x_ PMBus™ Command Set

[2] Application Note AN-1162. Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier.

[3] Application Note AN-1132. SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.

Revision History

IR38164

Revision: 2019-03-25, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
1.0	2018-01-23	Release of preliminary version
1.1	2018-02-13	Updated OCP limit.
2.0	2018-05-23	Release of final version
2.1	2018-09-26	Updated package drawings.
2.2	2019-03-25	Current reporting limation and corrected PMBUS spec revision.

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