

**Features**

- 2 channel integrated analog input Class D audio amplifier in a small 7 x 7 mm PQFN44 package
- No mechanical heatsink required
- High peak music power output
- Split or single power supply
- Differential or single-ended input
- Over-current, over-temperature and under voltage protections with self-reset feature
- Start/stop click noise reduction
- Clip and Fault reporting outputs
- High noise immunity
- RoHS compliant

**Typical Applications**

- Home theatre systems
- Docking station audio systems
- PC audio systems
- Musical instruments
- Karaoke amplifiers
- Game consoles
- Powered speaker systems
- General purpose audio power amplifiers

**Product Summary**

Topology	Half-Bridge, Full-Bridge
IR4302 Output power (Typical, THD+N=10%)	130 W / 4 Ω
	100 W / 3 Ω
IR4322 Output power (Typical, THD+N=10%)	100 W / 4 Ω
	100 W / 2 Ω
IR4312 Output power (Typical, THD+N=10%)	35 W / 4 Ω
	40 W / 3 Ω
*Residual noise (AES-17, IHF-A, typical)	250 μVrms
*THD+N (1kHz, 1W, 4 Ω, typical)	0.02 %

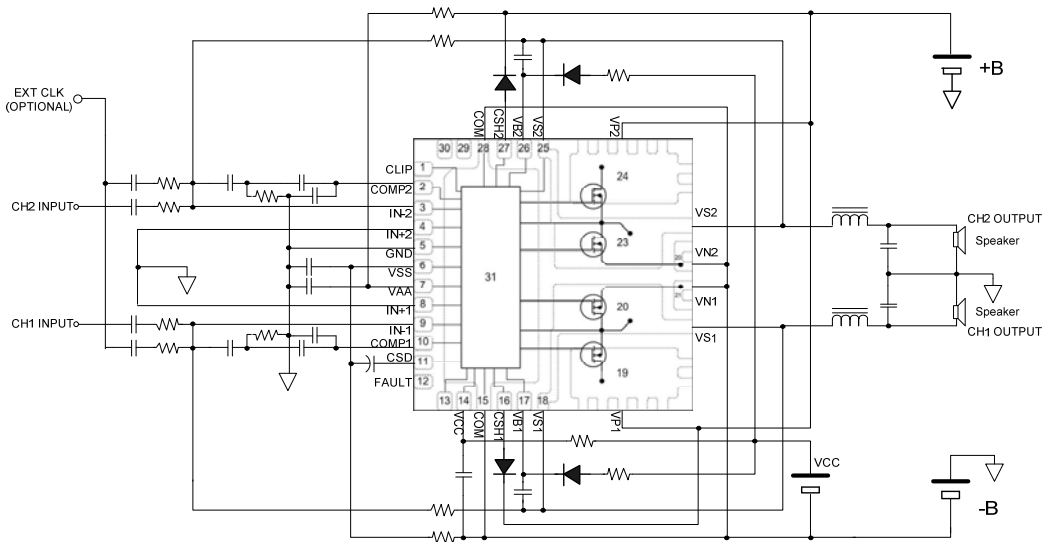
\* In typical application example

**Package**



7x7mm PQFN44L

**Typical Connection**



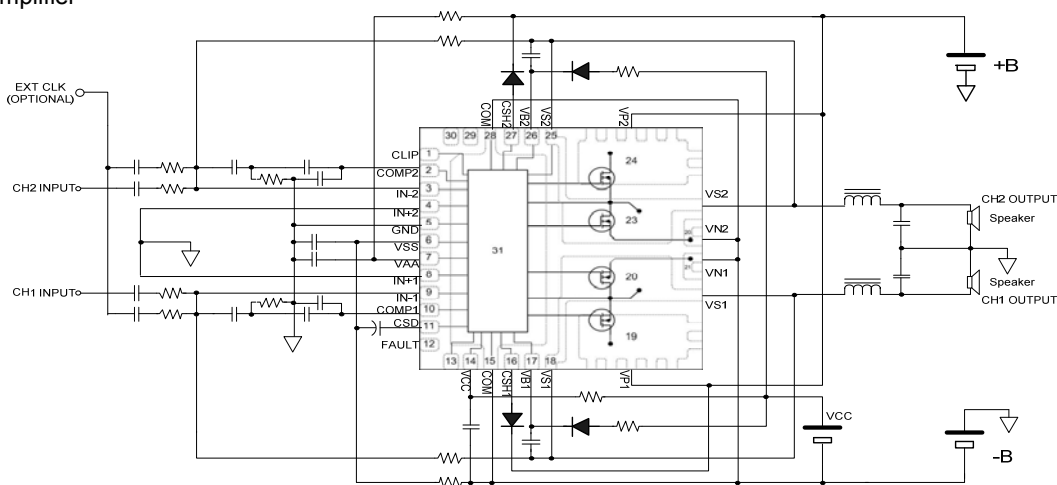
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## Description

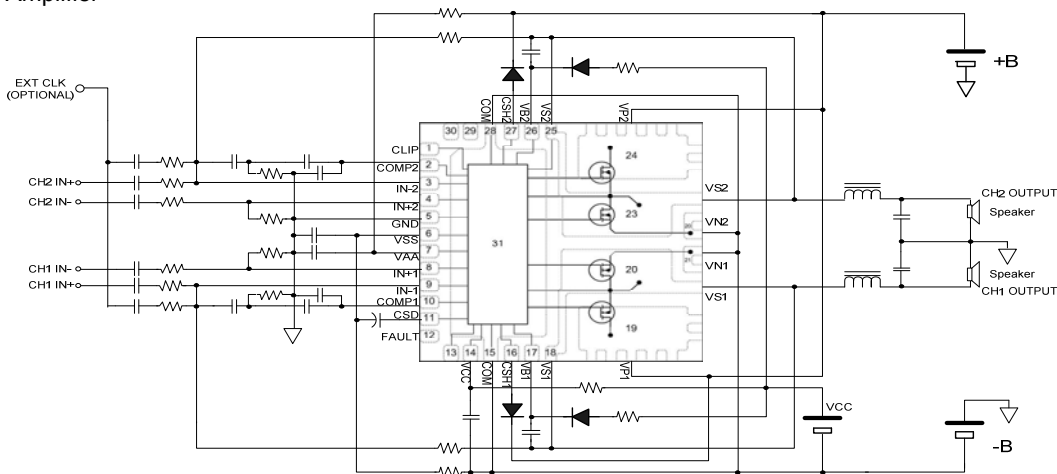
The IR43x2 integrates 2 channel PWM controller and digital audio MOSFETs forming a high performance Class D audio amplifier. As a result of fully optimized MOSFETs co-packed with a dedicated controller IC, the IR43X2 operates without mechanical heatsink attached in a typical music playback usage. High voltage ratings and noise immunity in the controller IC ensures reliable operation over various environmental conditions. A small 7x7 mm PQFN package enhances the benefit of smaller size of Class D topology. The IR43X2 series is a lead-free, ROHS compliant.

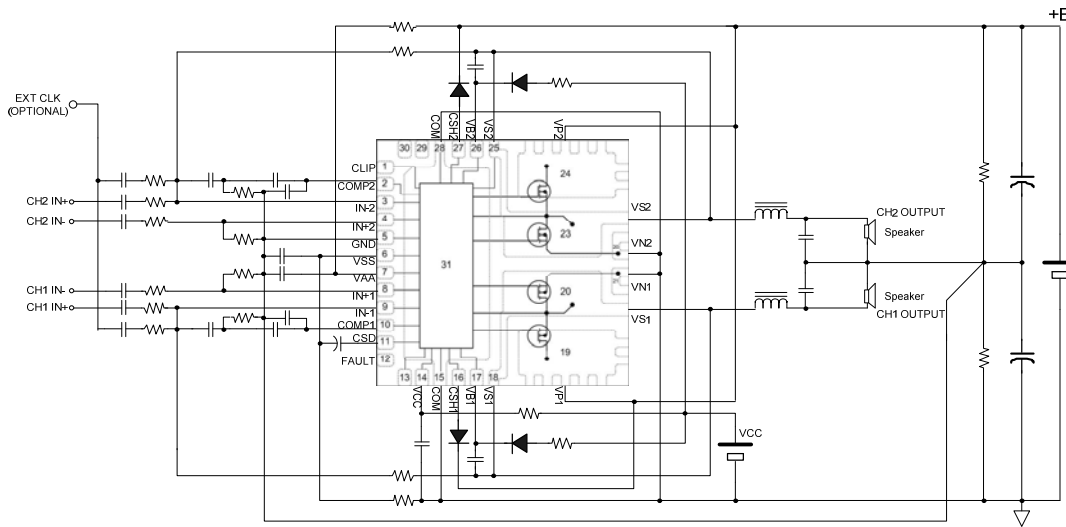
## Typical Connection Diagram

### 1. Inverting Amplifier



### 2. Differential Amplifier



**3. Single Power Supply (Inverting Amplifier)**

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup>	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>		MSL2 (per IPC/JEDEC J-STD-020C)	
	<b>Machine Model</b>	Class A (per JEDEC standard EIA/JESD22-A115)	
<b>ESD</b>	<b>Human Body Model</b>	IR4302M	Class 1B (per EIA/JEDEC standard JESD22-A114)
		IR4322M	Class 1A (per EIA/JEDEC standard JESD22-A114)
<b>IC Latch-Up Test</b>		Class I, Level A (per JESD78)	
<b>RoHS Compliant</b>		Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
<sup>††</sup> Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

<sup>†††</sup> Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN1=VN2; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V <sub>Pn</sub>	Positive power supply rail voltage, n=1-2	IR4302	-	80	V
		IR4322	-	60	
		IR4312	-	40	
V <sub>Bn</sub>	High side floating supply voltage	IR4302	-0.3	95	
		IR4322	-0.3	75	
		IR4312	-0.3	55	
V <sub>Sn</sub>	High side floating supply voltage <sup>††</sup> , n=1-2		V <sub>Bn</sub> -15	V <sub>Bn</sub> +0.3	
V <sub>CSHn</sub>	CSH pin input voltage, n=1-2		V <sub>Sn</sub> -0.3	V <sub>Bn</sub> +0.3	
V <sub>CC</sub>	Low side supply voltage <sup>††</sup>		-0.3	15	
V <sub>AA</sub>	Floating input positive supply voltage <sup>††</sup>	IR4302	-0.3	100	
		IR4322	-0.3	70	
		IR4312	-0.3	50	
V <sub>SS</sub>	Floating input negative supply voltage <sup>††</sup>		-1 (See I <sub>SSZ</sub> )	GND +0.3	
V <sub>IN+n</sub>	Floating input supply ground voltage, n=1-2		V <sub>SS</sub> -0.3	V <sub>AA</sub> +0.3	
I <sub>INn</sub>	Input current between IN- and IN+ pins <sup>†</sup> , n=1-2		-	±3	mA
V <sub>CSD</sub>	CSD pin input voltage		V <sub>SS</sub> -0.3	V <sub>AA</sub> +0.3	V
V <sub>COMPn</sub>	COMP pin input voltage, n=1-2		V <sub>SS</sub> -0.3	V <sub>AA</sub> +0.3	
V <sub>CLIP</sub>	CLIP pin input voltage		GND-0.3	V <sub>AA</sub> +0.3	
I <sub>CLIP</sub>	CLIP pin sinking current		-	5	mA
V <sub>FAULT</sub>	FAULT pin input voltage		GND-0.3	V <sub>AA</sub> +0.3	V
I <sub>FAULT</sub>	FAULT pin sinking current		-	5	mA
I <sub>AAZ</sub>	Floating input supply zener clamp current <sup>††</sup>		-	20	
I <sub>SSZ</sub>	Floating input negative supply zener clamp current <sup>††</sup>		-	20	
I <sub>CCZ</sub>	Low side supply zener clamp current <sup>†††</sup>		-	20	
I <sub>BSZn</sub>	Floating supply zener clamp current <sup>†††</sup> , n=1-2		-	20	
dV <sub>Sn</sub> /dt	Allowable Vs voltage slew rate, n=1-2		-	50	V/ns
dV <sub>SS</sub> /dt	Allowable Vss voltage slew rate <sup>†††</sup>		-	50	V/ms
I <sub>d@ 25°C</sub>	Continuous output current, from VPn to VS <sub>n</sub> , VS <sub>n</sub> to VN <sub>n</sub> , V <sub>CC</sub> =10V, V <sub>Bn</sub> -V <sub>Sn</sub> =10V	IR4302	-	6.5	A
		IR4322		7.0	
		IR4312		3.6	
I <sub>d@ 100°C</sub>	Continuous output current, from VPn to VS <sub>n</sub> , VS <sub>n</sub> to VN <sub>n</sub> , V <sub>CC</sub> =10V, V <sub>Bn</sub> -V <sub>Sn</sub> =10V	IR4302	-	5.4	
		IR4322		5.8	
		IR4312		2.9	
I <sub>DM</sub>	Pulsed output current, from VPn to VS <sub>n</sub> , VS <sub>n</sub> to VN <sub>n</sub> , V <sub>CC</sub> =10V, V <sub>Bn</sub> -V <sub>Sn</sub> =10V <sup>†††††</sup>	IR4302	-	26	
		IR4322		28	
		IR4312		15	

Pd	Power dissipation <sup>†††</sup> @ T <sub>C</sub> = 25°C	IR4302	-	25	W
		IR4322		25	
		IR4312		8	
Rth <sub>JC</sub>	Thermal resistance, junction to ambient <sup>††††</sup>	IR4302	-	5	°C/W
		IR4322		5	
		IR4312		14	
T <sub>JIC</sub>	Control IC junction temperature		-	150	°C
T <sub>JFET</sub>	FET junction temperature		-	150	
T <sub>S</sub>	Storage Temperature		-55	150	
T <sub>L</sub>	Lead temperature (Soldering, 10 seconds)		-	300	

† IN- and IN+ contain clamping diodes between the two pins.

†† V<sub>AA</sub>-V<sub>SS</sub>, V<sub>CC</sub>-COM and V<sub>Bn</sub>-V<sub>Sn</sub> contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.

††† For the rising and falling edges of step signal of 10V. V<sub>SS</sub>=15V to 200V.

†††† Per MOSFET

††††† Repetitive rating, pulse width limited by max. junction temperature

### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The  $V_{SS}$  and  $V_{Sn}$  offset ratings are tested with supplies biased at  $COM=VN1=VN2$ ,  $V_{AA}-V_{SS}=9.6V$ ,  $V_{CC}=12V$  and  $V_{Bn}-V_{Sn}=12V$ . All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition		Min	Max	Units
$V_{Pn}$	Positive power supply voltage, n=1-2, without heatsink	IR4302	-	46	V
		IR4322	-	46	
		IR4312	-	32	
	Positive power supply voltage, n=1-2, with heatsink	IR4302	-	62	
		IR4322	-	50	
		IR4312	-	32	
$V_{Bn}$	High side floating supply absolute voltage, n=1-2		$V_{Sn} + 10$	$V_{Sn} + 14$	V
$V_{Sn}$	High side floating supply offset voltage, n=1-2	IR4302	†	80	
		IR4322	†	60	
		IR4312	†	40	
$V_{AA}$	Floating input positive supply voltage <sup>††</sup>		$V_{SS} + 4.5$	$V_{SS} + 15$	
$V_{SS}$	Floating input negative supply voltage <sup>††</sup>	IR4302	0	80	
		IR4322	0	60	
		IR4312	0	40	
$I_{AAZ}$	Floating input supply zener clamp current <sup>††</sup>		1	15	mA
$I_{SSZ}$	Floating input negative supply zener clamp current <sup>††</sup>		1	15	
$V_{CC}$	Low side fixed supply voltage		10	15	V
$V_{IC}$	IN- and IN+ pins common mode input voltage		$V_{SS} + 2$	$V_{AA} - 2$	
$V_{IN-n}$	Inverting input voltage, n=1-2		$V_{IN+} - 0.5$	$V_{IN+} + 0.5$	
$V_{CSD}$	CSD pin input voltage		$V_{SS}$	$V_{AA}$	
$V_{COMPn}$	COMP pin input voltage, n=1-2		$V_{SS}$	$V_{AA}$	
$C_{COMPn}$	COMP pin phase compensation capacitor to GND, n=1-2		1	-	nF
$V_{CSHn}$	CSH pin input voltage, n=1-2		$V_{Sn}$	$V_{Bn}$	V
$dV_{SS}/dt$	Allowable $V_{SS}$ voltage slew rate upon power-up <sup>†††</sup>		-	50	V/ms
$f_{SW}$	Switching Frequency		-	500	kHz
$T_A$	Ambient Temperature		-40	100	°C

Logic operational for  $V_S$  equal to  $-5V$  to  $+80V$ . Logic state held for  $V_S$  equal to  $-5V$  to  $-V_{BS}$ .

†

†† GND input voltage is limited by  $I_{AAZ}$  and  $I_{SSZ}$ .

†††  $V_{SS}$  ramps up from 0V to 70V.

**Electrical Characteristics**
 $V_{CC}, V_{BS} = 12\text{ V}, V_{SS} = V_{S1} = V_{S2} = V_{N1} = V_{N2} = \text{COM} = 0\text{V}, V_{AA} = 9.6\text{V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Low Side Supply</b>						
$UV_{CC+}$	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
$UV_{CC-}$	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
$UV_{CCHYS}$	$UV_{CC}$ hysteresis	-	0.2	-	V	
$I_{QCC}$	Low side quiescent current	-	-	3	mA	
$I_{CC}$	Low side supply current	-	10	-	mA	f=400kHz
$V_{CLAMPLN}$	Low side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	$I_{CC} = 5\text{mA}$
<b>High Side Floating Supply</b>						
$UV_{BS+n}$	High side well UVLO positive threshold, n=1-2	8.0	8.5	9.0	V	
$UV_{BS-n}$	High side well UVLO negative threshold, n=1-2	7.8	8.3	8.8	V	
$UV_{BSHYSn}$	$UV_{BS}$ hysteresis, n=1-2	-	0.2	-	V	
$I_{QBSn}$	High side quiescent current, n=1-2	-	-	2.4	mA	
$V_{CLAMPn}$	High side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	$I_{BS} = 5\text{mA}$
<b>Floating Input Supply</b>						
$UV_{AA+}$	$VA+$ , $VA-$ floating supply UVLO positive threshold from $V_{SS}$	8.2	8.7	9.2	V	$V_{SS} = 0\text{V}$ , GND pin floating
$UV_{AA-}$	$VA+$ , $VA-$ floating supply UVLO negative threshold from $V_{SS}$	7.7	8.2	8.7	V	$V_{SS} = 0\text{V}$ , GND pin floating
$UV_{AAHYS}$	$UV_{AA}$ hysteresis	-	0.5	-	V	$V_{SS} = 0\text{V}$ , GND pin floating
$I_{QAA0}$	Floating Input positive quiescent supply current	-	1.5	3	mA	$V_{AA} = 9.6\text{V}$ , $V_{SS} = 0\text{V}$ , $V_{CSD} = V_{SS}$
$I_{QAA1}$	Floating Input positive quiescent supply current	-	4	6	mA	$V_{AA} = 9.6\text{V}$ , $V_{SS} = 0\text{V}$ , $V_{CSD} = V_{AA}$
$I_{QAA2}$	Floating Input positive quiescent supply current	-	5	7.5	mA	$V_{AA} = 9.6\text{V}$ , $V_{SS} = 0\text{V}$ , $V_{CSD} = \text{GND}$
$I_{LKM}$	Floating input side to Low side leakage current	-	-	50	$\mu\text{A}$	$V_{AA} = V_{SS} = V_{GND} = 100\text{V}$
$V_{CLAMPM+}$	$V_{AA}$ floating supply zener diode clamp voltage, positive, with respect to GND	4.9	5.1	5.4	V	$I_{AA} = 5\text{mA}$ , $I_{SS} = 5\text{mA}$ , $V_{GND} = 0\text{V}$ , $V_{CSD} = V_{SS}$
$V_{CLAMPM-}$	$V_{SS}$ floating supply zener diode clamp voltage, negative, with respect to GND	-5.4	-5.1	-4.9	V	$I_{AA} = 5\text{mA}$ , $I_{SS} = 5\text{mA}$ , $V_{GND} = 0\text{V}$ , $V_{CSD} = V_{SS}$



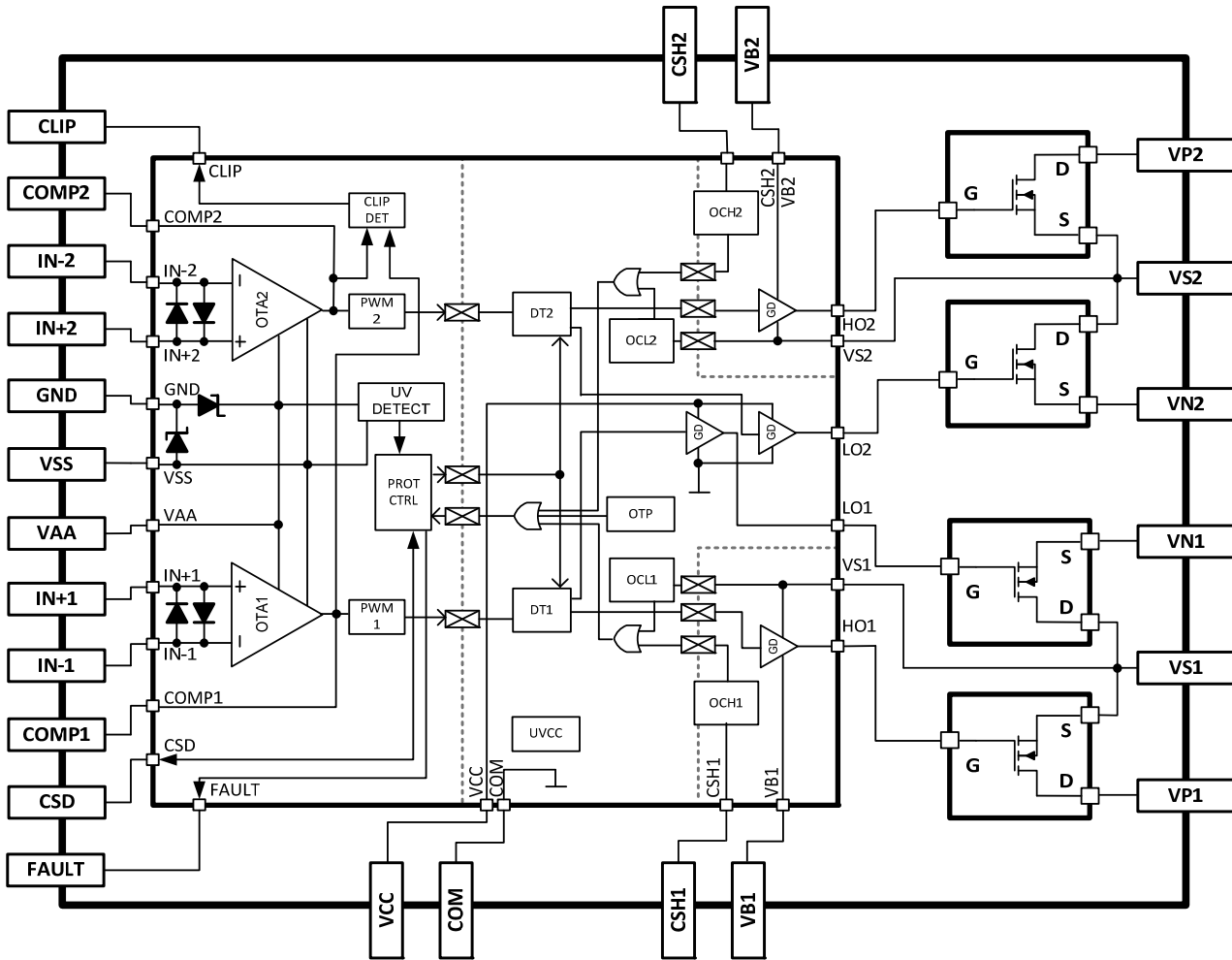
**Electrical Characteristics (cont'd)**
 $V_{CC}, V_{BS} = 12\text{ V}$ ,  $V_{SS} = V_{S1} = V_{S2} = V_{N1} = V_{N2} = \text{COM} = 0\text{V}$ ,  $V_{AA} = 9.6\text{V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Audio Input (<math>V_{GND}=0</math>, <math>V_{AA}=4.8\text{V}</math>, <math>V_{SS}=-4.8\text{V}</math>)</b>						
$V_{OSn}$	Input offset voltage, n=1-2	-18	0	18	mV	
$I_{BINn}$	Input bias current, n=1-2	-	-	40	nA	
GBWn	Small signal bandwidth in OTA, n=1-2	-	9	-	MHz	$C_{COMP}=1\text{nF}$ , $R_f=0$
$g_{mn}$	OTA transconductance, n=1-2	-	10	-	mS	$V_{IN+}=0\text{V}$ , $V_{IN-}=10\text{mV}$
$G_{Vn}$	OTA gain, n=1-2	50	-	-	dB	
<b>PWM</b>						
$V_{th_{PWM}}$	PWM comparator threshold in COMP	-	$(V_{AA} - V_{SS})/2$	-	V	
$f_{OTAn}$	COMP pin star-up local oscillation frequency, n=1-2	0.7	1.0	1.5	MHz	$V_{CSD} = \text{GND}$
$T_{on\_n}$	COMP to VS rising edge propagation delay, n=1-2	-	370	-	ns	
$T_{off\_n}$	COMP to VS trailing edge propagation delay, n=1-2	-	320	-	ns	
DTn	Deadtime: Low-side turn-off to High-side turn-on ( $DT_{LO-HO}$ ) & High-side turn-off to Low-side turn-on ( $DT_{HO-LO}$ ), n=1-2	-	50	-	ns	$V_P=30\text{V}$ , $V_N=-30\text{V}$ ,
<b>Power MOSFET (FET1, FET2, FET3, FET4) (IR4302)</b>						
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	80	-	-	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$R_{DS(ON)}$	FET on resistance	-	39	50	m $\Omega$	$V_{GS}=10\text{V}$ , $I_D=3.3\text{A}$
Qg	Total gate charge	-	7.3	-	nC	
$I_{LK0}$	VP leakage current, VS=VN	-	-	20	$\mu\text{A}$	$V_P=80\text{V}$ , $V_{CSD} = V_{SS}$
$I_{LK1}$	VP leakage current, VS=VP	-	-	50	$\mu\text{A}$	
<b>Power MOSFET (FET1, FET2, FET3, FET4) (IR4322)</b>						
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	-	-	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$R_{DS(ON)}$	FET on resistance	-	30	40	m $\Omega$	$V_{GS}=10\text{V}$ , $I_D=3.3\text{A}$
Qg	Total gate charge	-	8.3	-	nC	
$I_{LK0}$	VP leakage current, VS=VN	-	-	20	$\mu\text{A}$	$V_P=60\text{V}$ , $V_{CSD} = V_{SS}$
$I_{LK1}$	VP leakage current, VS=VP	-	-	50	$\mu\text{A}$	
<b>Power MOSFET (FET1, FET2, FET3, FET4) (IR4312)</b>						
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	40	-	-	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$R_{DS(ON)}$	FET on resistance	-	44	56	m $\Omega$	$I_D=3.6\text{A}$
Qg	Total gate charge	-	4.5	-	nC	$V_{GS}=10\text{V}$
$I_{LK0}$	VP leakage current, VS=VN	-	-	20	$\mu\text{A}$	$V_P=40\text{V}$ , $V_{CSD} = V_{SS}$
$I_{LK1}$	VP leakage current, VS=VP	-	-	50	$\mu\text{A}$	

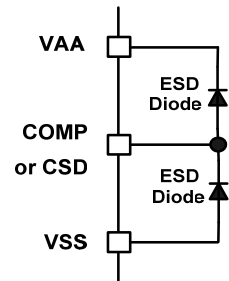
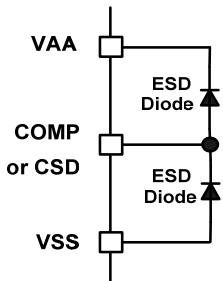
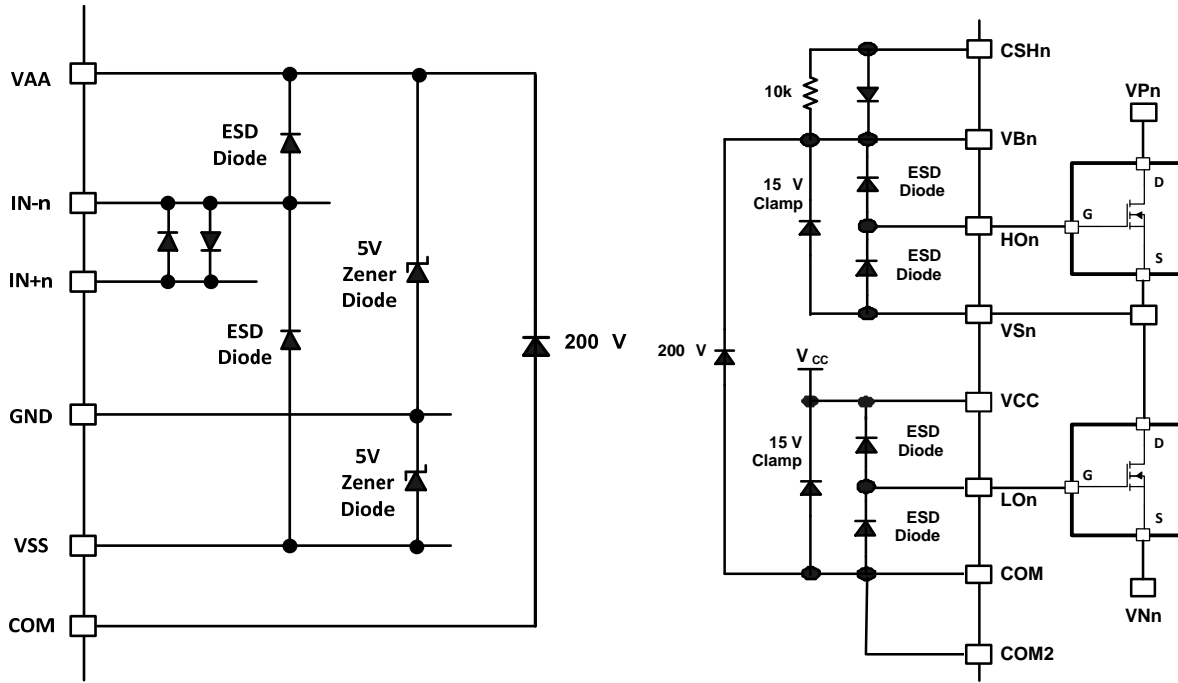
**Electrical Characteristics (cont'd)**
 $V_{CC}, V_{BS} = 12\text{ V}, V_{SS} = V_{S1} = V_{S2} = V_{N1} = V_{N2} = \text{COM} = 0\text{ V}, V_{AA} = 9.6\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Protection</b>						
$I_{OCPn}$	Over current detection Positive threshold, n=1-2	-	16	-	A	
$I_{OCNn}$	Over current detection Negative threshold, n=1-2	-	-16	-	A	
Vth1	CSD pin shutdown release threshold	$0.62 \times V_{AA}$	$0.70 \times V_{AA}$	$0.78 \times V_{AA}$	V	
Vth2	CSD pin self reset threshold	$0.26 \times V_{AA}$	$0.30 \times V_{AA}$	$0.34 \times V_{AA}$	V	
$I_{CSD+}$	CSD pin discharge current	70	100	130	$\mu\text{A}$	$V_{CSD} = V_{SS} + 4.8\text{ V}$
$I_{CSD-}$	CSD pin charge current	70	100	130	$\mu\text{A}$	$V_{CSD} = V_{SS} + 4.8\text{ V}$
$t_{SDn}$	Shutdown propagation delay from $V_S < V_{th1}$ to Shutdown, n=1-2	-	-	250	ns	COMP = $V_{SS}$
$t_{OCPn}$	CHn propagation delay time from $I_{On} > I_{OCPn}$ to Shutdown, n=1-2	-	-	500	ns	COMP = $V_{SS}$
$t_{OCNn}$	CHn propagation delay time from $I_{On} < I_{OCNn}$ to Shutdown, n=1-2	-	-	500	ns	COMP = $V_{SS}$
Vth+ <sub>CLIP</sub>	Clip detection positive threshold in COMP	$0.85 \times V_{AA}$	$0.90 \times V_{AA}$	$0.95 \times V_{AA}$	V	
Vth- <sub>CLIP</sub>	Clip detection negative threshold in COMP	$0.05 \times V_{AA}$	$0.10 \times V_{AA}$	$0.15 \times V_{AA}$	V	
$t_{CLIP}$	Clipping detection propagation delay	-	40	-	ns	
$t_{CLIPmin}$	Clipping detection minimum output duration	-	3	-	$\mu\text{s}$	
$T_{SD}$	Over temperature shutdown threshold in controller IC	-	105	-	$^\circ\text{C}$	
$T_{SDHYS}$	Over temperature shutdown threshold hysteresis	-	7	-	$^\circ\text{C}$	

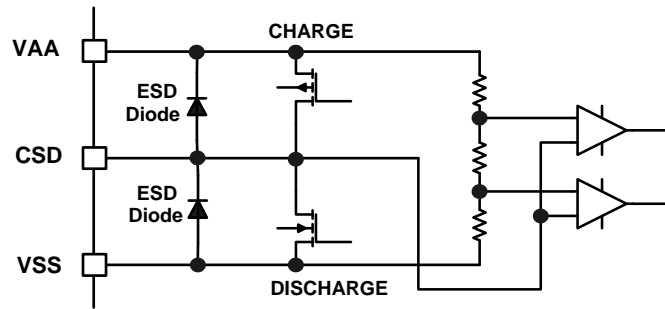
## Functional Block Diagram



## Input/Output Pin Equivalent Circuit Diagrams



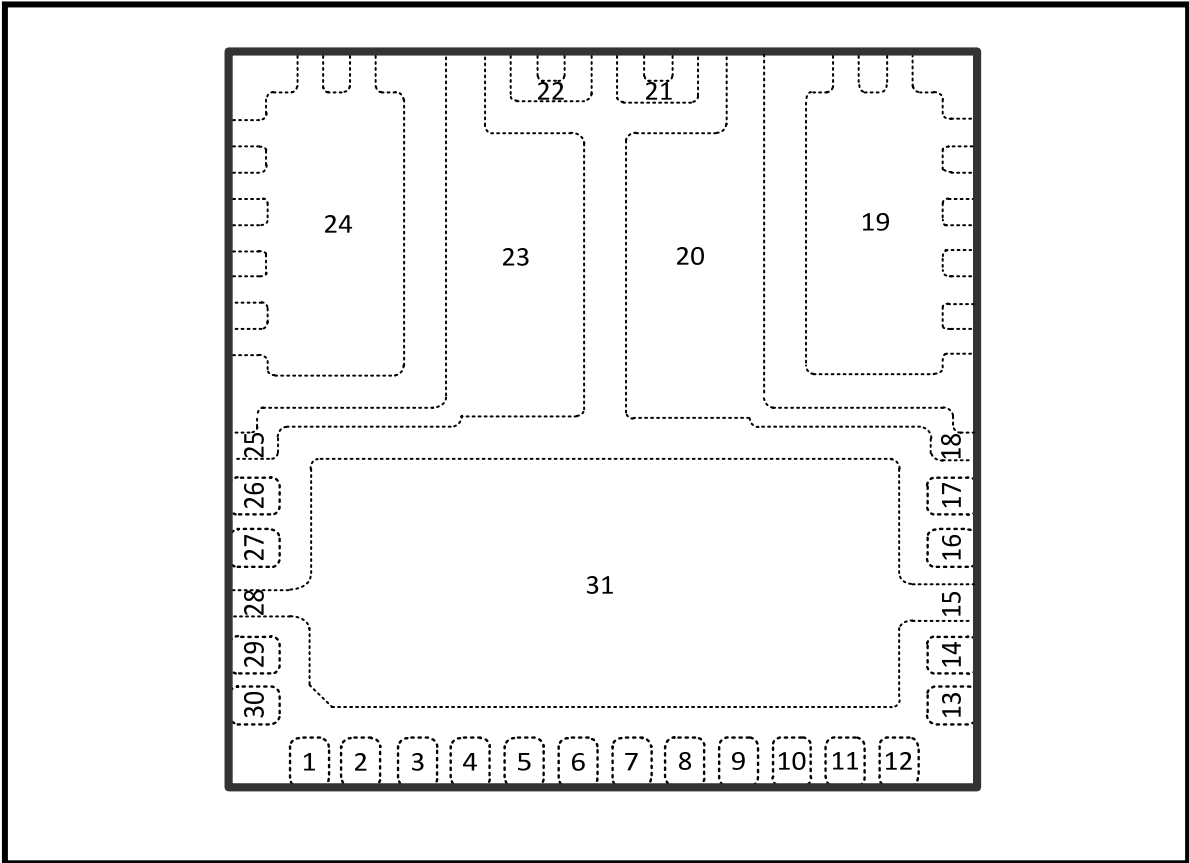
Input/Output Pin Equivalent Circuit Diagrams (Cont'd)

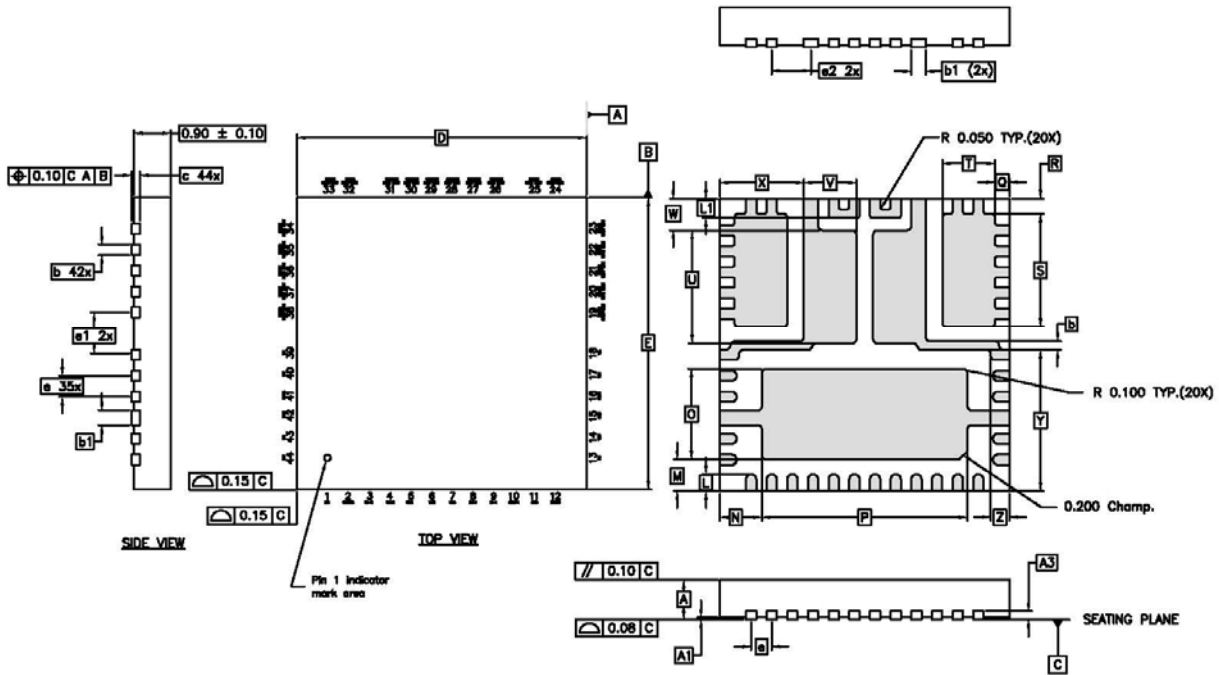


**Lead Definitions**

Pin #	Symbol	Description
1	CLIP	Clipping detection output, open drain, referenced to GND
2	COMP2	CH2 PWM comparator input
3	IN-2	CH2 Analog inverting input
4	IN+2	CH2 Analog non-inverting input
5	GND	GND for internal shunt zener diodes to VAA and VSS
6	VSS	Floating input negative supply
7	VAA	Floating input positive supply
8	IN+1	CH1 Analog non-inverting input
9	IN-1	CH1 Analog inverting input
10	COMP1	CH1 PWM comparator input
11	CSD	Shutdown timing capacitor / shutdown input
12	FAULT	Fault reporting output, open drain, referenced to GND
13	NC	
14	VCC	Low side supply
15	COM	Low side supply return, internally connected to pin 31
16	CSH1	CH1 High side over current sensing input, referenced to VS1
17	VB1	CH1 High side floating supply
18	VS1	CH1 PWM output, internally connected to pin 20
19	VP1	CH1 Positive power supply
20	VS1	CH1 PWM output
21	VN1	CH1 Negative power supply, connect to COM externally
22	VN2	CH2 Negative power supply, connect to COM externally
23	VS2	CH2 PWM output, internally connected to pin 25
24	VP2	CH2 Positive power supply
25	VS2	CH2 PWM output
26	VB2	CH2 High side floating supply
27	CSH2	CH2 High side over current sensing input, referenced to VS2
28	COM	Low side supply return, internally connected to pin 31
29	NC	
30	NC	
31	COM	Low side supply return

Lead Assignments (Top View)



**Package Details**


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	.032	.039
A1	0.00	0.05	.0000	.0020
A3	0.20	REF	0.008	REF
b	0.18	0.30	.0071	.0118
b1	0.30	0.40	.0118	.0157
D	7.00 BASIC		.276 BASIC	
E	7.00 BASIC		.276 BASIC	
L	0.30	0.50	.0118	.0197
L1	0.35	0.55	.0138	.0217
e	0.50 BASIC		.0197 BASIC	
e1	1.00 BASIC		.0394 BASIC	
e2	0.95 BASIC		.0374 BASIC	
M	0.65	0.85	.0256	.0335
N	0.91	1.11	.0358	.0437
O	2.06	2.26	.0811	.0890
P	4.88	5.08	.1921	.2000

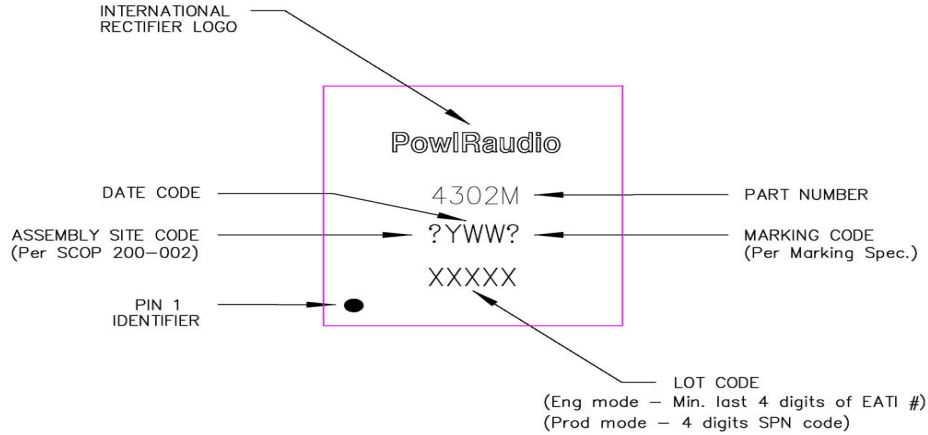
Q	0.25	0.45	.0098	.0177
R	0.25	0.45	.0098	.0177
S	2.82	2.82	.1031	.1110
T	1.17	1.37	.0461	.0539
U	2.82	2.82	.1031	.1110
V	1.17	1.37	.0461	.0539
W	0.85	0.85	.0256	.0335
X	1.92	2.12	.0756	.0835
Y	3.27	3.47	.1287	.1366
Z	0.35	0.55	.0138	.0217



## Board Mounting Information

Refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.

## Part Marking Information



## Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR4302M	PQFN44 7x7mm	Tape and Reel	3000	IR4302MTRPBF
IR4322M	PQFN44 7x7mm	Tape and Reel	3000	IR4322MTRPBF
IR4312M	PQFN44 7x7mm	Tape and Reel	3000	IR4312MTRPBF

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