Sup*IR*Buck™

USER GUIDE FOR IRDC3710-DF EVALUATION BOARD

DESCRIPTION

The IR3710M is single phase sync-buck PWM controller IC optimized for efficiency in high performance portable electronics. The switching modulator uses constant ON-time control. Constant ON-time with diode emulation provides the highest light load efficiency required for all applications.

Key features offered by the IR3710M include: programmable switching frequency, soft start, forced continuous conduction mode (FCCM) operation at light load and over current protection.

Additional features include pre-bias startup, very precise 0.5V reference, over/under voltage fault protection, power good output, and enable input with voltage monitoring capability. The gate drive is designed to operate up to 7.5V to enhance over all system efficiency.

This user guide contains the schematic and bill of materials for the IRDC3710-DF evaluation board. The guide describes operation and use of the evaluation board itself. Detailed specifications and application information for IR3710M is available in the IR3710M data sheet.

BOARD FEATURES

- V_{in} = +12V Typical (8-19V input Voltage range. See note below)
- PV_{cc}= +5.0V
- Vcc=+3.3V
- V_{out} = +1.1V @ 0- 24A
- F_s = 300kHz @ 24A
- L = 0.5uH
- C_{in}= 2x10uF (ceramic 1210) + 1x330uF (electrolytic)
- C_{out}= 2x10uF (ceramic 1206) + 2x330uF(SP Cap)

Note: At low input line an additional 10uF ceramic capacitor is recommended at input to handle higher ripple current)

CONNECTIONS and OPERATING INSTRUCTIONS

A regulated +12V input supply should be connected to VIN+ and Vin-. A maximum 24A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IRDC3710-DF has three input connectors, one for gate drive supply (PVcc),one for biasing (Vcc) and the third one as input voltage (Vin). Separate supplies should be applied to these inputs. PVcc input should be a well regulated 4.5V-5.5V supply and it would be connected to +5V and PGND and Vcc input should be a well regulated 3.0V-3.6V supply and it would be connected to +3.3V and AGND. An external signal can be provided as Enable signal to turn on or turn off the converter if desired. This signal is not required to power up the Evaluation board as EN pin is connected to a voltage divider from Vin. The absolute maximum voltage of Enable signal is +3.9V.

The evaluation board is configured for use with 2x10uF (ceramic 1206) + 2x330uF (SP) capacitors. However, the design can be modified for an all ceramic output cap configuration by adding the inductor DCR sensing circuit as show in the schematic.

Table 1: Connections

Connection	Signal Name
VIN+	VIN (+12V)
VIN-	Ground of VIN
+5V	PVcc input (+5.0V)
+3.3V	Vcc input (+3.3V)
PGND	Ground for PVcc input
AGND	Ground for Vcc input
VOUT+	V_{out} (+1.1V)
VOUT+	Ground of V_{out}
Enable	Enable input

LAYOUT

The PCB is a 4-layer board. All layers are 2 Oz. copper. The IR3710M and other components are mounted on the top and bottom side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3710M. The feedback resistors are connected to the output voltage at the point of regulation and are located close to IR3710M. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

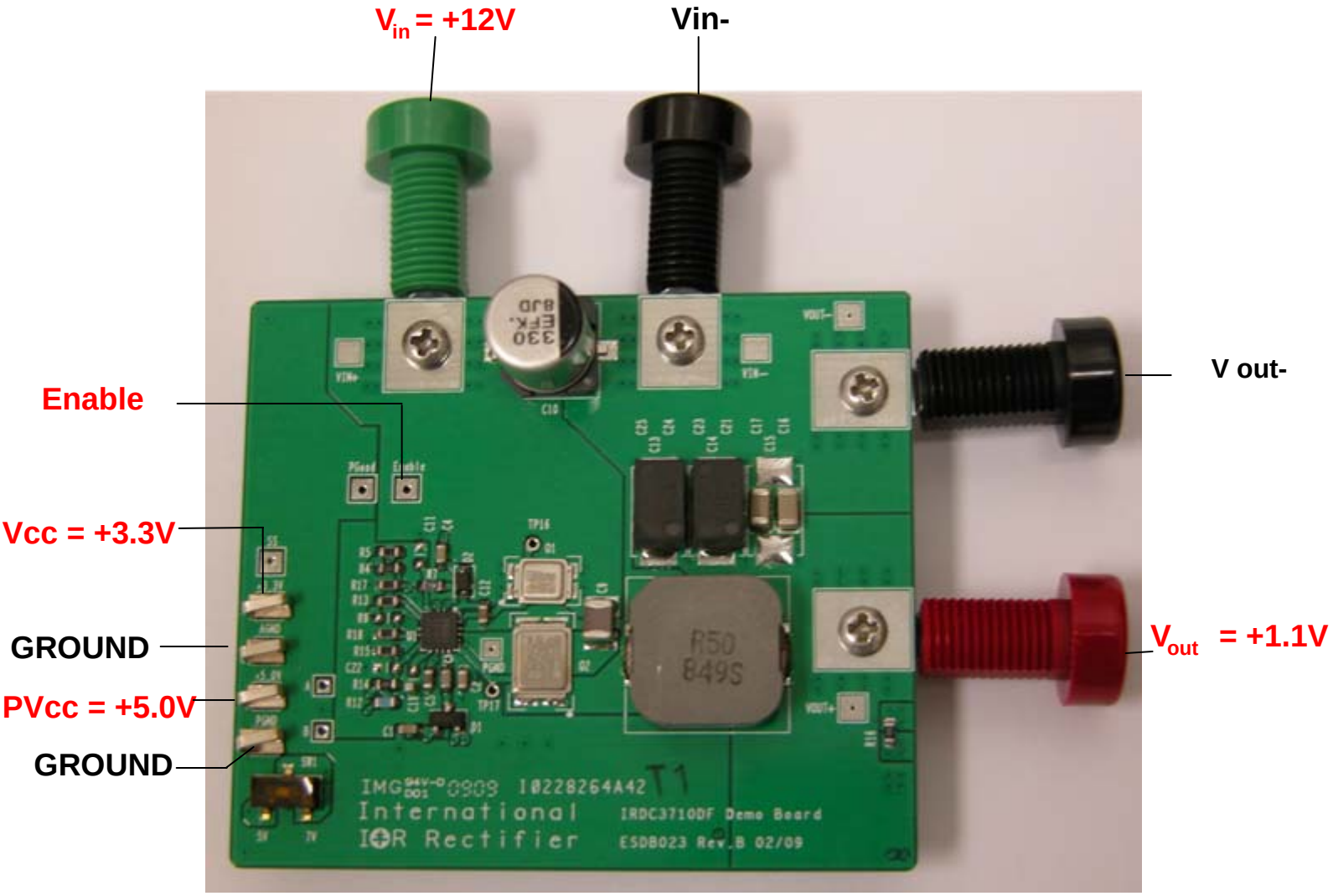


Figure 1: Connection diagram of IRDC3710-DF evaluation board

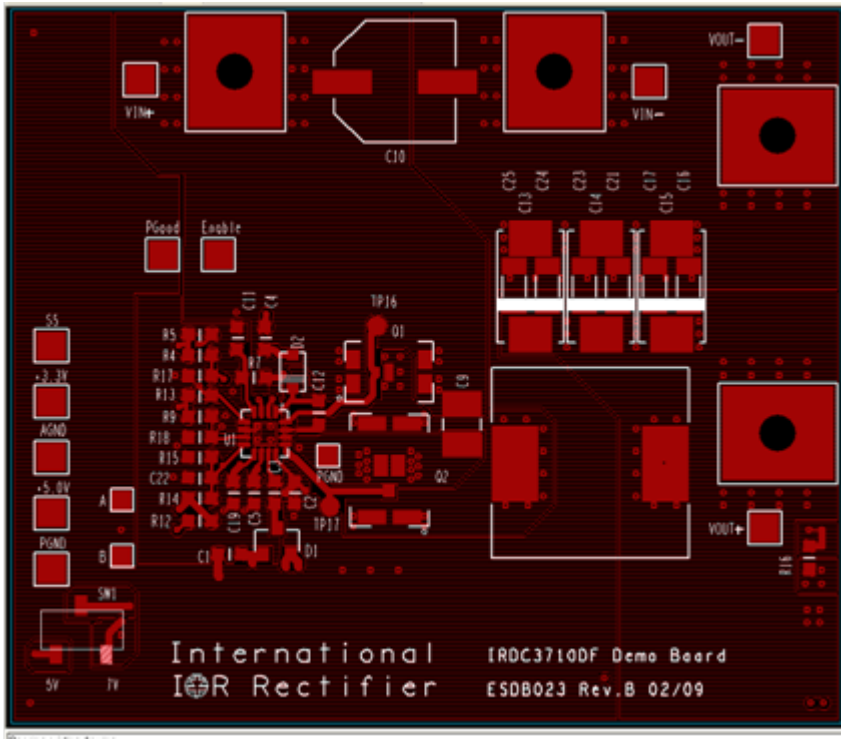


Figure 2: PCB layout, top layer

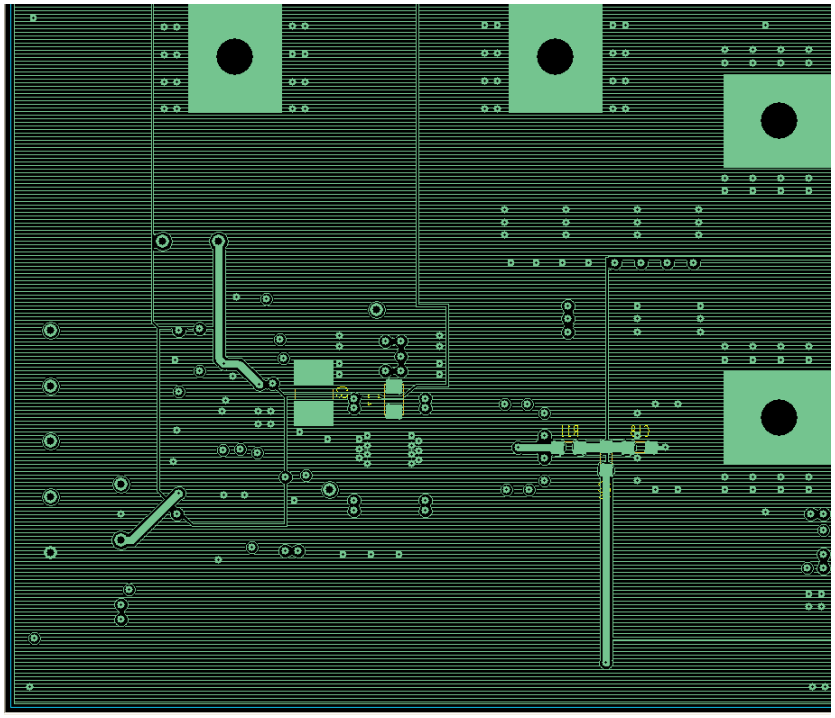


Figure 3: PCB layout, bottom layer

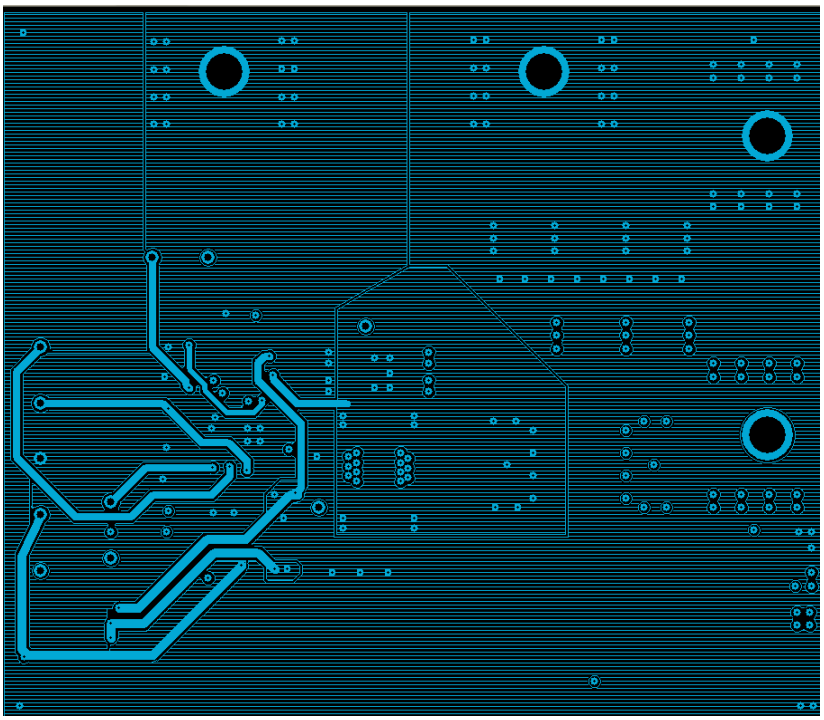


Figure 4: Board layout, mid-layer I

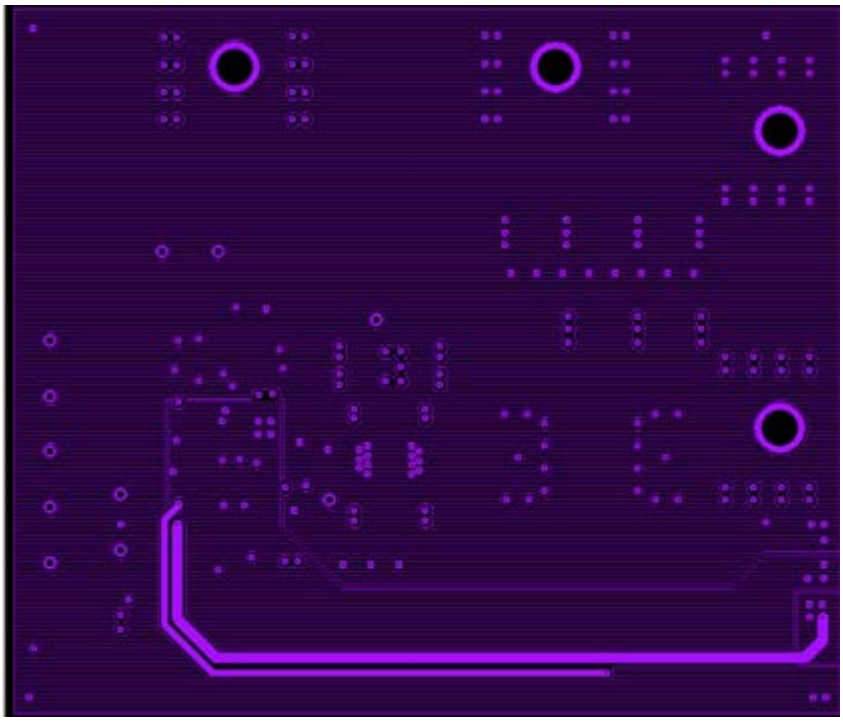


Figure 5: Board layout, mid-layer II

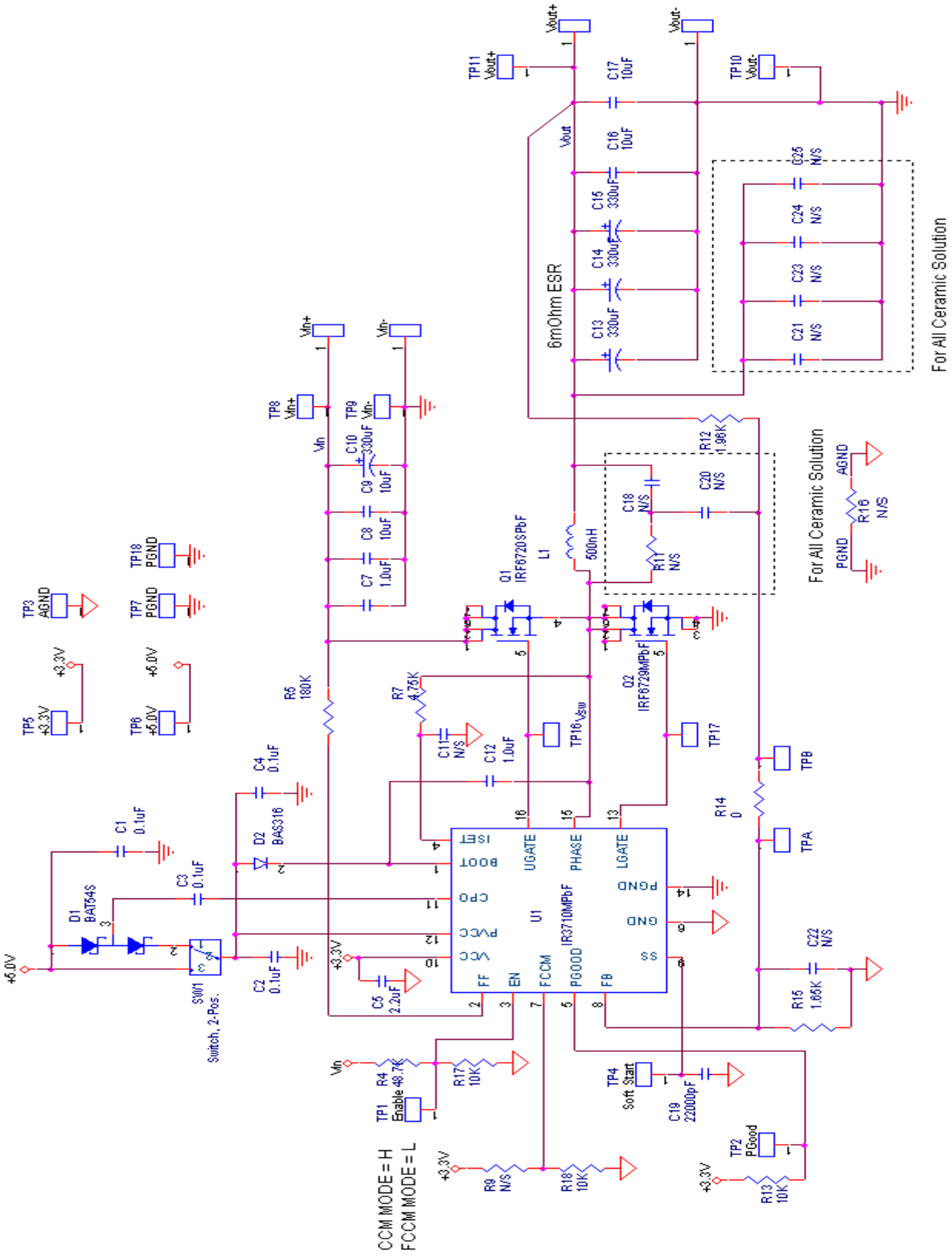


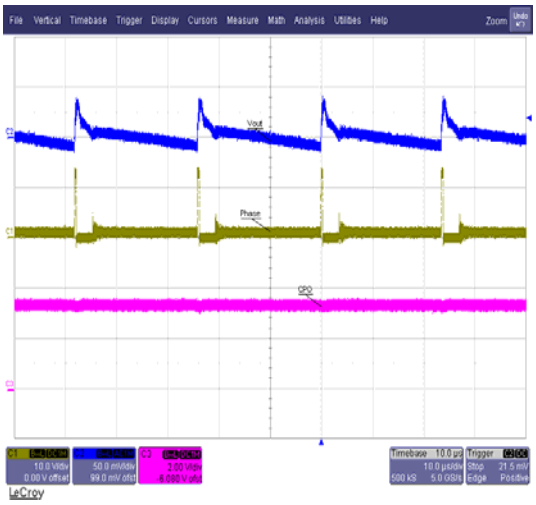
Figure 6: Schematic of the IRDC3710-DF Evaluation board

Bill of Materials

1	4	C1,C2,C3,C4	0.1uF	Ceramic,25V,0603,X7R,10%
2	1	C5	2.2uF	Ceramic, 6.3V, 0603, X7R, 10%
3	1	C7	1.0uF	Ceramic, 25V, 0805, X5R, 10%
4	2	C8,C9	10uF	Ceramic,25V,1210,X5R,10%
5	1	C10	330uF	SMD Elecrolytic, 25V,F-size,20%
6	5	C11,C15C18,C20,C22	N/S	No Stuff
7	1	C12	1.0uF	Ceramic,25V,0603,X5R,10%
8	2	C13,C14	330uF	SP-Cap,Dcase,4V,20%
9	2	C16,C17	10uF	Ceramic,6.3V,1206,X5R,20%
10	1	C19	22000pF	Ceramic,50V,0603,X7R,10%
11	4	C21,C23,C24,C25	N/S	No Stuff
12	1	D1	BAT54S	Dual Diode,40V,BAT54S,SOT-23
13	1	D2	BAS316	Phillips 30V , 0.25A
14	1	L1	500nH	SMT-Inductor,0.8mOhms,Toko FDUE1245-R50M
15	1	Q1	IRF6720S2TRPBF	IRF6720 30V
16	1	Q2	IRF6729MTRPBF	IRF6729 30V
17	1	R4	48.7K	Thick-film,0603,1/10W,1%
18	1	R5	180K	Thick-film,0603,1/10W,1%
19	1	R7	4.75k	Thick-film,0603,1/10 W,1%
20	3	R9,R11,R16	N/S	No Stuff
21	1	R12	1.96K	Thick-film,0603,1/10W,1%
22	3	R13,R17,R18	10K	Thick-film,0603,1/10W,1%
23	1	R14	0	Thick-film,0603,1/10 W,5%
24	1	R15	1.65K	Thick-film,0603,1/10W,1%
25	1	SW1	Switch, 2-Pos.	Switch, DIP, 2-Pos., SPDT
31	1	U1	IR3710MMPbF	IR3710M, Controller,PQFN,3x3mm

TYPICAL OPERATING WAVEFORMS

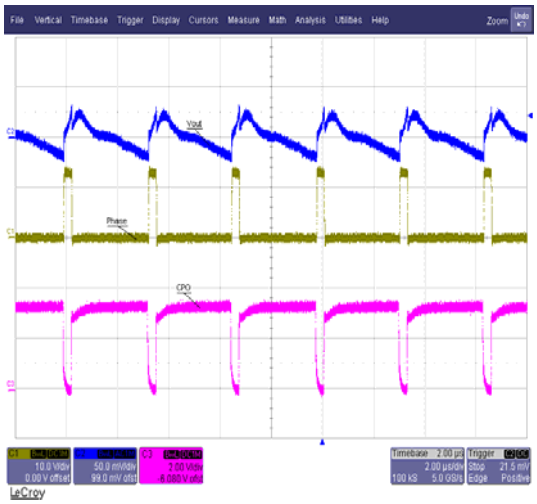
Vin=12V, PVcc=5.0V, Vcc=3.3V,Vo=1.1V, Io=0- 24A, , Room Temperature, No Air Flow



Ch1-Phase Voltage(10V/Div)
Ch3-CPO(2V/Div)

Ch2-Vout(50mV/div)
Time: 10uS/Div)

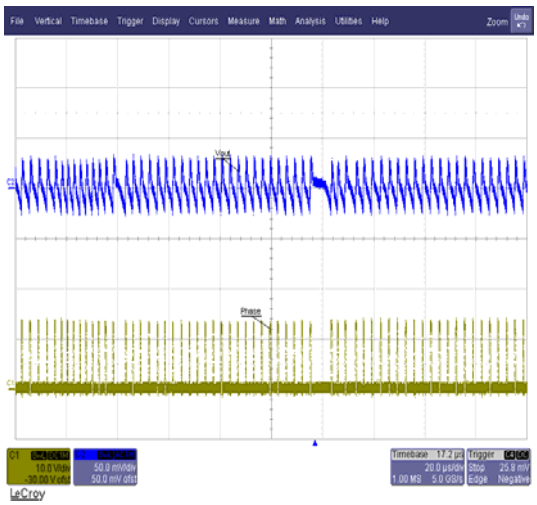
Figure 7: Charge Pump Off at Iout = 0.5A



Ch1-Phase Voltage(10V/Div)
Ch3-CPO(2V/Div)

Ch2-Vout(50mV/div)
Time: 2uS/Div)

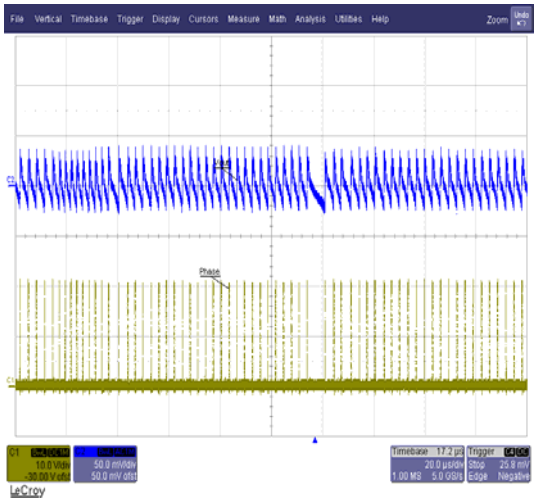
Figure 8: Charge Pump On at Iout =5A



Ch1-Phase Voltage (10V/Div)

Ch2-Vout(50mV/Div)

Figure 9: Load Step (5A to 15A) Transient at 12Vin



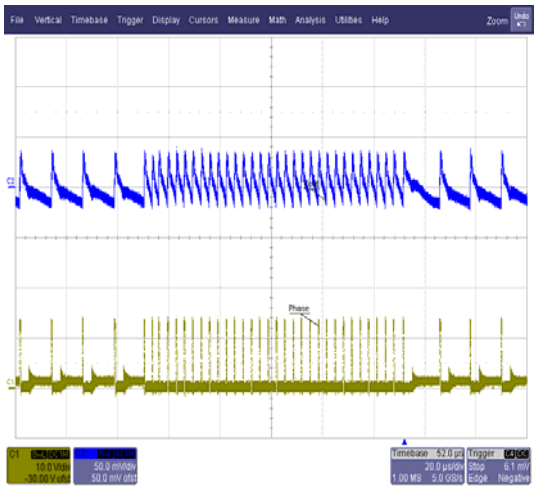
Ch1-Phase Voltage (10V/Div)

Ch2-Vout(50mV/Div)

Figure 10: Load Step (5A to 15A) Transient at 19Vin

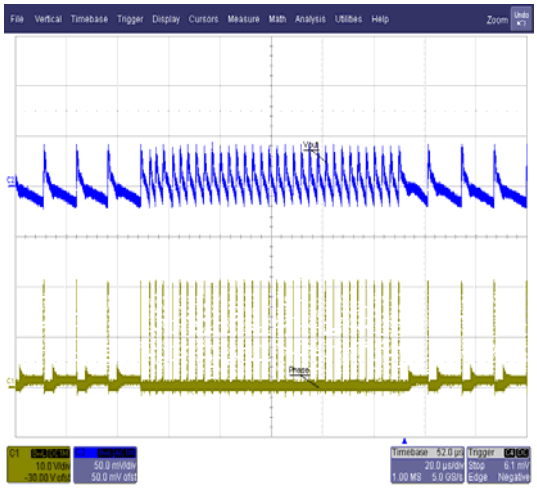
TYPICAL OPERATING WAVEFORMS

Vin=12V, PVcc=5.0V, Vcc=3.3V,Vo=1.1V, Io=0- 24A, Room Temperature, No Air Flow



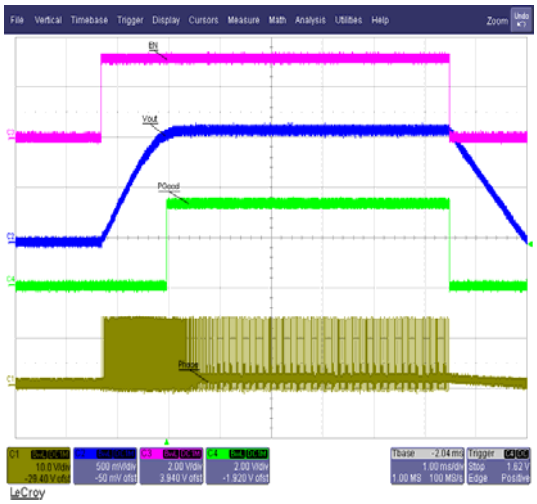
Ch1-Phase Voltage (10V/Div) Ch2-Vout(50mV/Div)

Figure 11: DCM/CCM transition from 1.0A to 5A at 12Vin



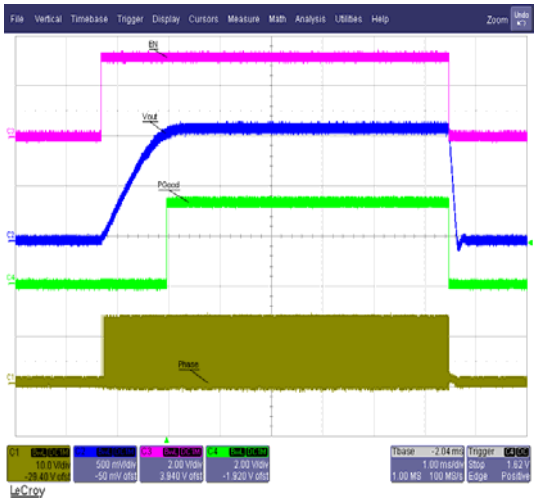
Ch1-Phase Voltage (10V/Div) Ch2-Vout(50mV/Div)

Figure 12: DCM/CCM transition from 1.0A to 5A at 19Vin



Ch1-Phase Voltage (10V/Div)
Ch3-EN(2V/Div)
Ch2-Vout(500mV/Div)
Ch4-PGood(2V/Div)

Figure 13: Startup/Shutdown 12Vin at 1.0A



Ch1-Phase Voltage (10V/Div)
Ch3-EN(2V/Div)
Ch2-Vout(500mV/Div)
Ch4-PGood(2V/Div)

Figure 14: Startup/Shutdown 12Vin at 5.0A

TYPICAL OPERATING WAVEFORMS
Vin=12V, PVcc=5.0V, Vcc=3.3V, Vo=1.1V, Io=0- 24A, , Room Temperature, No Air Flow

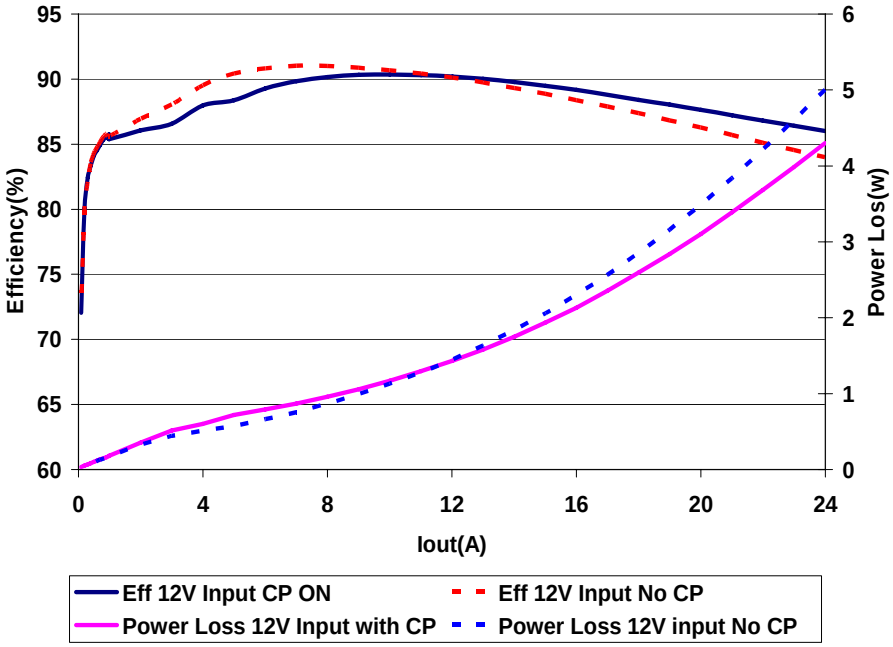


Figure 15: Typical Efficiency and Power Loss at Vin-12V

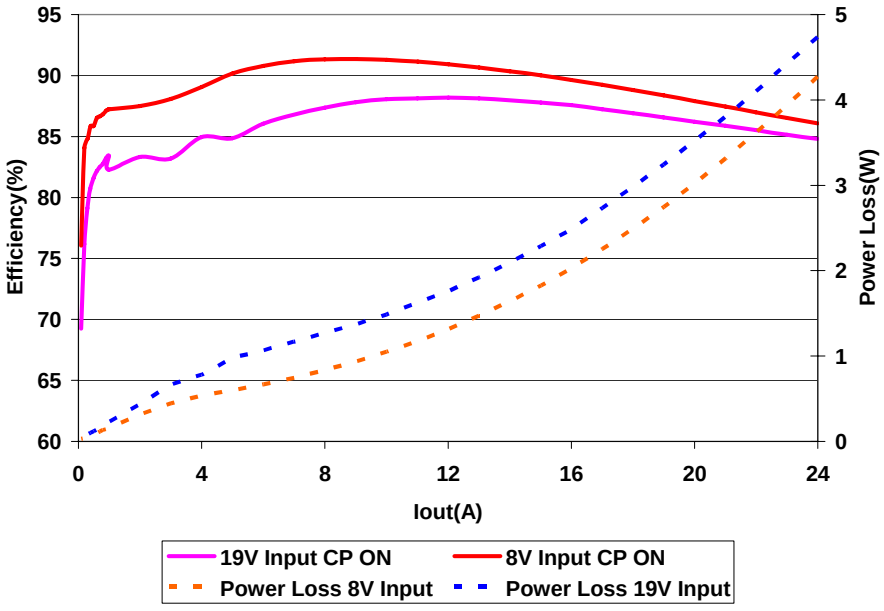


Figure 16: Typical Efficiency and Power Loss at Vin=8V and 19V

TYPICAL OPERATING WAVEFORMS

Vin=12V, PVcc=5.0V, Vcc=3.3V, Vo=1.1V, Io=0- 24A, , Room Temperature, No Air Flow

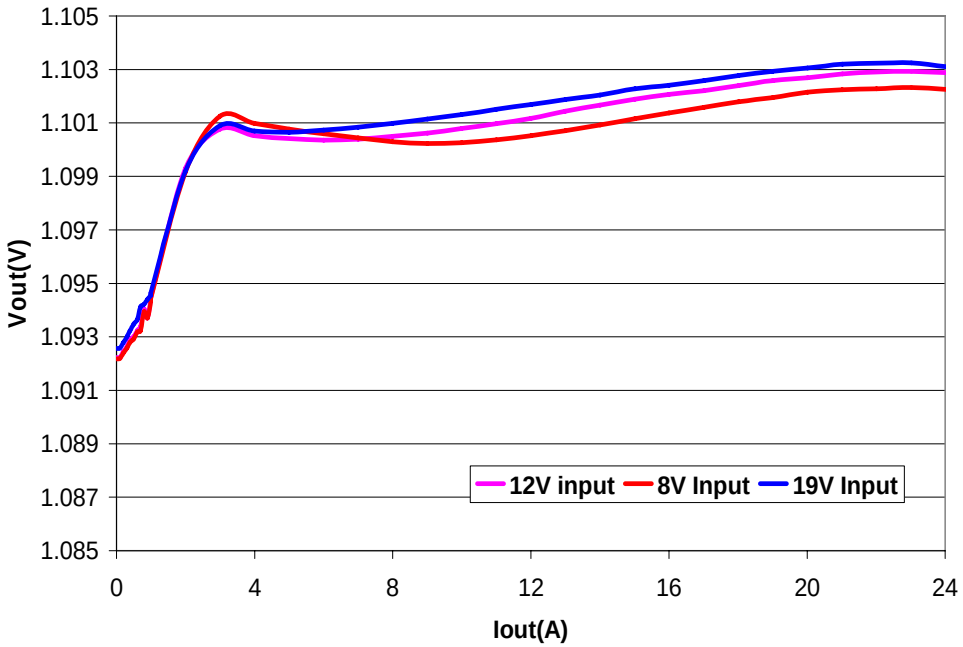
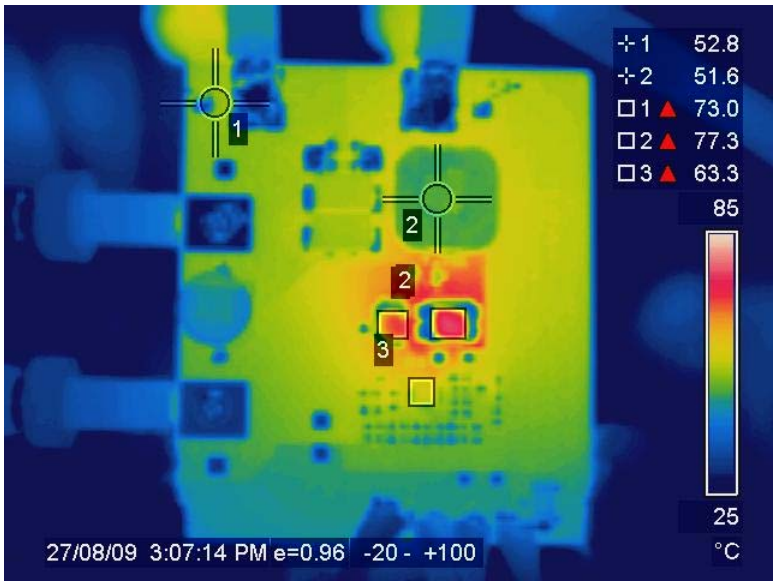


Figure 17: Typical Output Voltage Regulation

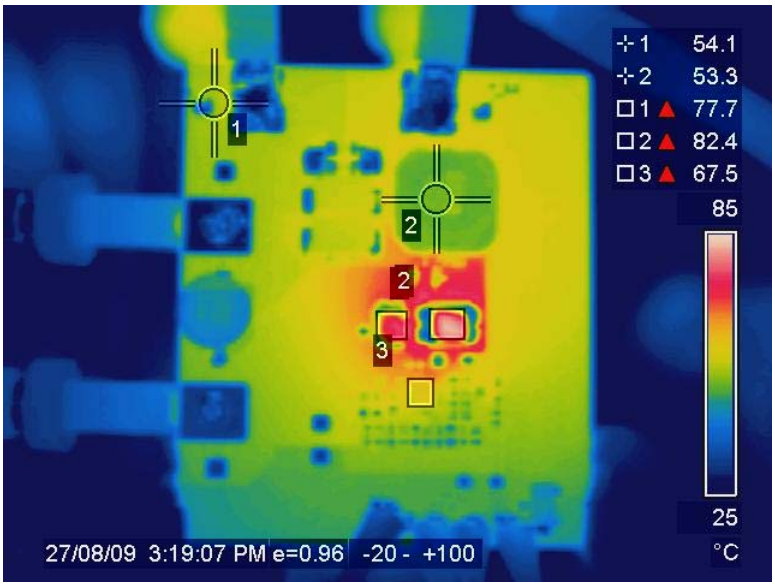


Q1: 73.0°C, Q2:77.3°C, Inductor: 51.6°C, PCB: 52.8°C

Figure 18:Thermal Image @12Vin, 24A, With CP On

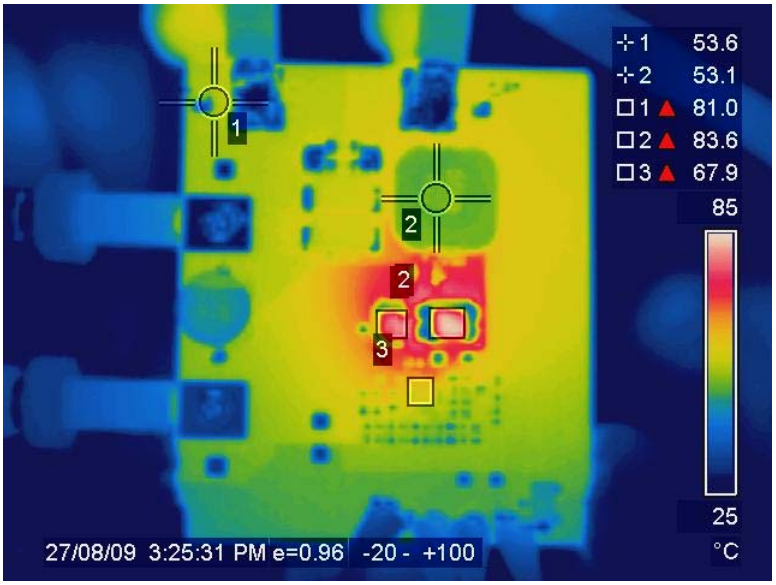
TYPICAL OPERATING WAVEFORMS

Vin=12V, PVcc=5.0V, Vcc=3.3V, Vo=1.1V, Io=0- 24A, , Room Temperature, No Air Flow



Q1: 77.7°C, Q2:82.4°C,Inductor: 53.3°C, PCB: 54.1°C

Figure 19: Thermal Image @19Vin, 24A, With CP On

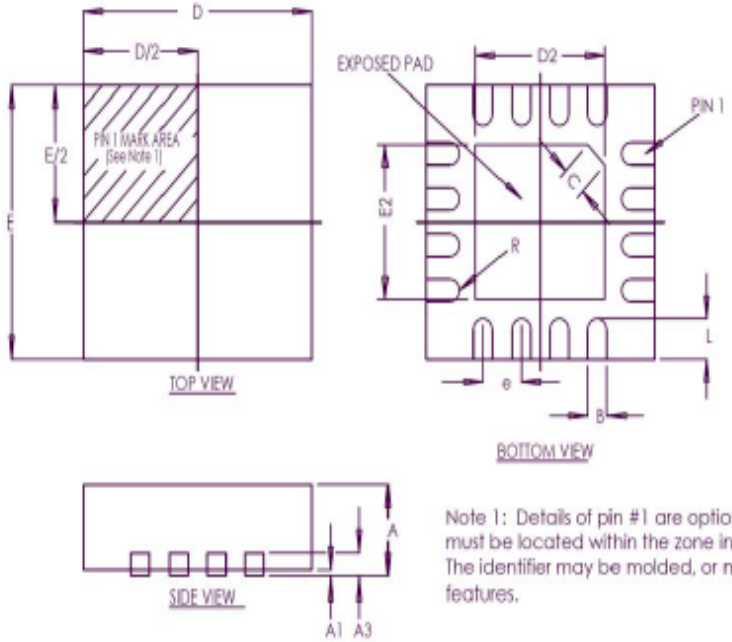


Q1:81°C,Q2:83.6°C, Inductor: 53.1°C, PCB: 53.6°C

Figure 20: Thermal Image @12Vin, 24A, With CP Off

PACKAGE INFORMATION

3X3 MLP LEAD FREE PACKAGE AND LAYOUT INFORMATION



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL	16-PIN 3x3 (unit: MM)		
DESIGN	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D		3.00 BSC	
D2	1.6	1.70	1.8
E		3.00 BSC	
E2	1.6	1.70	1.8
e		0.50 TYP	
L	0.30	0.40	0.50
R	0.125	---	---
C		0.35 TYP	

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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