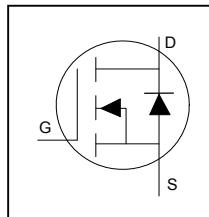


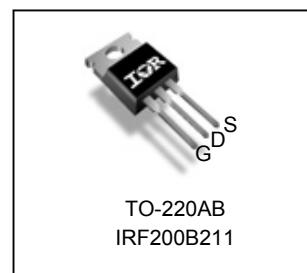
## Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC and AC/DC converters
- DC/AC Inverters

HEXFET® Power MOSFET

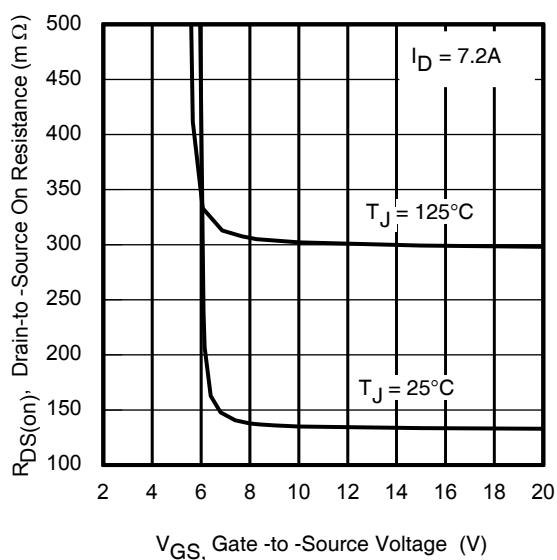


$V_{BSS}$	200V
$R_{DS(on)}$ typ. max	135mΩ
	170mΩ
$I_D$ (Silicon Limited)	12A

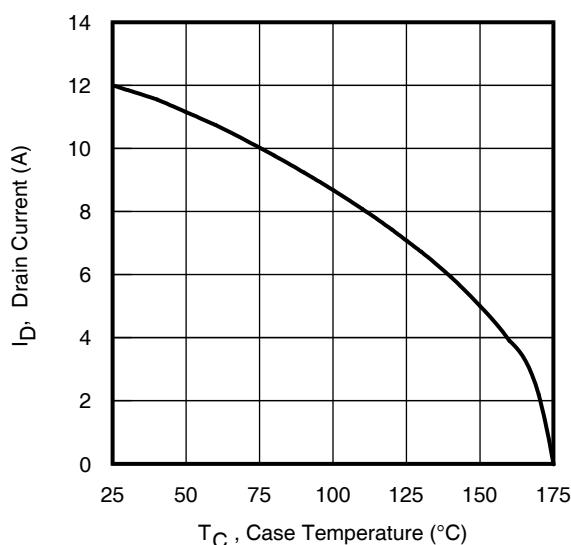


G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF200B211	TO-220	Tube	50	IRF200B211



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	12	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	9.0	
$I_{DM}$	Pulsed Drain Current ②	34	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	80	W
	Linear Derating Factor	0.53	W/ $^\circ C$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ C$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	88	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ⑧	72	
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ⑨	98	
$I_{AR}$	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	1.88	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

**Static @  $T_J = 25^\circ C$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.21	—	V/ $^\circ C$	Reference to $25^\circ C$ , $I_D = 1mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	135	170	$m\Omega$	$V_{GS} = 10V, I_D = 7.2A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	4.9	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 125^\circ C$
$I_{GS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_G$	Gate Resistance	—	2.7	—	$\Omega$	

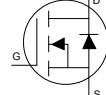
**Notes:**

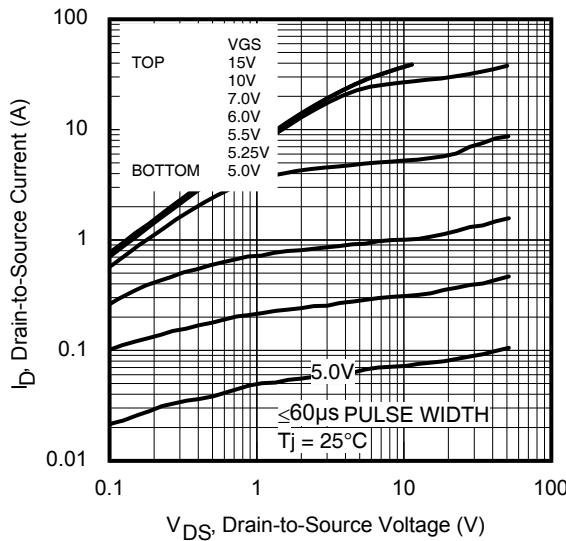
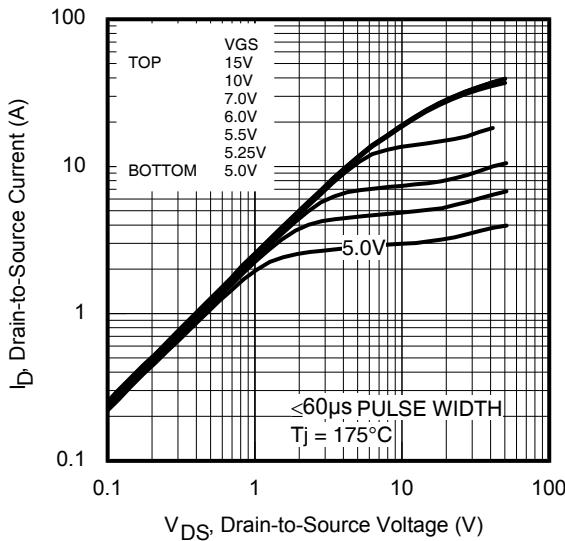
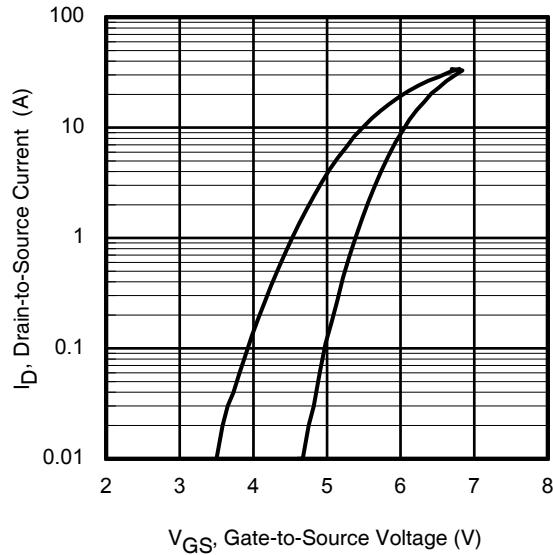
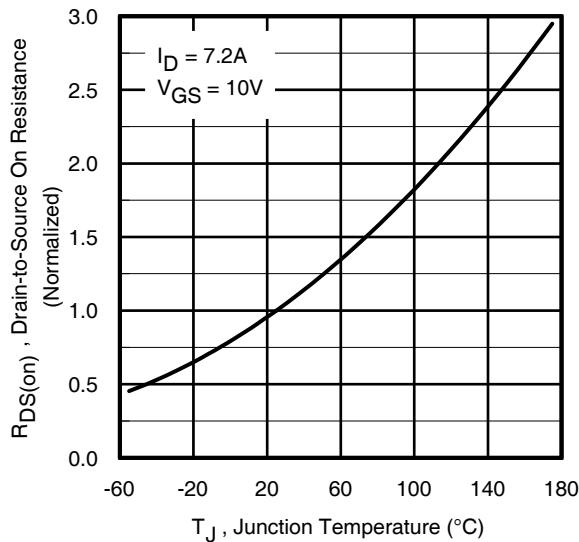
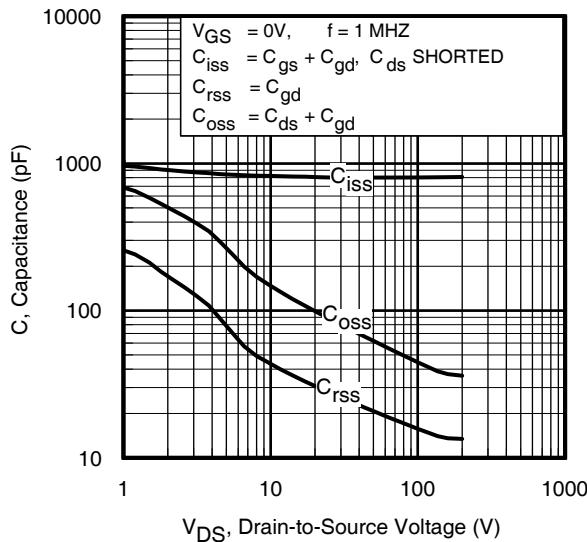
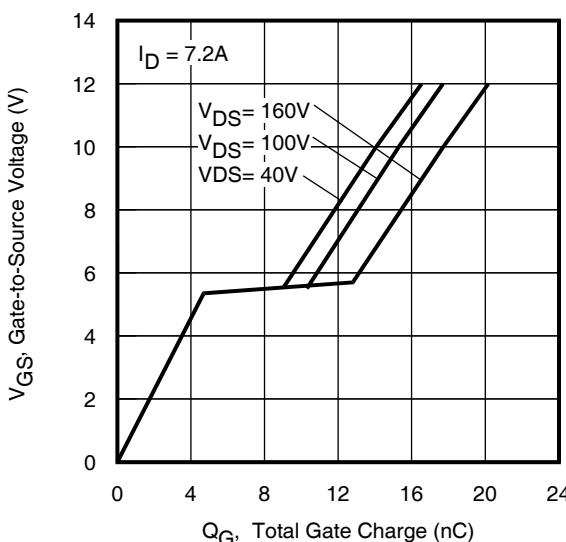
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ C$ ,  $L = 3.4mH$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 7.2A$ ,  $V_{GS} = 10V$ .
- ③  $I_{SD} \leq 7.2A$ ,  $dI/dt \leq 1184A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ C$ .
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ C$ .
- ⑧ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ C$ ,  $L = 1.0mH$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 11.5A$ ,  $V_{GS} = 10V$ .
- ⑨ This value determined from sample failure population, starting  $T_J = 25^\circ C$ ,  $L = 3.4mH$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 7.2A$ ,  $V_{GS} = 10V$ .

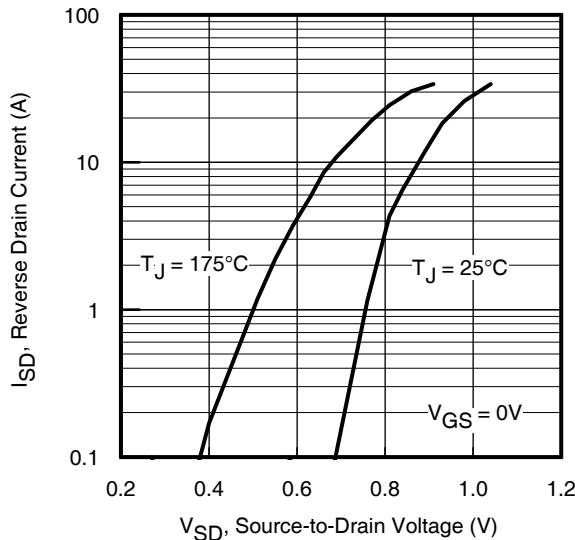
Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	13	—	—	S	$V_{DS} = 50\text{V}$ , $I_D = 7.2\text{A}$
$Q_g$	Total Gate Charge	—	15.3	23	nC	$I_D = 7.2\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	5.1	—		$V_{DS} = 100\text{V}$
$Q_{gd}$	Gate-to-Drain Charge	—	5.6	—		$V_{GS} = 10\text{V}$ <sup>④</sup>
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	10.2	—		
$t_{d(on)}$	Turn-On Delay Time	—	6.5	—	ns	$V_{DD} = 130\text{V}$
$t_r$	Rise Time	—	9.5	—		$I_D = 7.2\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	11.3	—		$R_G = 2.7\Omega$
$t_f$	Fall Time	—	6.5	—		$V_{GS} = 10\text{V}$ <sup>④</sup>
$C_{iss}$	Input Capacitance	—	790	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	62	—		$V_{DS} = 50\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	21	—		$f = 1.0\text{MHz}$ , See Fig.TBD
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	66	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $160\text{V}$ <sup>⑥</sup>
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	83	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $160\text{V}$ <sup>⑤</sup>

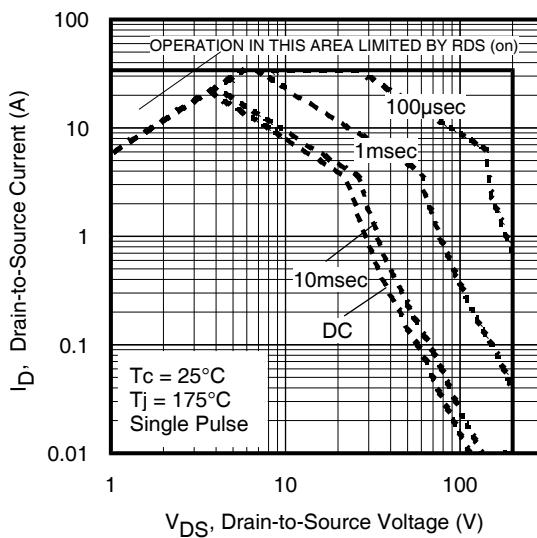
## Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	12	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	34		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = 7.2\text{A}$ , $V_{GS} = 0\text{V}$ ④
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	—	32.5	—	V/ns	$T_J = 175^\circ\text{C}$ , $I_S = 7.2\text{A}$ , $V_{DS} = 200\text{V}$
$t_{rr}$	Reverse Recovery Time	—	68	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 100\text{V}$
		—	83	—		$T_J = 125^\circ\text{C}$ $I_F = 7.2\text{A}$ ,
$Q_{rr}$	Reverse Recovery Charge	—	195	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ④
		—	280	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	4.3	—	A	$T_J = 25^\circ\text{C}$

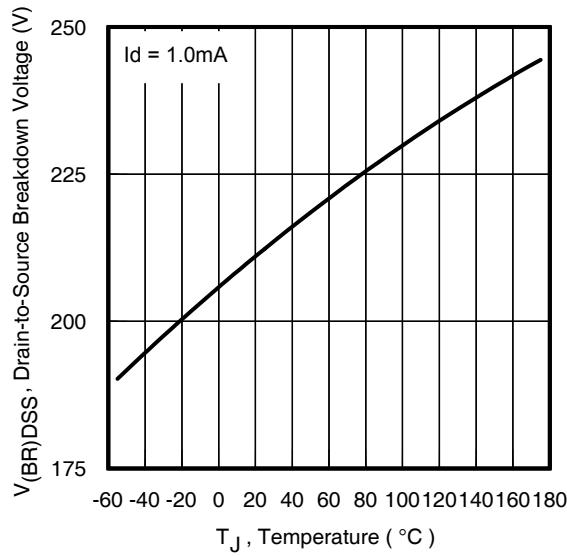
**Fig 3.** Typical Output Characteristics**Fig 4.** Typical Output Characteristics**Fig 5.** Typical Transfer Characteristics**Fig 6.** Normalized On-Resistance vs. Temperature**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage



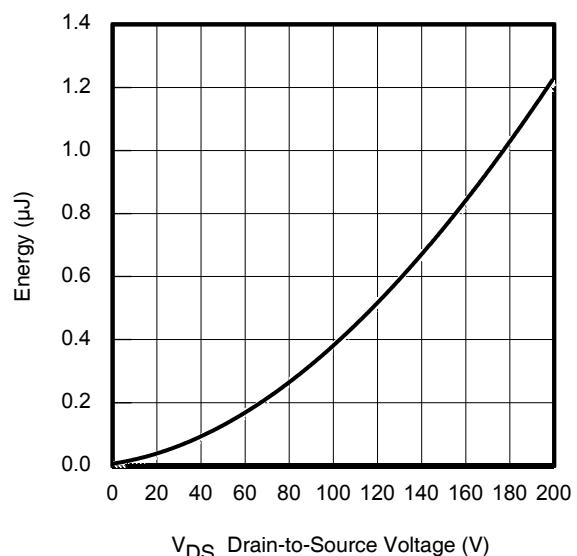
**Fig 9.** Typical Source-Drain Diode Forward Voltage



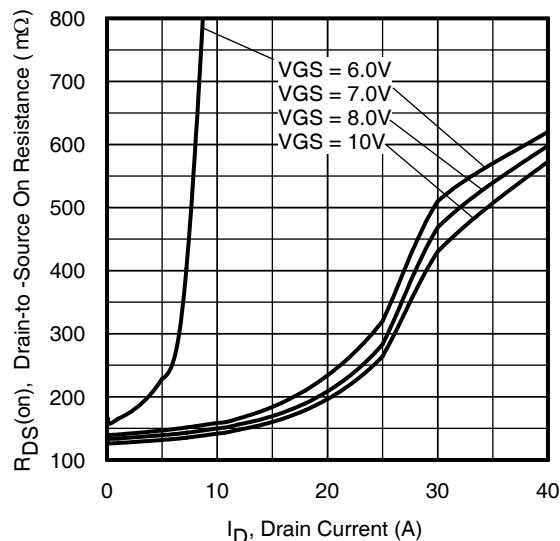
**Fig 10.** Maximum Safe Operating Area



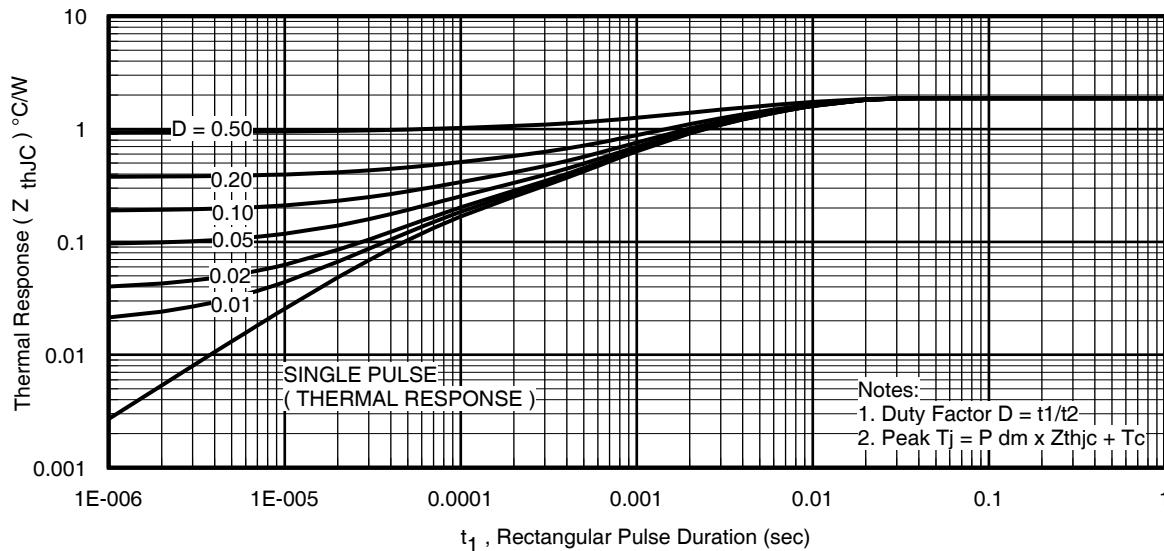
**Fig 11.** Drain-to-Source Breakdown Voltage



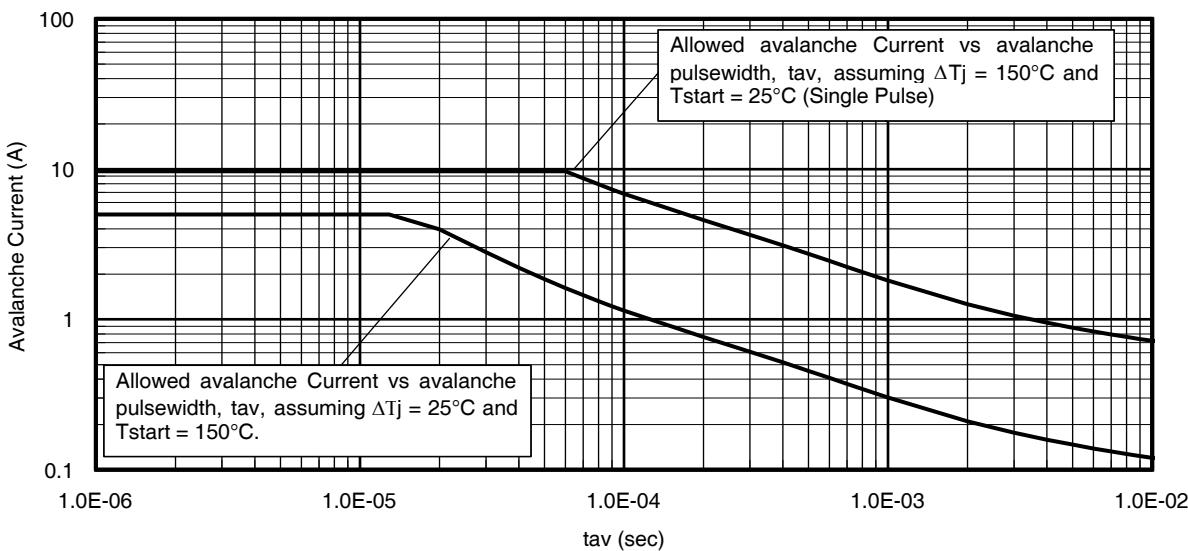
**Fig 12.** Typical  $C_{oss}$  Stored Energy



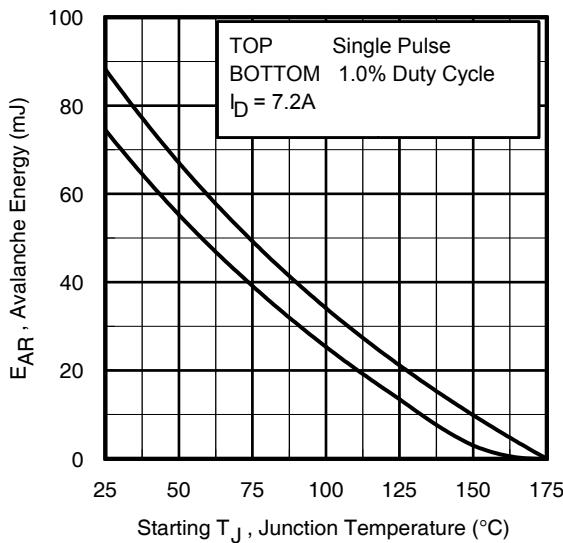
**Fig 13.** Typical On– Resistance vs. Drain Current



**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



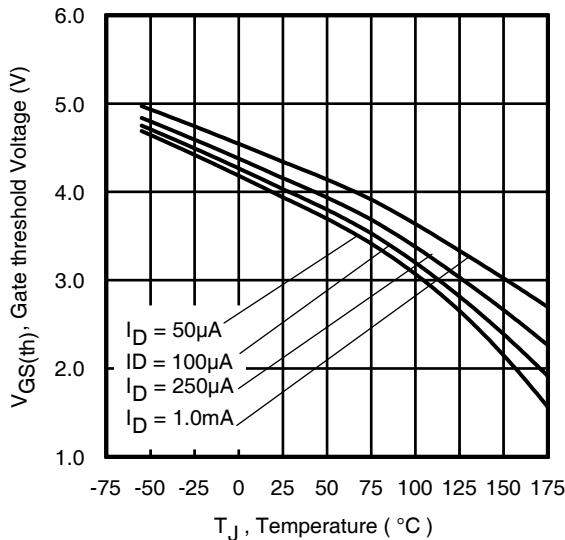
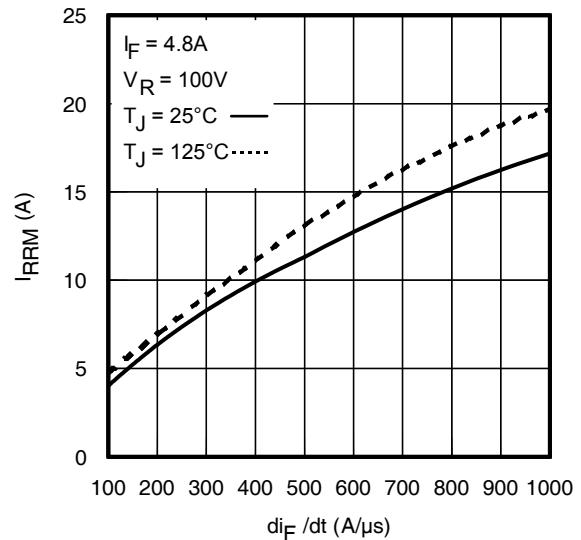
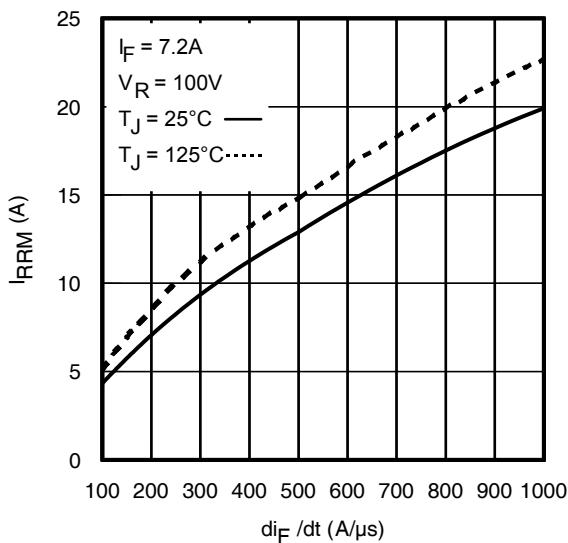
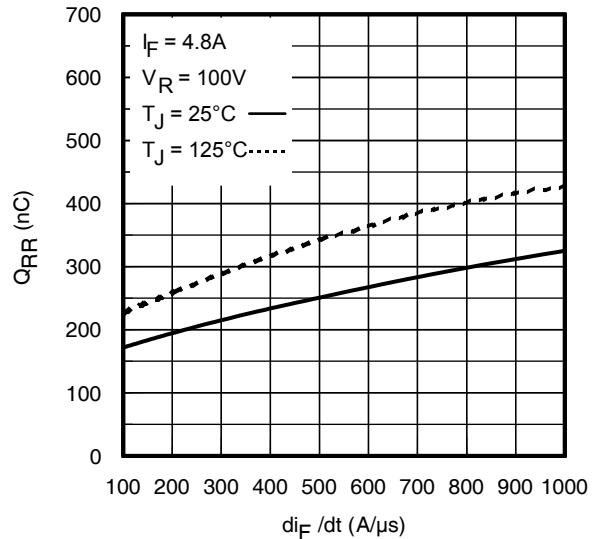
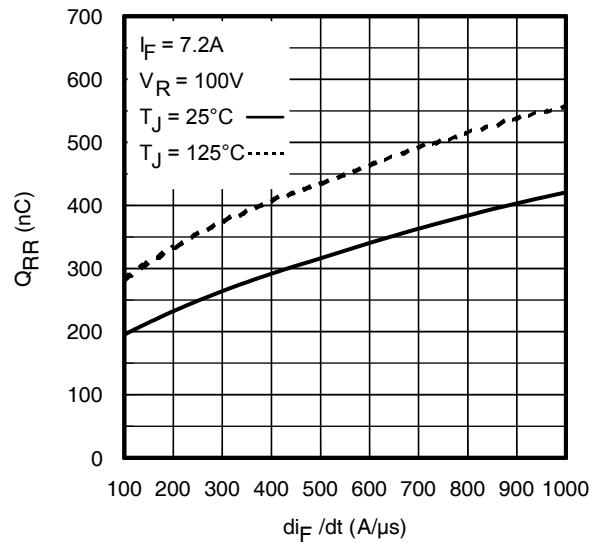
**Fig 15.** Avalanche Current vs. Pulse Width

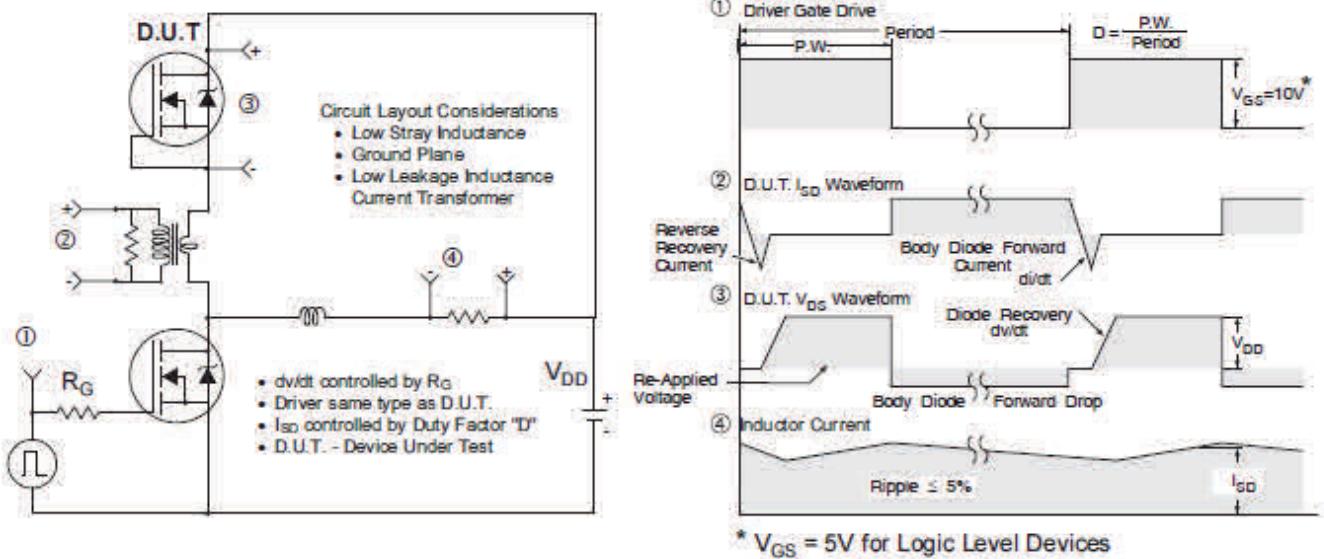


**Fig 16.** Maximum Avalanche Energy vs. Temperature

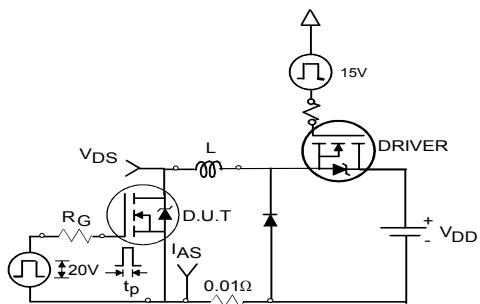
#### Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T<sub>jmax</sub>. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T<sub>jmax</sub> is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. P<sub>D</sub> (ave) = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I<sub>av</sub> = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T<sub>jmax</sub> (assumed as 25°C in Figure 14, 15).  
t<sub>av</sub> = Average time in avalanche.  
D = Duty cycle in avalanche = tav · f  
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 14)  
 $P_D \text{ (ave)} = 1/2 \cdot (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS (AR)} = P_D \text{ (ave)} \cdot t_{av}$

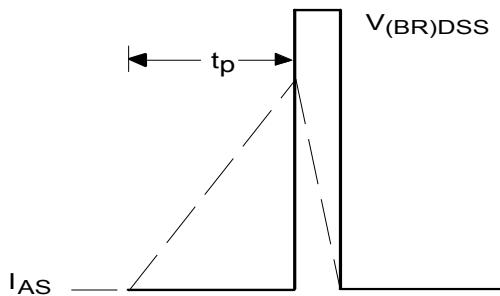
**Fig 17.** Threshold Voltage vs. Temperature**Fig 18.** Typical Recovery Current vs.  $di/dt$ **Fig 19.** Typical Recovery Current vs.  $di/dt$ **Fig 20.** Typical Stored Charge vs.  $di/dt$ **Fig 21.** Typical Stored Charge vs.  $di/dt$



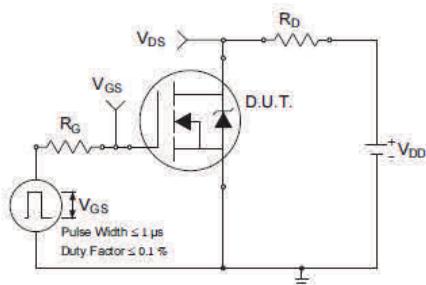
**Fig 22.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



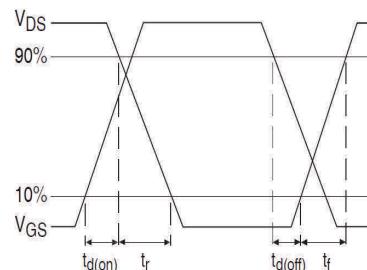
**Fig 23a.** Unclamped Inductive Test Circuit



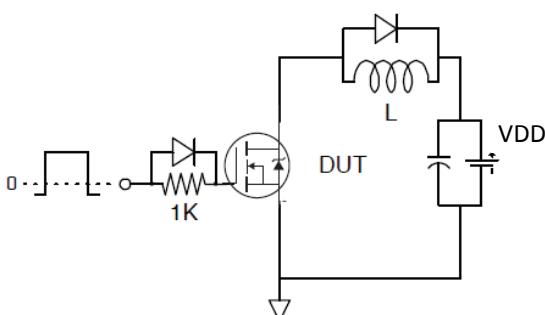
**Fig 23b.** Unclamped Inductive Waveforms



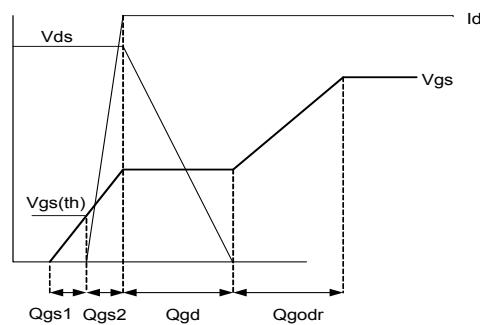
**Fig 24a.** Switching Time Test Circuit



**Fig 24b.** Switching Time Waveforms

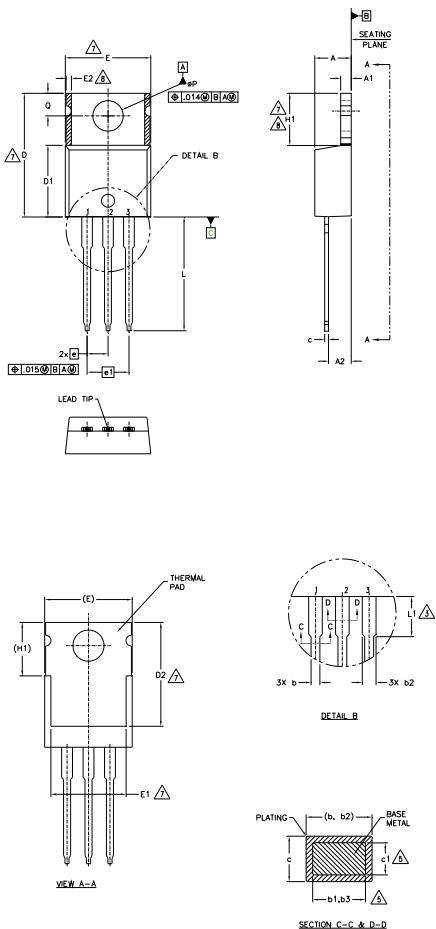


**Fig 25a.** Gate Charge Test Circuit



**Fig 25b.** Gate Charge Waveform

## TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



### NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E1,H1,D1 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.83	.140	.190		
A1	1.14	1.40	.045	.055		
A2	2.03	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.97	.015	.038	5	
b2	1.14	1.78	.045	.070	5	
b3	1.14	1.73	.045	.068	5	
c	0.36	0.61	.014	.024	5	
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650	4	
D1	8.38	9.02	.330	.355		
D2	11.68	12.88	.460	.507	7	
E	9.65	10.67	.380	.420	4,7	
E1	6.86	8.89	.270	.350	7	
E2	-	0.76	-	.030	8	
e	2.54	BSC	.100	BSC		
e1	5.08	BSC	.200	BSC	7,8	
H1	5.84	6.86	.230	.270		
L	12.70	14.73	.500	.580		
L1	3.56	4.06	.140	.160	3	
ØP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

#### IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter

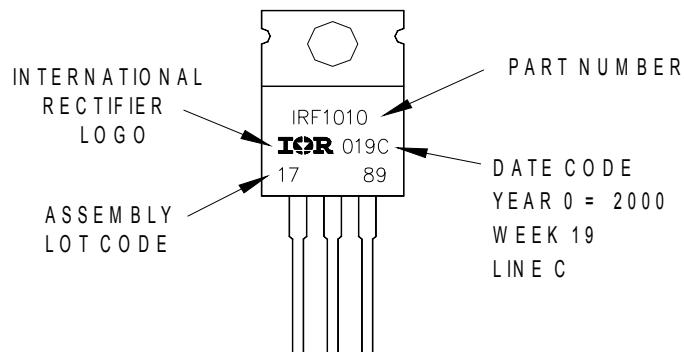
#### DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-220	N/A
<b>RoHS Compliant</b>	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

<sup>††</sup> Applicable version of JEDEC standard at the time of product release.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA  
To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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