

IRF3007PbF

Typical Applications

- Industrial Motor Drive

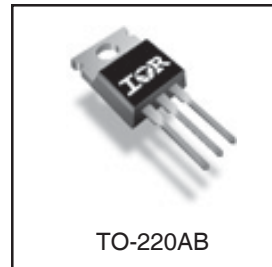
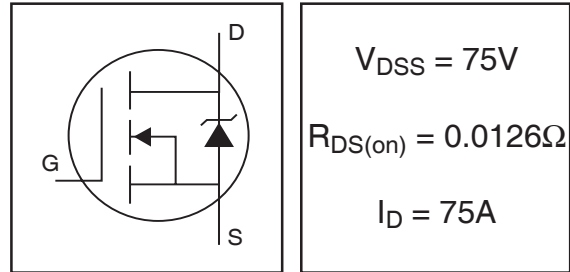
Features

- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free

Description

This design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

HEXFET® Power MOSFET



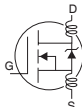
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon limited)	80	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig.9)	56	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package limited)	75	
I_{DM}	Pulsed Drain Current ①	320	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	280	mJ
E_{AS} (6 sigma)	Single Pulse Avalanche Energy Tested Value ②	946	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	1.1 (10)	N•m (lb•in)

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.74	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.084	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	10.5	12.6	mΩ	V _{GS} = 10V, I _D = 48A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	180	—	—	S	V _{DS} = 25V, I _D = 48A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	89	130	nC	I _D = 48A
Q _{gs}	Gate-to-Source Charge	—	21	32		V _{DS} = 60V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	30	45		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	12	—	ns	V _{DD} = 38V
t _r	Rise Time	—	80	—		I _D = 48A
t _{d(off)}	Turn-Off Delay Time	—	55	—		R _G = 4.6Ω
t _f	Fall Time	—	49	—		V _{GS} = 10V ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	3270	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	520	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	78	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	3500	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	340	—		V _{GS} = 0V, V _{DS} = 60V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	640	—		V _{GS} = 0V, V _{DS} = 0V to 60V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	80⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	320		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 48A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	85	130	ns	T _J = 25°C, I _F = 48A, V _{DD} = 38V
Q _{rr}	Reverse Recovery Charge	—	280	420	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T_J = 25°C, L = 0.24mH
R_G = 25Ω, I_{AS} = 48A, V_{GS} = 10V (See Figure 12).
- ③ I_{SD} ≤ 48A, di/dt ≤ 330A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.

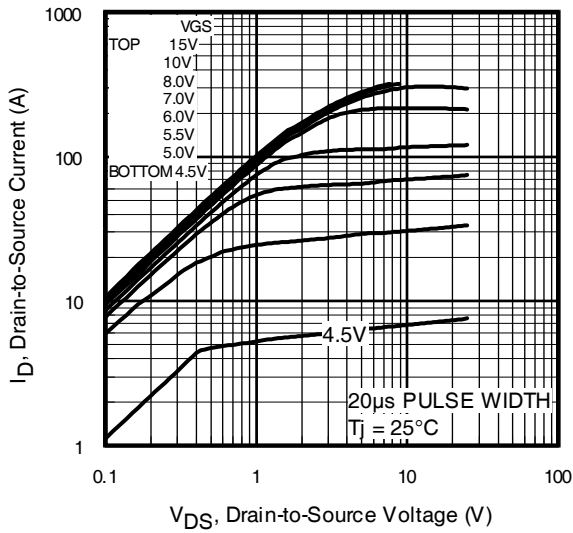


Fig 1. Typical Output Characteristics

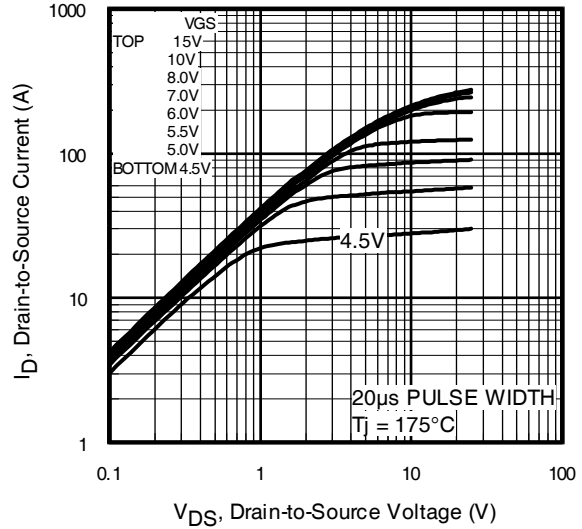


Fig 2. Typical Output Characteristics

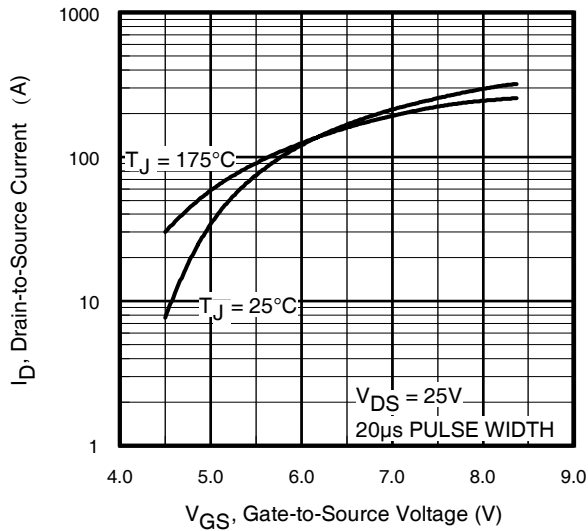


Fig 3. Typical Transfer Characteristics

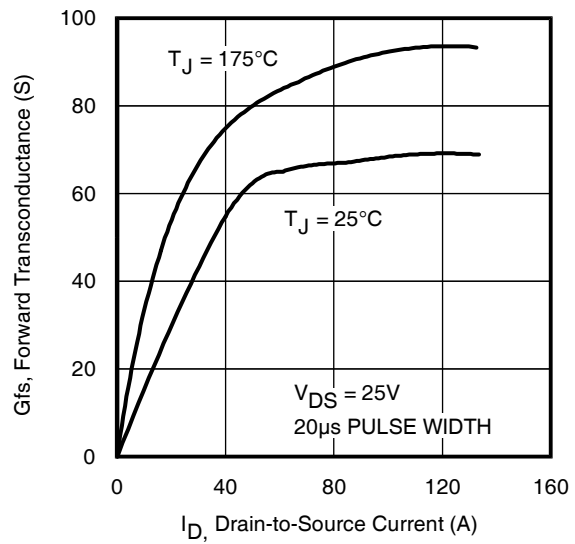


Fig 4. Typical Forward Transconductance Vs. Drain Current

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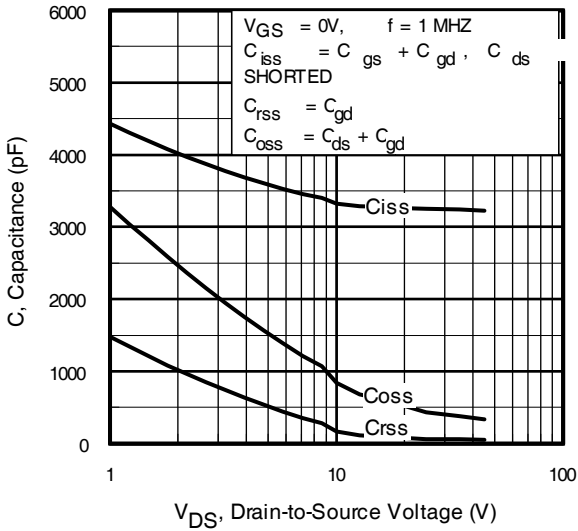


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

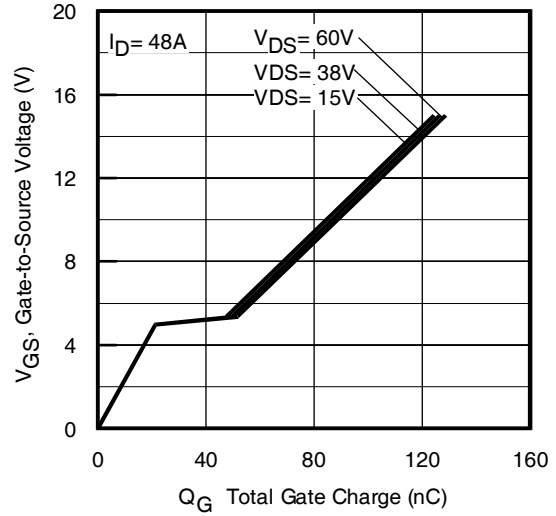


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

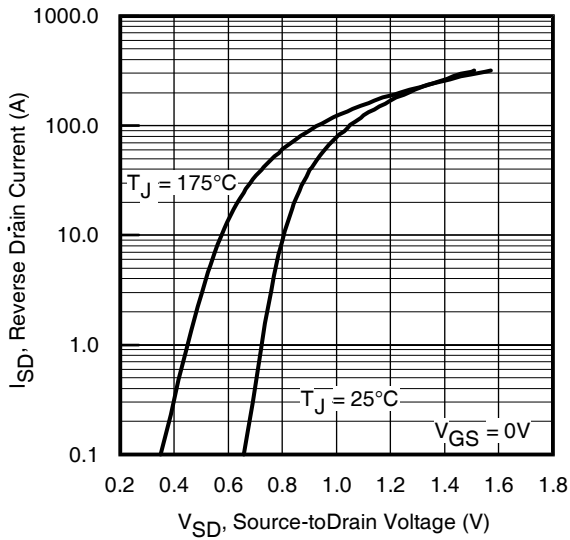


Fig 7. Typical Source-Drain Diode Forward Voltage

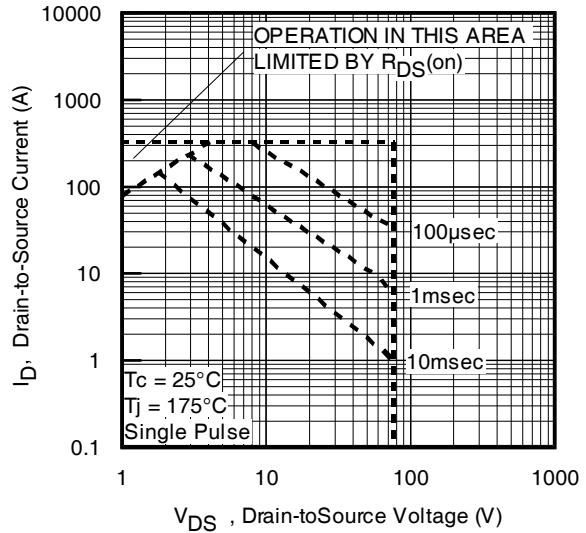


Fig 8. Maximum Safe Operating Area

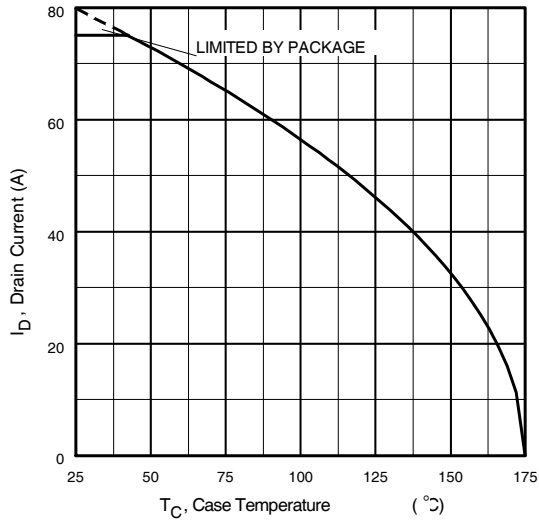


Fig 9. Maximum Drain Current Vs. Case Temperature

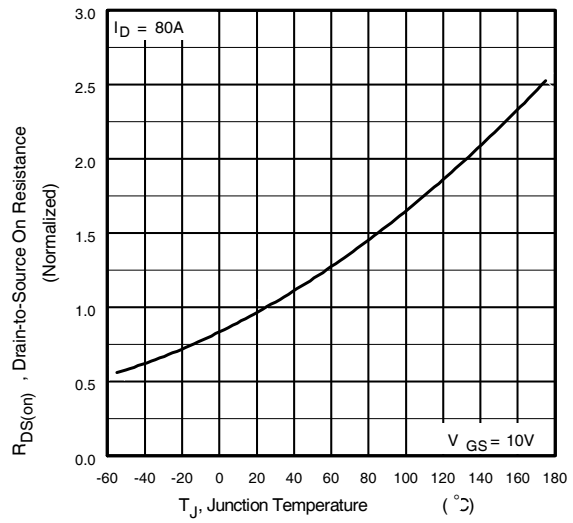


Fig 10. Normalized On-Resistance Vs. Temperature

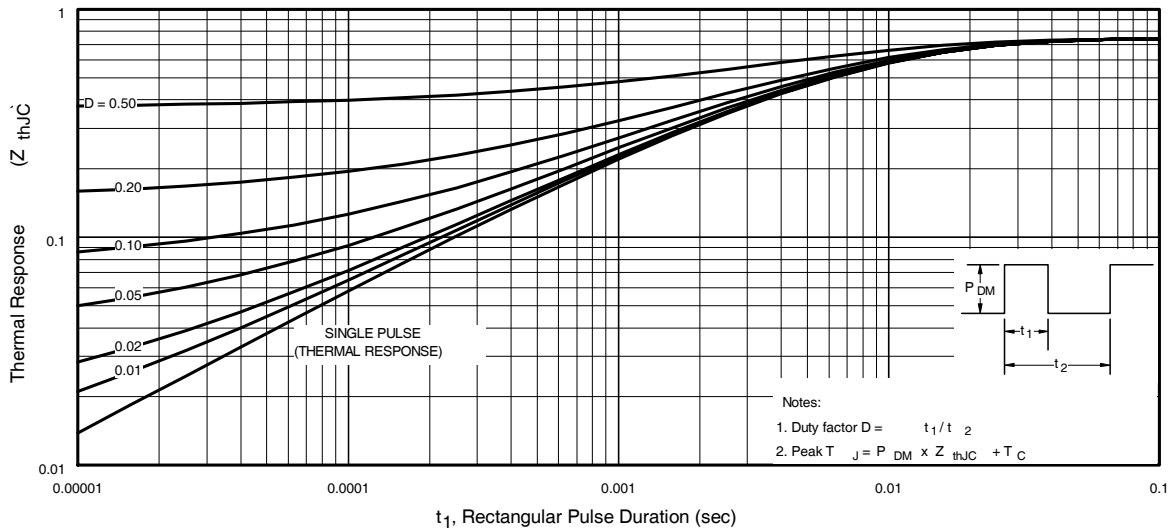


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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International
IR Rectifier

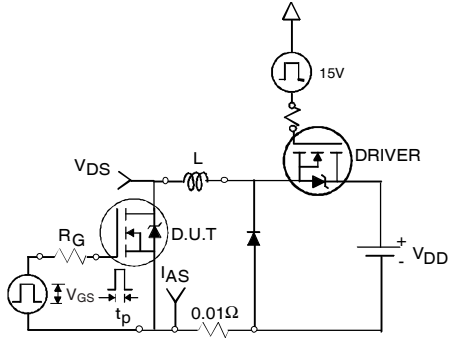


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform

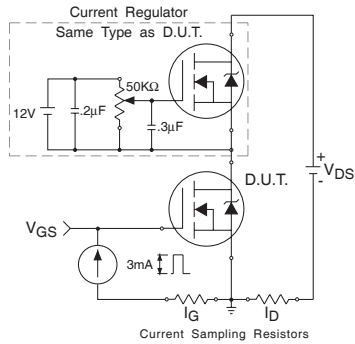


Fig 13b. Gate Charge Test Circuit

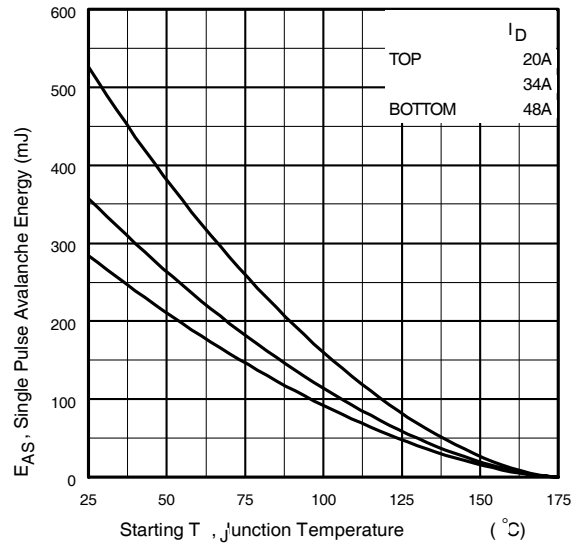


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

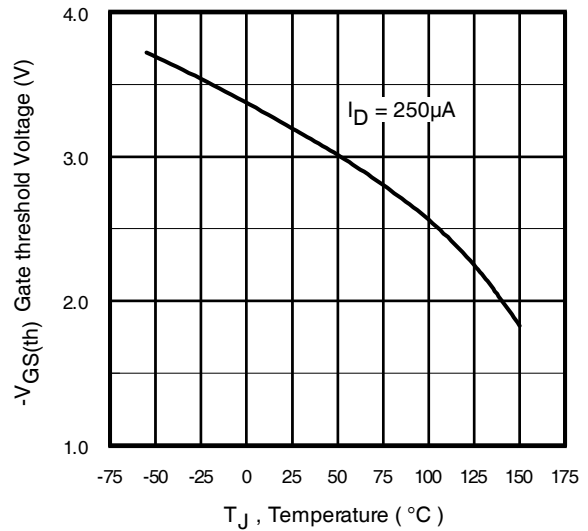


Fig 14. Threshold Voltage Vs. Temperature

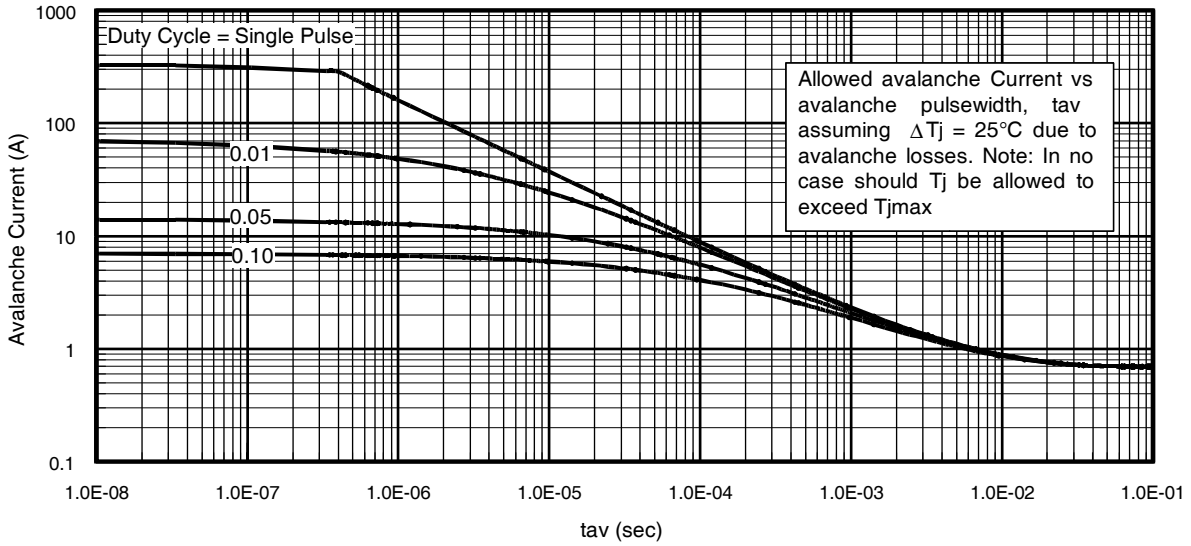


Fig 15. Typical Avalanche Current Vs. Pulsewidth

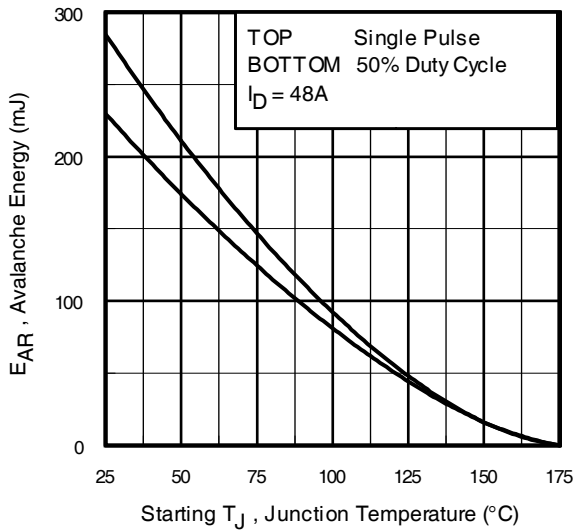


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

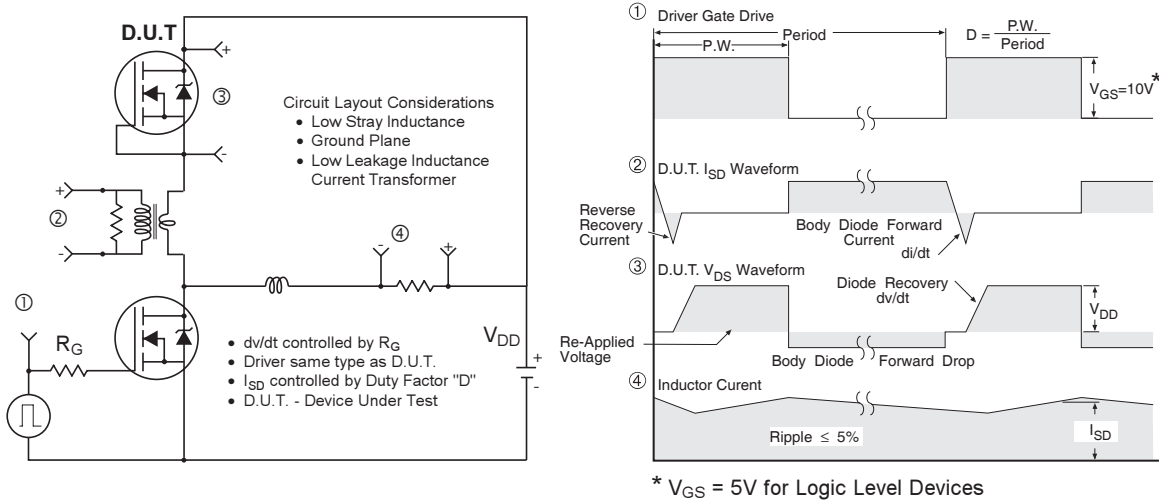


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

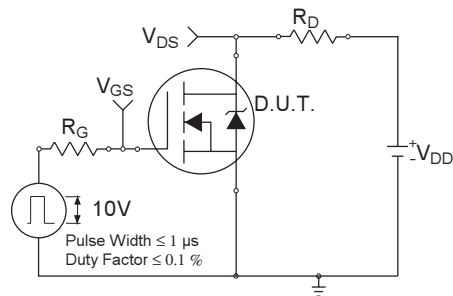


Fig 18a. Switching Time Test Circuit

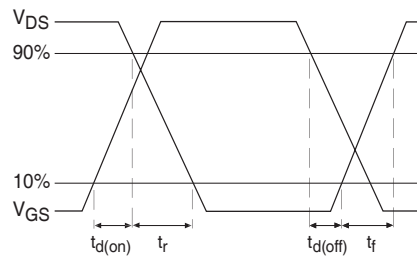
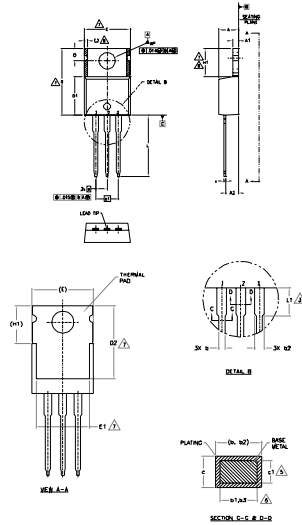


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1- DIMENSIONS AND TOLERANCING AS PER ASME Y14.5 M-1994
 - 2- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS)
 - 3- LEAD DIMENSION AND FINISH UNCONTROLLED IN LT
 - 4- DIMENSION G, D1 & E DO NOT INCLUDE MOLDFORMING. MOLDFORMING SHALL NOT EXCEED 0.007 (0.07) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EDGES OF THE PLASTIC BODY.
 - 5- DIMENSION M IS 0.125 (1/8) OF APPLY TO BASE METAL ONLY.
 - 6- CONTROLLING DIMENSIONS: INCHES
 - 7- THERMAL PAD CENTER OPTIMAL WITH DIMENSIONS (D1) D2 & E1
 - 8- DIMENSION (D1) IS NOT DEFINED A 20% WHITE STAMPING AND INSULATION PROTECTIONS ARE ALLOWED
 - 9- OUTLINE CONFORMS TO JEDEC TO-220 D (MILL) AND D2 (MILL) DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

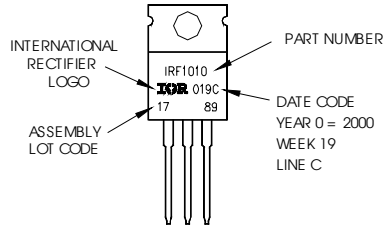
SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.43	.020	.056	
A2	2.03	2.92	.080	.115	
B	0.38	1.02	.015	.040	
B1	0.38	0.97	.015	.038	5
B2	1.14	1.78	.045	.070	
B3	1.14	1.73	.045	.068	5
C	0.36	0.61	.014	.024	
C1	0.36	0.56	.014	.022	5
D	14.32	16.51	.563	.650	4
D1	8.38	9.37	.330	.369	
D2	11.68	12.88	.460	.507	
E	9.85	10.67	.380	.420	4, 7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
F	-	-	-	-	
G	-	-	-	-	
H	5.84	6.86	.230	.270	7, 8
L	12.70	14.73	.500	.580	
L1	2.56	4.06	.100	.160	3
M	3.54	4.06	.139	.161	
Q	2.54	3.43	.100	.135	

- USE DIMENSIONS:
- 1- CASE
 - 2- BODY
 - 3- LEAD
 - 4- CENTER
 - 5- DIMENSION
 - 6- CENTER
 - 7- DIMENSION
 - 8- DIMENSION

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-220AB package is not recommended for Surface Mount Application

Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#)