

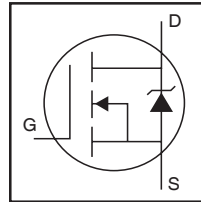
**Applications**

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

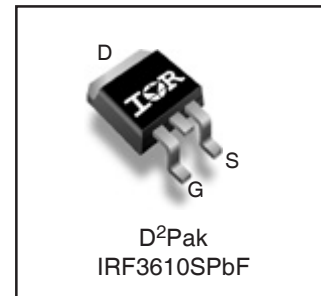
**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

HEXFET® Power MOSFET



$V_{DSS}$		<b>100V</b>
$R_{DS(on)}$	typ.	<b>9.3mΩ</b>
	max.	<b>11.6mΩ</b>
$I_D$		<b>103A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	103	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	73	
$I_{DM}$	Pulsed Drain Current ②	410	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	333	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	23	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

**Avalanche Characteristics**

$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	460	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ③⑤	—	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	—	40	

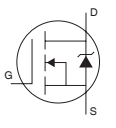
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	9.3	11.6	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 62A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	110	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 62A
R <sub>G</sub>	Internal Gate Resistance	—	2.2	—	Ω	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

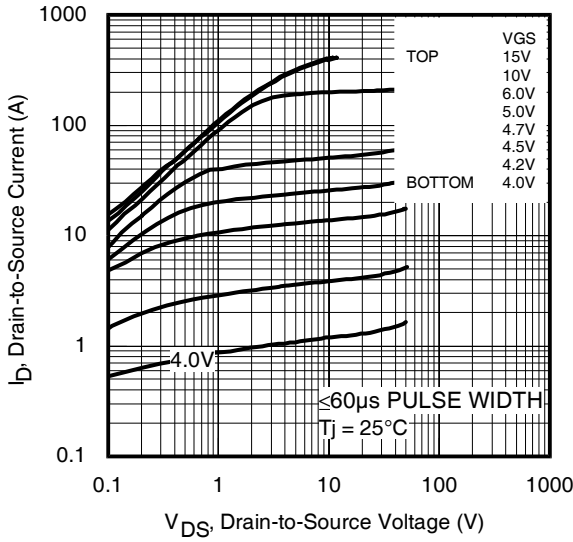
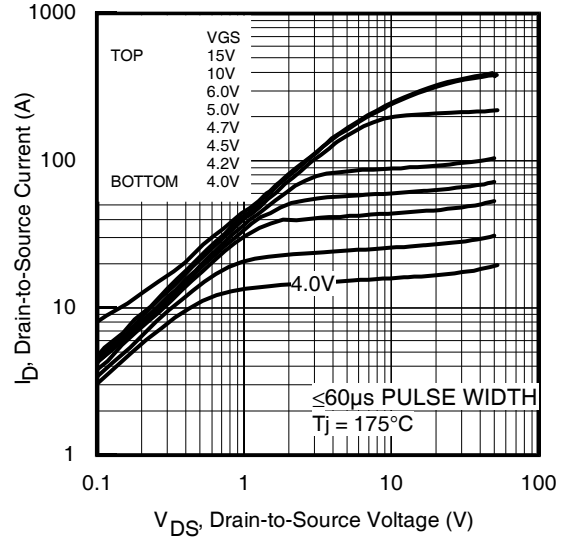
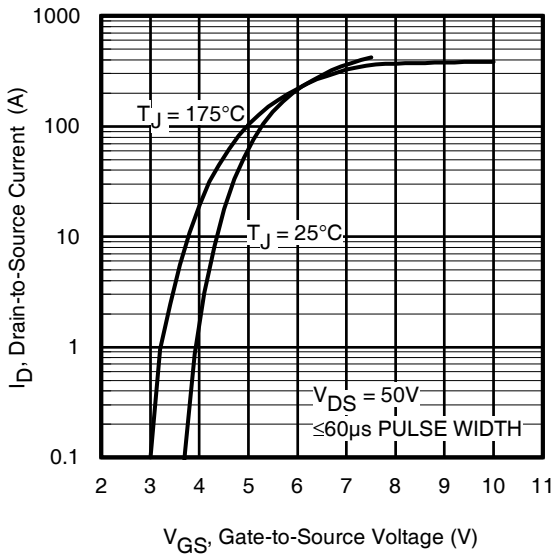
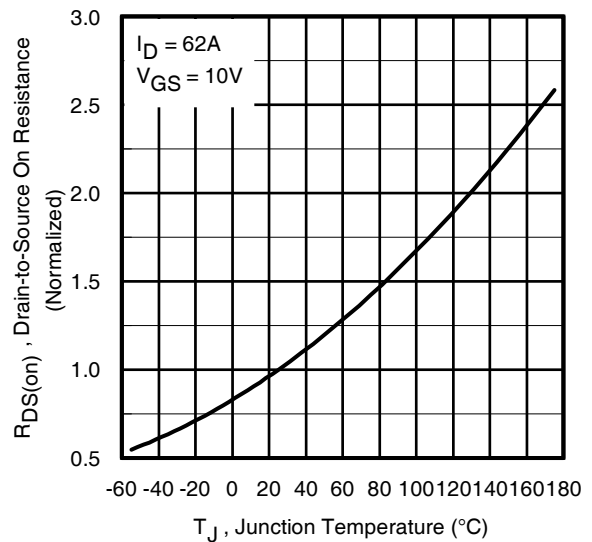
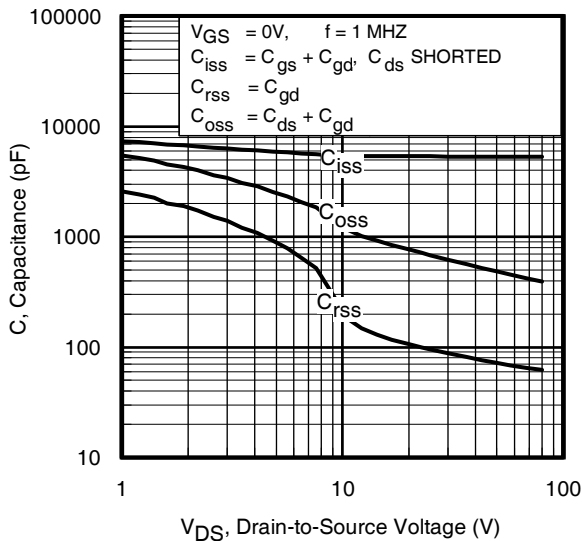
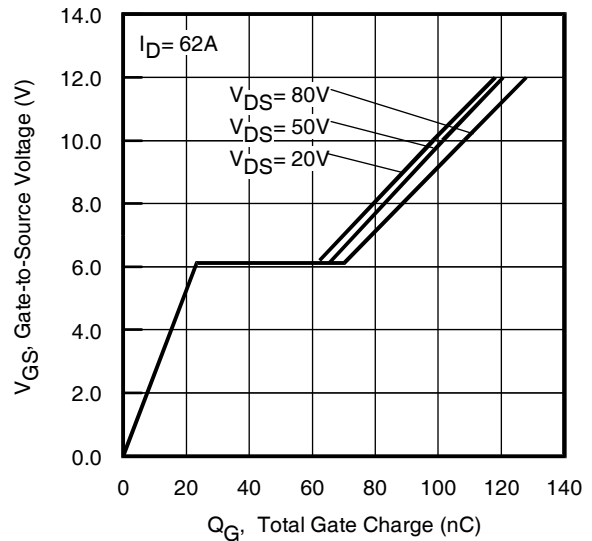
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q <sub>g</sub>	Total Gate Charge	—	100	150	nC	I <sub>D</sub> = 62A V <sub>DS</sub> = 50V V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>gs</sub>	Gate-to-Source Charge	—	23	—		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	42	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	58	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	15	—	ns	V <sub>DD</sub> = 65V
t <sub>r</sub>	Rise Time	—	55	—		I <sub>D</sub> = 62A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	77	—		R <sub>G</sub> = 2.7Ω
t <sub>f</sub>	Fall Time	—	43	—		V <sub>GS</sub> = 10V <sup>④</sup>
C <sub>iss</sub>	Input Capacitance	—	5380	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	690	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	100	—		f = 1.0 MHz, See Fig. 5
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)	—	560	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V <sup>⑥</sup> , See Fig. 11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related)	—	750	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V <sup>⑤</sup>

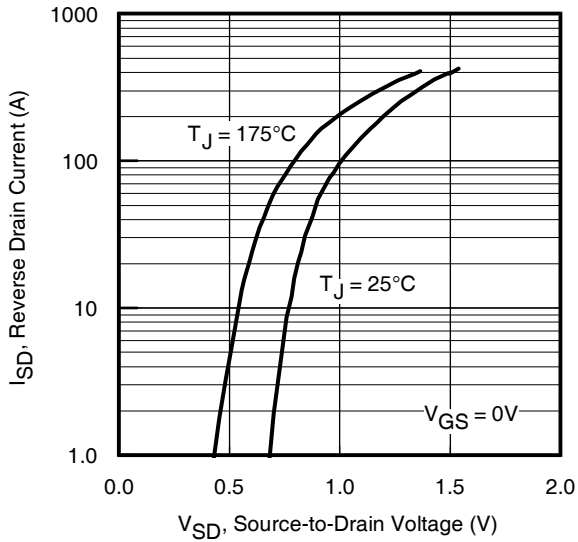
**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	103	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	410	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 62A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	110	—	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 85V, T <sub>J</sub> = 125°C I <sub>F</sub> = 62A
Q <sub>rr</sub>	Reverse Recovery Charge	—	570	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>④</sup> T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	-9.5	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

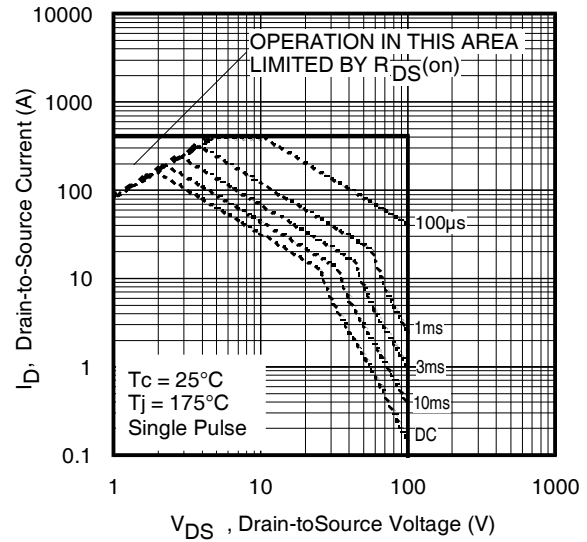
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.24mH  
R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 62A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 62A, di/dt ≤ 1935A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.
- ⑨ R<sub>θJC</sub> value shown is at time zero.

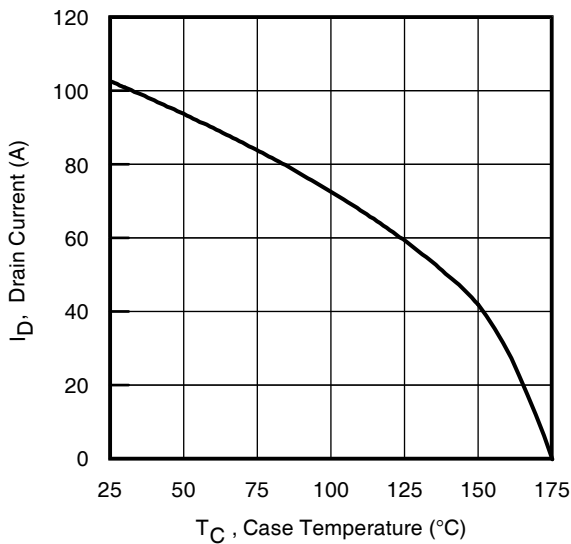

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**



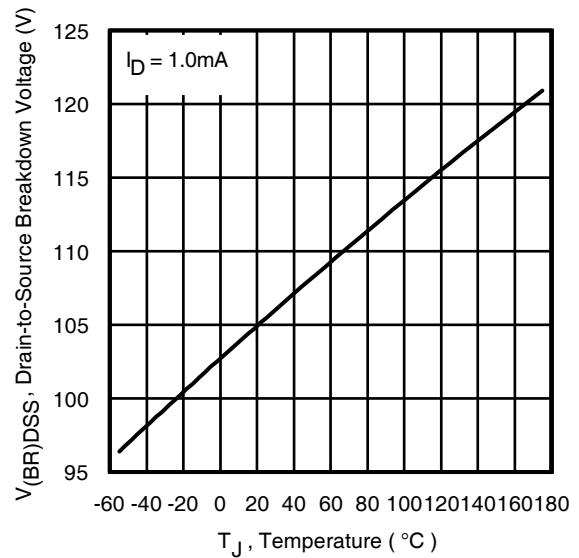
**Fig 7.** Typical Source-Drain Diode Forward Voltage



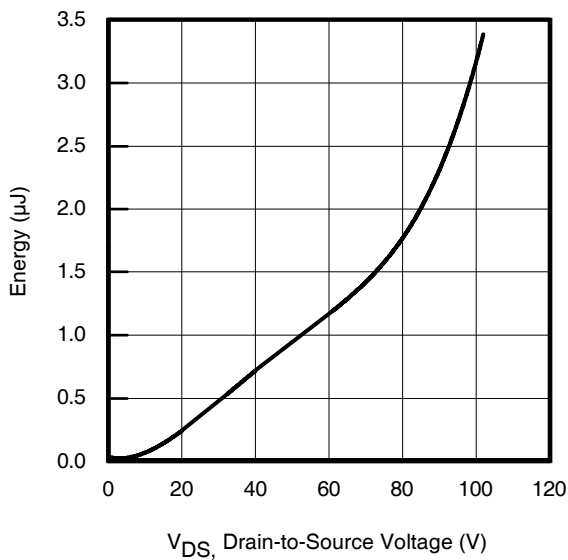
**Fig 8.** Maximum Safe Operating Area



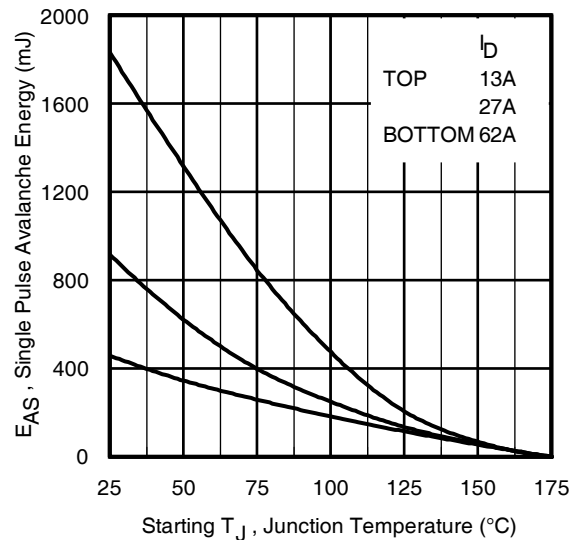
**Fig 9.** Maximum Drain Current vs. Case Temperature



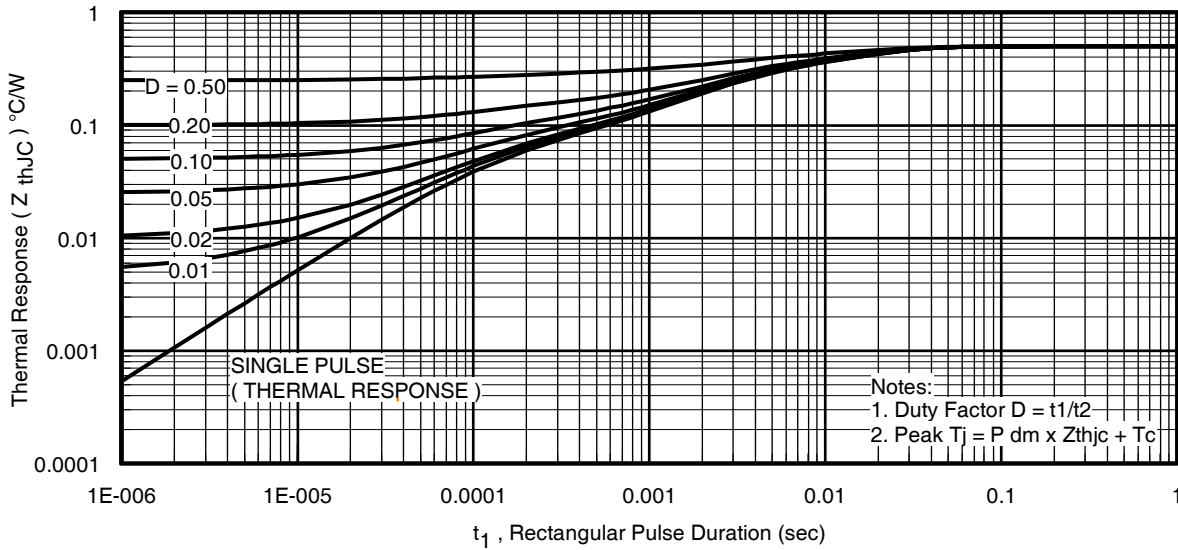
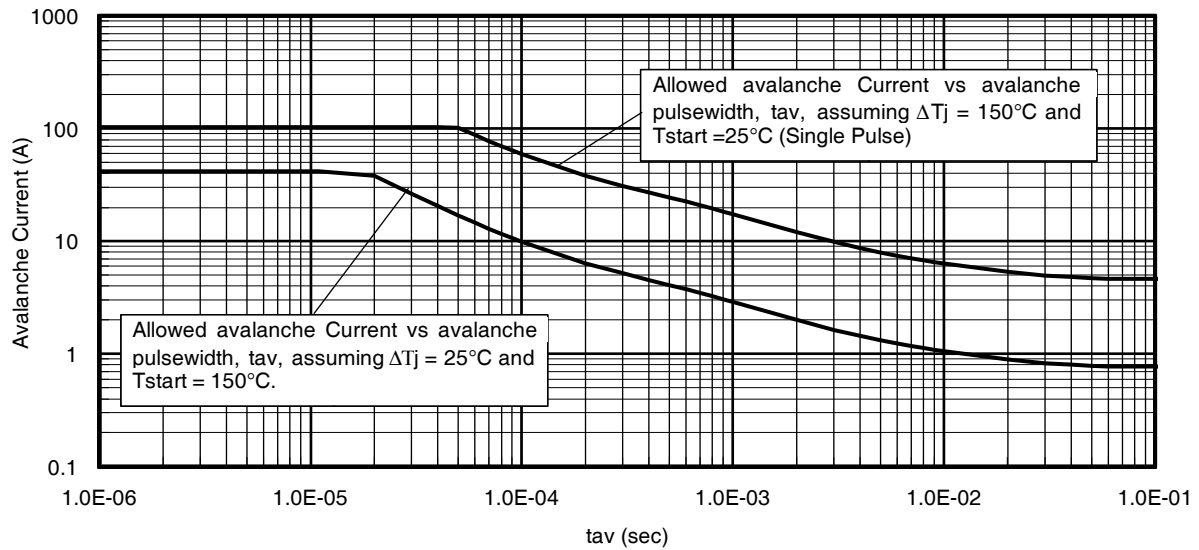
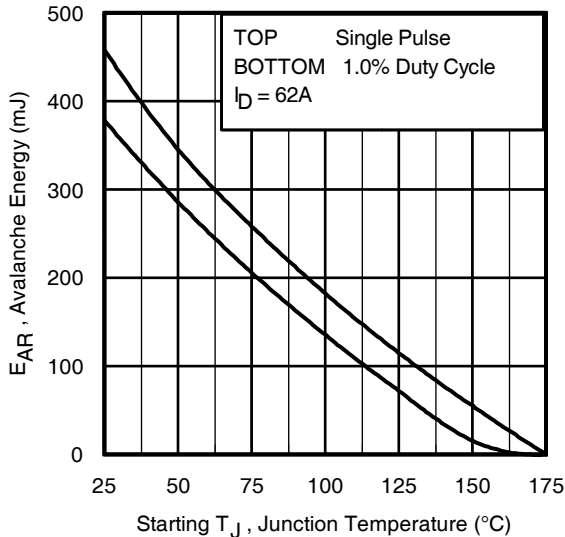
**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

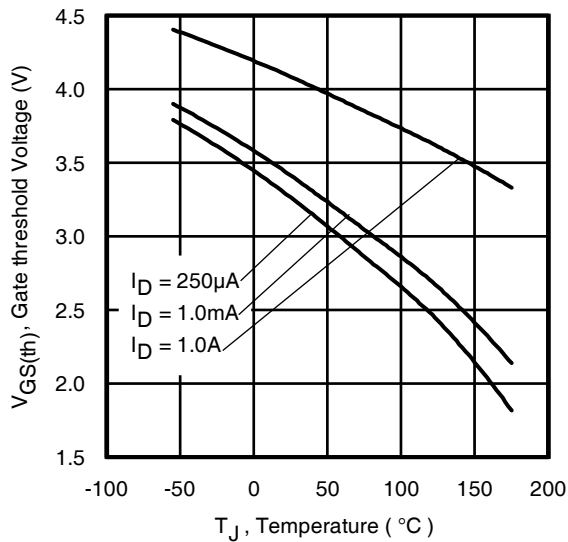
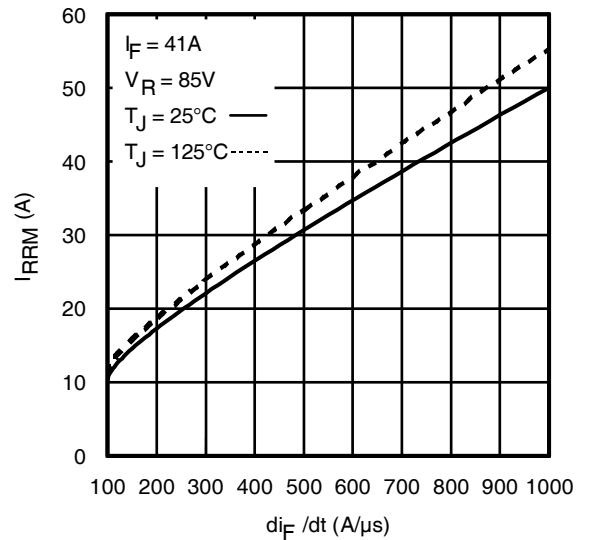
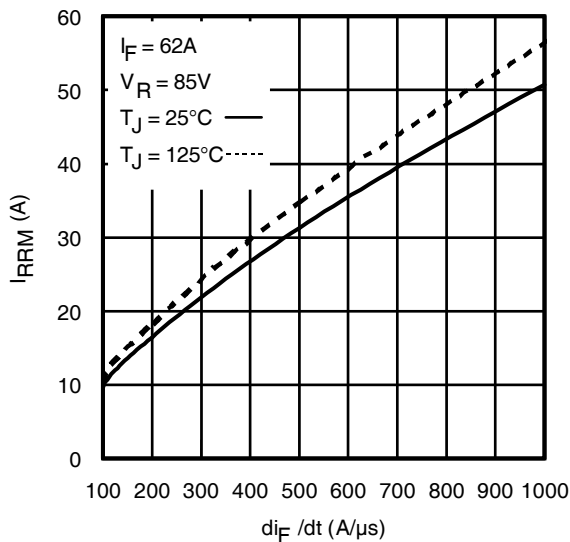
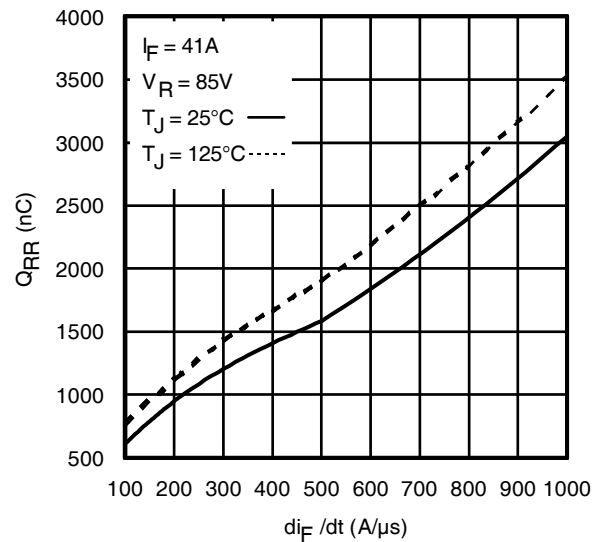
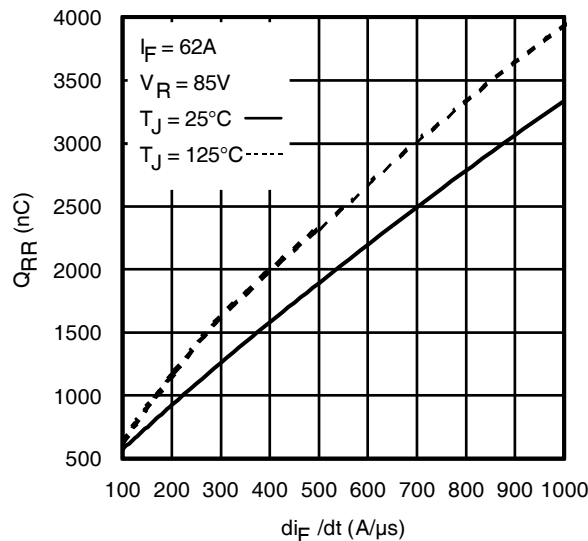

**Fig 13. Maximum Effective Transient Thermal Impedance Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulse Width**

**Fig 15. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

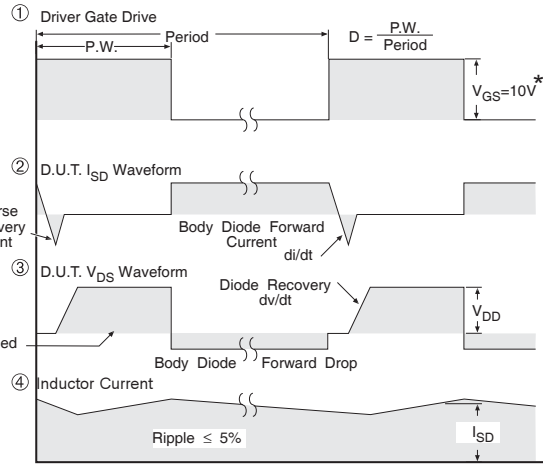
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 13, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig 16.** Threshold Voltage vs. Temperature

**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 18 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 19 -** Typical Stored Charge vs.  $di_F/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



**Fig 22a. Unclamped Inductive Test Circuit**



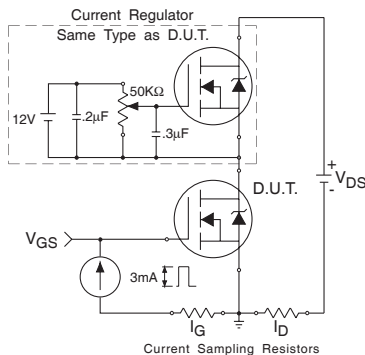
**Fig 22b. Unclamped Inductive Waveforms**



**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



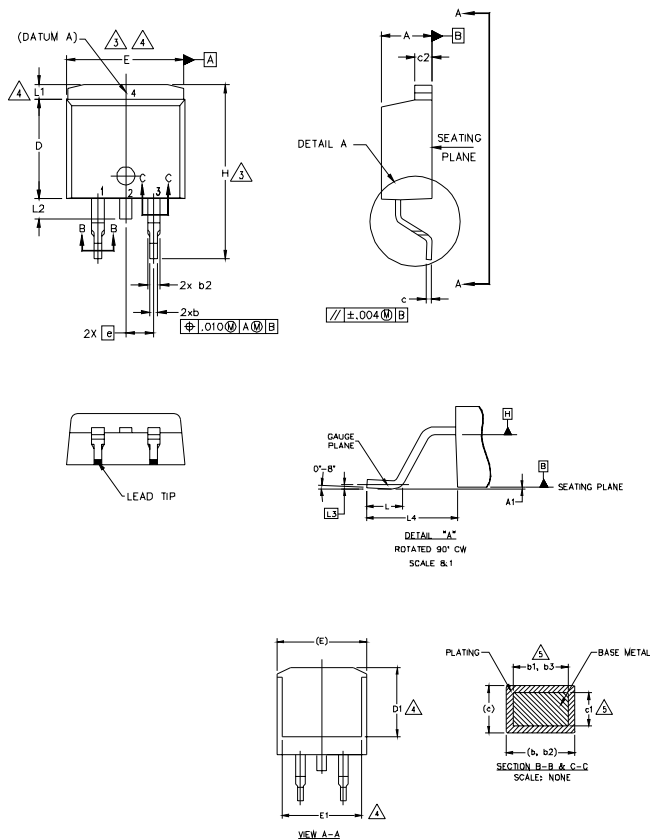
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

## D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	5
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3, 4
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

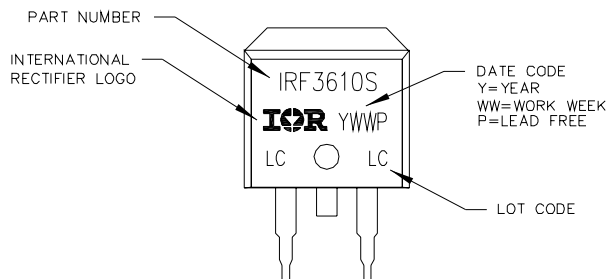
- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

**DIODES**

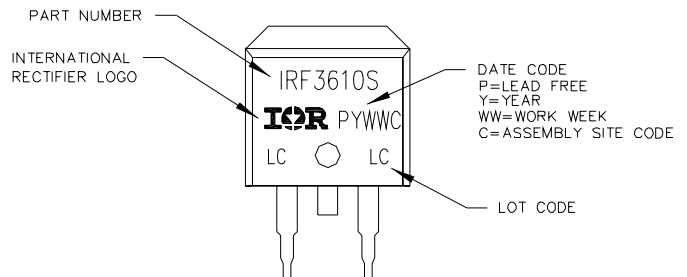
- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

\* PART DEPENDENT.

## D<sup>2</sup>Pak (TO-263AB) Part Marking Information



OR

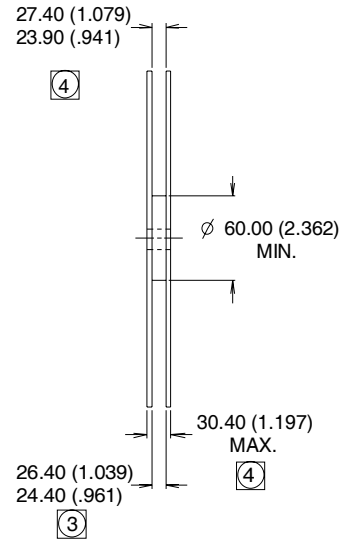
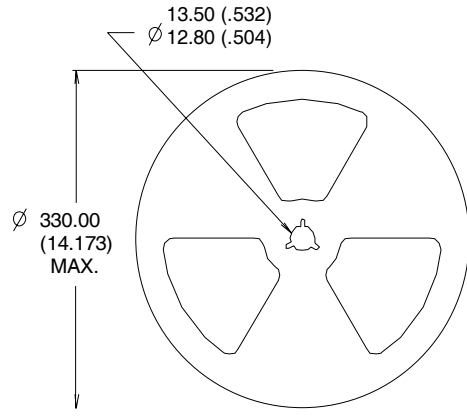
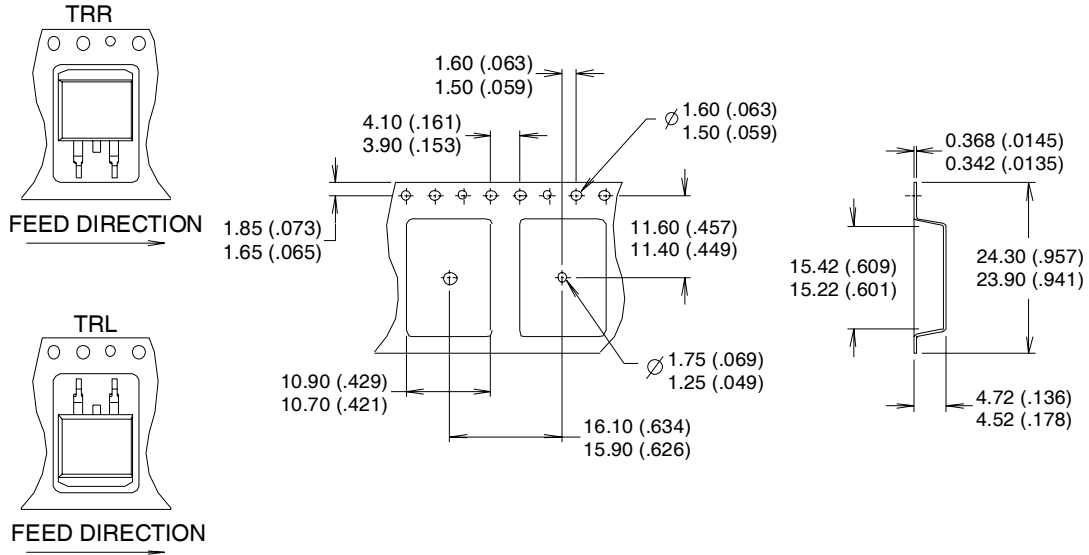


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



## D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#)