

MOSFET

MOSFET - StrongIRFET™

Benefits

- Optimized for broadest availability from distribution partners
- 175°C junction temperature rated
- 100% UIL tested
- Product validation according to JEDEC standard
- Pb-Free ; RoHS Compliant ; Halogen-Free

Potential applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies

Product validation

Fully qualified according to JEDEC for Industrial Applications

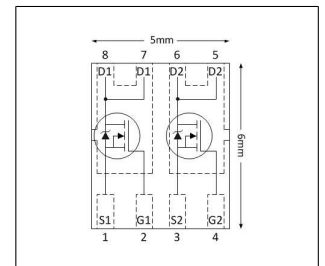
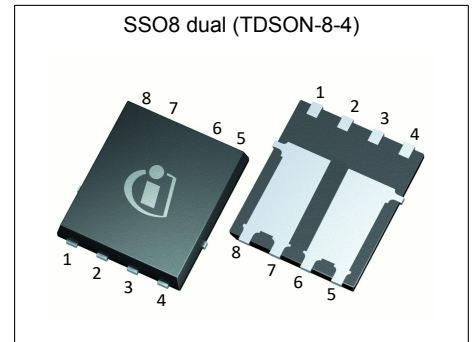


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),typ}$	5.1	$m\Omega$
$R_{DS(on),max}$	6.2	$m\Omega$
I_D	65	A



Type / Ordering Code	Package	Marking	Related Links
IRF40H233	PG-TDSON-8-4	H233	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	65 46 35	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	260	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	71	mJ	$I_D=35\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	50 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}^4)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom ⁵⁾	R_{thJC}	-	-	3	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	45	°C/W	-
Device on PCB, 6 cm ² cooling area ⁴⁾	R_{thJA}	-	-	40	°C/W	-
Device on PCB, RTHJA(<10s)	R_{thJA}	-	-	25	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁵⁾ RthJC is measured at Tj approximately 90°C.

3 Electrical characteristics
 at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	41	-	mV/°C	$I_D=1\text{ mA}$, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.9	V	$V_{DS}=V_{GS}$, $I_D=50\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1 150	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.1	6.2	m Ω	$V_{GS}=10\text{ V}$, $I_D=35\text{ A}$
Gate resistance ¹⁾	R_G	-	1.8	-	Ω	-
Transconductance	g_{fs}	-	60	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=35\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	2200	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	380	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	260	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=26\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=35\text{ A}$, $R_{G,ext}=2.7\text{ }\Omega$
Rise time	t_r	-	67	-	ns	$V_{DD}=26\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=35\text{ A}$, $R_{G,ext}=2.7\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	$V_{DD}=26\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=35\text{ A}$, $R_{G,ext}=2.7\text{ }\Omega$
Fall time	t_f	-	30	-	ns	$V_{DD}=26\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=35\text{ A}$, $R_{G,ext}=2.7\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	$V_{DD}=20\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	6.7	-	nC	$V_{DD}=20\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	15.7	-	nC	$V_{DD}=20\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	20.6	-	nC	$V_{DD}=20\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	45	57	nC	$V_{DD}=20\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	$V_{DD}=20\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	38	-	-	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ²⁾	Q_{oss}	-	13	-	-	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	39	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	260	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.94	1.3	V	$V_{GS}=0\text{ V}, I_F=35\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	22	-	ns	$V_R=34\text{ V}, I_F=35\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	16	-	nC	$V_R=34\text{ V}, I_F=35\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

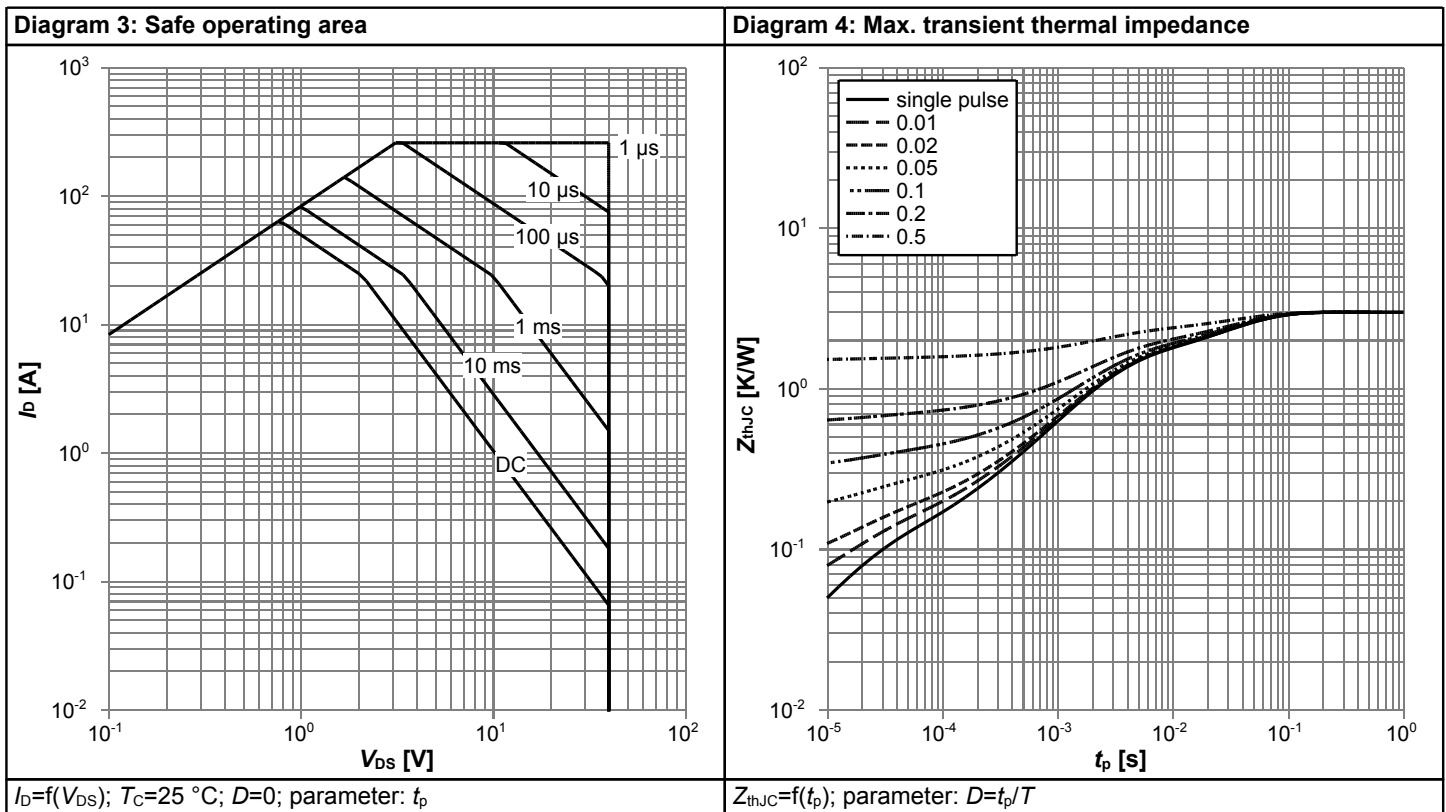
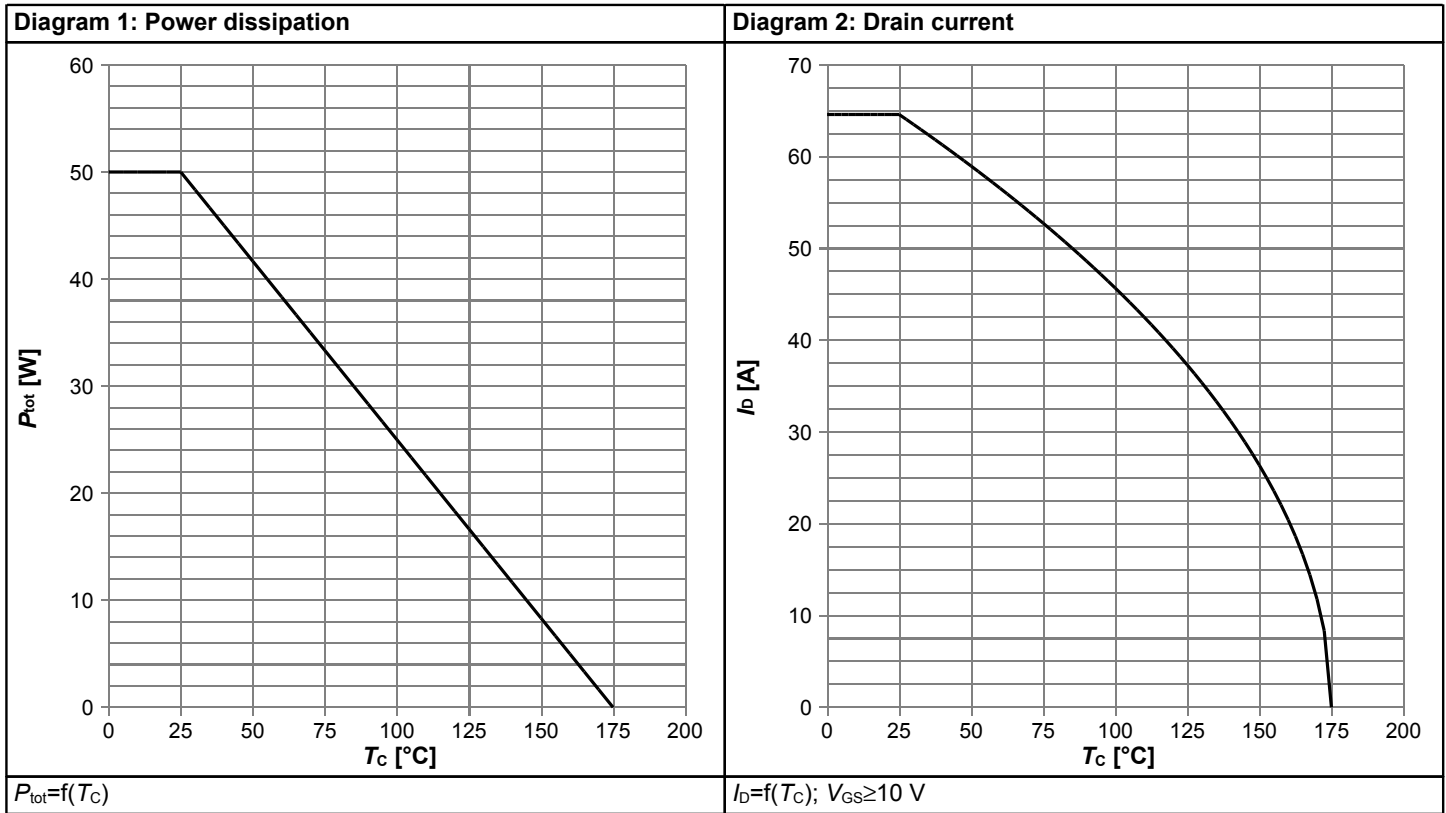
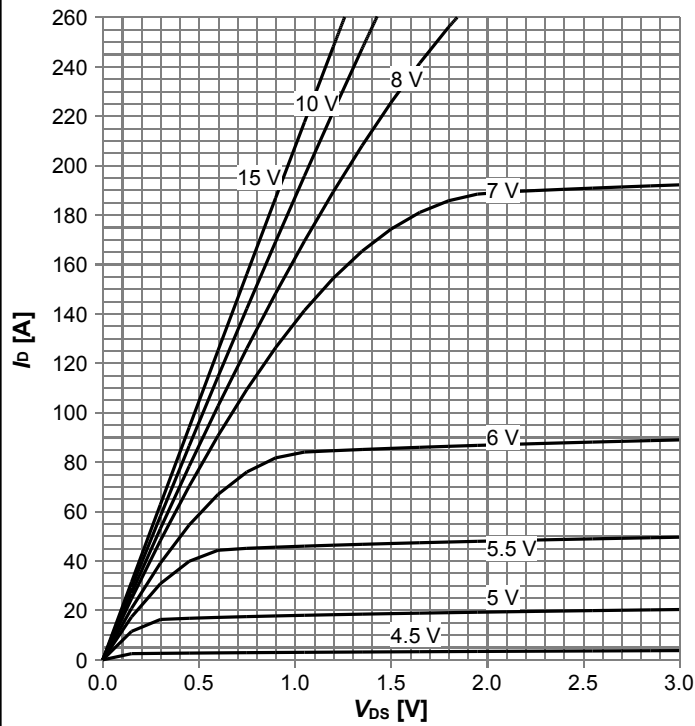
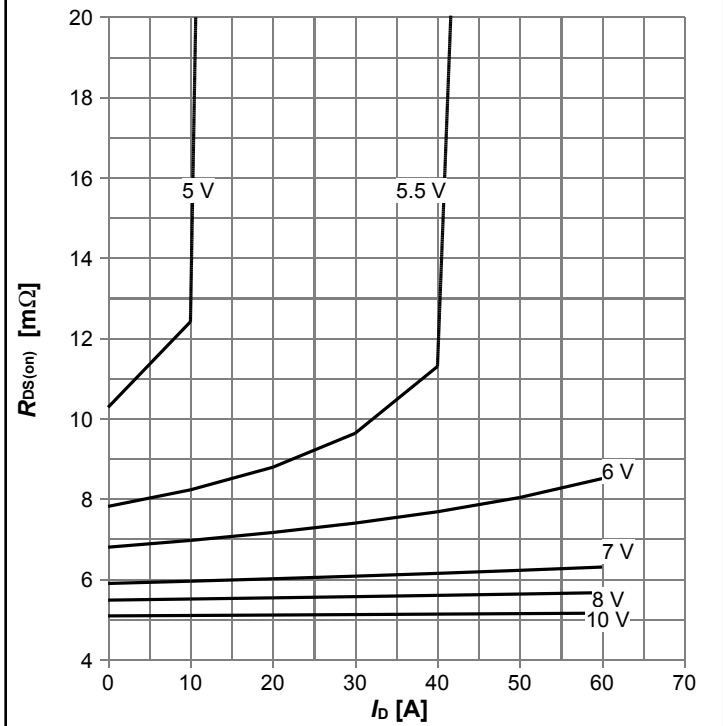


Diagram 5: Typ. output characteristics



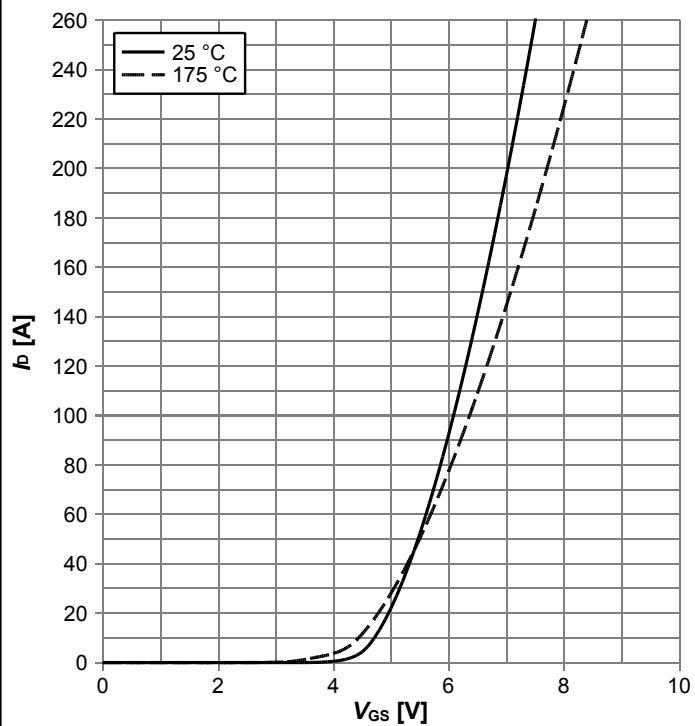
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



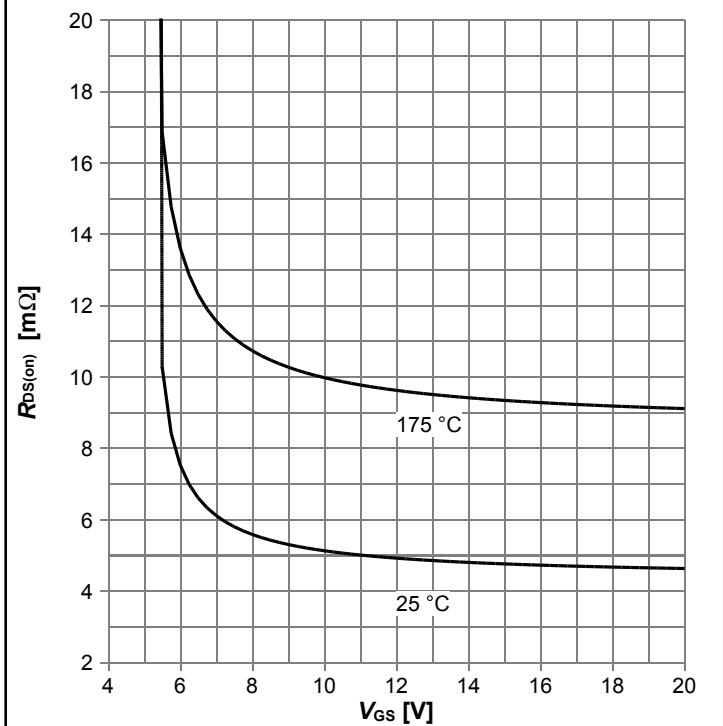
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



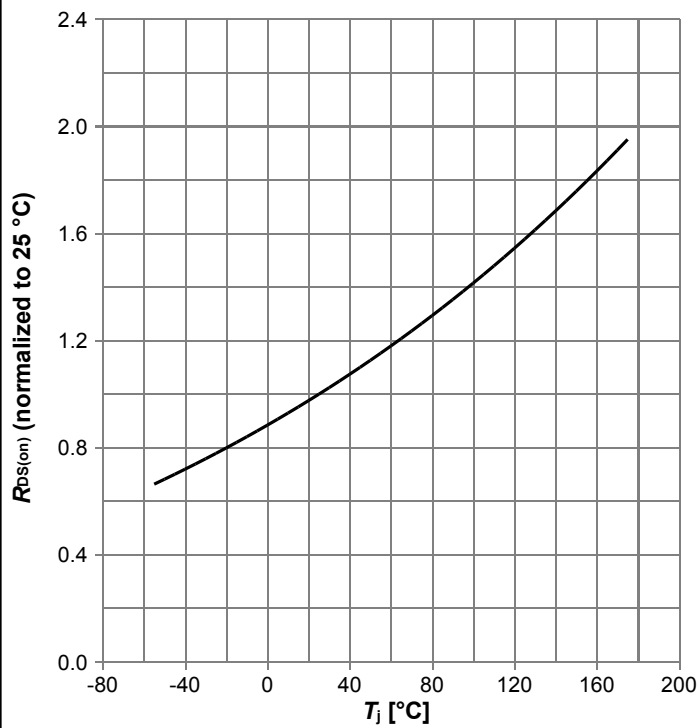
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



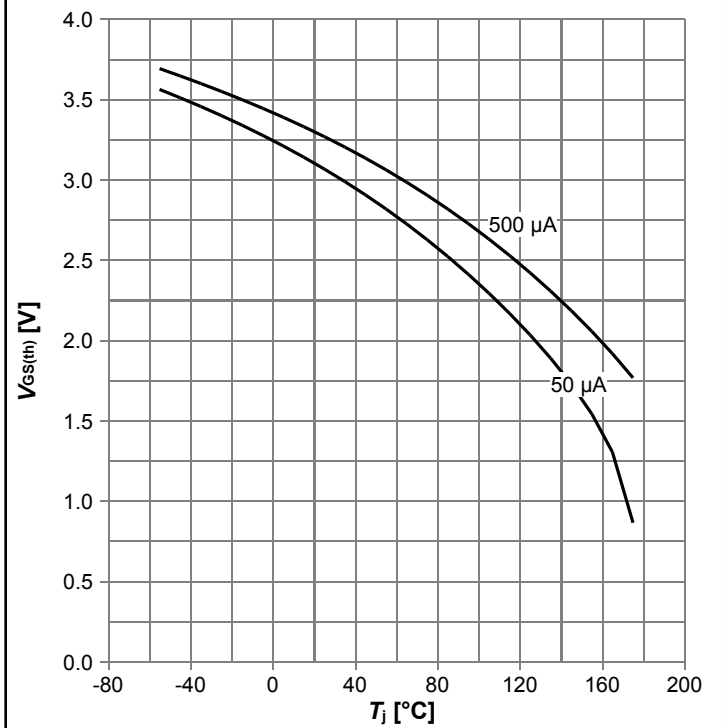
$R_{DS(on)} = f(V_{GS})$, $I_D = 35\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



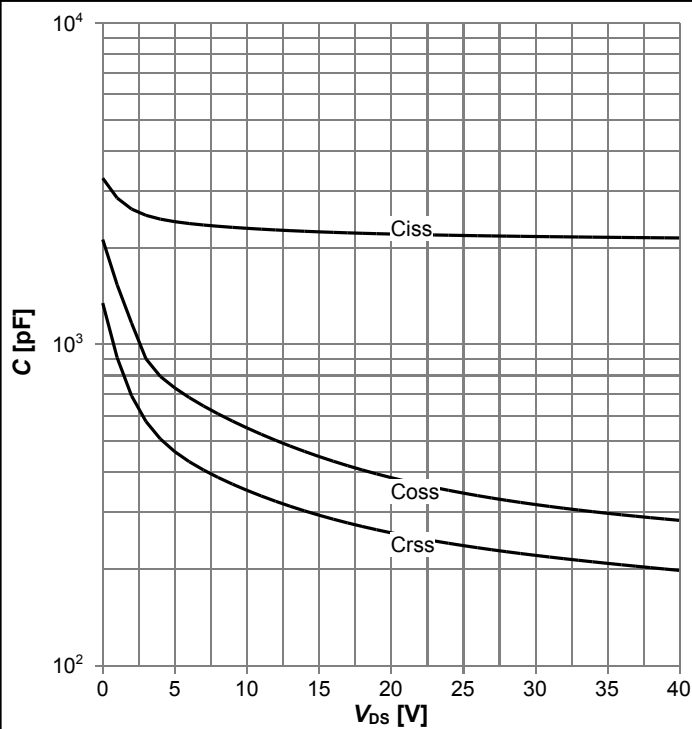
$R_{DS(on)}=f(T_j)$, $I_D=35\text{ A}$, $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



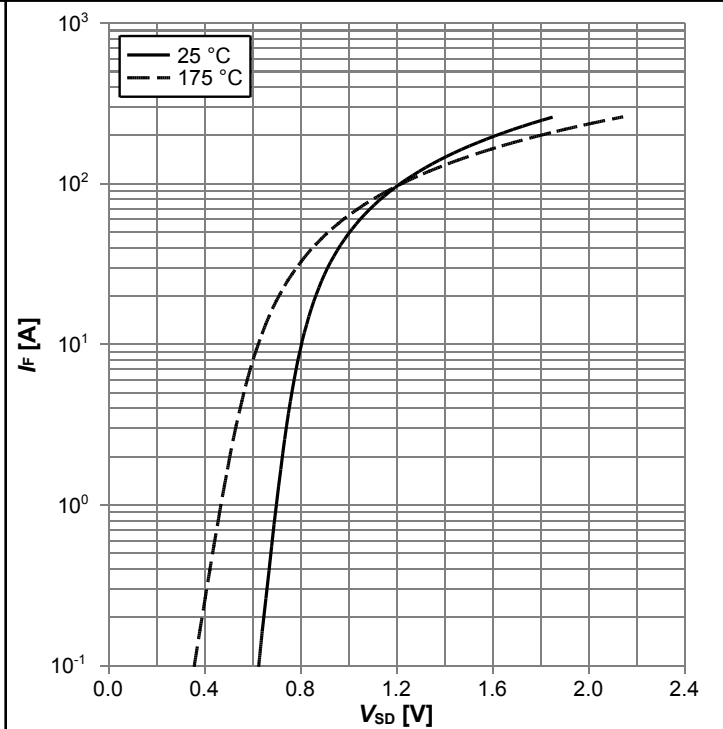
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



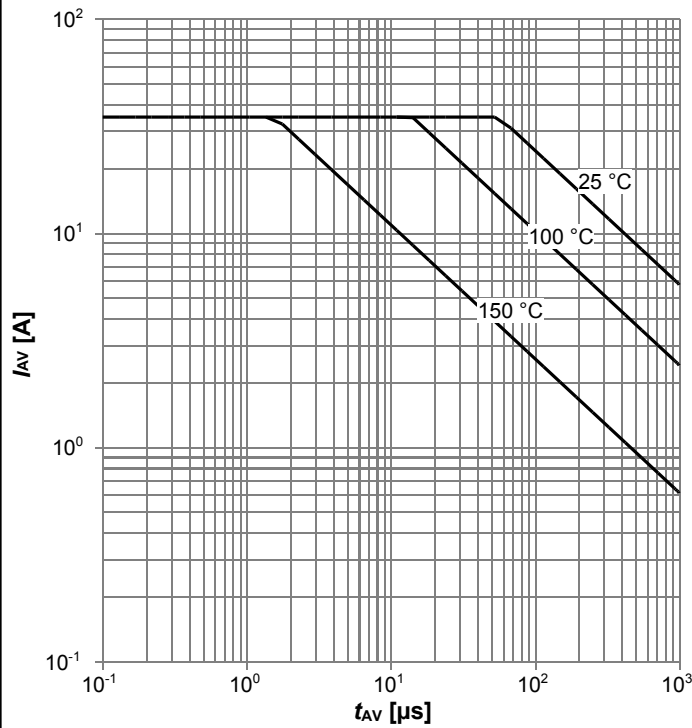
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



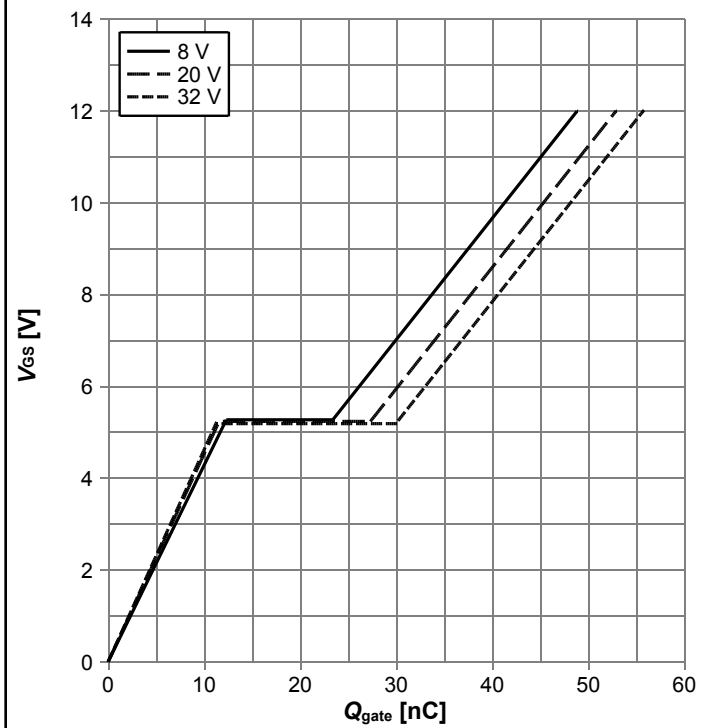
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



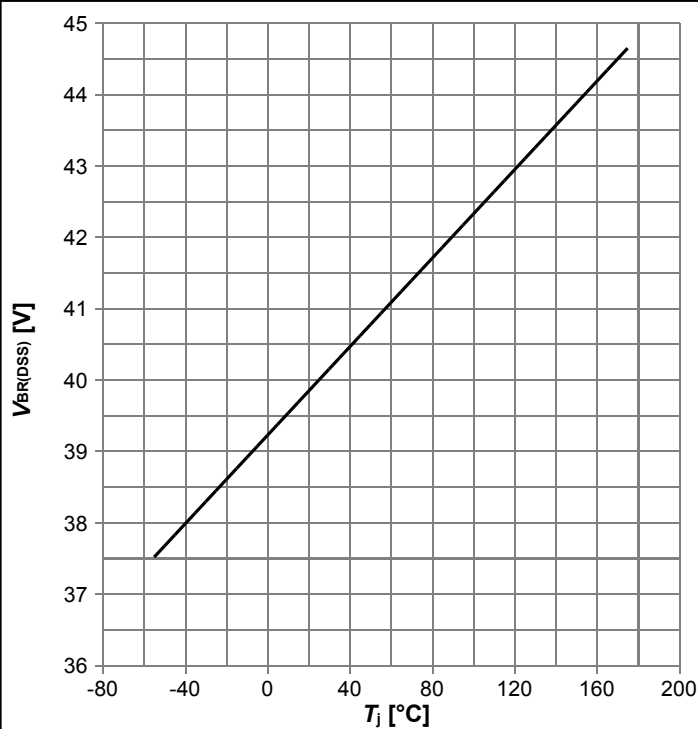
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}), I_D=35 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines

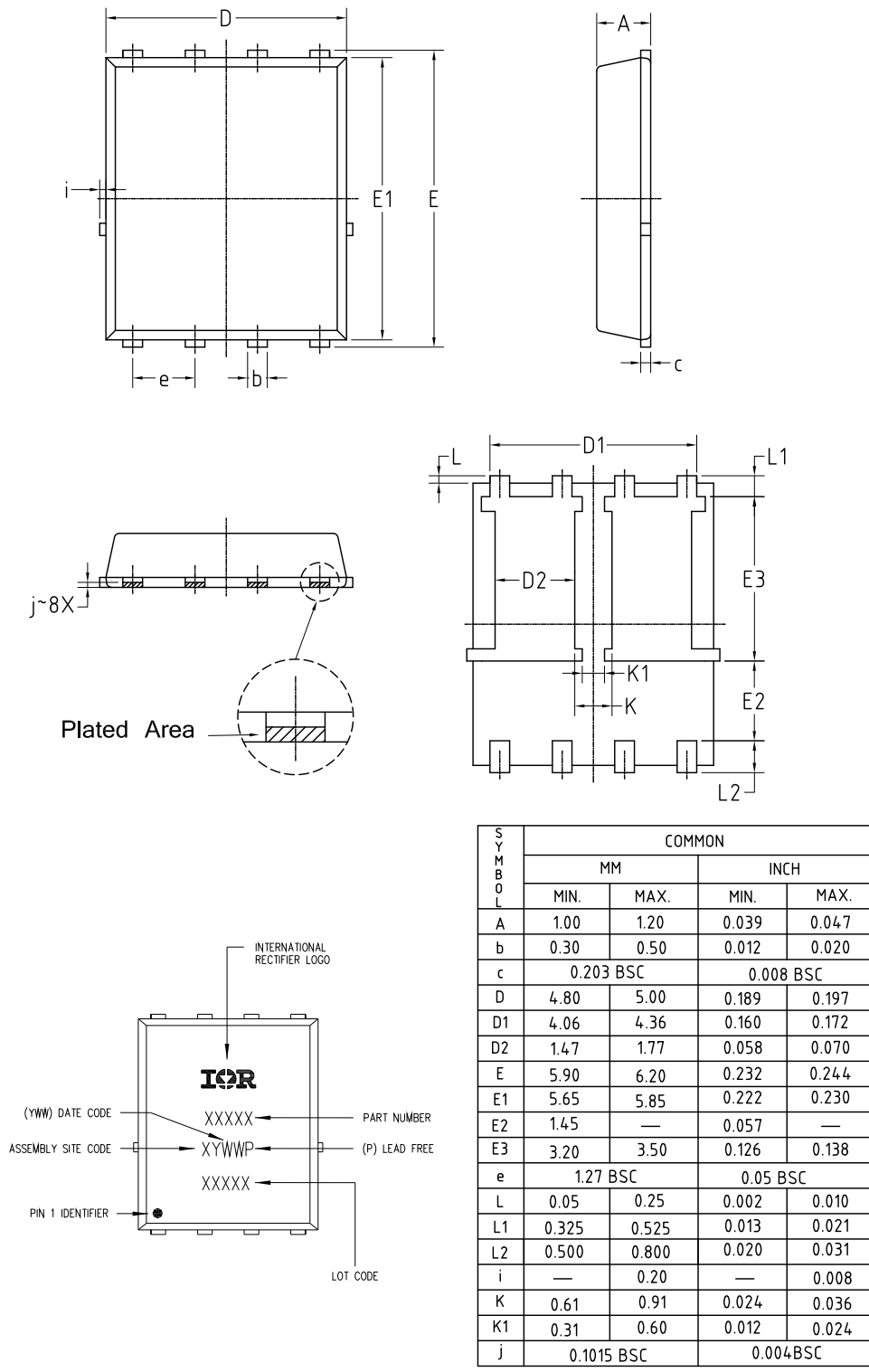
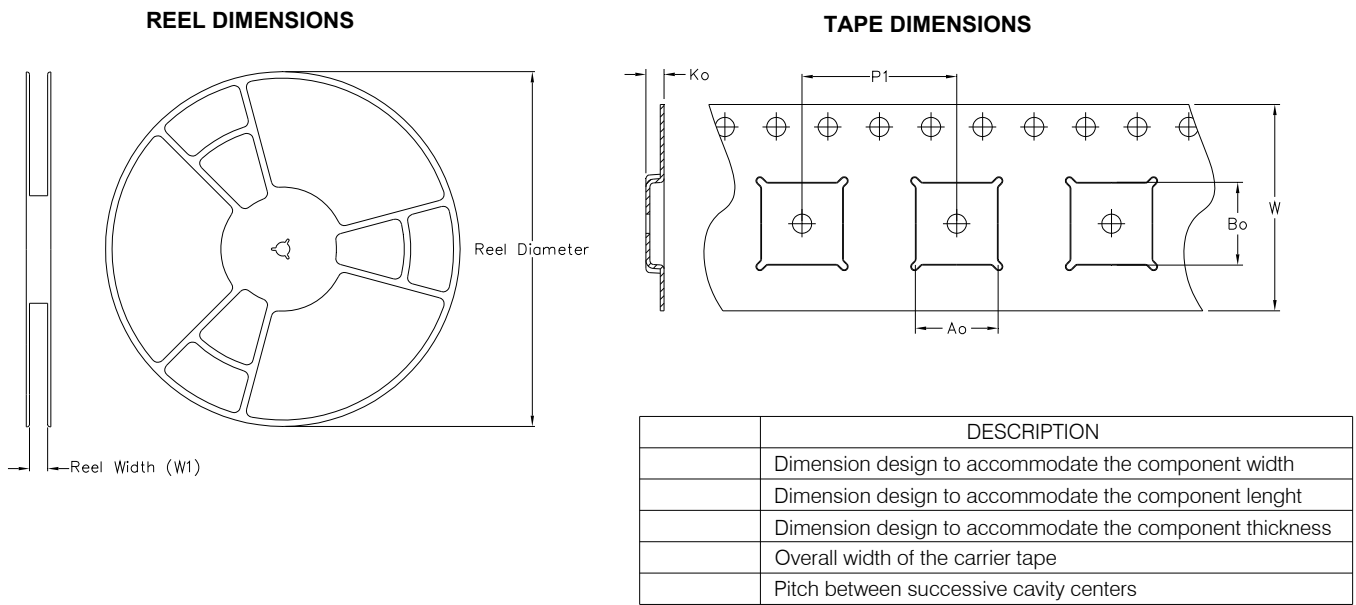
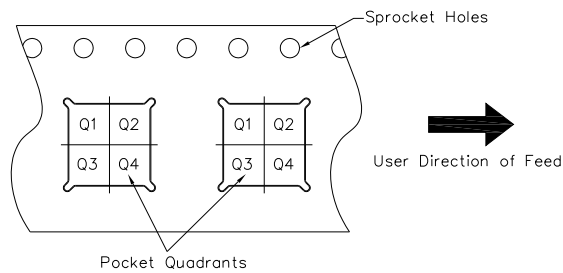


Figure 1 Outline PG-TDSON-8-4, dimensions in mm/inches



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Figure 2 Outline PG-TDSON-8-4, dimensions in mm/inches

Revision History

IRF40H233

Revision: 2020-06-29, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2018-07-05	Release of preliminary version
2.0	2018-07-12	Release of final version
2.1	2018-07-16	Update Potential Application
2.2	2020-01-20	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™
2.3	2020-06-29	Updated Datasheet based on new current rating and application note:App-AN_1912_PL51_2001_180356

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