International Rectifier

IRF530NPbF

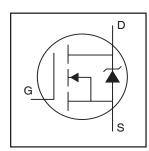
HEXFET® Power MOSFET

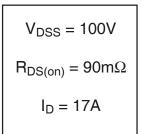
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

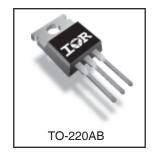
Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.







Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	17	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	12	A
I _{DM}	Pulsed Drain Current ①	60	
P _D @T _C = 25°C	Power Dissipation	70	W
	Linear Derating Factor	0.47	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I _{AR}	Avalanche Current①	9.0	A
E _{AR}	Repetitive Avalanche Energy ^①	7.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	7.4	V/ns
TJ	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case		2.15	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50		°C/W
$R_{\theta JA}$	Junction-to-Ambient		62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.11		V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance			90	mΩ	V _{GS} = 10V, I _D = 9.0A ④
V _{GS(th)}	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
9fs	Forward Transconductance	12			S	V _{DS} = 50V, I _D = 9.0A⊕
I _{DSS}	Drain-to-Source Leakage Current			25	μA	V _{DS} = 100V, V _{GS} = 0V
פפטי	Brain to Godice Edanage Garrent			250	μΛ	$V_{DS} = 80V, V_{GS} = 0V, T_{J} = 150^{\circ}C$
1	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Reverse Leakage			-100	l IIA	V _{GS} = -20V
Q _g	Total Gate Charge			37		$I_D = 9.0A$
Q _{gs}	Gate-to-Source Charge			7.2	nC	$V_{DS} = 80V$
Q _{gd}	Gate-to-Drain ("Miller") Charge			11		V_{GS} = 10V, See Fig. 6 and 13
t _{d(on)}	Turn-On Delay Time		9.2			$V_{DD} = 50V$
t _r	Rise Time		22		ns	$I_{D} = 9.0A$
t _{d(off)}	Turn-Off Delay Time		35		115	$R_G = 12\Omega$
t _f	Fall Time		25			V _{GS} = 10V, See Fig. 10 ④
L _D	Internal Drain Inductance		4.5			Between lead,
					nH	6mm (0.25in.)
L _S	Internal Source Inductance		7.5			from package
						and center of die contact
C _{iss}	Input Capacitance		920			V _{GS} = 0V
Coss	Output Capacitance		130			$V_{DS} = 25V$
C _{rss}	Reverse Transfer Capacitance		19		pF	f = 1.0MHz, See Fig. 5
E _{AS}	Single Pulse Avalanche Energy ²		340⑤	93©	mJ	I _{AS} = 9.0A, L = 2.3mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current			17		MOSFET symbol
	(Body Diode)		17	A	showing the	
I _{SM}	Pulsed Source Current			60	1 ^	integral reverse
	(Body Diode)①		60		p-n junction diode.	
V _{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C$, $I_S = 9.0A$, $V_{GS} = 0V$ ④
t _{rr}	Reverse Recovery Time		93	140	ns	$T_J = 25^{\circ}C, I_F = 9.0A$
Q _{rr}	Reverse Recovery Charge		320	480	nC	di/dt = 100A/µs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- $\begin{tabular}{ll} \hline @ Starting $T_J=25^\circ$C, $L=2.3mH$ \\ $R_G=25\Omega$, $I_{AS}=9.0A$, $V_{GS}=10V$ (See Figure 12) \\ \hline \end{tabular}$
- $\label{eq:loss} \begin{array}{l} \text{ } 3 \text{ } I_{SD} \leq 9.0A, \ di/dt \leq 410A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \\ T_{J} \leq 175^{\circ}C \end{array}$
- 4 Pulse width \leq 400 μ s; duty cycle \leq 2%.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- $\ \, \mbox{\ \ \, } \mbox{\ \ } \mbox{\$

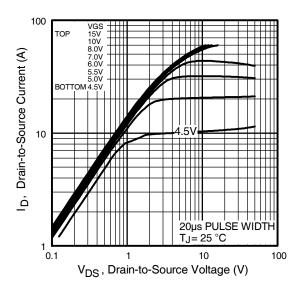


Fig 1. Typical Output Characteristics

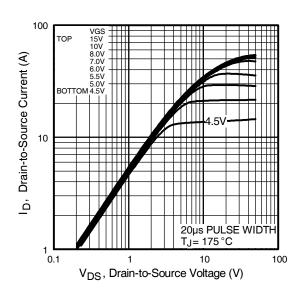


Fig 2. Typical Output Characteristics

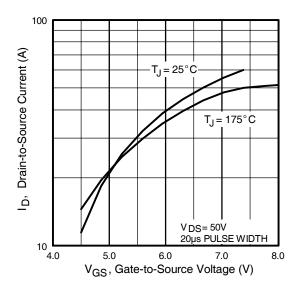


Fig 3. Typical Transfer Characteristics

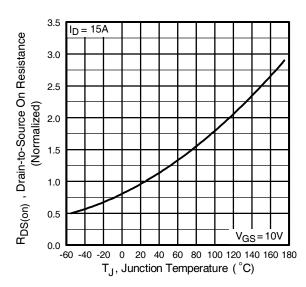


Fig 4. Normalized On-Resistance Vs. Temperature

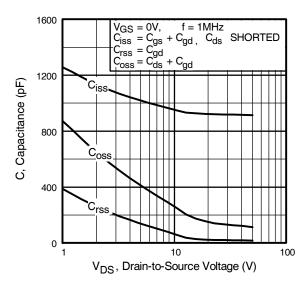


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

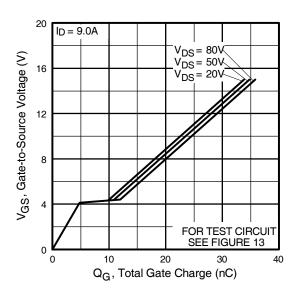


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

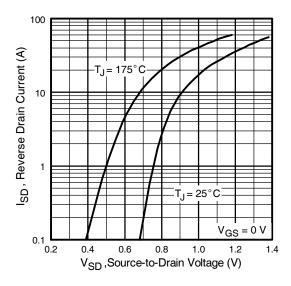


Fig 7. Typical Source-Drain Diode Forward Voltage

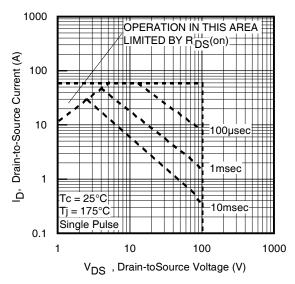


Fig 8. Maximum Safe Operating Area

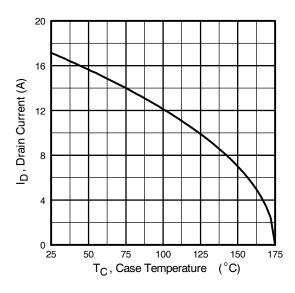


Fig 9. Maximum Drain Current Vs. Case Temperature

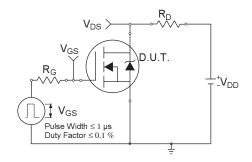


Fig 10a. Switching Time Test Circuit

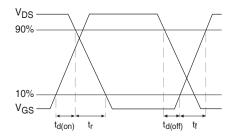


Fig 10b. Switching Time Waveforms

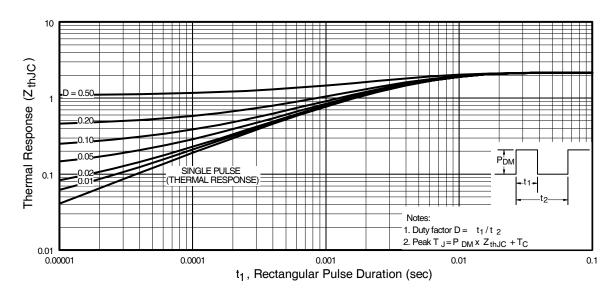


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

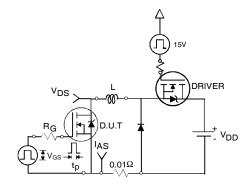


Fig 12a. Unclamped Inductive Test Circuit

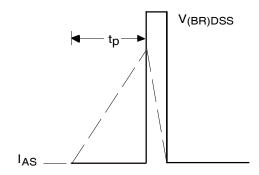


Fig 12b. Unclamped Inductive Waveforms

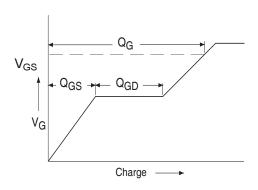


Fig 13a. Basic Gate Charge Waveform

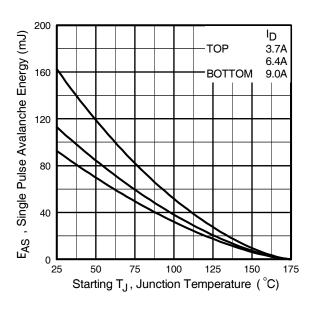


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

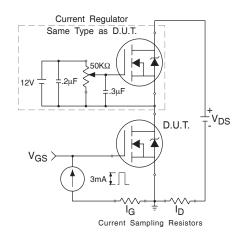
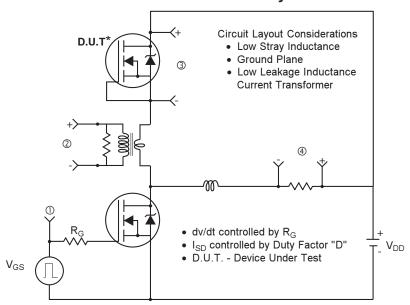
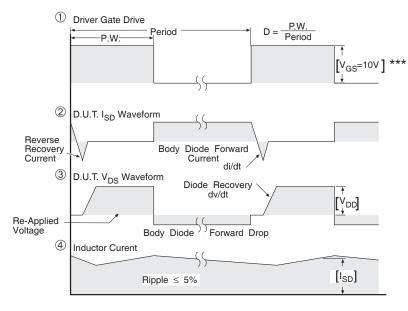


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

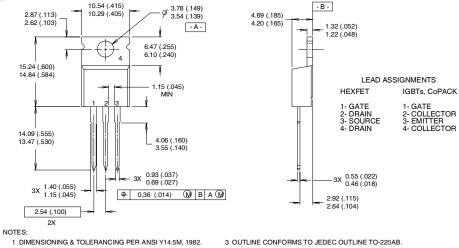


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- 2 CONTROLLING DIMENSION : INCH
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

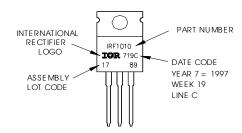
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010 LOT CODE 1789

ASSEMBLED ON WW 19, 1997

IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free



Data and specifications subject to change without notice. This product has been designed and qualified for the Industrial market. Qualification Standards can be found on IR's Web site.



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Note: For the most current drawings please refer to the IR website at: http://www.irf.com/package/

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