

IRF5806PbF

HEXFET[®] Power MOSFET

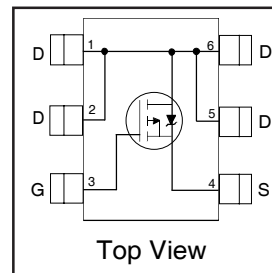
- Ultra Low On-Resistance
- P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Low Gate Charge
- Lead-Free
- Halogen-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
-20V	86m Ω @ $V_{GS} = -4.5V$	-4.0A
	147m Ω @ $V_{GS} = -2.5V$	-3.0A

Description

These P-channel MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

The TSOP-6 package with its customized leadframe produces a HEXFET[®] power MOSFET with $R_{DS(on)}$ 60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and $R_{DS(on)}$ reduction enables a current-handling increase of nearly 300% compared to the SOT-23.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	-20	V
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-4.0	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-3.3	
I_{DM}	Pulsed Drain Current ^①	-16.5	
P_D @ $T_A = 25^\circ C$	Maximum Power Dissipation ^③	2.0	W
P_D @ $T_A = 70^\circ C$	Maximum Power Dissipation ^③	1.3	W
	Linear Derating Factor	0.02	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	$^\circ C$


Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ^③	62.5	$^\circ C/W$

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.011	—	V/°C	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	47.1	86	mΩ	$V_{GS} = -4.5V, I_D = -4.0A$ ②
		—	67.5	147		$V_{GS} = -2.5V, I_D = -3.0A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	—	-1.2	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	6.4	—	—	S	$V_{DS} = -10V, I_D = -4.0A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-15	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	8.3	11.4	nC	$I_D = -4.0A$
Q_{gs}	Gate-to-Source Charge	—	1.2	—		$V_{DS} = -16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.6	—		$V_{GS} = -4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	6.2	9.3	ns	$V_{DD} = -10V, V_{GS} = -4.5V$
t_r	Rise Time	—	27	41		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	94	140		$R_G = 6.0\Omega$
t_f	Fall Time	—	126	190		$R_D = 10\Omega$ ②
C_{iss}	Input Capacitance	—	594	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	114	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	87	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-16.5		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	116	174	ns	$T_J = 25^\circ\text{C}, I_F = -2.0A$
Q_{rr}	Reverse Recovery Charge	—	90	135	nC	$di/dt = -100A/\mu s$ ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

③ When mounted on 1 inch square Copper board, $t \leq 10\text{sec}$.

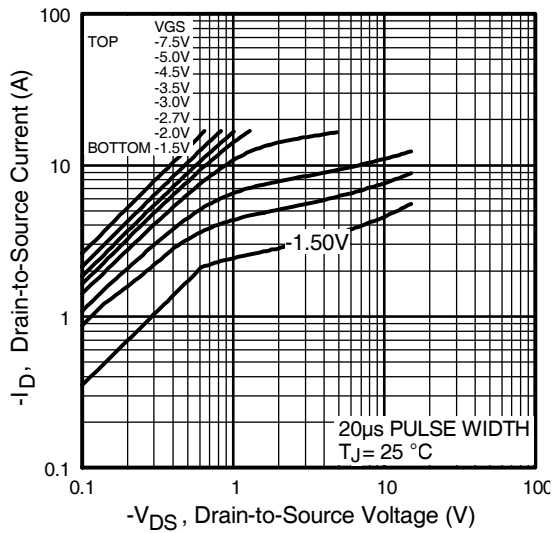


Fig 1. Typical Output Characteristics

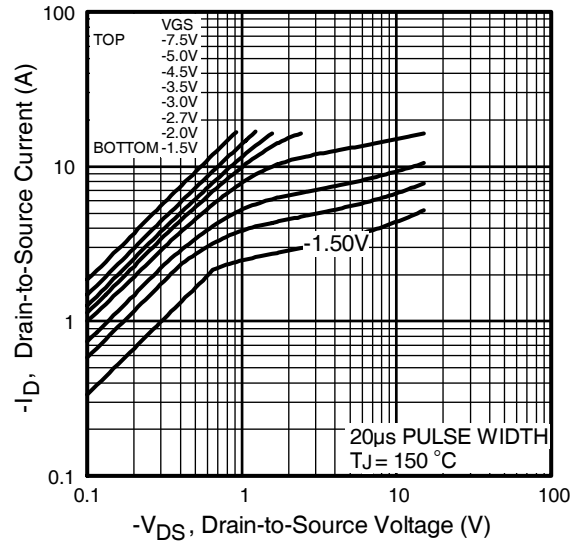


Fig 2. Typical Output Characteristics

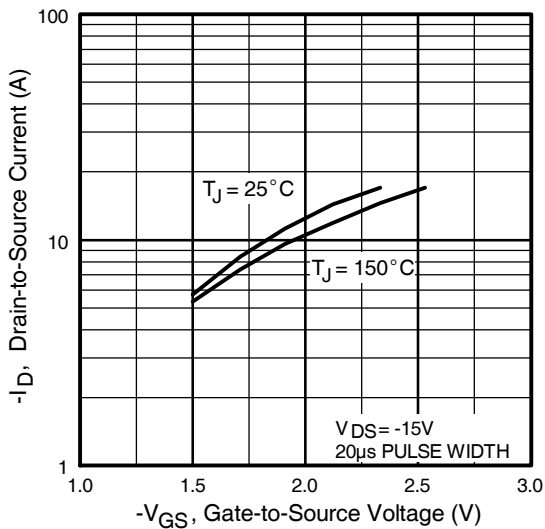


Fig 3. Typical Transfer Characteristics

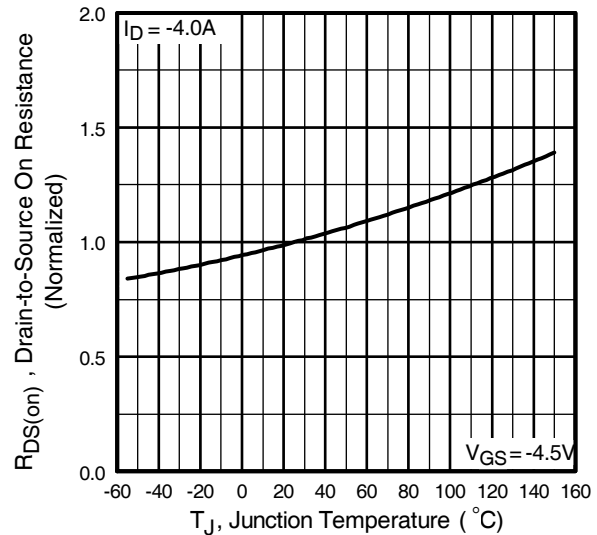


Fig 4. Normalized On-Resistance Vs. Temperature

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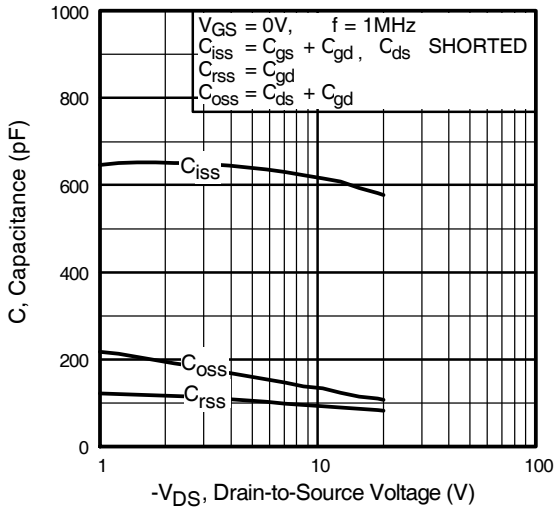


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

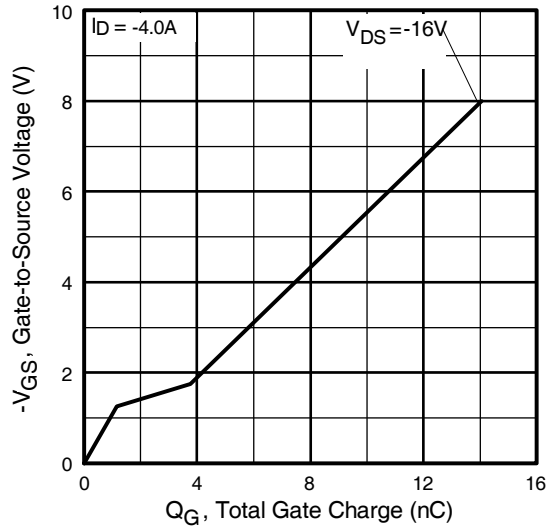


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

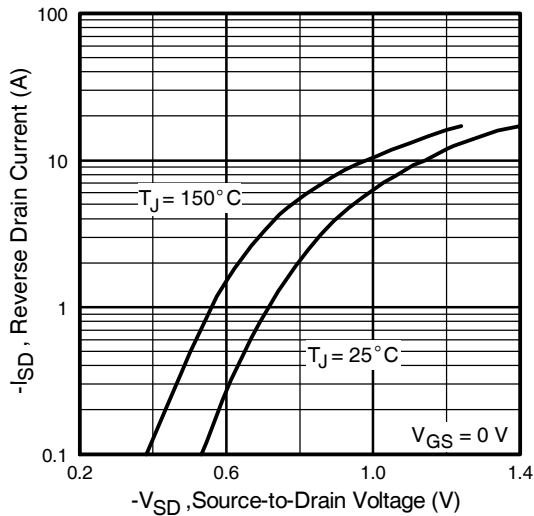


Fig 7. Typical Source-Drain Diode Forward Voltage

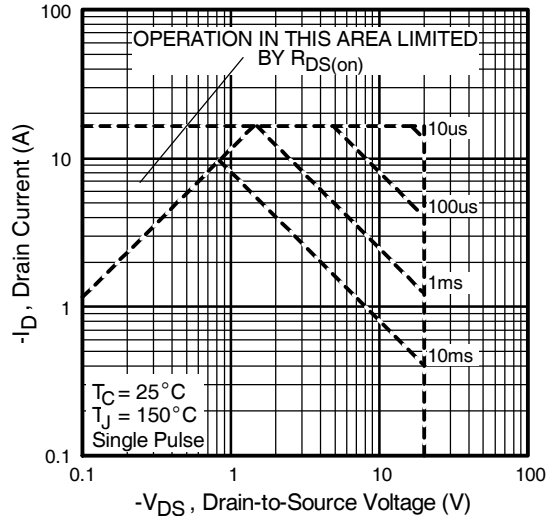


Fig 8. Maximum Safe Operating Area

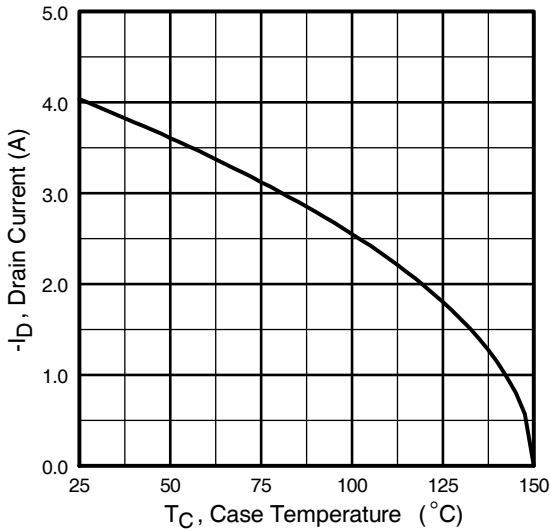


Fig 9. Maximum Drain Current Vs. Case Temperature

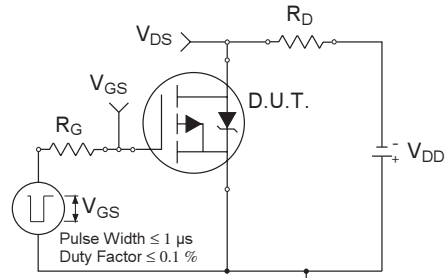


Fig 10a. Switching Time Test Circuit

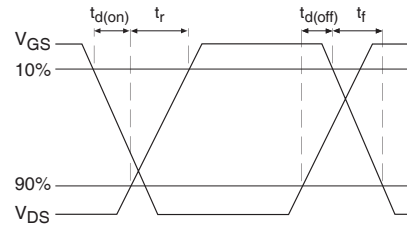


Fig 10b. Switching Time Waveforms

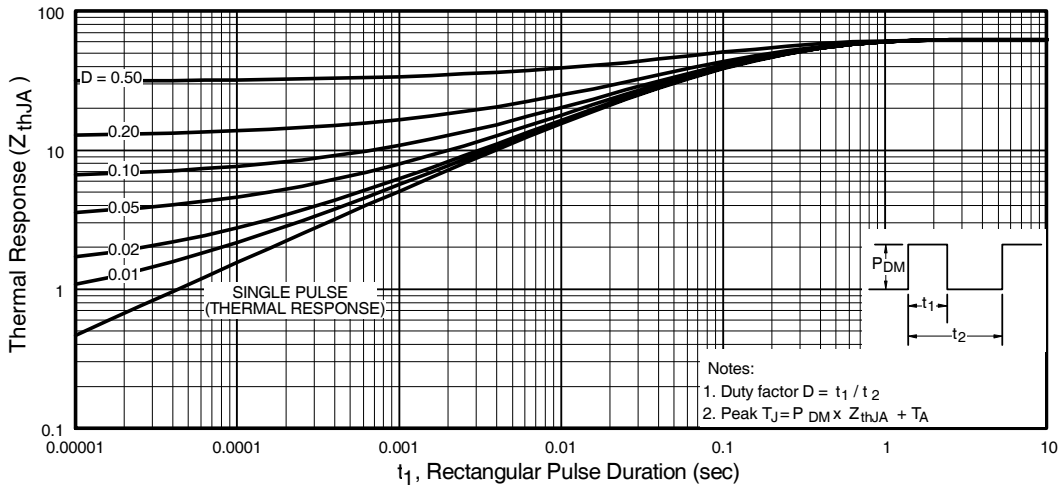


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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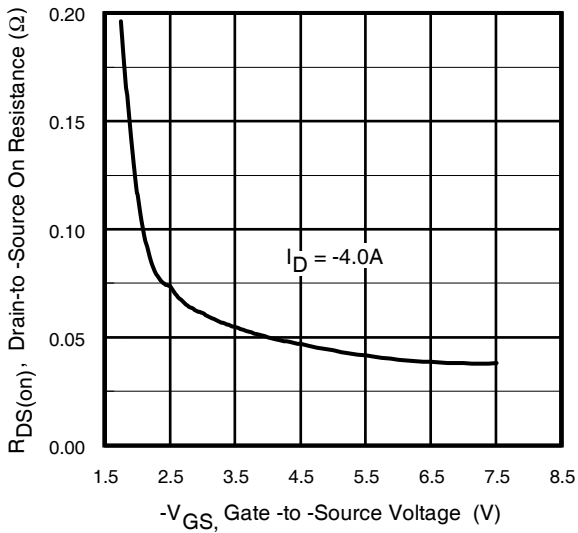


Fig 12. Typical On-Resistance Vs. Gate Voltage

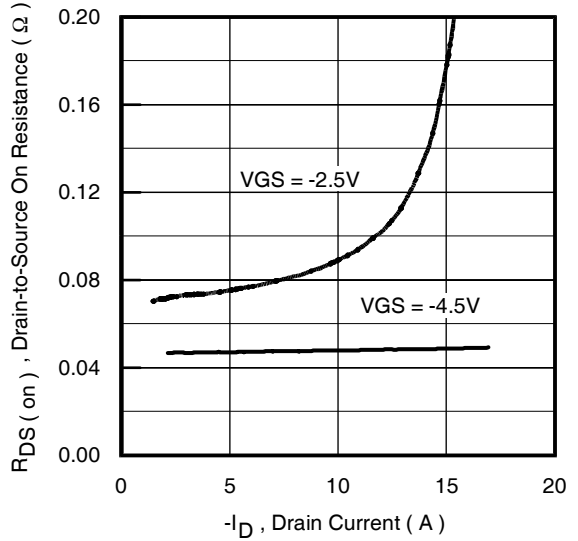


Fig 13. Typical On-Resistance Vs. Drain Current

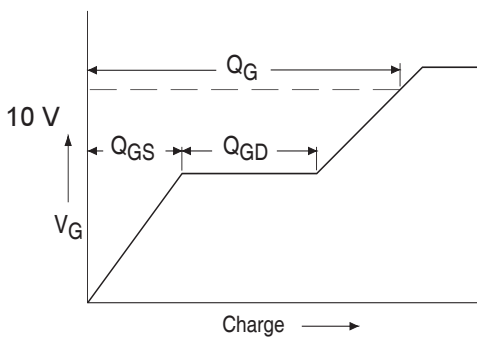


Fig 14a. Basic Gate Charge Waveform

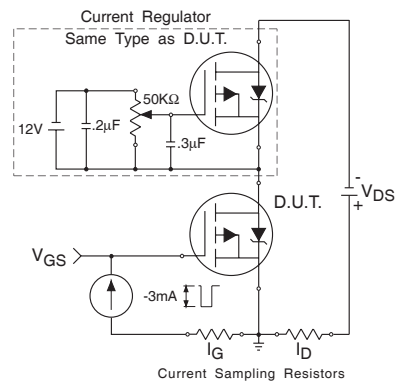


Fig 14b. Gate Charge Test Circuit

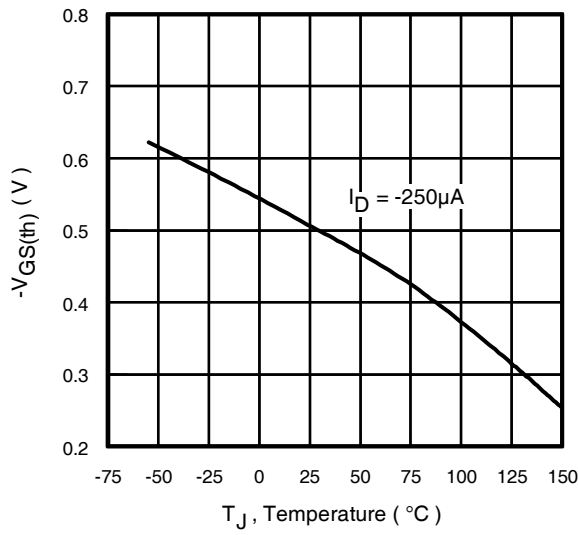


Fig 15. Typical $V_{GS(th)}$ Vs. Junction Temperature

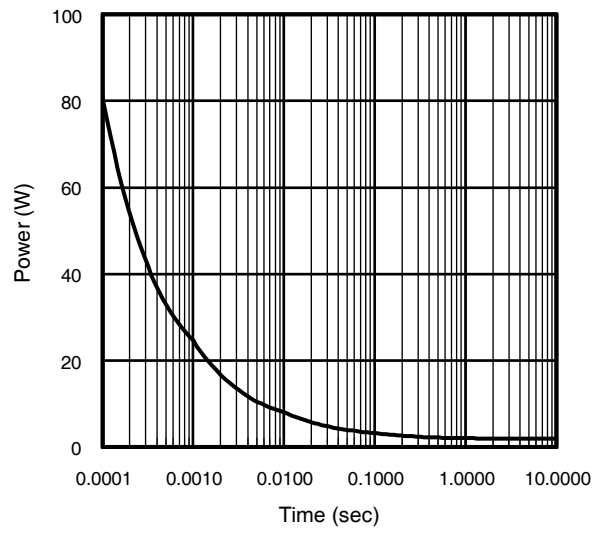
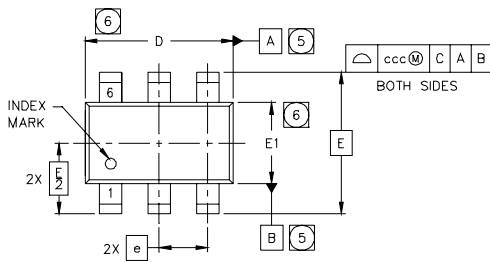


Fig 16. Typical Power Vs. Time

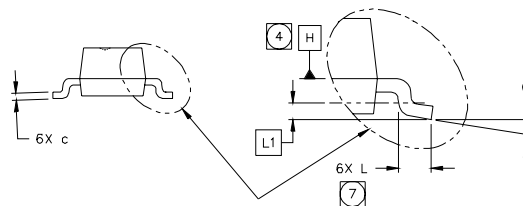
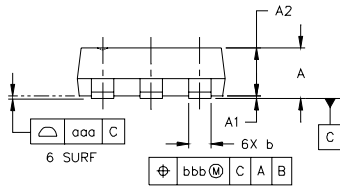
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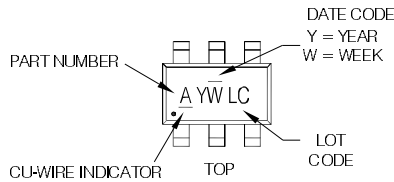
TSOP-6 Package Outline



SYMBOL	MO-193AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	.0433
A1	0.01	---	0.10	.0004	---	.0039
A2	0.80	0.90	1.00	.0315	.0354	.0393
b	0.25	---	0.50	.0099	---	.0196
c	0.10	---	0.26	.004	---	.010
D	2.90	3.00	3.10	.115	.118	.122
E	2.75 BSC			.108 BSC		
E1	1.30	1.50	1.70	.052	.059	.066
e	1.00 BSC			.039 BSC		
L	0.20	0.40	0.60	.0079	.0157	.0236
L1	0.30 BSC			.0118 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.004		
bbb	0.15			.006		
ccc	0.25			.010		



TSOP-6 Part Marking Information



PART NUMBER CODE REFERENCE:

A = SI3443DV K = IRF5810
 B = IRF5800 L = IRF5804
 C = IRF5850 M = IRF5803
 D = IRF5851 N = IRF5802
 E = IRF5852
 F = IRF5801
 I = IRF5805
 J = IRF5806

Notes:

- A line above the work week (as shown here) indicates Lead-Free
- A line below the part number (as shown here) indicates Cu-wire

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

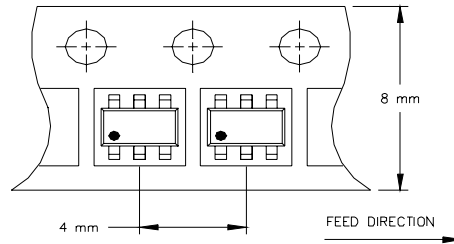
YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
2006	6		
2007	7		
2008	8		
2009	9		
2010	0	24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
2006	F		
2007	G		
2008	H		
2009	J		
2010	K	50	X
		51	Y
		52	Z

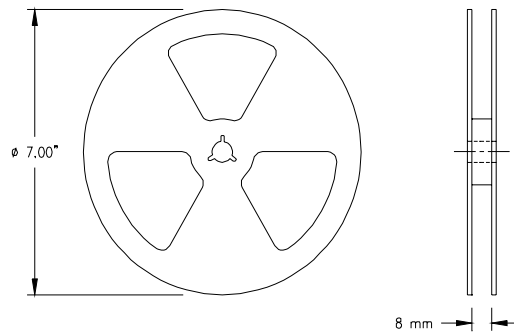
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

TSOP-6 Tape & Reel Information



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#)