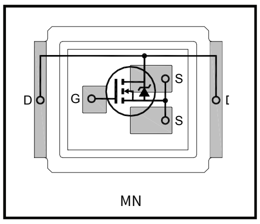
IR MOSFET

DirectFET™ Power MOSFET ①②

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$ (typ.)
100V min.	**± 20V max**	**10.3mΩ @ 10V**
$Q_{g\ tot}$	Q_{gd}	$V_{gs(th)}$
28nC	**9.0nC**	**3.7V**



Quality Requirement Category: Consumer

Applications

- RoHS Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specifies MOSFETs
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- Low Profile (< 0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Applicable DirectFET® Outline and Substrate Outline (see pg. 13, 14 for details) ①

SH	SJ	SP		MZ	MN					

Description

The IRF6644PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET® packaging to achieve the lowest on-state resistance in a package that has a footprint of a SO-8 and only 0.7 mm profile. The DirectFET® package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET® package allows dual sided cooling to maximize thermal transfer in power systems improving previous best thermal resistance by 80%.

The IRF6644PbF is optimized for primary side bridge topologies in isolated DC-DC applications, for wide range universal input Telecom applications (36V-75V), and for secondary side synchronous rectification in regulated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes the device ideal for high performance isolated DC-DC converters.

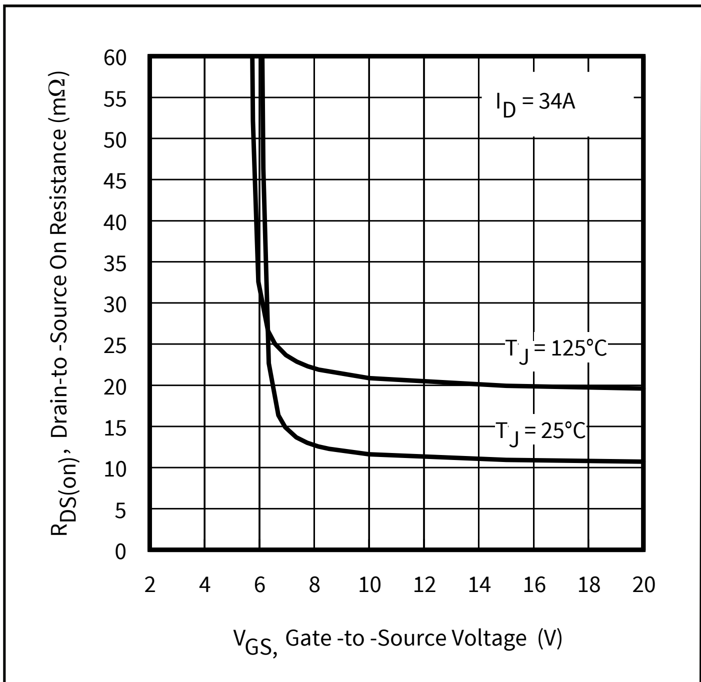


Figure 1 Typical On-Resistance vs. Gate Voltage

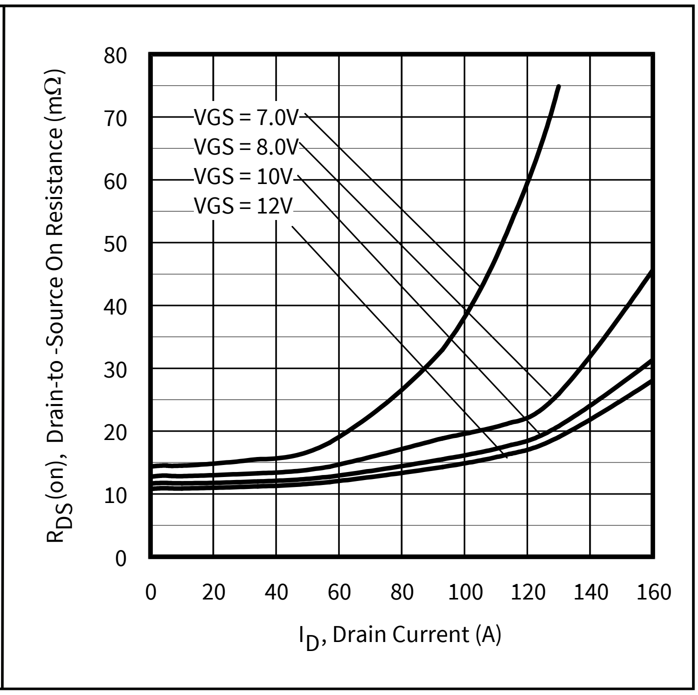


Figure 2 Typical On-Resistance vs. Drain Current

Table of Contents

1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	100	V
$R_{DS(on)\ max}$	13	mΩ
I_D @ T_C @ 25°C	57	A
I_D @ T_A @ 25°C	10	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at T_J=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current (Silicon Limited) ④	I_D	T_C = 25°C, V_{GS} @ 10V	57	A
Continuous Drain Current (Silicon Limited) ④	I_D	T_C = 70°C, V_{GS} @ 10V	46	
Continuous Drain Current (Silicon Limited) ③	I_D	T_A= 25°C, V_{GS} @ 10V	10	
Pulsed Drain Current ⑤	I_{DM}	T_C = 25°C	228	
Maximum Power Dissipation ④	P_D	T_C = 25°C	89	W
Maximum Power Dissipation ④	P_D	T_C = 70°C	57	
Maximum Power Dissipation ③	P_D	T_A = 25°C	2.8	
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Peak Soldering Temperature	T_P	-	270	°C
Operating and Storage Temperature	T_J, T_{STG}	-	-40 ... 150	

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Ambient ③	$R_{\theta JA}$	-	-	-	45	°C/W
Junction-to-Ambient ⑧	$R_{\theta JA}$	-	-	12.5	-	
Junction-to-Ambient ⑨	$R_{\theta JA}$	-	-	20	-	
Junction-to-Case ④ ⑩	$R_{\theta JC}$	-	-	-	1.4	
Junction-to-PCB Mounted	$R_{\theta JA\text{-}PCB}$	-	-	1.0	-	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ⑥	E_{AS}	86	mJ
Avalanche Current ⑥	I_{AR}	34	A

Notes:

① *Click on this section to link to the appropriate technical paper.*
② *Click on this section to link to the DirectFET™ Website.*
③ *Surface mounted on 1 in. square Cu board, steady state.*
④ *TC measured with thermocouple mounted to top (Drain) of part.*
⑤ *Repetitive rating; pulse width limited by max. junction temperature.*
⑥ *(Starting T_J = 25°C, L = 0.15mH, R_G = 50Ω, I_{AS} = 34A.*
⑦ *Pulse width ≤ 400µs; duty cycle ≤ 2%.*
⑧ *Used double sided cooling, mounting pad with large heat sink.*
⑨ *Mounted on minimum footprint full size board with metalized back and with small clip heat sink.*
⑩ *R_θ is measured at T_J of approximately 90°C.*

3 Electrical characteristics

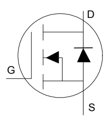
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	100	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 1mA	-	0.1	-	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 34A ⑦	-	10.3	13	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 150µA	2.8	3.7	4.8	V
Gate Threshold Voltage Temp. Coefficient	$\Delta V_{GS(th)}/\Delta T_J$		-	-11	-	mV°/C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	-	-	20	µA
		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C			250	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	-	-	100	nA
	I_{GSS}	V_{GS} = -20V	-	-	-100	
Gate Resistance	R_G	-	-	1.6	-	Ω

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	V_{DS} = 10V, I_D = 34A	65	-	-	S
Total Gate Charge	Q_g	I_D = 34A V_{DS} = 50V V_{GS} = 10V See Fig.8	-	28	42	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}		-	7.0	-	
Post-Vth Gate-to-Source Charge	Q_{gs2}		-	3.0	-	
Gate-to-Drain Charge	Q_{gd}		-	9.0	-	
Gate Charge Overdrive	Q_{godr}		-	9.0	-	
Switch Charge (Qgs2 + Qgd)	Q_{sw}		-	16	-	
Output Charge	Q_{oss}	V_{DS} = 16V ,V_{GS} = 0V	-	18	-	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50V	-	9.5	-	ns
Rise Time	t_r	I_D = 34A	-	16	-	
Turn-Off Delay Time	$t_{d(off)}$	R_G = 1.8Ω	-	15	-	
Fall Time	t_f	V_{GS} = 10V ⑦	-	5.7	-	
Input Capacitance	C_{iss}	V_{GS} = 0V	-	1770	-	pF
Output Capacitance	C_{oss}	V_{DS} = 50V	-	280	-	
Reverse Transfer Capacitance	C_{rss}	f = 1.0MHz	-	60	-	
Output Capacitance	C_{oss}	V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz	-	2025	-	
Output Capacitance	C_{oss}	V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz	-	245	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	57	A
Pulsed Source Current (Body Diode) ⑤	I_{SM}		-	-	228	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = 34A,V_{GS} = 0V ⑦	-	-	1.3	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 34A, V_{DD} = 50V	-	53	80	ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100A/µs	-	97	146	nC

4 Electrical characteristic diagrams

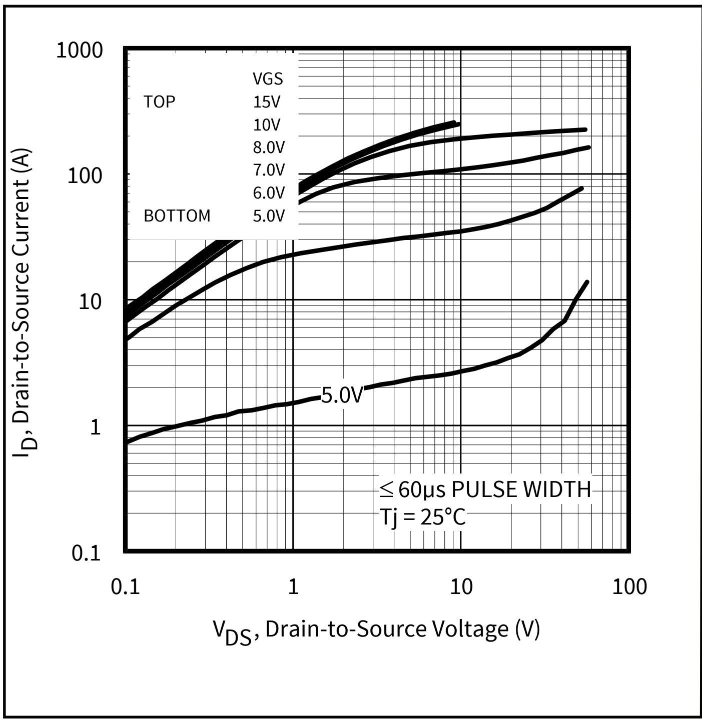


Figure 3 Typical Output Characteristics

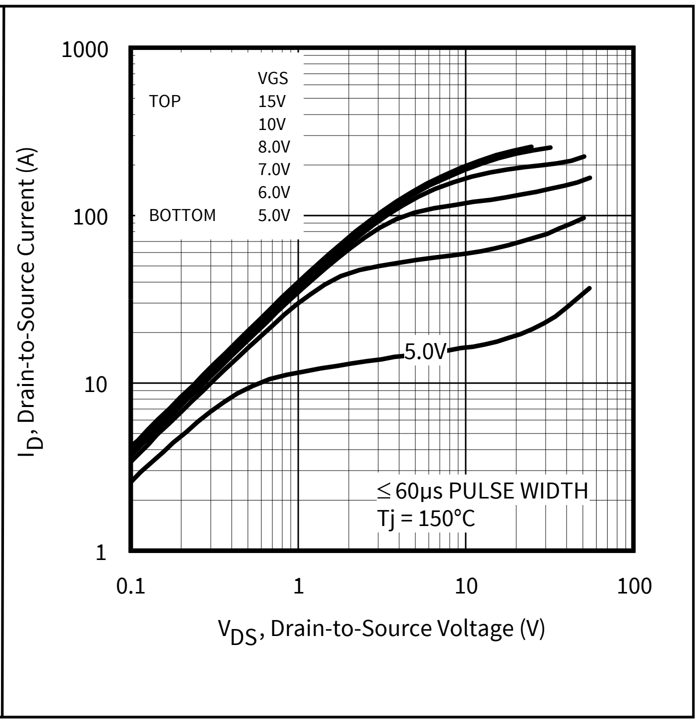


Figure 4 Typical Output Characteristics

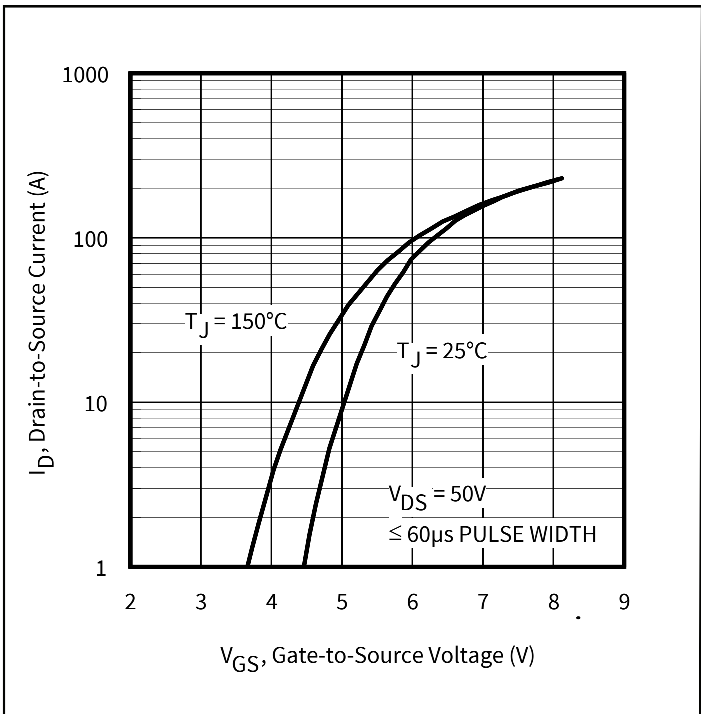


Figure 5 Typical Transfer Characteristics

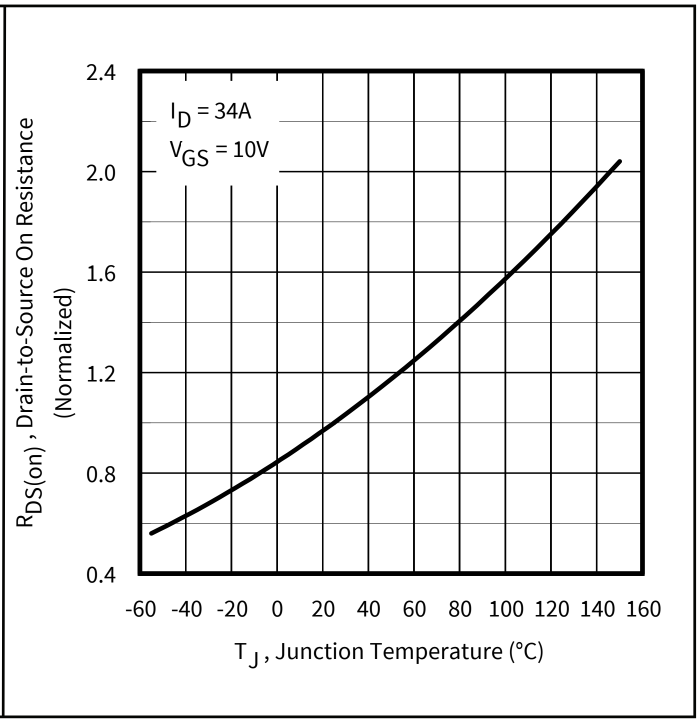


Figure 6 Normalized On-Resistance vs. Temperature

Electrical characteristic diagrams

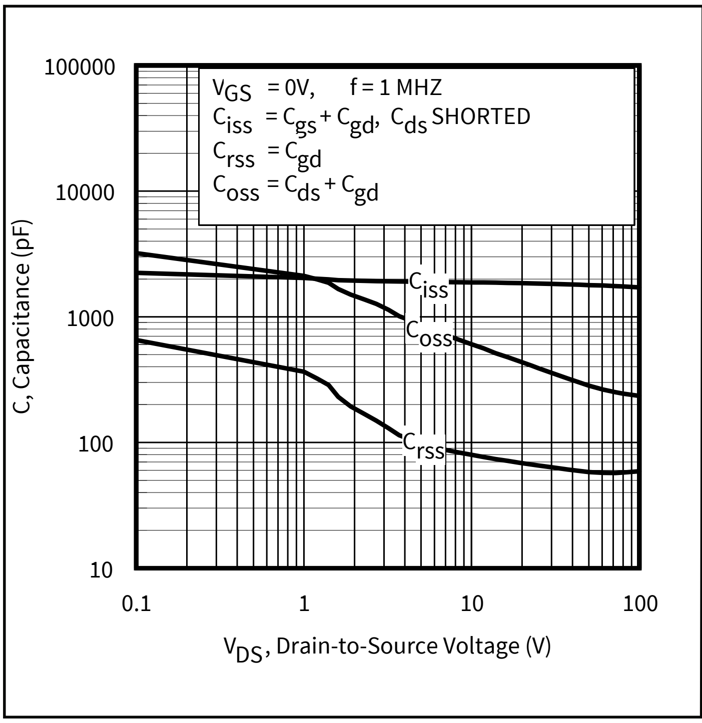


Figure 7 Typical Capacitance vs. Drain-to-Source Voltage

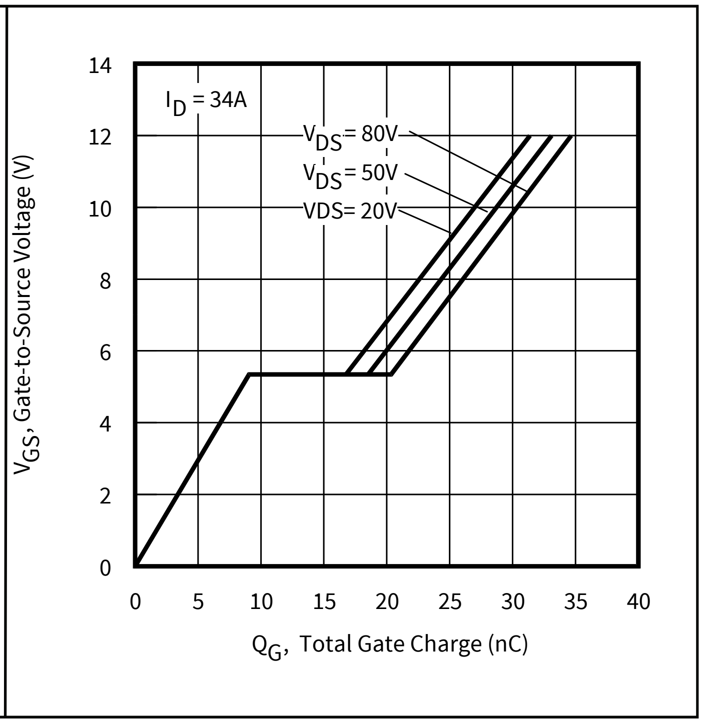


Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage

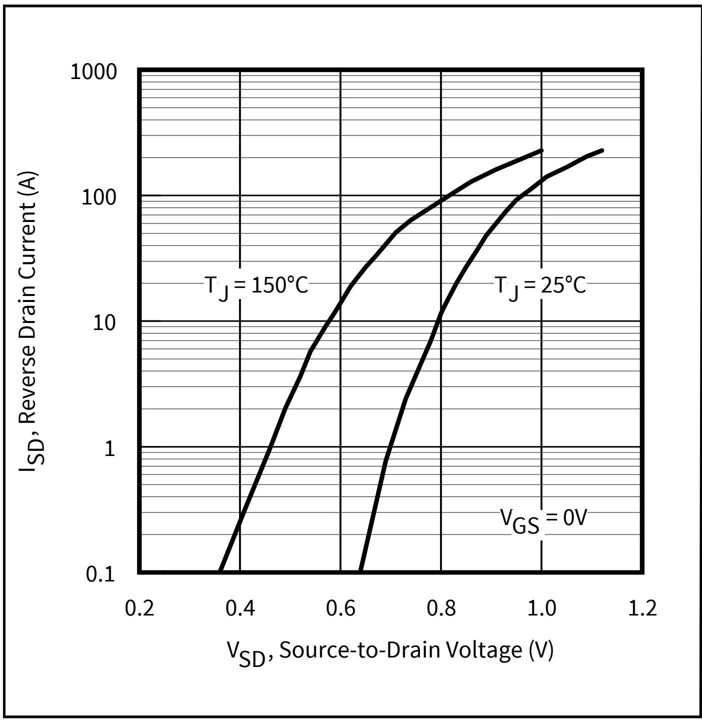


Figure 9 Typical Source-Drain Diode Forward Voltage

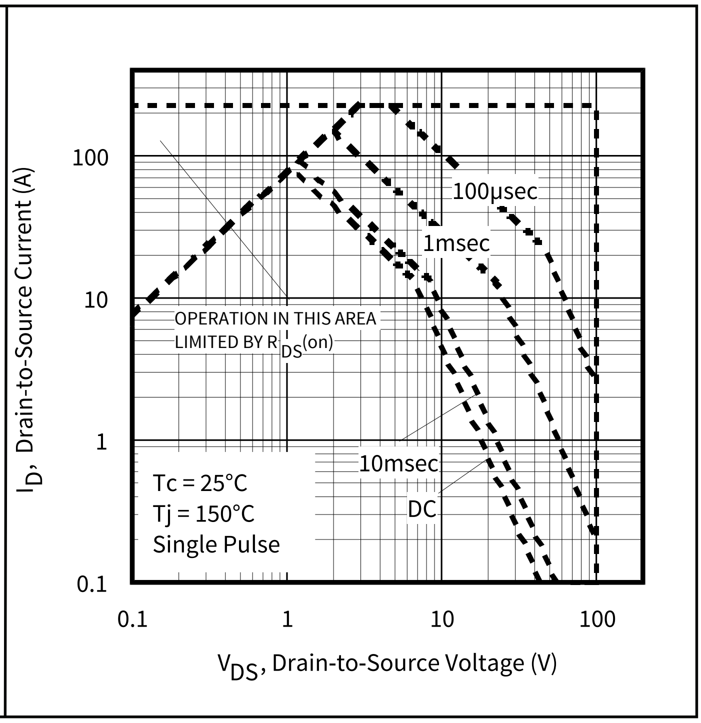


Figure 10 Maximum Safe Operating Area

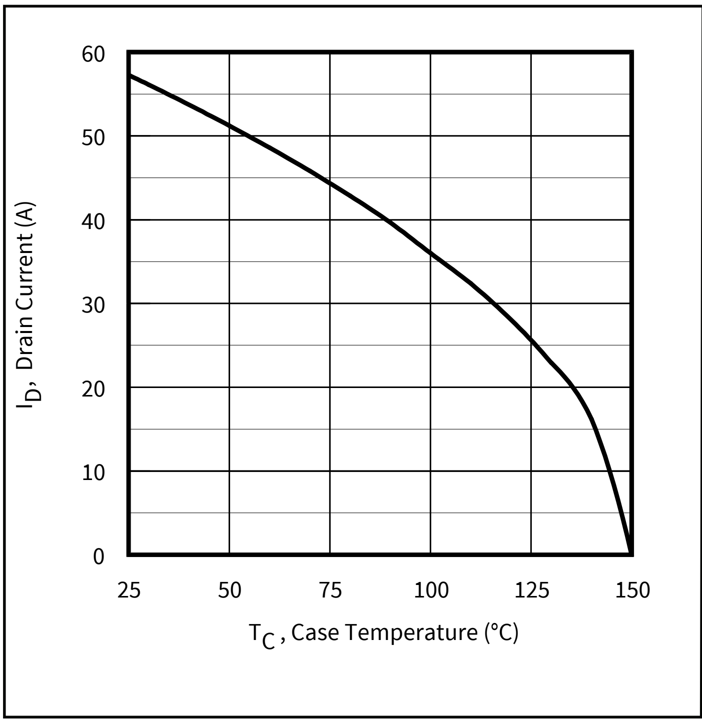


Figure 11 **Maximum Drain Current vs. Case Temperature**

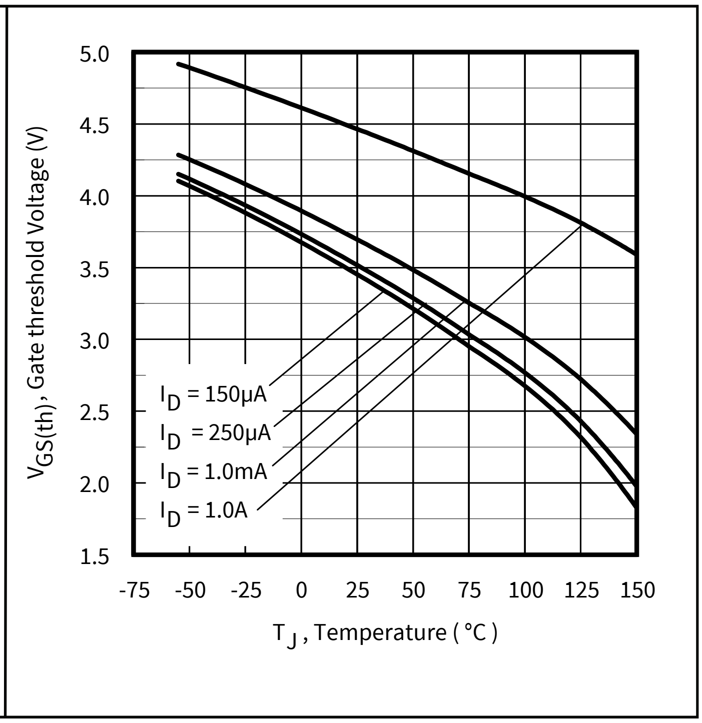


Figure 12 **Typical Threshold Voltage vs. Junction Temperature**

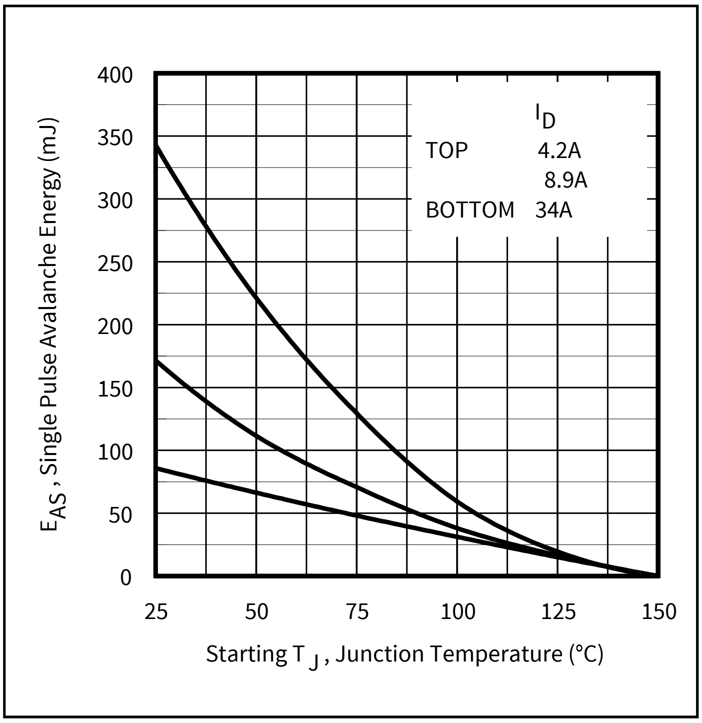


Figure 13 **Maximum Avalanche Energy vs. Drain Current**

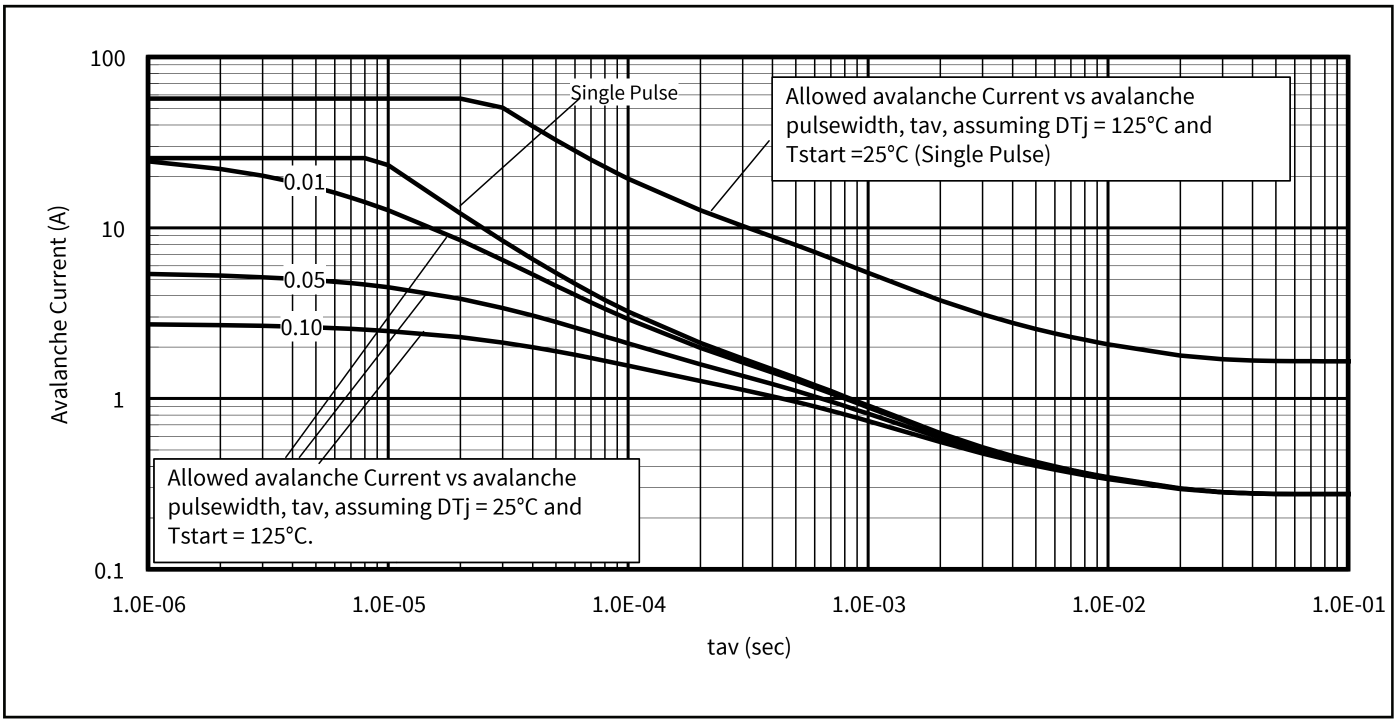


Figure 14 **Typical Avalanche Current vs. Pulse Width**

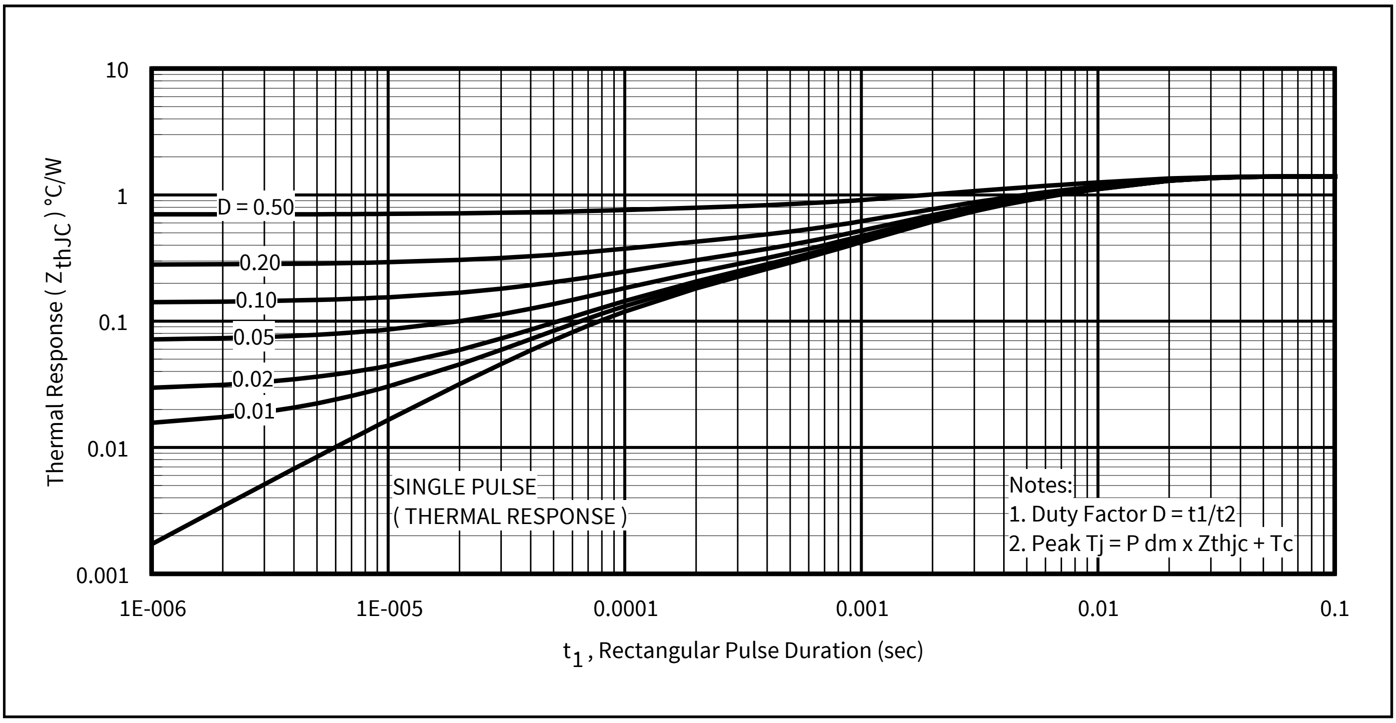
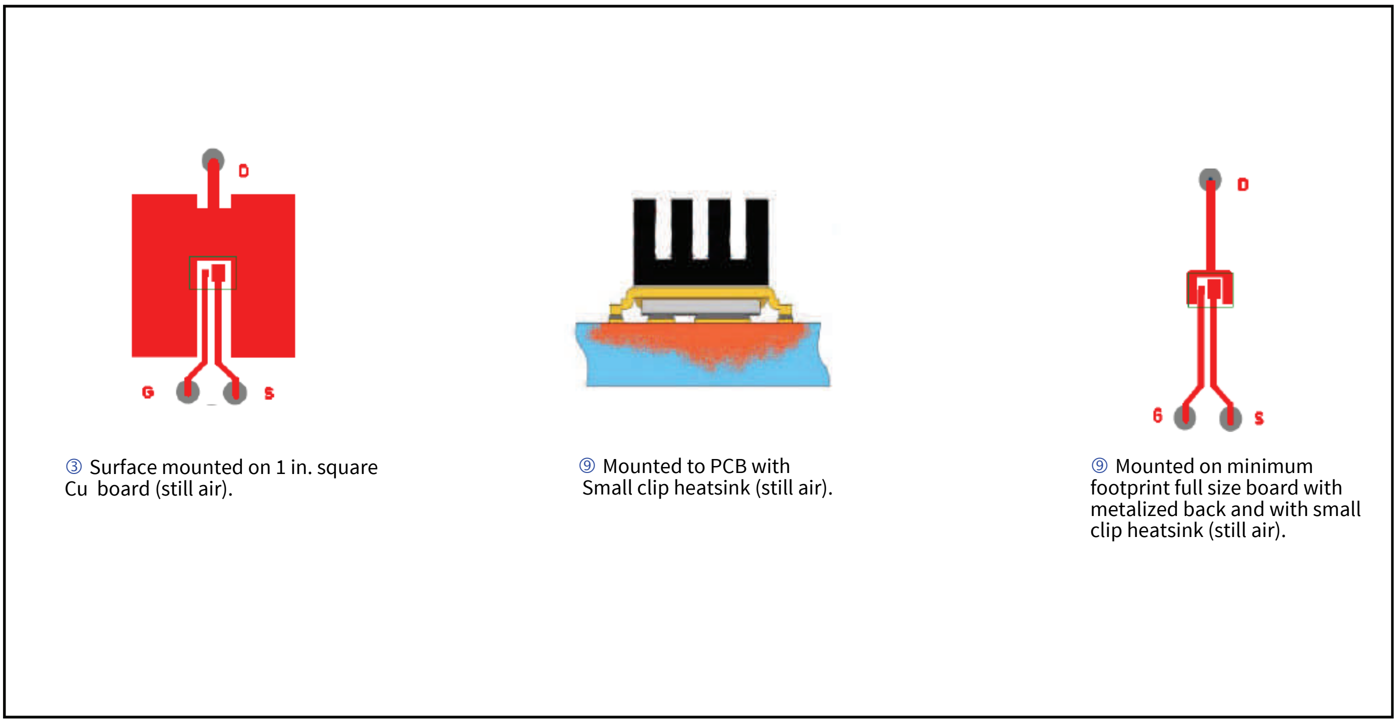


Figure 15 **Maximum Effective Transient Thermal Impedance, Junction-to-Case**



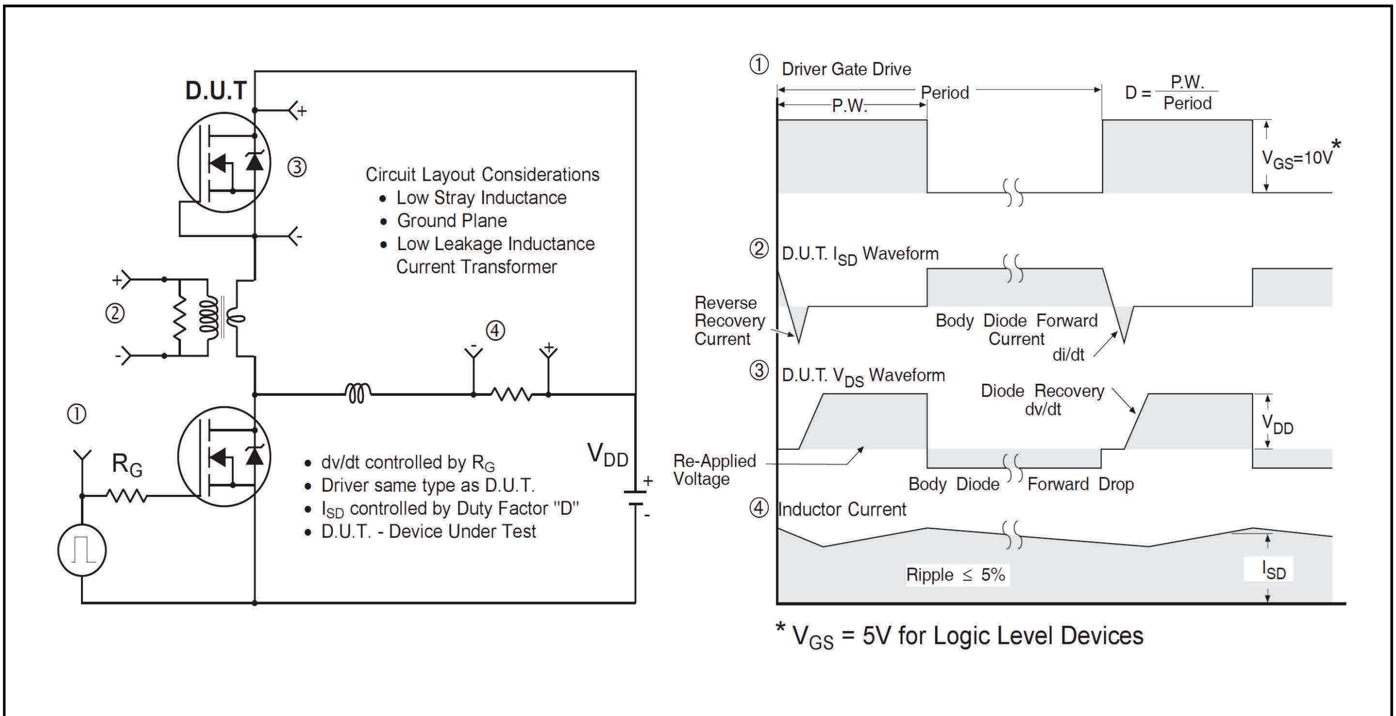
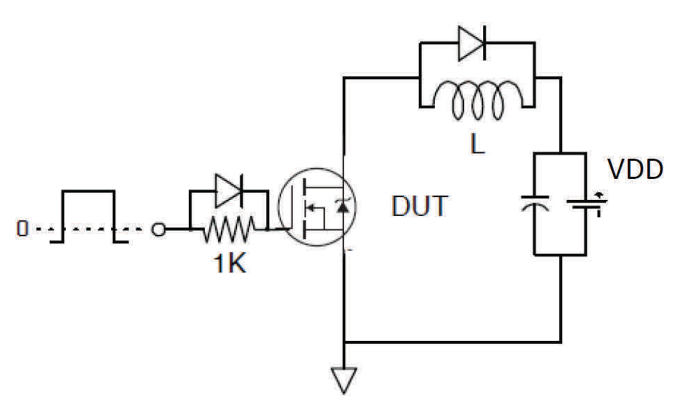


Figure 16 Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET™ Power MOSFETs



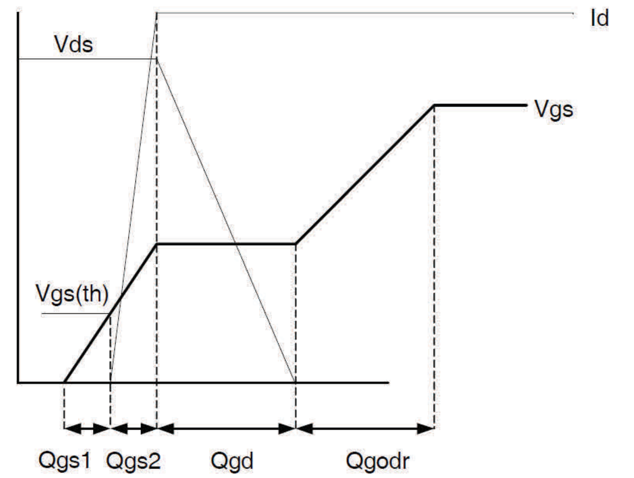
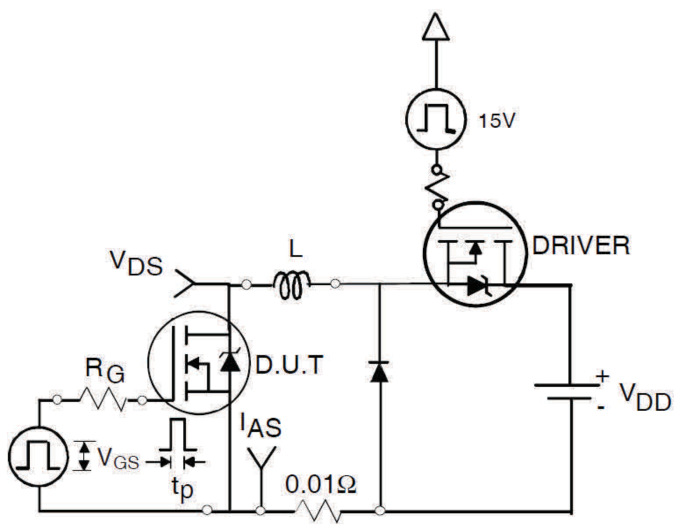


Figure 17a **Gate Charge Test Circuit**

Figure 17b **Gate Charge Waveform**



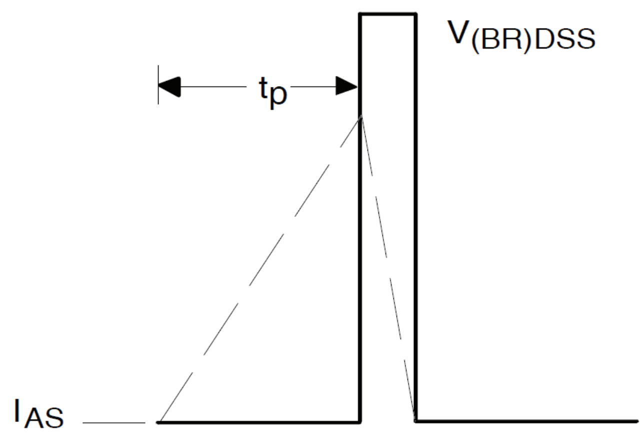


Figure 18a **Unclamped Inductive Test Circuit**

Figure 18b **Unclamped Inductive Waveforms**

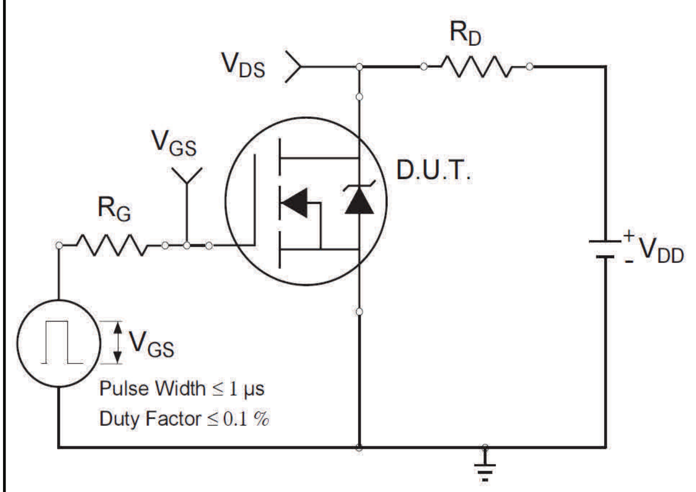


Figure 19a **Switching Time Test Circuit**

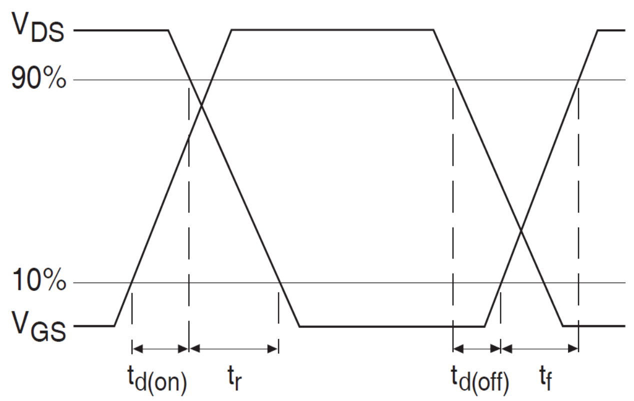
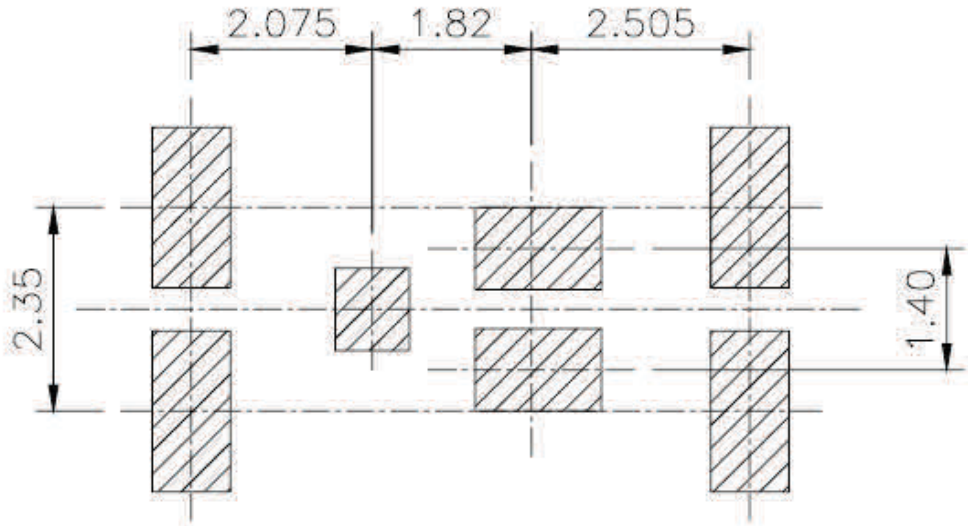
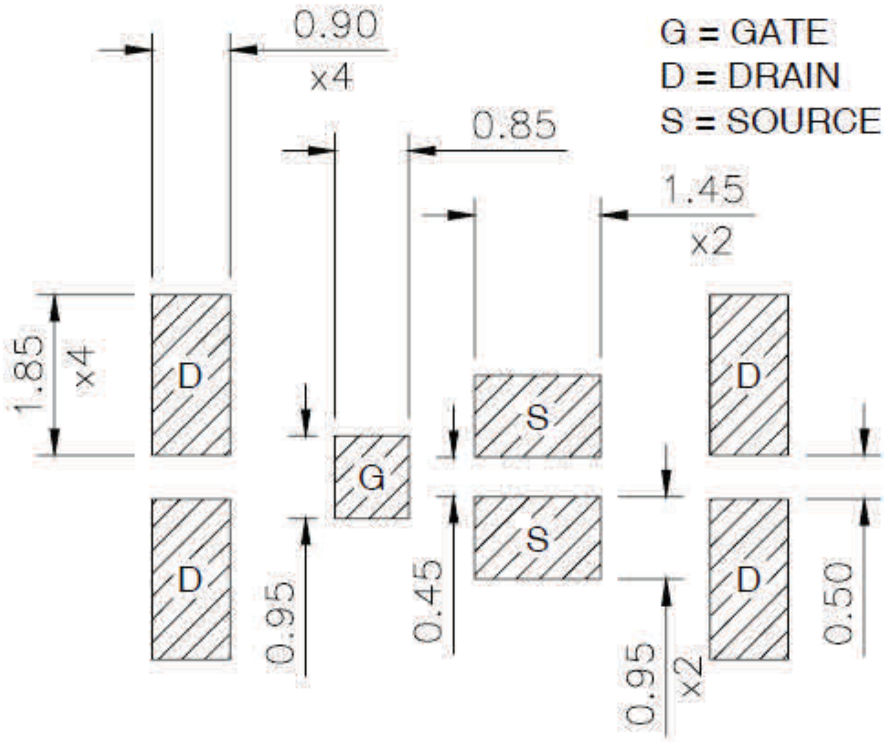


Figure 19b **Switching Time Waveforms**

5 Package Information

DirectFET™ Board Footprint, MN Outline
Please see DirectFET™ application note AN-1035 for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.

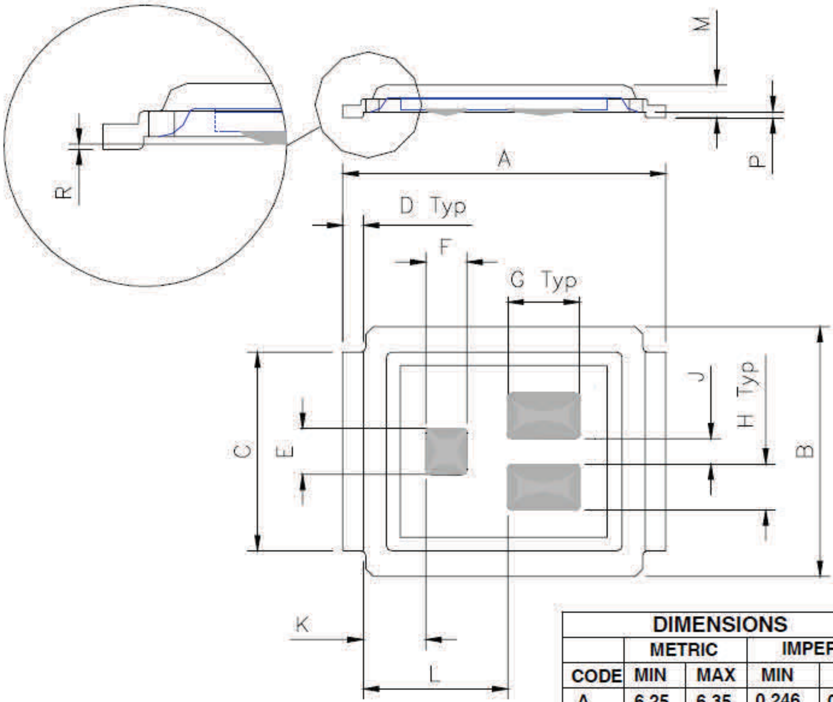




Note: For the most current drawing please refer to website at : www.irf.com/package/

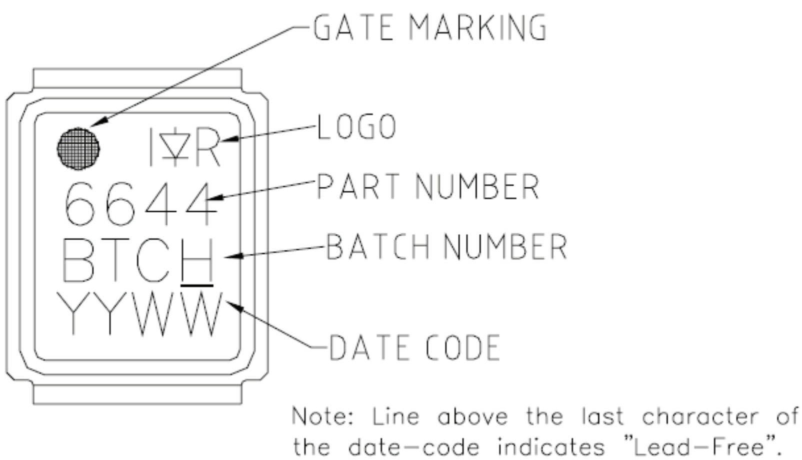
DirectFET™ Outline Dimension, MN Outline (Medium Size Can, N-Designation).

Please see DirectFET™ application note AN-1035 for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.



DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.88	0.92	0.034	0.036
F	0.78	0.82	0.031	0.032
G	1.38	1.42	0.054	0.056
H	0.88	0.92	0.034	0.036
J	0.48	0.52	0.019	0.020
K	1.16	1.29	0.046	0.051
L	2.74	2.91	0.109	0.115
M	0.616	0.676	0.0235	0.0274
R	0.020	0.080	0.0008	0.0031
P	0.08	0.17	0.003	0.007

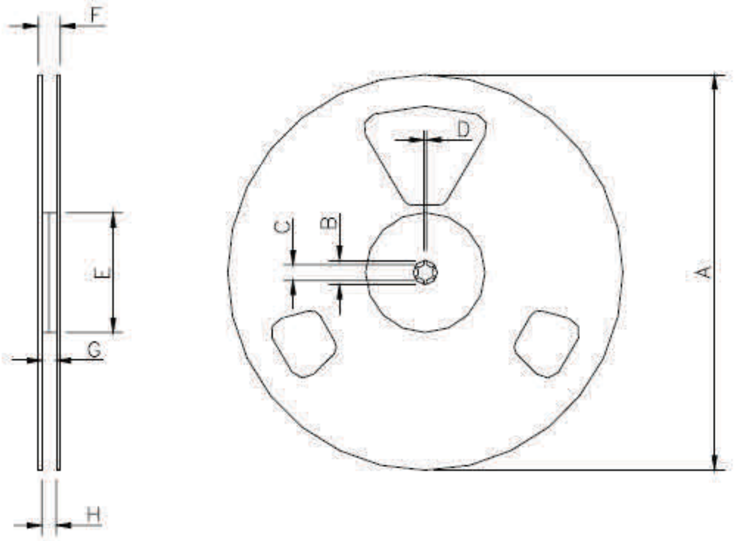
DirectFET™ Part Marking



Note: For the most current drawing please refer to website at : www.irf.com/package/

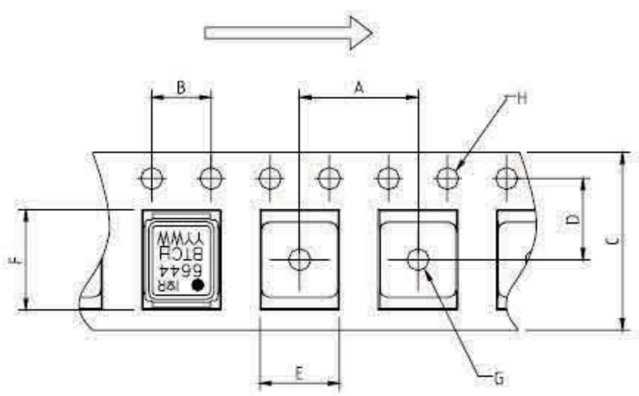
Tape & Reel Information

DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6644TRPBF). For 1000 parts on 7" reel, order IRF6644TR1PBF

REEL DIMENSIONS								
	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C



DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to website at : www.irf.com/package/

6 Qualification Information

Qualification Information

Qualification Level	Consumer (per JEDEC JESD47F) †	
Moisture Sensitivity Level	DirectFET™ Medium Can	MSL1 (per JEDEC J-STD-020D)†
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2006-08-18	• First release data sheet.
All page	2.0	2017-03-28	• This is Unique datasheet Project with Id Ratings based on RthJC. • The datasheet is converted in New Infineon Template.

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Document reference

IMPORTANT NOTICE

WARNINGS

IMPORTANT NOTICE

WARNINGS