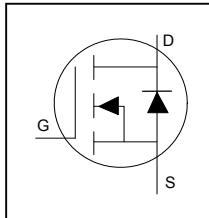


## Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

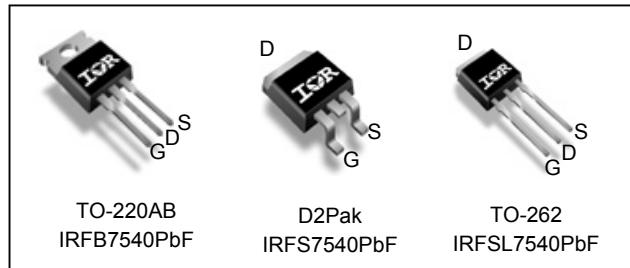
HEXFET® Power MOSFET



<b>V<sub>DS</sub>(SS)</b>	<b>60V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>4.2mΩ</b>
	<b>max</b> <b>5.1mΩ</b>
<b>I<sub>D</sub></b>	<b>110A</b>

## Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB7540PbF	TO-220	Tube	50	IRFB7540PbF
IRFSL7540PbF	TO-262	Tube	50	IRFSL7540PbF
IRFS7540PbF	D2-Pak	Tube	50	IRFS7540PbF
		Tape and Reel Left	800	IRFS7540TRLPbF

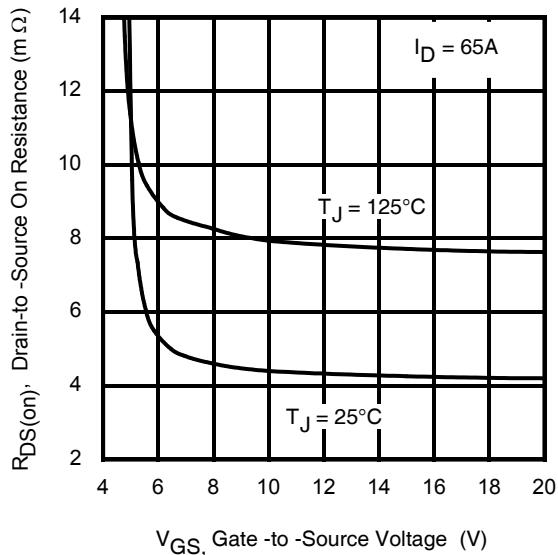


Fig 1. Typical On-Resistance vs. Gate Voltage

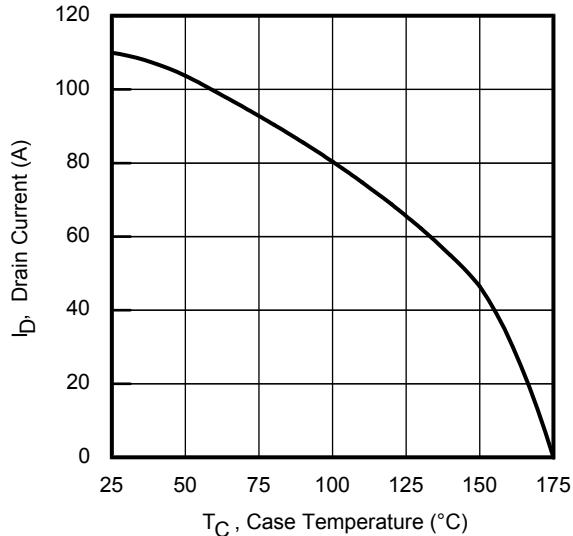


Fig 2. Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	110	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	80	
I <sub>DM</sub>	Pulsed Drain Current ①	430	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

**Avalanche Characteristics**

E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ②	180	mJ
E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ③	313	
I <sub>AR</sub>	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ⑦	—	0.95	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat Greased Surface (TO-220)	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient (TO-220)	—	62	
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) (D <sup>2</sup> Pak) ⑧	—	40	

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	48	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	4.2	5.1	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 65A
		—	5.4	—		V <sub>GS</sub> = 6.0V, I <sub>D</sub> = 33A
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.1	—	3.7	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G</sub>	Gate Resistance	—	2.2	—	Ω	

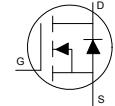
**Notes:**

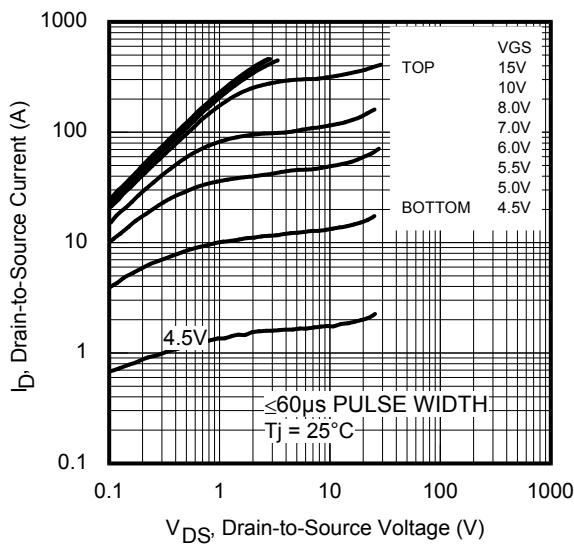
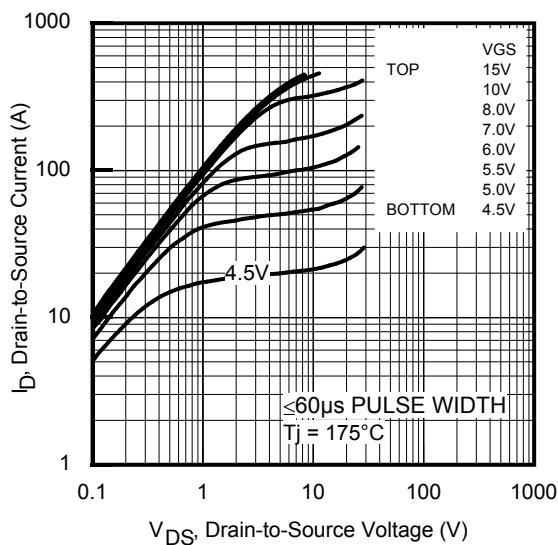
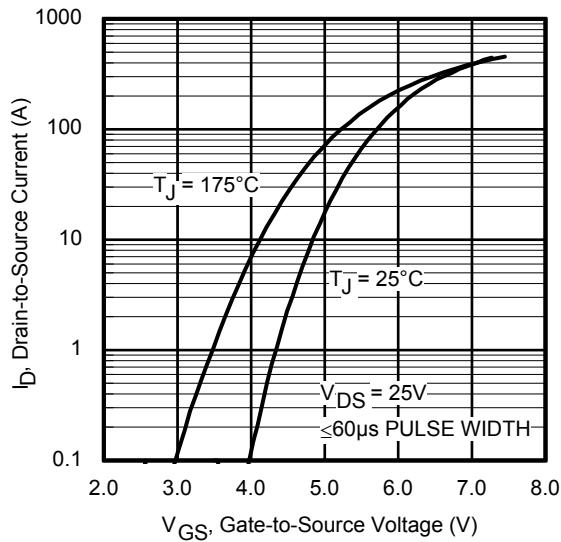
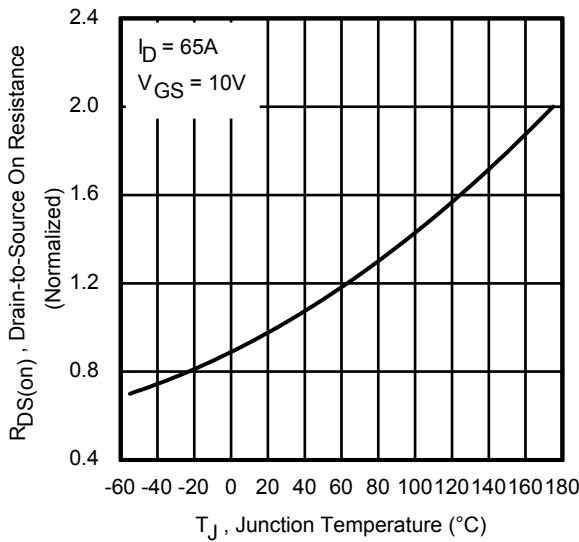
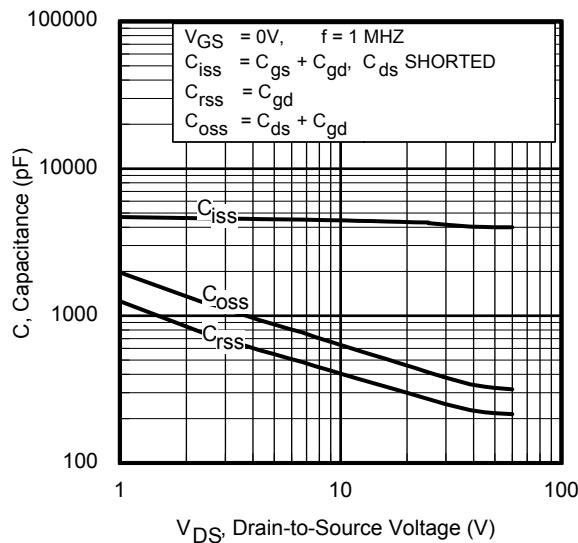
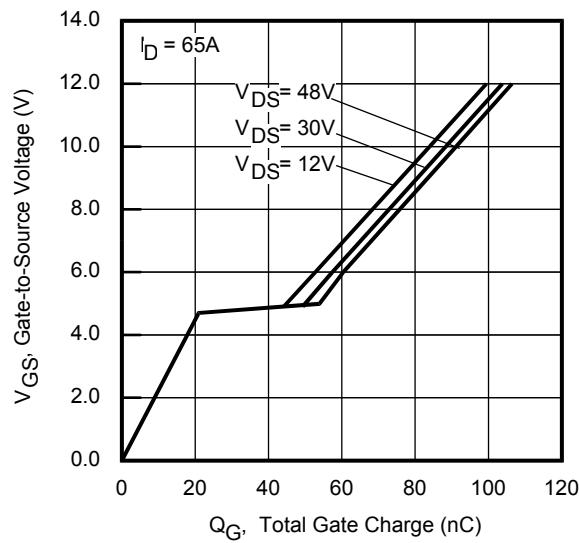
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 86μH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 65A, V<sub>GS</sub> = 10V.
- ③ I<sub>SD</sub> ≤ 65A, di/dt ≤ 1130A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑨ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 1mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 25A, V<sub>GS</sub> = 10V.

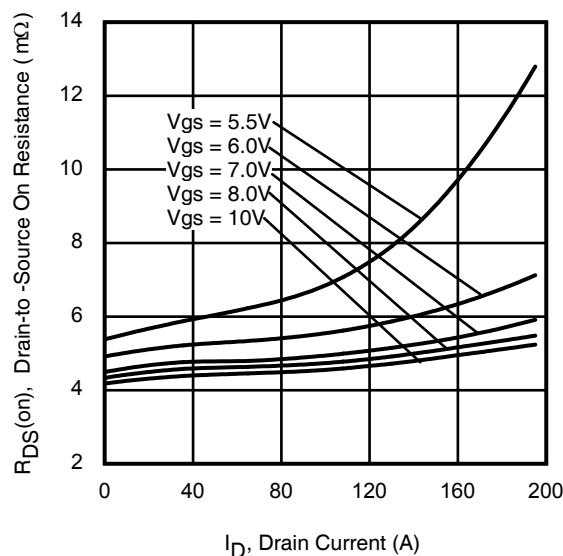
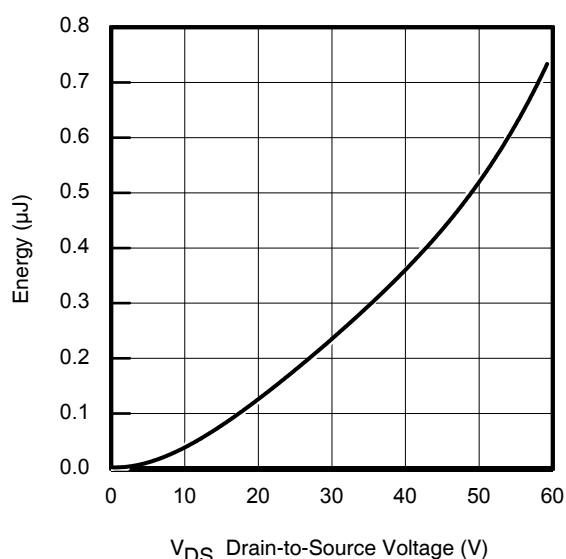
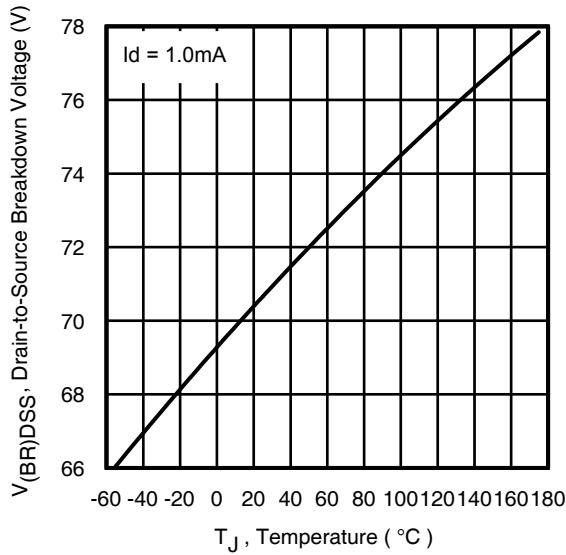
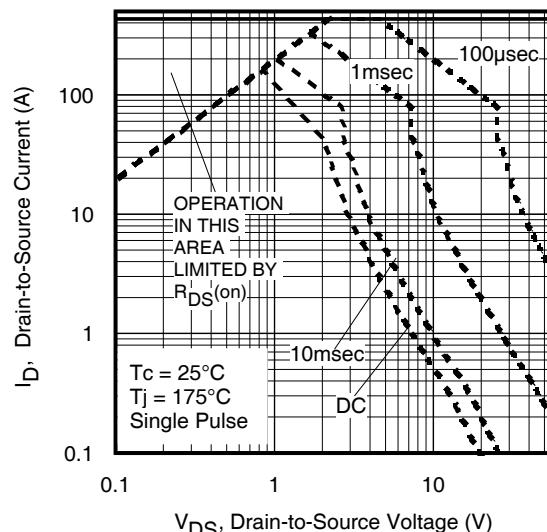
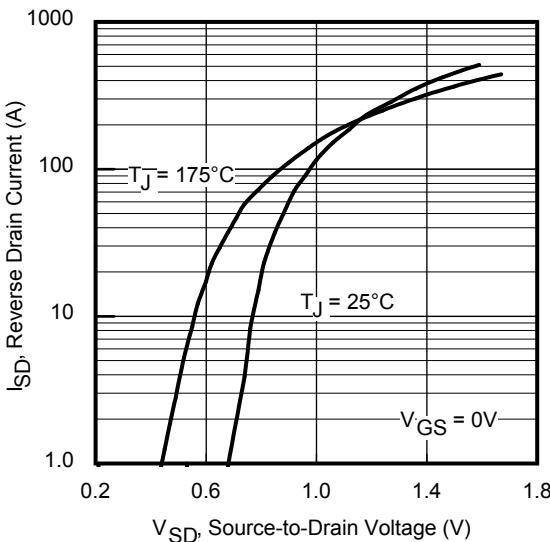
Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

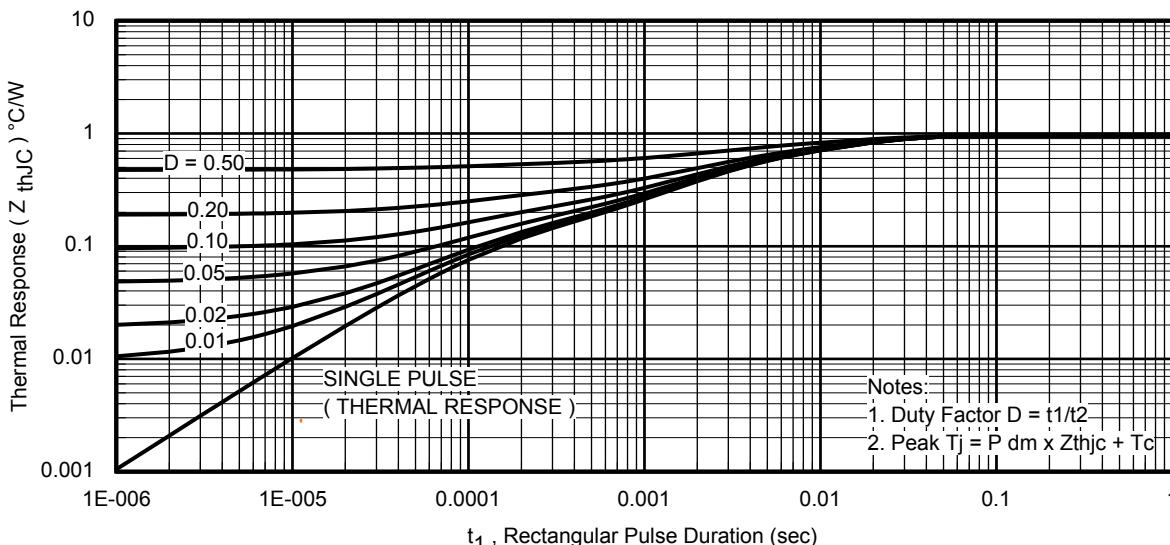
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	110	—	—	S	$V_{DS} = 10\text{V}$ , $I_D = 65\text{A}$
$Q_g$	Total Gate Charge	—	88	130	nC	$I_D = 65\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	22	—		$V_{DS} = 30\text{V}$
$Q_{gd}$	Gate-to-Drain Charge	—	28	—		$V_{GS} = 10\text{V}$
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	60	—		
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 30\text{V}$
$t_r$	Rise Time	—	76	—		$I_D = 65\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	58	—		$R_G = 2.7\Omega$
$t_f$	Fall Time	—	56	—		$V_{GS} = 10\text{V}$ ④
$C_{iss}$	Input Capacitance	—	4555	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	415	—		$V_{DS} = 25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	270	—		$f = 1.0\text{MHz}$ , See Fig.7
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	430	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $48\text{V}$ ⑥
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	550	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $48\text{V}$ ⑤

## Diode Characteristics

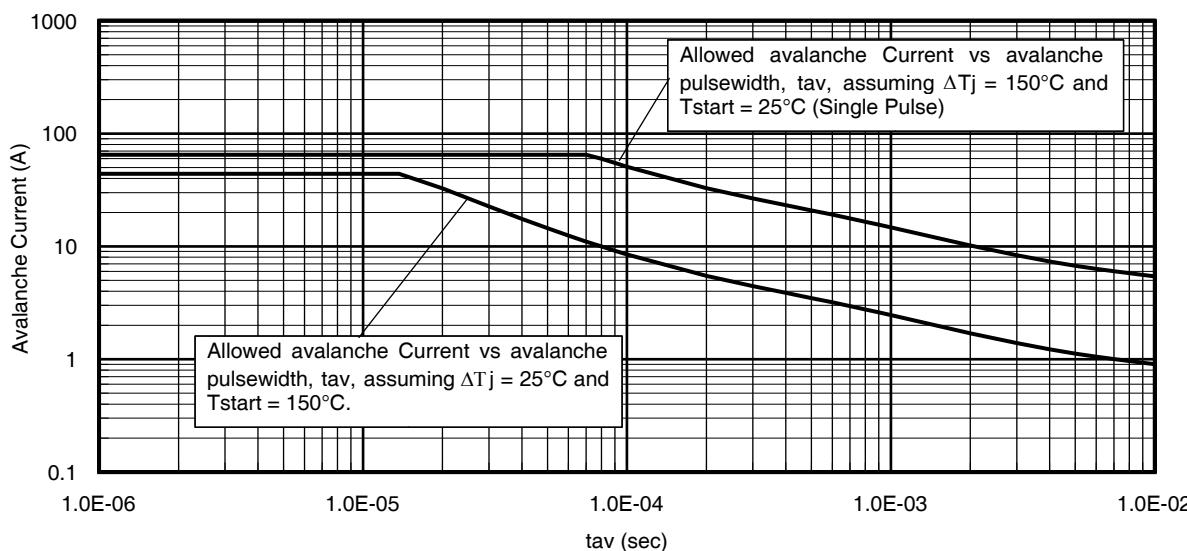
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	110	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	430		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_s = 65\text{A}$ , $V_{GS} = 0\text{V}$ ④
$dv/dt$	Peak Diode Recovery $dv/dt$	—	11	—	V/ns	$T_J = 175^\circ\text{C}$ , $I_s = 65\text{A}$ , $V_{DS} = 60\text{V}$ ③
$t_{rr}$	Reverse Recovery Time	—	33	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51\text{V}$
		—	37	—		$T_J = 125^\circ\text{C}$ $I_F = 65\text{A}$ ,
$Q_{rr}$	Reverse Recovery Charge	—	36	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ④
		—	47	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	1.9	—	A	$T_J = 25^\circ\text{C}$

**Fig 3.** Typical Output Characteristics**Fig 4.** Typical Output Characteristics**Fig 5.** Typical Transfer Characteristics**Fig 6.** Normalized On-Resistance vs. Temperature**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage

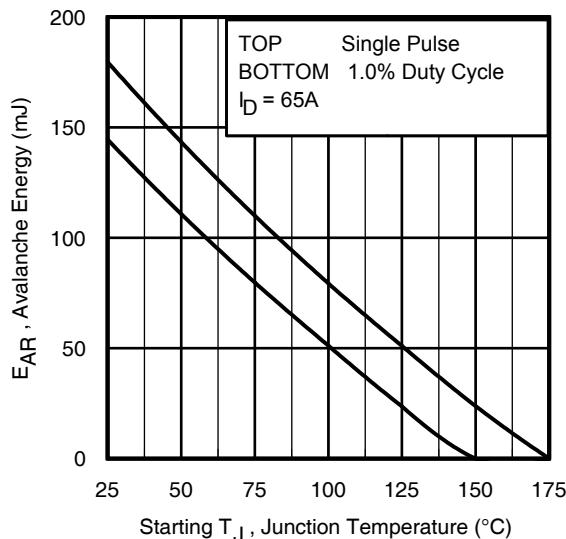




**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



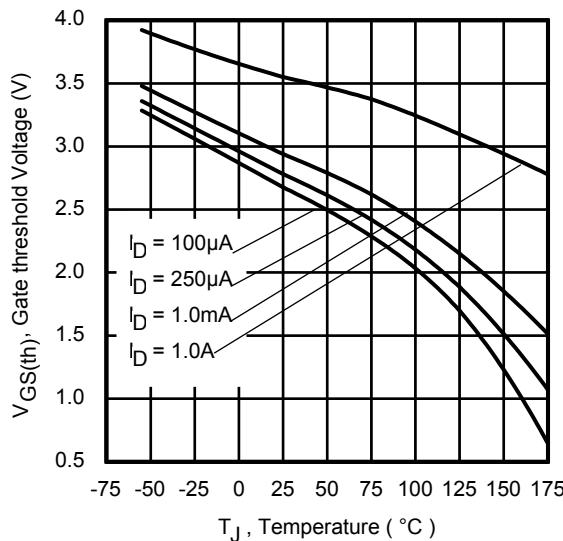
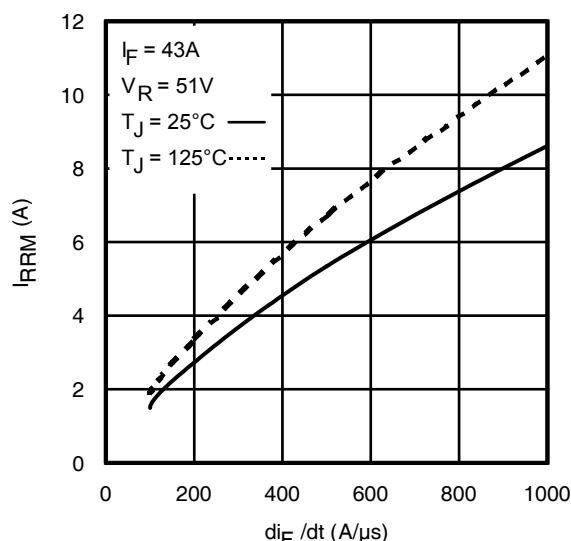
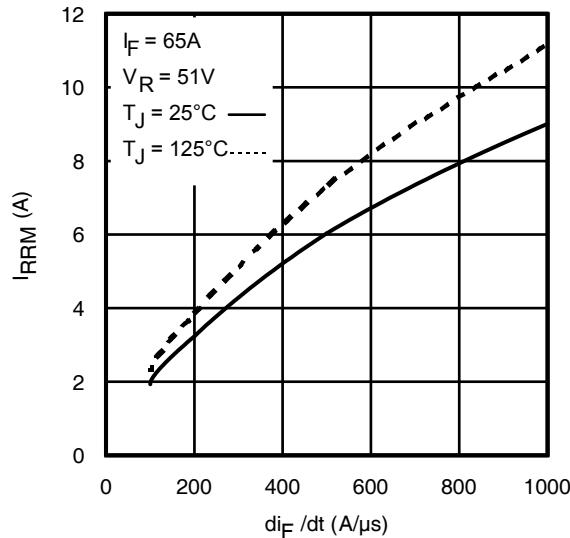
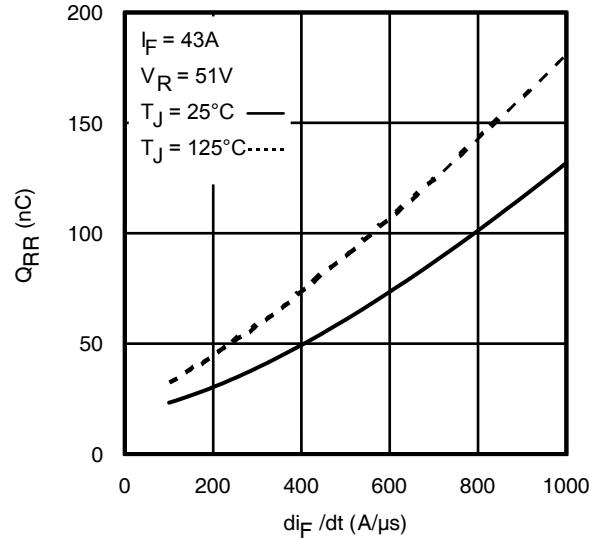
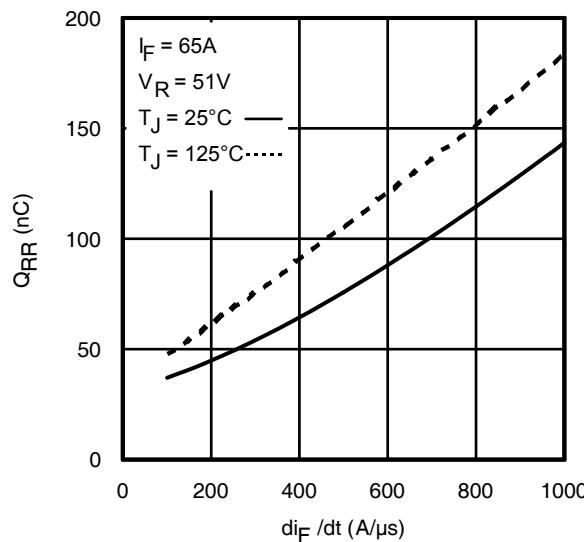
**Fig 15.** Avalanche Current vs. Pulse Width



**Fig 16.** Maximum Avalanche Energy vs. Temperature

#### Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
  2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
  3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
  4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
  5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
  6.  $I_{av}$  = Allowable avalanche current.
  7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ\text{C}$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 14)
- $PD(ave) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $EAS(AR) = P_{D(ave)} \cdot t_{av}$

**Fig 17.** Threshold Voltage vs. Temperature**Fig 18.** Typical Recovery Current vs.  $di/dt$ **Fig 19.** Typical Recovery Current vs.  $di/dt$ **Fig 20.** Typical Stored Charge vs.  $di/dt$ **Fig 21.** Typical Stored Charge vs.  $di/dt$

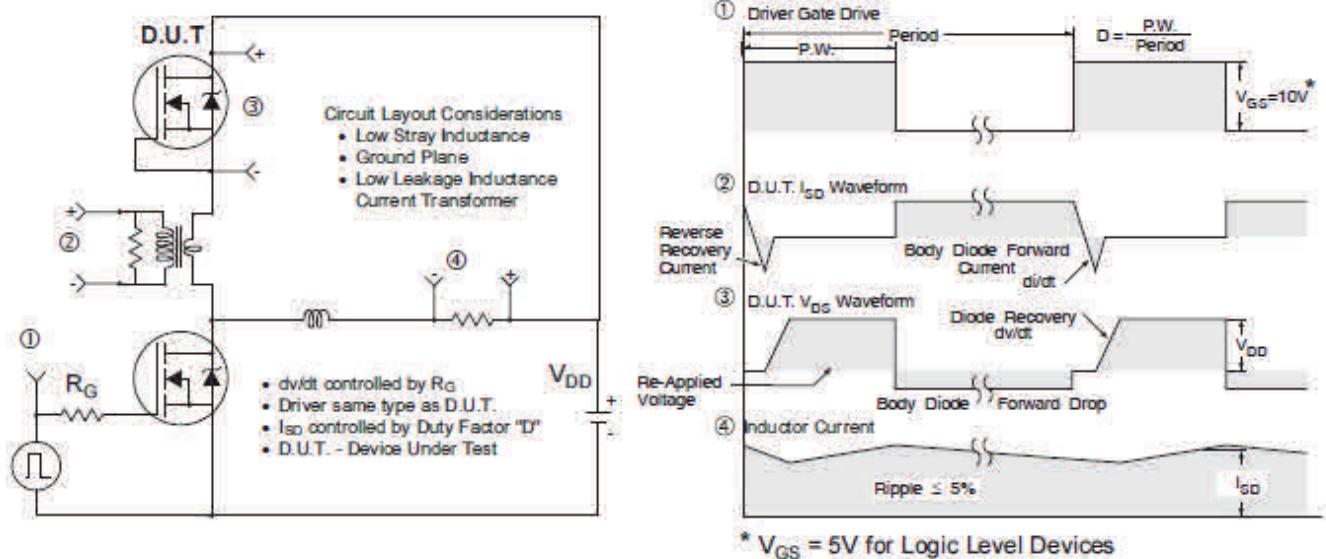


Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

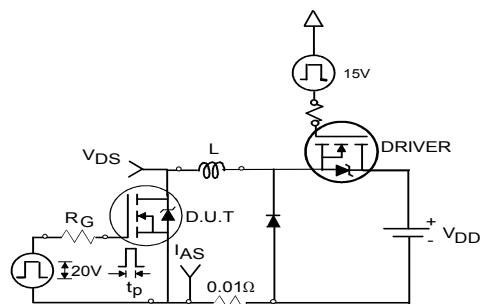


Fig 23a. Unclamped Inductive Test Circuit

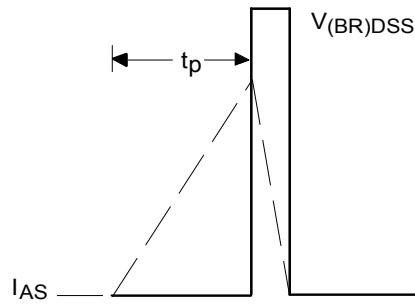


Fig 23b. Unclamped Inductive Waveforms

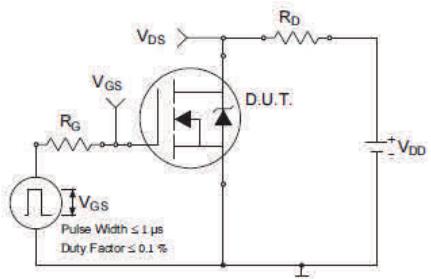


Fig 24a. Switching Time Test Circuit

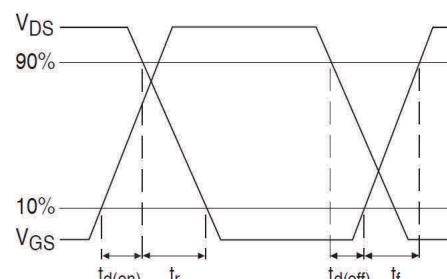


Fig 24b. Switching Time Waveforms

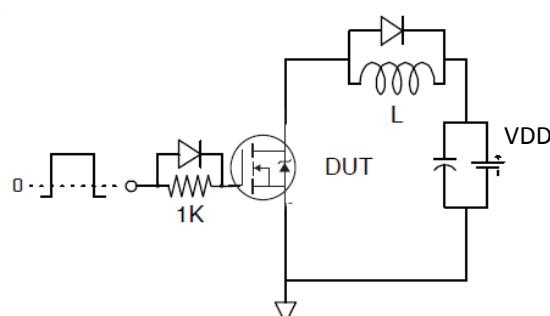


Fig 25a. Gate Charge Test Circuit

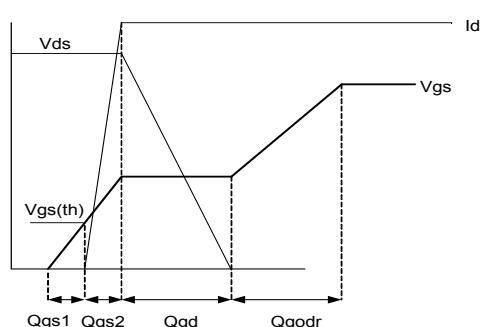
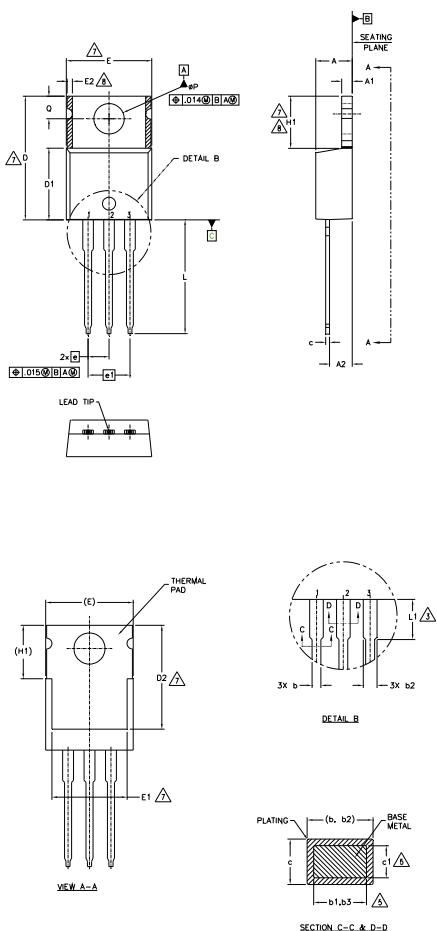


Fig 25b. Gate Charge Waveform

## TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



## NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.83	.140	.190		
A1	1.14	1.40	.045	.055		
A2	2.03	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.97	.015	.038	5	
b2	1.14	1.78	.045	.070	5	
b3	1.14	1.73	.045	.068	5	
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650	4	
D1	8.38	9.02	.330	.355		
D2	11.68	12.88	.460	.507	7	
E	9.65	10.67	.380	.420	4,7	
E1	6.86	8.89	.270	.350	7	
E2	-	0.76	-	.030	8	
e	2.54 BSC		.100 BSC			
e1	5.08 BSC		.200 BSC		7,8	
H1	5.84	6.86	.230	.270		
L	12.70	14.73	.500	.580		
L1	3.56	4.06	.140	.160	3	
ØP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		

## LEAD ASSIGNMENTS

## HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

## IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter

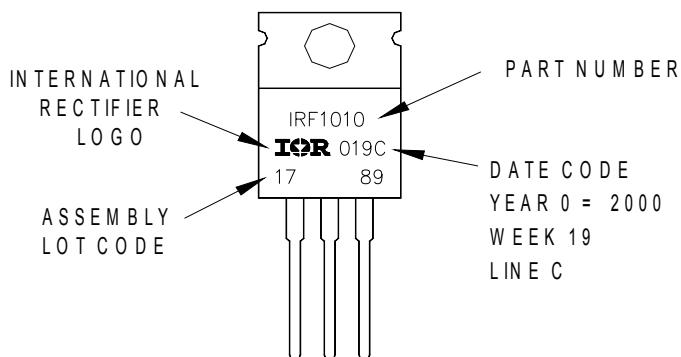
## DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

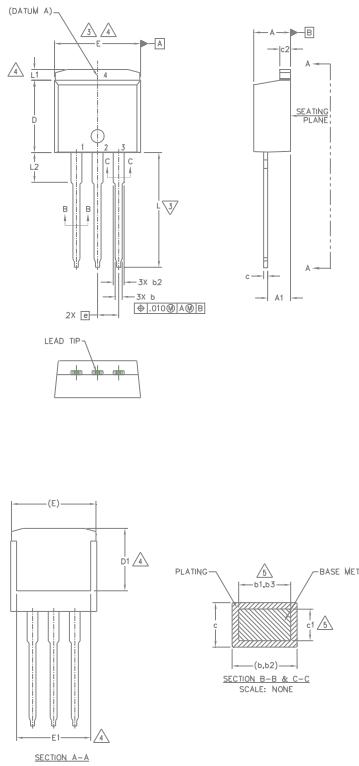
Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	2.03	3.02	.080	.119		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068	5	
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	—	.270	—	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	—	.245	—	4	
e	2.54	BSC	.100	BSC		
L	13.46	14.10	.530	.555		
L1	—	1.65	—	.065	4	
L2	3.56	3.71	.140	.146		

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

### LEAD ASSIGNMENTS

#### IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

#### HEXFET

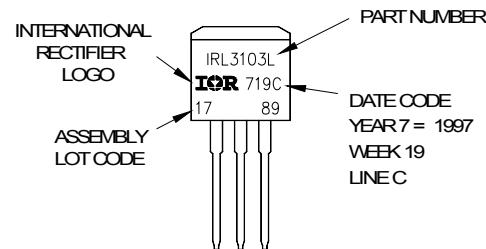
- |           |                                     |
|-----------|-------------------------------------|
| 1. GATE   | 1. ANODE (TWO DIE) / OPEN (ONE DIE) |
| 2. DRAIN  | 2. 4. CATHODE                       |
| 3. SOURCE | 3. ANODE                            |
| 4. DRAIN  |                                     |

#### DIODES

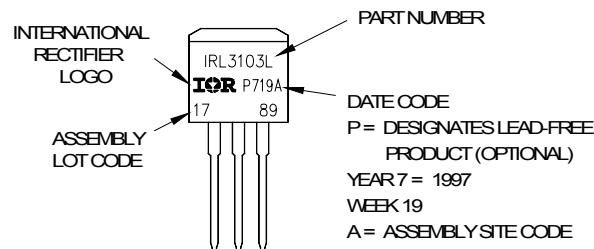
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW19, 1997  
 IN THE ASSEMBLY LINE "C"

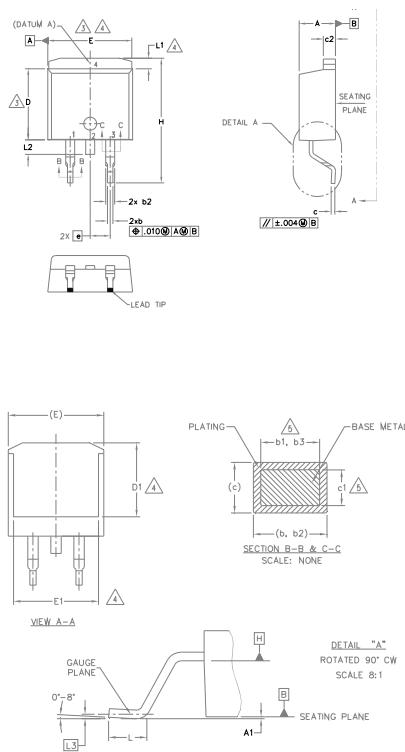
Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))**

SYMBOL	DIMENSIONS		NOTES	
	MILLIMETERS	INCHES		
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	.160	.190
A1	0.00	0.254	.000	.010
b	0.51	0.99	.020	.039
b1	0.51	0.89	.020	.035
b2	1.14	1.78	.045	.070
b3	1.14	1.73	.045	.068
c	0.38	0.74	.015	.029
c1	0.38	0.58	.015	.023
c2	1.14	1.65	.045	.065
D	8.38	9.65	.330	.380
D1	6.86	—	.270	—
E	9.65	10.67	.380	.420
E1	6.22	—	.245	—
e	2.54	BSC	.100	BSC
H	14.61	15.88	.575	.625
L	1.78	2.79	.070	.110
L1	—	1.68	—	.066
L2	—	1.78	—	.070
L3	0.25	BSC	.010	BSC

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

## LEAD ASSIGNMENTS

## DIODES

- 1.— ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.— CATHODE
- 3.— ANODE

## HEXFET

- 1.— GATE
- 2, 4.— DRAIN
- 3.— SOURCE

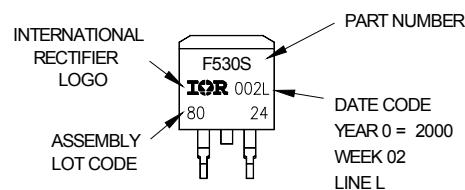
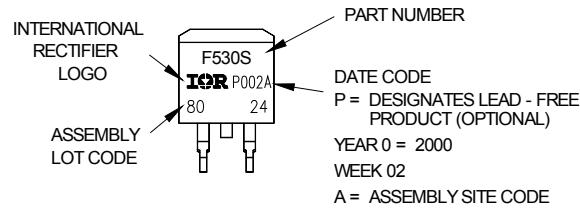
## IGBTs, CoPACK

- 1.— GATE
- 2, 4.— COLLECTOR
- 3.— Emitter

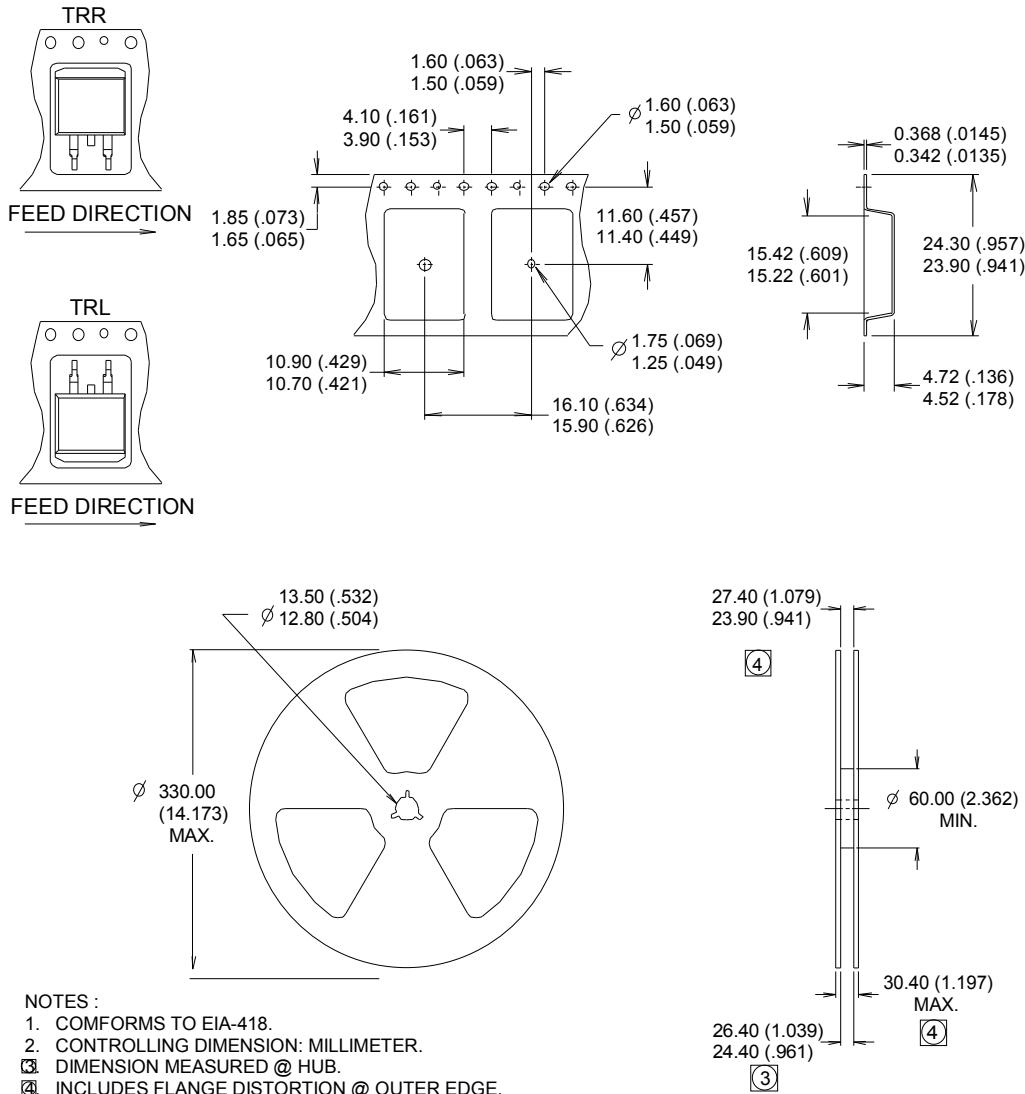
**D<sup>2</sup>Pak (TO-263AB) Part Marking Information**

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"

OR

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-220	N/A
	D <sup>2</sup> Pak	MSL1
	TO-262	N/A
<b>RoHS Compliant</b>	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

<sup>††</sup> Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
11/6/2014	<ul style="list-style-type: none"> <li>• Updated <math>E_{AS} (L=1mH) = 313mJ</math> on page 2</li> <li>• Updated note 8 "Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 25A</math>, <math>V_{GS} = 10V</math>". on page 2</li> <li>• Updated package outline on page 9,10,11.</li> </ul>

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