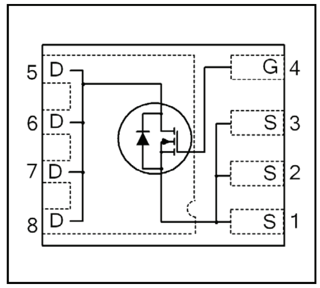
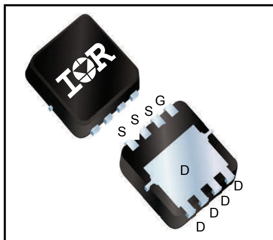
HEXFET® Power MOSFET

V_{DSS}	25	V
V_{GS} max	±20	V
$R_{DS(on)}$ max (@ V_{GS} = 10V)	7.7	mΩ
(@ V_{GS} = 4.5V)	13.4	
Qg (typical)	7.7	nC
I_D (@$T_{C\ (Bottom)}$ = 25°C)	25⑦	A





PQFN 3.3X3.3 mm

Applications

- Control MOSFET for synchronous buck converter

Features		Benefits
Low Thermal Resistance to PCB (<4.1°C/W)		Enable better Thermal Dissipation
Low Profile (<1.05mm)		Increased Power Density
Industry-Standard Pin out	results in	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques	⇒	Easier Manufacturing
RoHS Compliant, Halogen-Free		Environmentally Friendlier
MSL1, Consumer Qualification		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHM8235PbF	PQFN 3.3 mm x 3.3 mm	Tape and Reel	4000	IRFHM8235TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	16	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	13	
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V	50⑥⑦	
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V	32⑥⑦	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Source Bonding Technology Limited)	25⑦	
I_{DM}	Pulsed Drain Current ①	240⑧	
P_D @T_A = 25°C	Power Dissipation ⑤	3.0	W
P_D @$T_{C(Bottom)}$ = 25°C	Power Dissipation ⑤	30	
	Linear Derating Factor ⑤	0.024	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑧ are on page 10

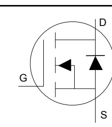
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	19	—	mV/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.2	7.7	mΩ	V_{GS} = 10V, I_D = 20A ③
		—	10.3	13.4		V_{GS} = 4.5V, I_D = 16A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS} = V_{GS}, I_D = 25μA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.9	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V_{DS} = 20V, V_{GS} = 0V
		—	—	150		V_{DS} = 20V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	43	—	—	S	V_{DS} = 10V, I_D = 20A
Q_g	Total Gate Charge	—	16	—	nC	V_{GS} = 10V, V_{DS} = 13V, I_D = 20A
Q_g	Total Gate Charge	—	7.7	12	nC	V_{DS} = 13V V_{GS} = 4.5V I_D = 20A
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	1.9	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.3	—		
Q_{gd}	Gate-to-Drain Charge	—	2.7	—		
Q_{godr}	Gate Charge Overdrive	—	1.5	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	4.0	—		
Q_{oss}	Output Charge	—	6.4	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	1.6	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	7.9	—	ns	V_{DD} = 13V, V_{GS} = 4.5V I_D = 20A R_G=1.8Ω
t_r	Rise Time	—	16	—		
$t_{d(off)}$	Turn-Off Delay Time	—	7.5	—		
t_f	Fall Time	—	5.2	—		
C_{iss}	Input Capacitance	—	1040	—	pF	V_{GS} = 0V V_{DS} = 10V f = 1.0MHz
C_{oss}	Output Capacitance	—	300	—		
C_{rss}	Reverse Transfer Capacitance	—	120	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	41	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	25⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	240⑧		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 20A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	10	15	ns	T_J = 25°C, I_F = 20A, V_{DD} = 13V
Q_{rr}	Reverse Recovery Charge	—	4.9	7.4	nC	di/dt = 300A/μs ③

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	4.1	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	42	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	42	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	—	28	

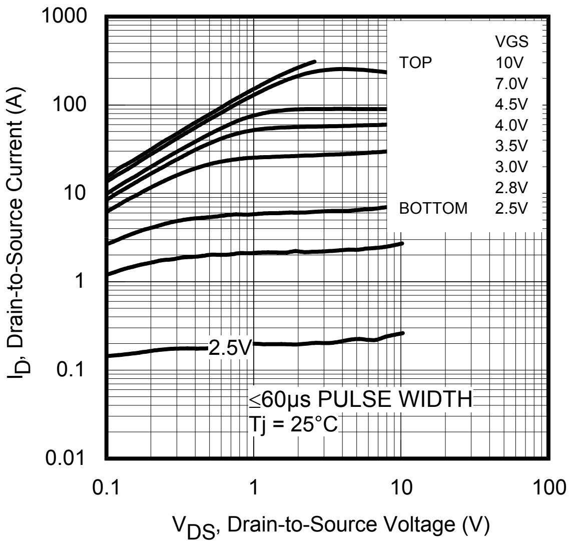


Fig 1. Typical Output Characteristics

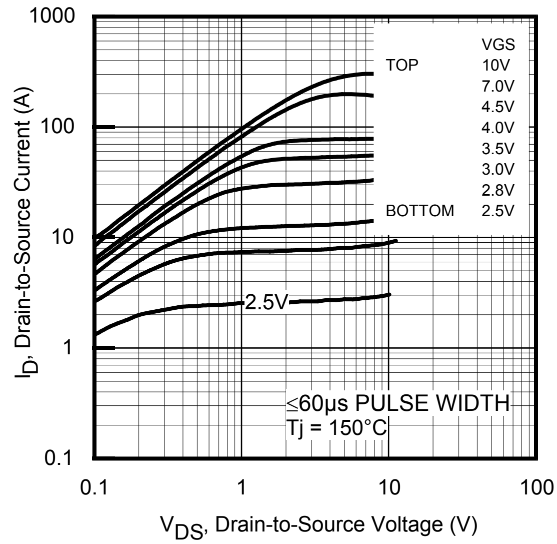


Fig 2. Typical Output Characteristics

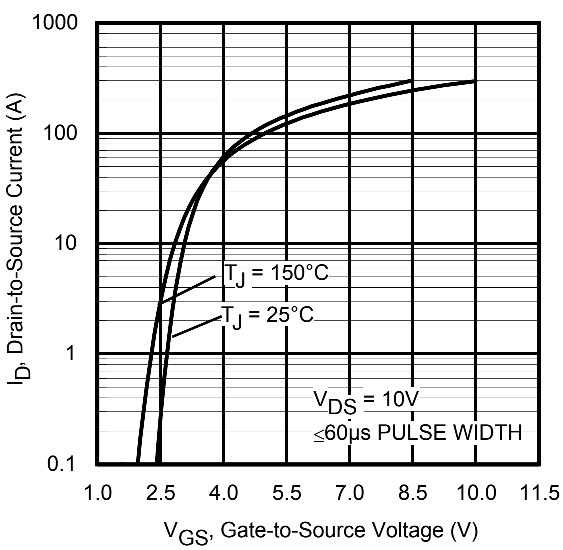


Fig 3. Typical Transfer Characteristics

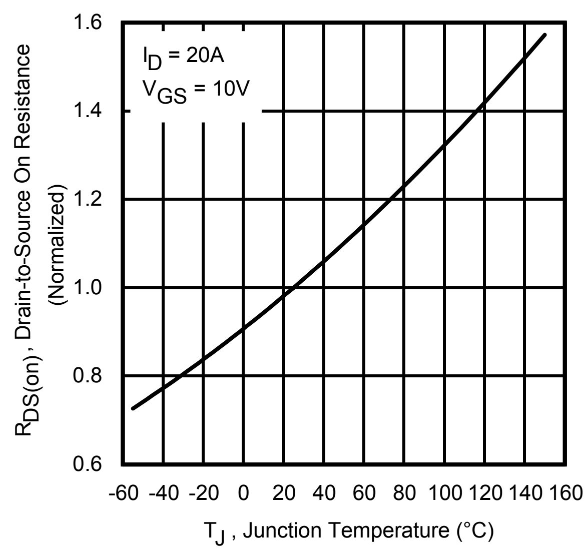


Fig 4. Normalized On-Resistance vs. Temperature

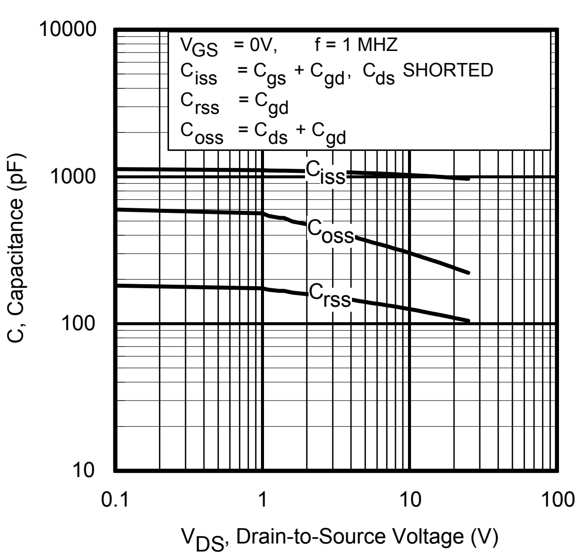


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

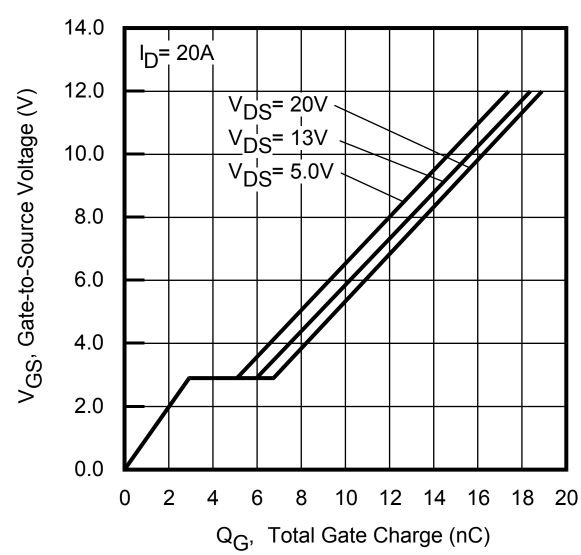


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

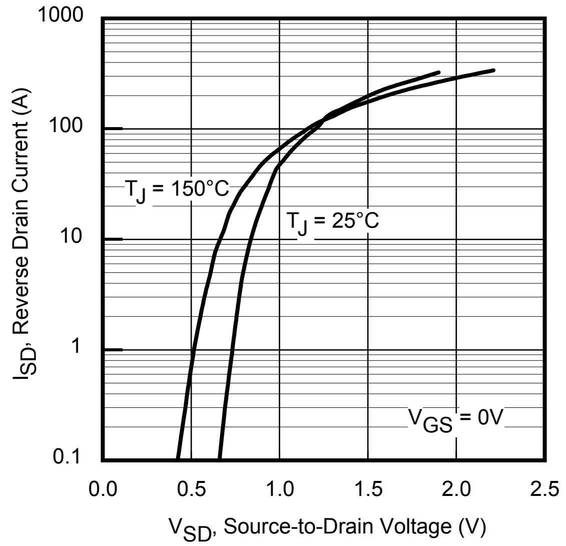


Fig 7. Typical Source-Drain Diode Forward Voltage

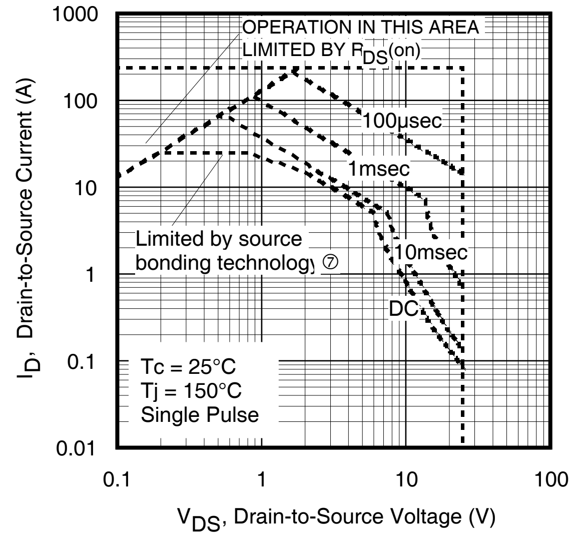


Fig 8. Maximum Safe Operating Area

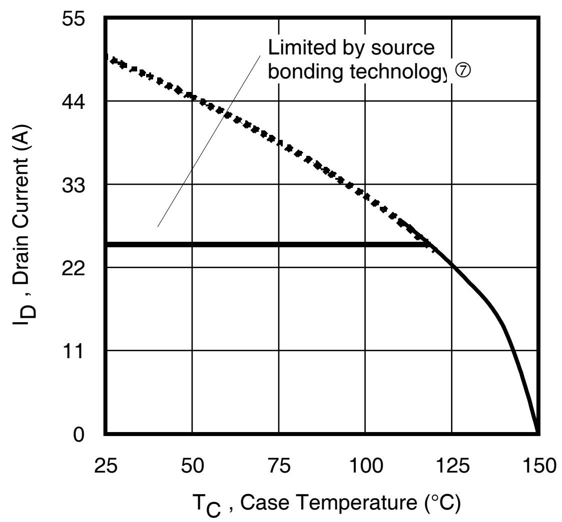


Fig 9. Maximum Drain Current vs. Case Temperature

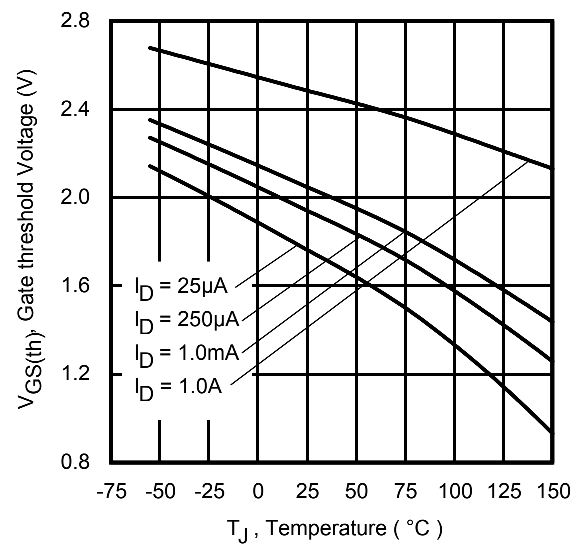


Fig 10. Threshold Voltage Vs. Temperature

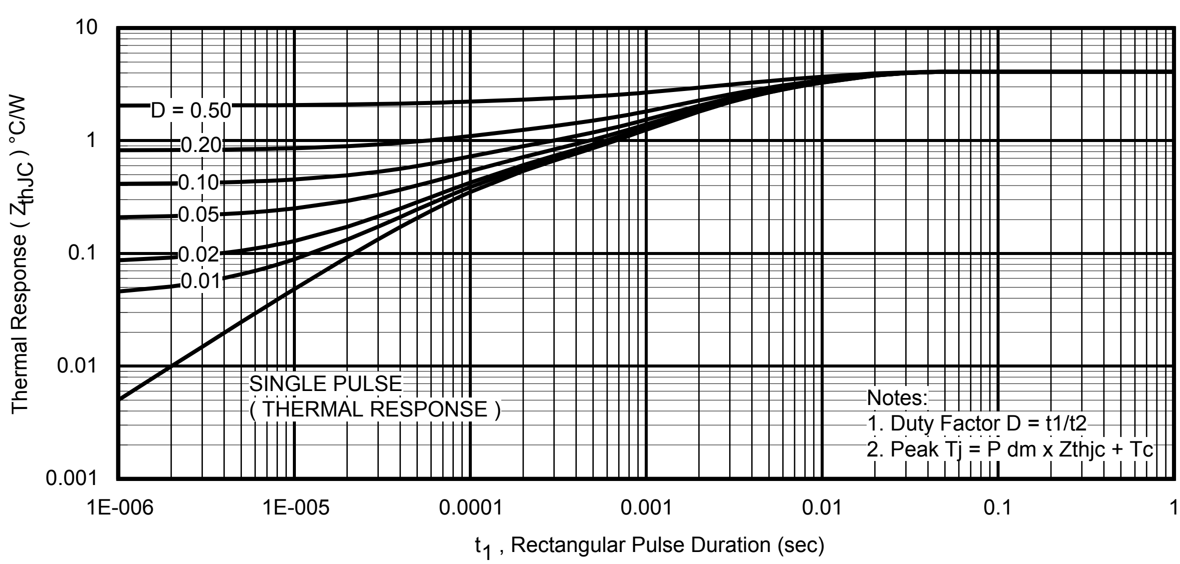


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

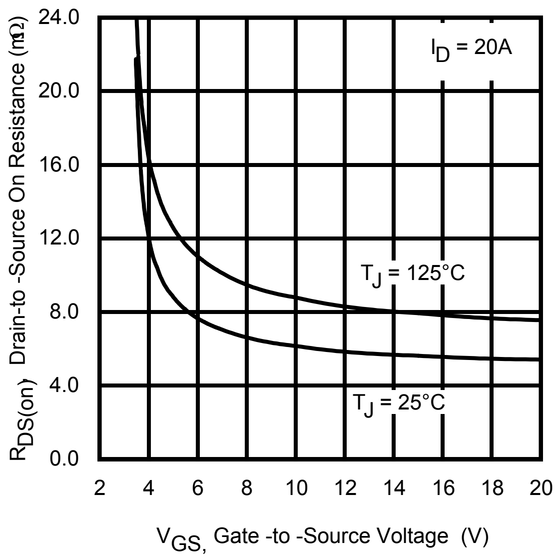


Fig 12. On-Resistance vs. Gate Voltage

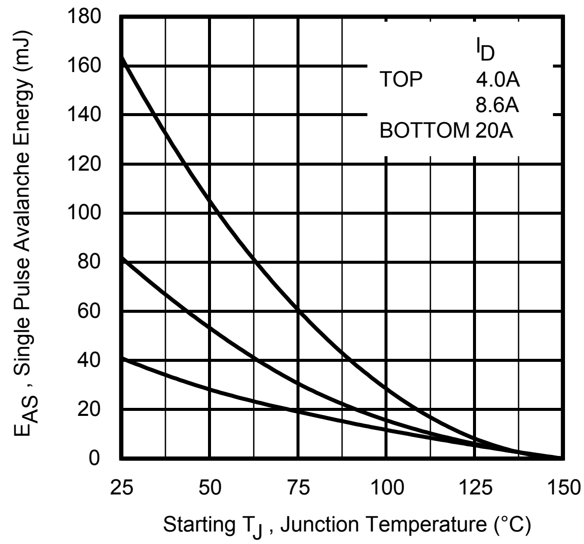


Fig 13. Maximum Avalanche Energy vs. Drain Current

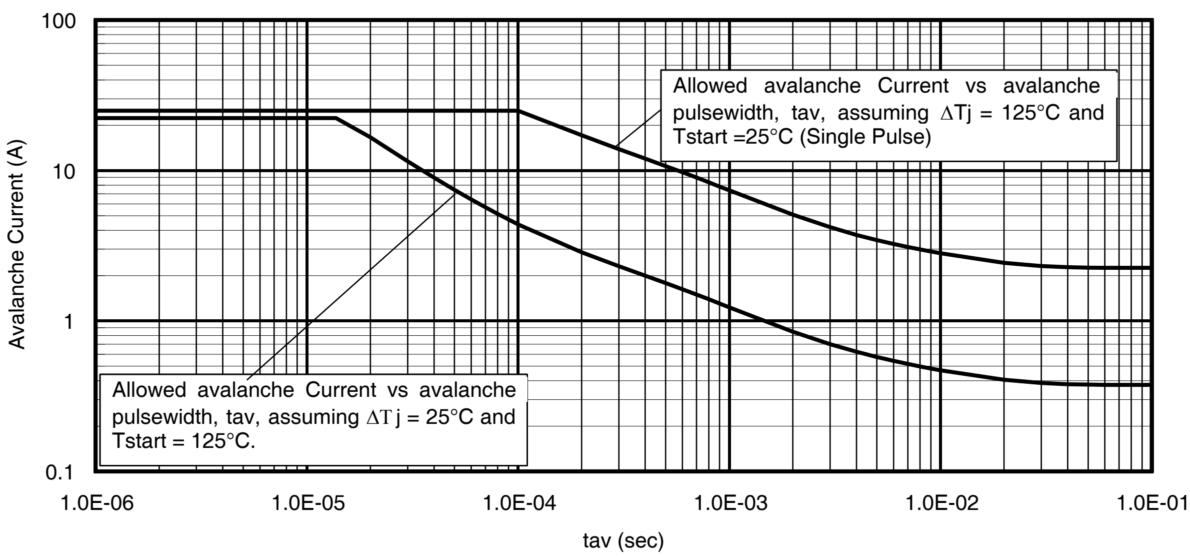


Fig 14. Single avalanche event: pulse current vs. pulse width

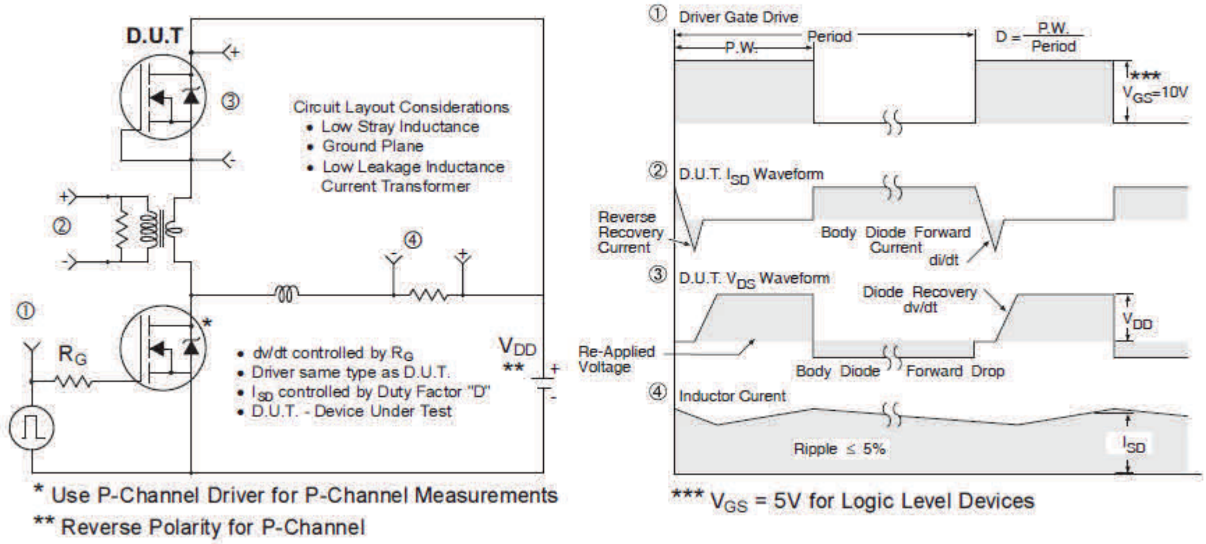


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

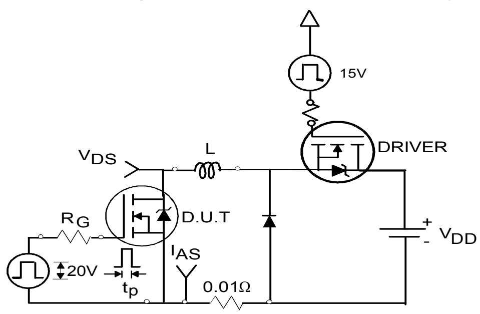


Fig 16a. Unclamped Inductive Test Circuit

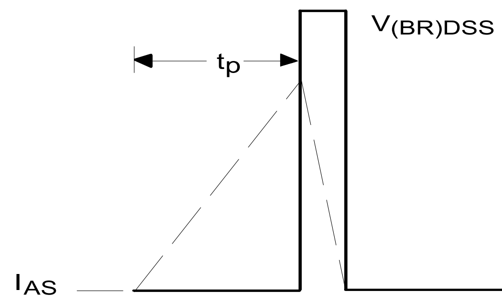


Fig 16b. Unclamped Inductive Waveforms

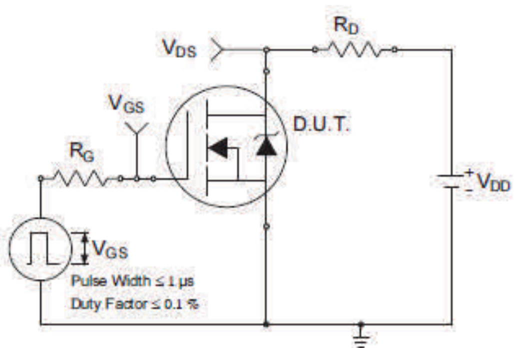


Fig 17a. Switching Time Test Circuit

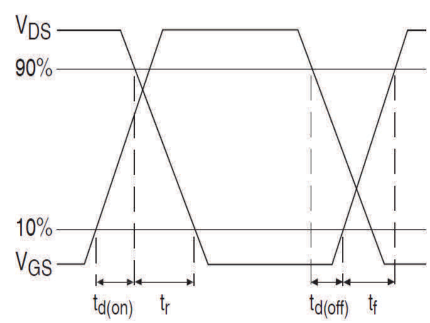


Fig 17b. Switching Time Waveforms

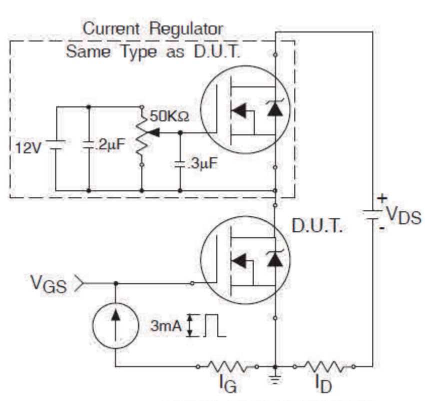


Fig 18a. Gate Charge Test Circuit

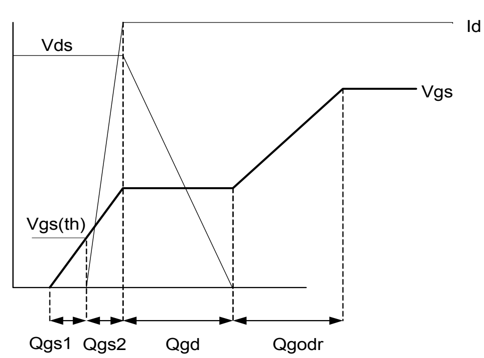


Fig 18b. Gate Charge Waveform

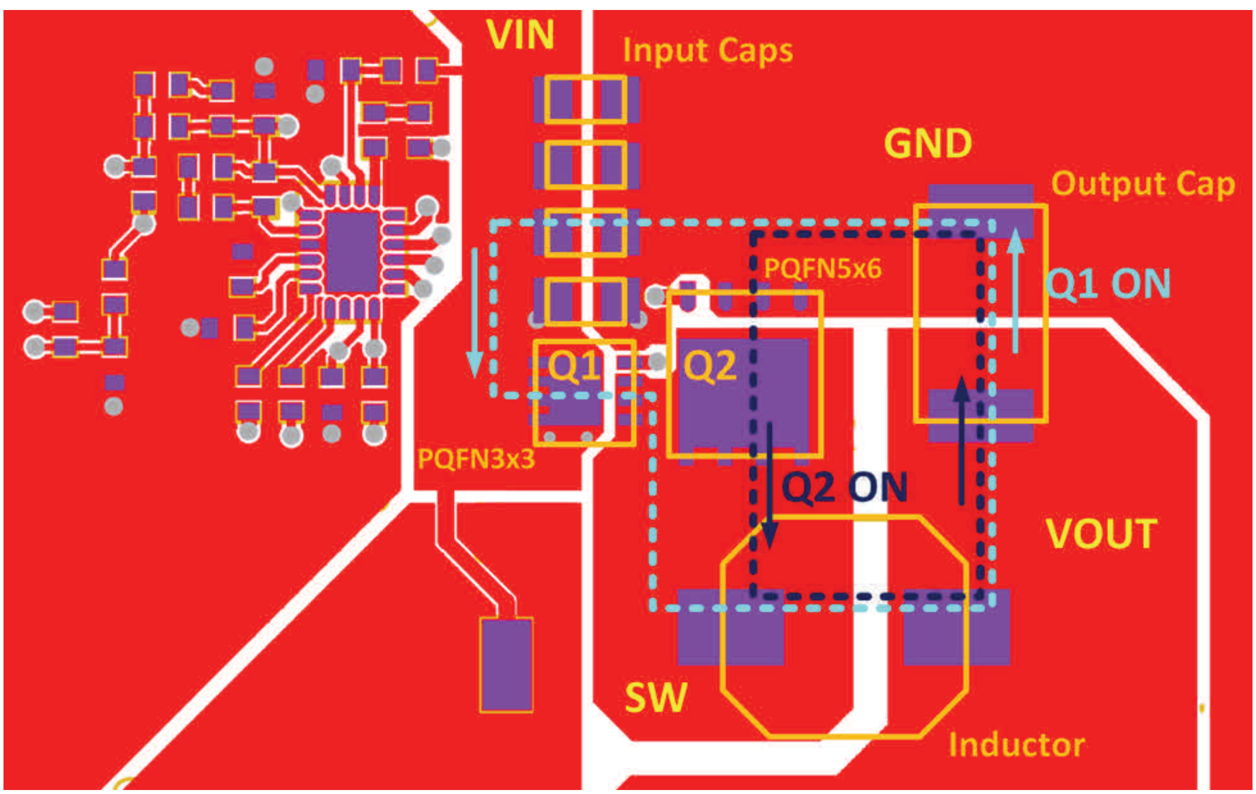
Placement and Layout Guidelines

The typical application topology for this product is the synchronous buck converter. These converters operate at high frequencies (typically around 400 kHz). During turn-on and turn-off switching cycles, the high di/dt currents circulating in the parasitic elements of the circuit induce high voltage ringing which may exceed the device rating and lead to undesirable effects. One of the major contributors to the increase in parasitics is the PCB power circuit inductance.

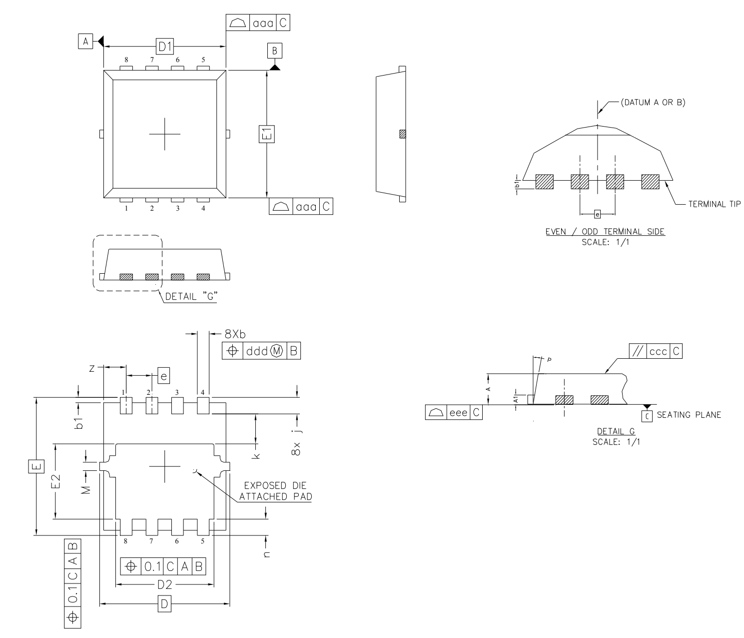
This section introduces a simple guideline that mitigates the effect of these parasitics on the performance of the circuit and provides reliable operation of the devices.

To reduce high frequency switching noise and the effects of Electromagnetic Interference (EMI) when the control MOSFET (Q1) is turned on, the layout shown in Figure 19 is recommended. The input bypass capacitors, control MOSFET and output capacitors are placed in a tight loop to minimize parasitic inductance which in turn lowers the amplitude of the switch node ringing, and minimizes exposure of the MOSFETs to repetitive avalanche conditions.

When the synchronous MOSFET (Q2) is turned on, high average DC current flows through the path indicated in Figure 19. Therefore, the Q2 turn-on path should be laid out with a tight loop and wide traces at both ends of the inductor to minimize loop resistance.

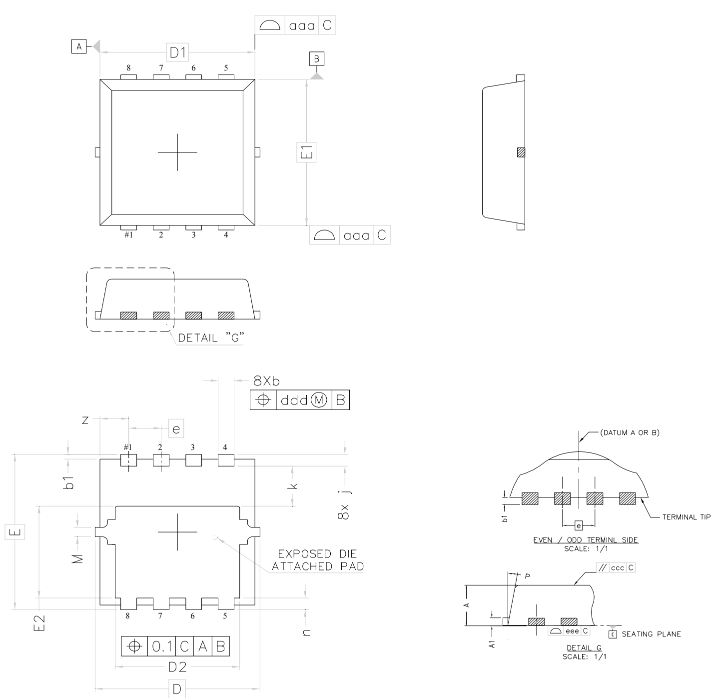


PQFN 3.3 x 3.3 Outline “C” Package Details



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	.0276	.0315
A1	0.10	0.25	.0039	.0098
b	0.25	0.35	.0098	.0138
b1	0.05	0.15	.0020	.0059
D	3.20	3.40	.1260	.1339
D1	3.00	3.20	.1181	.1260
D2	2.39	2.59	.0941	.1020
E	3.25	3.45	.1280	.1358
E1	3.00	3.20	.1181	.1260
E2	1.78	1.98	.0701	.0780
e	0.65 BSC		.0255 BSC	
j	0.30	0.50	.0118	.0197
k	0.59	0.79	.0232	.0311
n	0.30	0.50	.0118	.0197
M	0.03	0.23	.0012	.0091
P	10°	12°	10°	12°
z	0.50	0.70	.0197	.0276

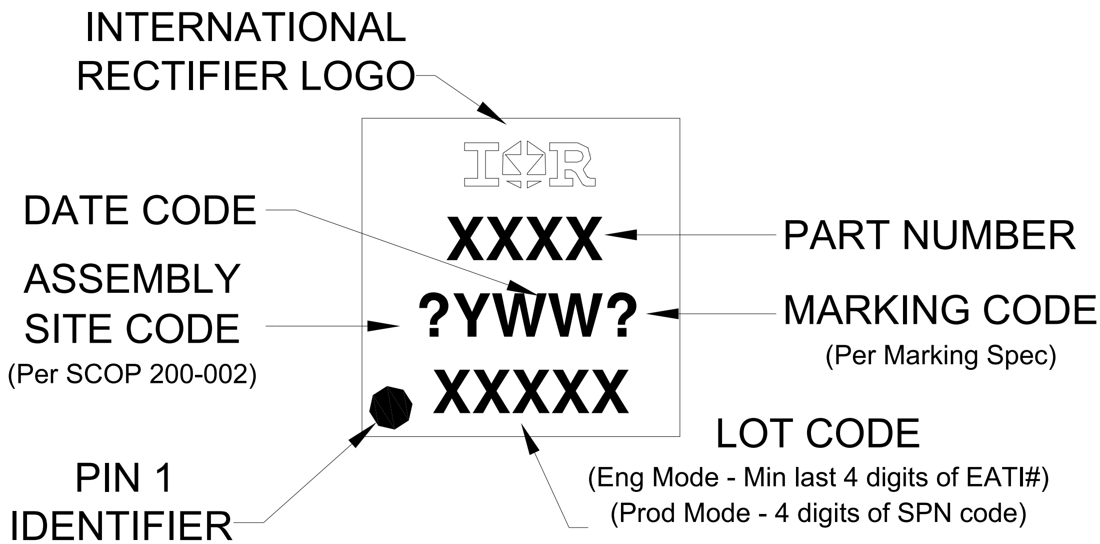
PQFN 3.3 x 3.3 Outline “G” Package Details



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	0.90	.0315	.0354
A1	0.12	0.22	.0047	.0086
b	0.22	0.42	.0087	.0165
b1	0.05	0.15	.0020	.0059
D	3.30 BSC		.1299 BSC	
D1	3.10 BSC		.1220 BSC	
D2	2.29	2.69	.0902	.1059
E	3.30 BSC		.1299 BSC	
E1	3.10 BSC		.1220 BSC	
E2	1.85	2.05	.0728	.0807
e	0.65 BSC		.0255 BSC	
j	0.15	0.35	.0059	.0137
k	0.75	0.95	.0295	.0374
n	0.15	0.35	.0059	.0137
M	NOM. 0.20		NOM. .0078	
P	9°	11°	9°	11°

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

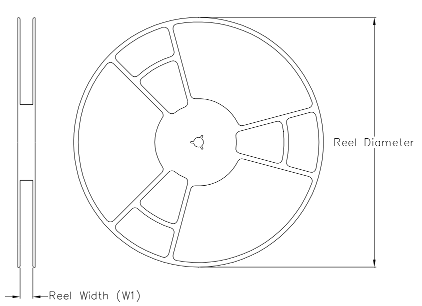
PQFN 3.3mm x 3.3mm Outline Part Marking



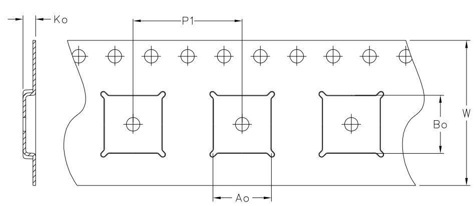
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

PQFN 3.3mm x 3.3mm Outline Tape and Reel

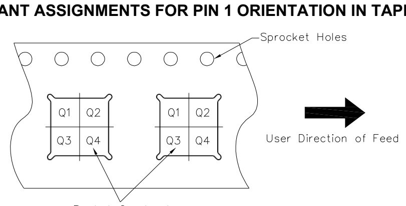
REEL DIMENSIONS



TAPE DIMENSIONS



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



CODE	DIMENSION (MM) MIN	DIMENSION (MM) MAX	DIMENSION (INCH) MIN	DIMENSION (INCH) MAX
Ao	3.50	3.70	.138	.146
Bo	3.50	3.70	.138	.146
Ko	1.10	1.30	.043	.051
P_1	7.90	8.10	.311	.319
W	11.80	12.20	.465	.480
W_1	12.30	12.50	.484	.492
Qty	4000			
Reel Diameter		13 Inches		

CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Consumer†† (per JEDEC JESD47F guidelines)	
Moisture Sensitivity Level	PQFN 3.3mm x 3.3mm	MSL1 (per JEDEC J-STD-020D†††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 0.21mH, R_G = 50Ω, I_{AS} = 20A.
③ Pulse width ≤ 400µs; duty cycle ≤ 2%.
④ R_θ is measured at T_J of approximately 90°C.
⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material. Please refer to AN-994 for more details: http://www.irf.com/technical-info/appnotes/an-994.pdf
⑥ Calculated continuous current based on maximum allowable junction temperature.
⑦ Current is limited to 25A by source bonding technology.
⑧ Pulse drain current is limited to 100A by source bonding technology.

Revision History

Date	Comments
6/5/2014	• Updated schematic on page 1 • Updated part marking on page 8 • Updated tape and reel on page 9
6/30/2014	• Remove “SAWN” package outline on page 8.
2/23/2016	• Updated datasheet with corporate template • Updated package outline to reflect the PCN # (241-PCN30-Public) for “Option C” and “Option G” on page 8.

Published by
Infineon Technologies AG
81726 München, Germany