

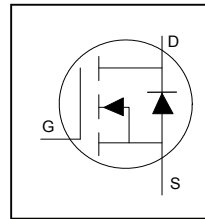
**Application**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

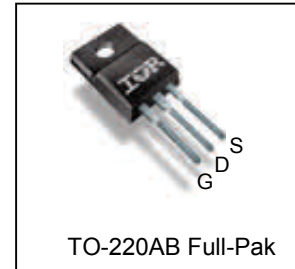
**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET

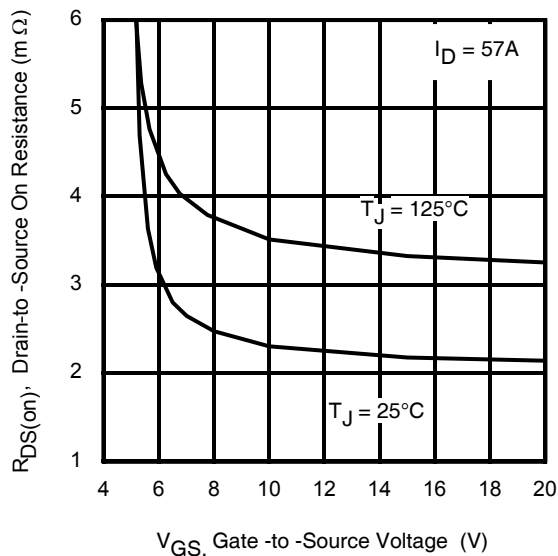


<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>2.0mΩ</b>
	<b>max</b>
<b>I<sub>D</sub></b>	<b>95A</b>

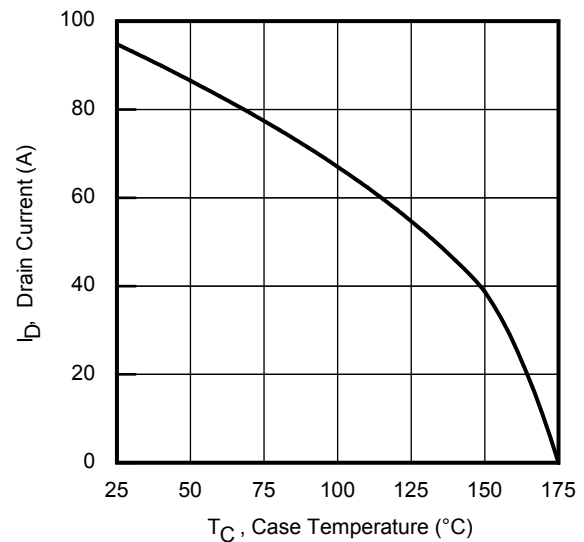


<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFI7440GPbF	TO-220 Full-Pak	Tube	50	IRFI7440GPbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	95	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	67	
$I_{DM}$	Pulsed Drain Current ①	380	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	42	W
	Linear Derating Factor	0.28	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	201	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	407	
$I_{AR}$	Avalanche Current ①	See Fig. 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	3.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	37	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 2\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.0	2.5	mΩ	$V_{GS} = 10\text{V}, I_D = 57\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.3	—	Ω	

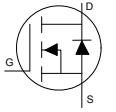
**Notes:**

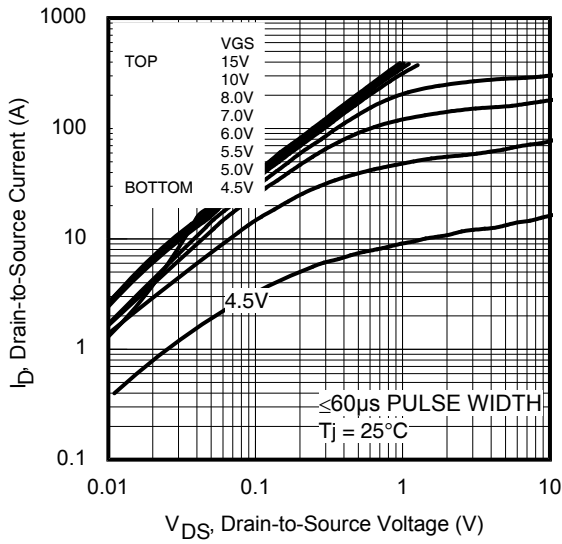
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 124\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 57\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 57\text{A}$ ,  $di/dt \leq 962\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 29\text{A}$ ,  $V_{GS} = 10\text{V}$ .

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

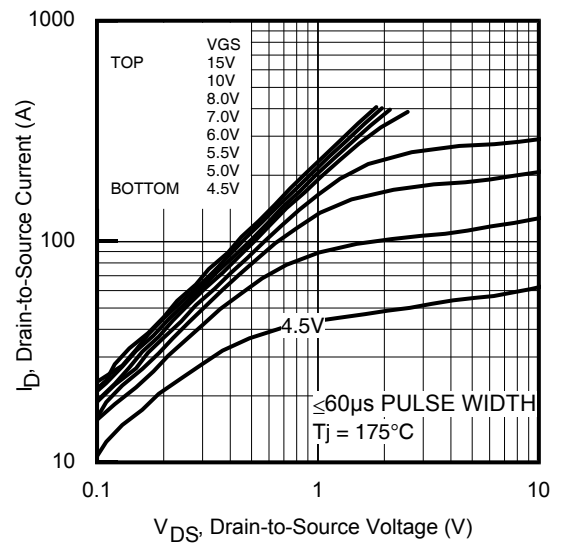
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	144	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 57A
Q <sub>g</sub>	Total Gate Charge	—	88	132	nC	I <sub>D</sub> = 57A V <sub>DS</sub> = 20V V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	22	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	30	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	58	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	11	—	ns	V <sub>DD</sub> = 20V I <sub>D</sub> = 30A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V④
t <sub>r</sub>	Rise Time	—	42	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	56	—		
t <sub>f</sub>	Fall Time	—	36	—		
C <sub>iss</sub>	Input Capacitance	—	4549	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig.7
C <sub>oss</sub>	Output Capacitance	—	689	—		
C <sub>riss</sub>	Reverse Transfer Capacitance	—	450	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	835	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	981	—		

**Diode Characteristics**

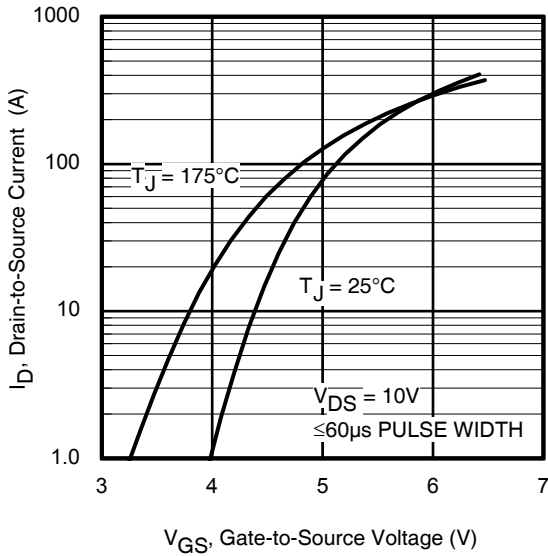
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)①	—	—	95	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	380		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 57A, V <sub>GS</sub> = 0V ④
dv/dt	Peak Diode Recovery dv/dt③	—	5.1	—	V/ns	T <sub>J</sub> = 175°C, I <sub>S</sub> = 57A, V <sub>DS</sub> = 40V④
t <sub>rr</sub>	Reverse Recovery Time	—	36 38	—	ns	T <sub>J</sub> = 25°C V <sub>DD</sub> = 34V T <sub>J</sub> = 125°C I <sub>F</sub> = 57A, di/dt = 100A/μs ④
Q <sub>rr</sub>	Reverse Recovery Charge	—	45 49	—		
I <sub>RRM</sub>	Reverse Recovery Current	—	2.1	—	A	T <sub>J</sub> = 25°C



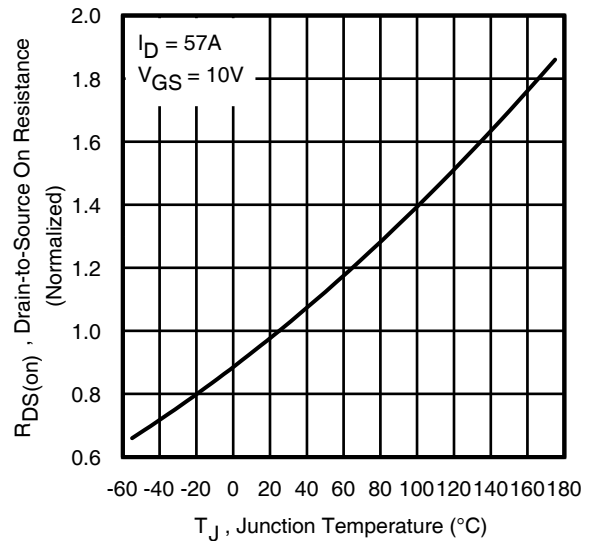
**Fig 3.** Typical Output Characteristics



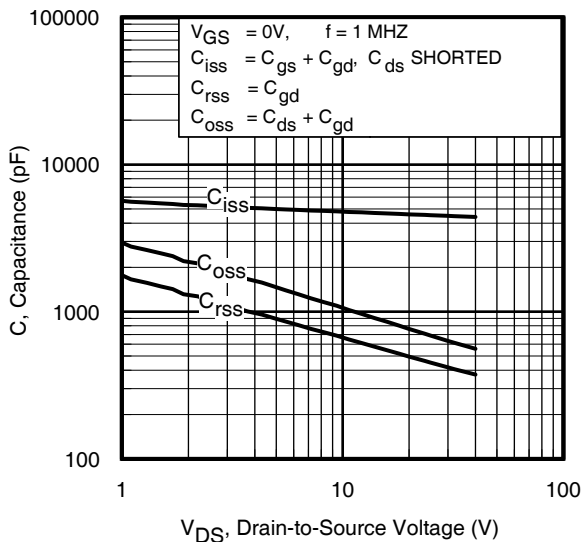
**Fig 4.** Typical Output Characteristics



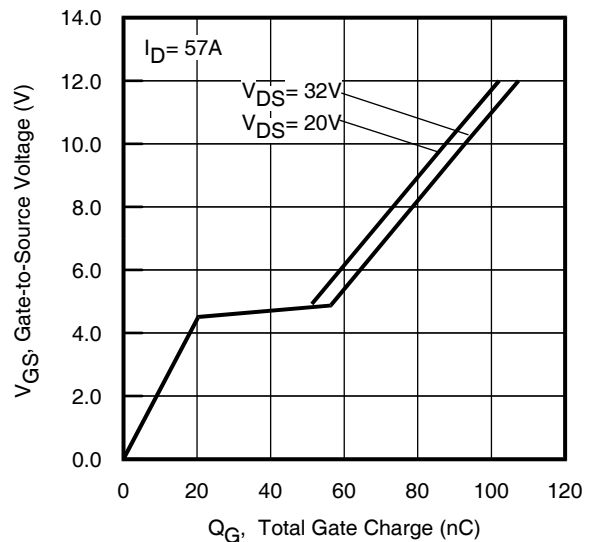
**Fig 5.** Typical Transfer Characteristics



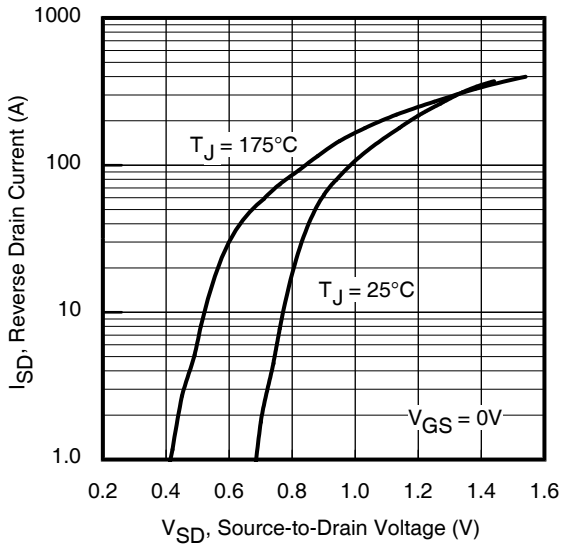
**Fig 6.** Normalized On-Resistance vs. Temperature



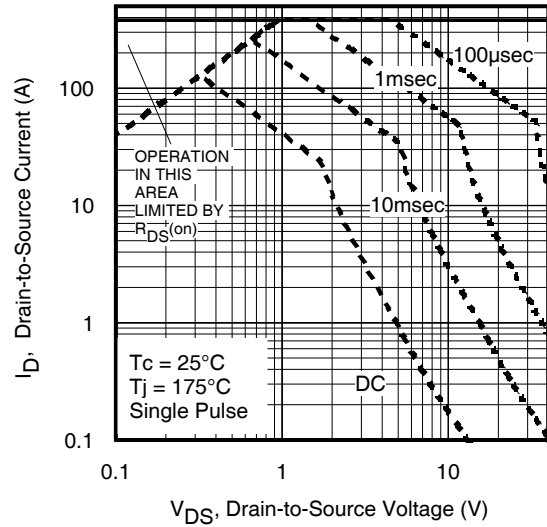
**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage



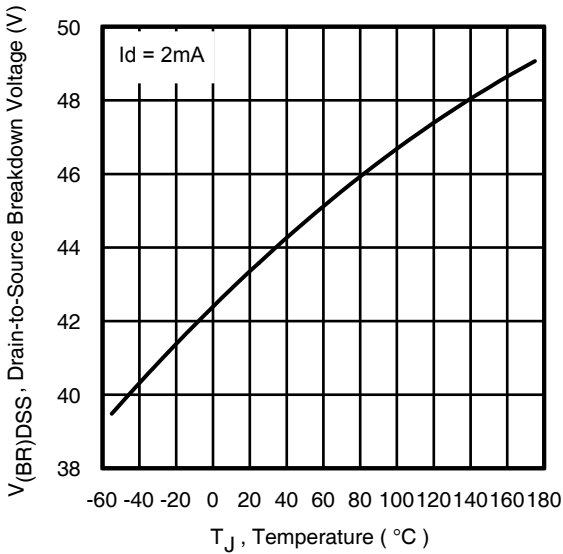
**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage



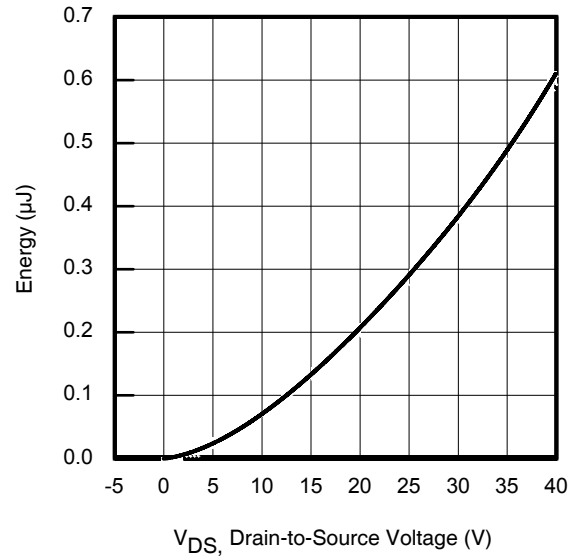
**Fig 9.** Typical Source-Drain Diode Forward Voltage



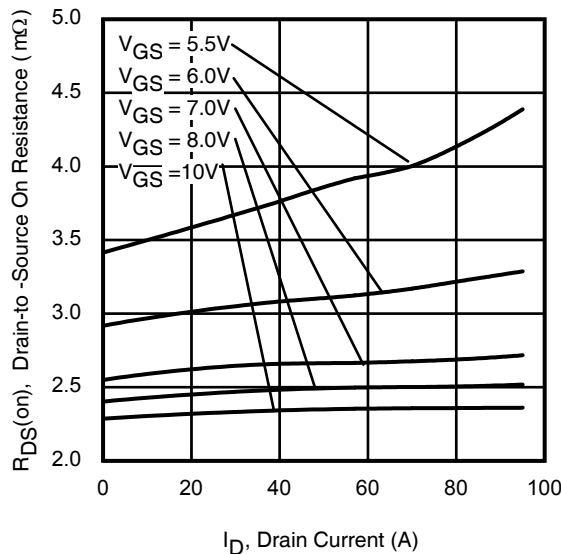
**Fig 10.** Maximum Safe Operating Area



**Fig 11.** Drain-to-Source Breakdown Voltage



**Fig 12.** Typical  $C_{oss}$  Stored Energy



**Fig 13.** Typical On-Resistance vs. Drain Current

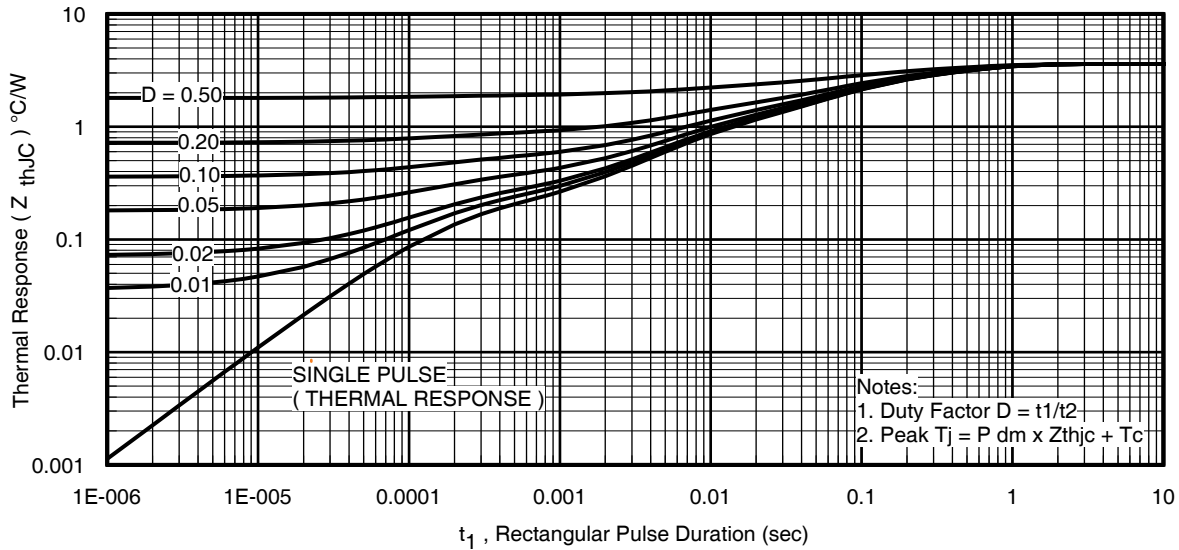


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

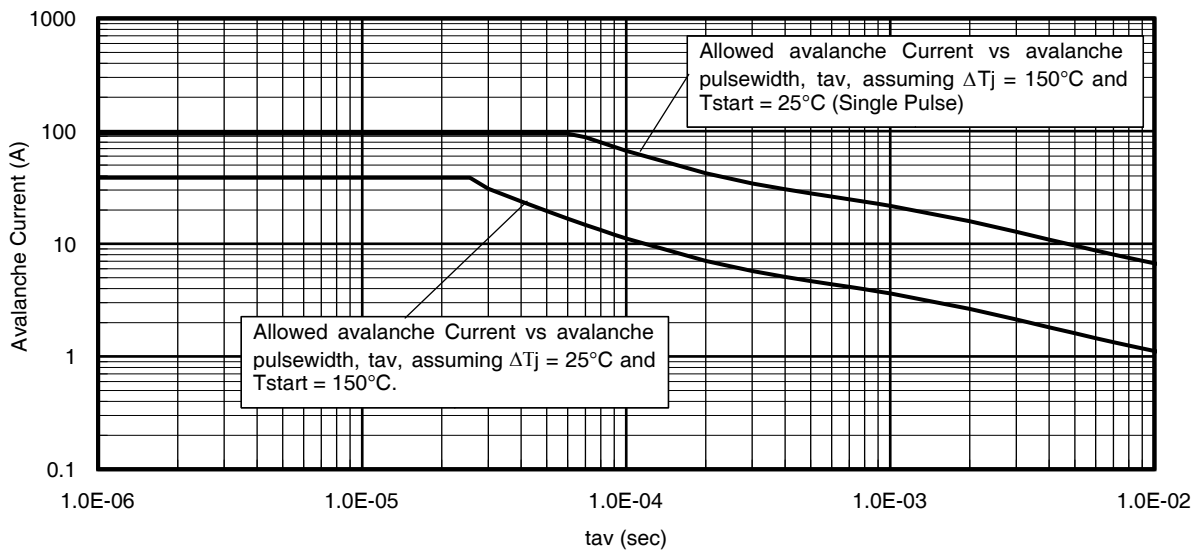


Fig 15. Avalanche Current vs. Pulse Width

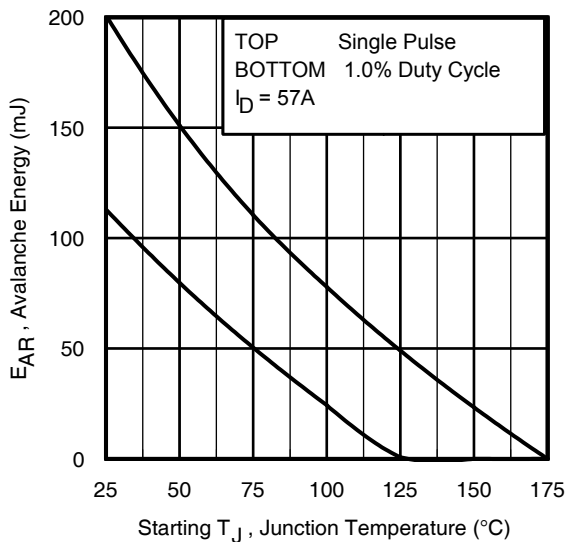
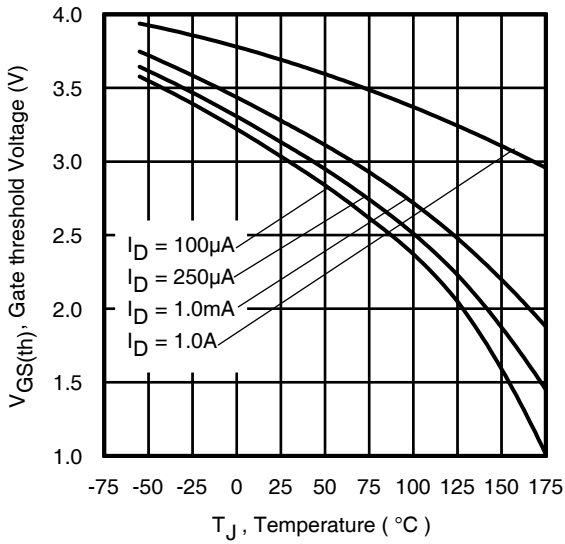


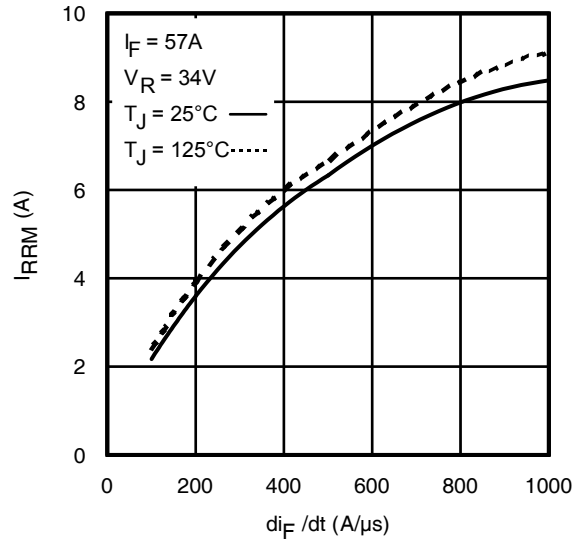
Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
**(For further info, see AN-1005 at www.irf.com)**

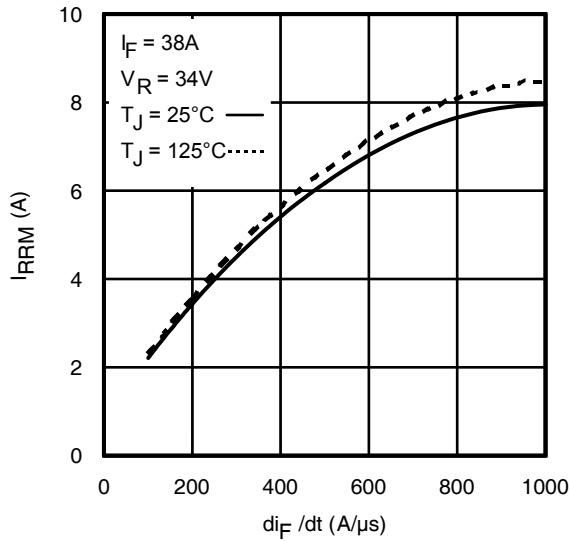
1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$



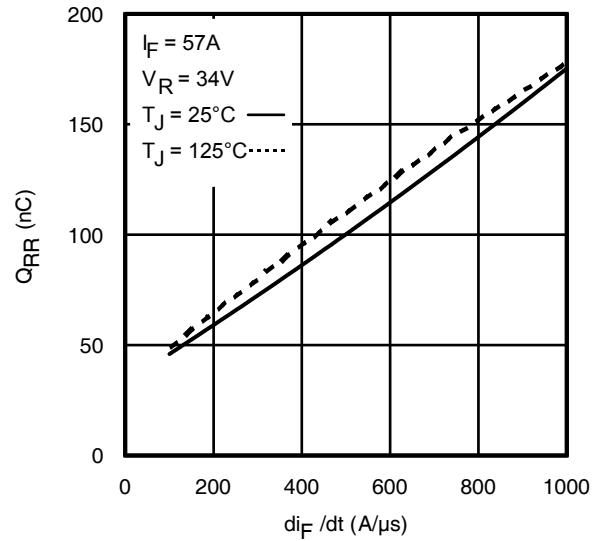
**Fig 17.** Threshold Voltage vs. Temperature



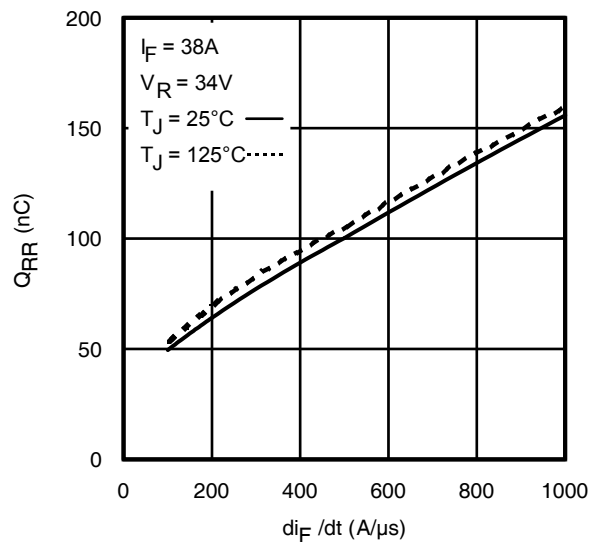
**Fig 18.** Typical Recovery Current vs.  $di_F/dt$



**Fig 19.** Typical Recovery Current vs.  $di_F/dt$



**Fig 20.** Typical Stored Charge vs.  $di_F/dt$



**Fig 21.** Typical Stored Charge vs.  $di_F/dt$

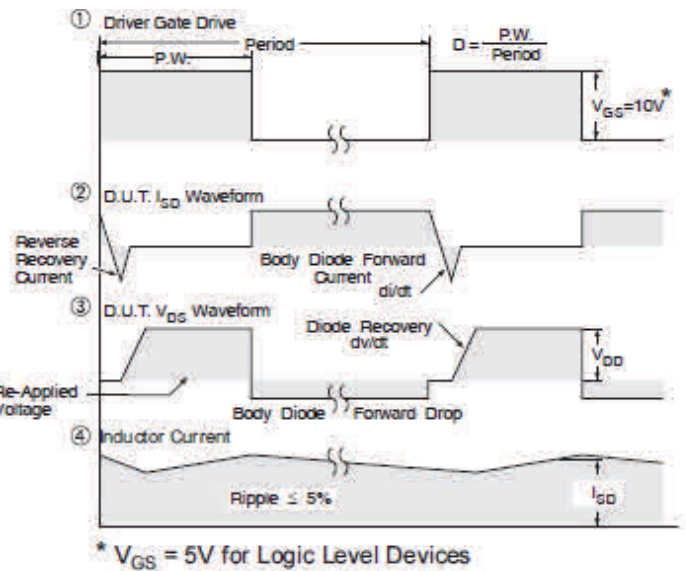
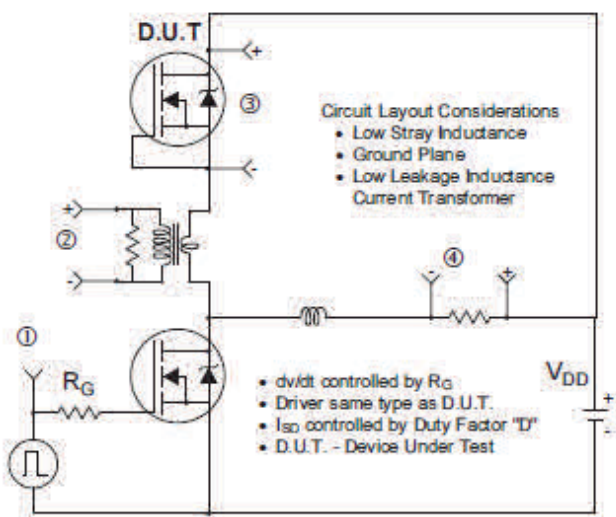


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

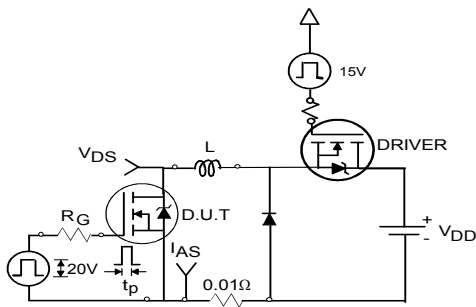


Fig 23a. Unclamped Inductive Test Circuit

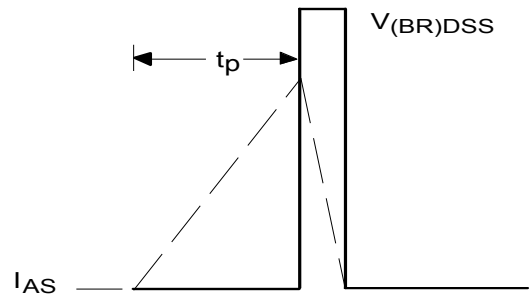


Fig 23b. Unclamped Inductive Waveforms



Fig 24a. Switching Time Test Circuit



Fig 24b. Switching Time Waveforms



Fig 25a. Gate Charge Test Circuit

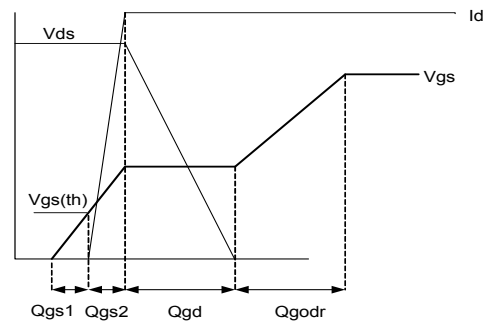
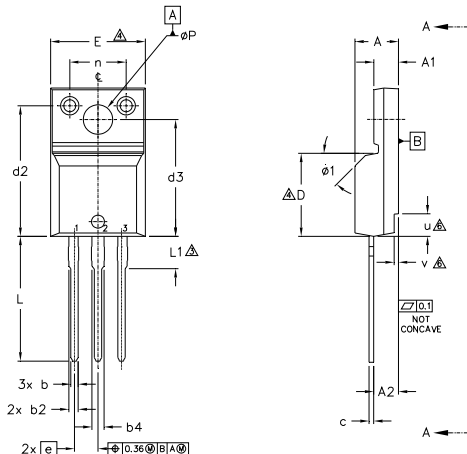


Fig 25b. Gate Charge Waveform

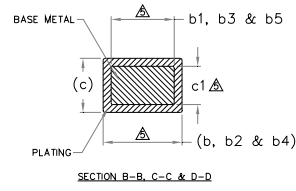
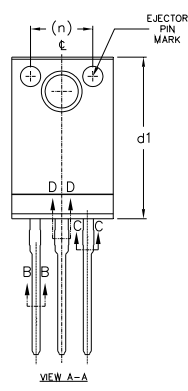
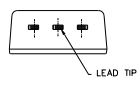


**TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))**


- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
  - 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
  - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
  - 7.0 CONTROLLING DIMENSION : INCHES.

- LEAD ASSIGNMENTS
- HEXFEEET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE

- IGBTs, CoPACK
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER

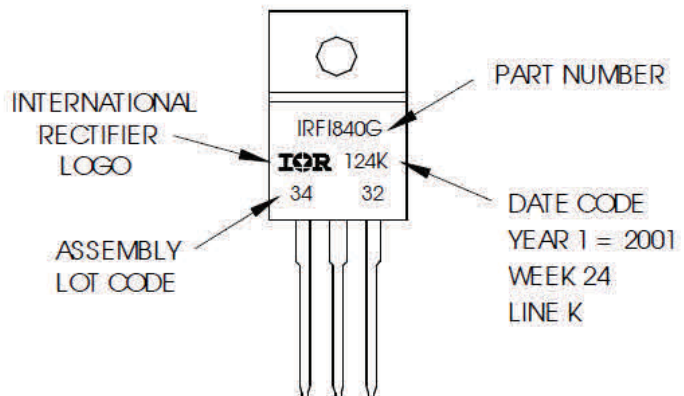


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	5
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	5
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	5
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	4
e	2.54 BSC		.100 BSC		
L	13.21	13.72	.520	.540	
L1	3.10	3.68	.122	.145	3
n	6.05	6.60	.238	.260	
phi P	3.05	3.45	.120	.136	
u	2.39	2.49	.094	.098	6
v	0.41	0.51	.016	.020	6
phi 1	-	45°	-	45°	

**TO-220 Full-Pak Part Marking Information**

EXAMPLE: THIS IS AN IRFI840G  
 WITH ASSEMBLY  
 LOT CODE 3432  
 ASSEMBLED ON WW24, 2001  
 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position  
 indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-220 Full-Pak	N/A
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

<b>Date</b>	<b>Comments</b>
11/18/2014	<ul style="list-style-type: none"> <li>Updated <math>E_{AS(L=1mH)} = 407mJ</math> on page 2</li> <li>Updated note 8 "Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 29A</math>, <math>V_{GS} = 10V</math>". on page 2</li> </ul>
12/16/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected typo test condition for Switch time ID from "57A" to "30A" on page 3.</li> </ul>

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