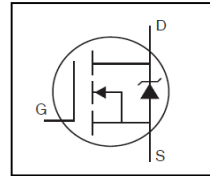


- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

HEXFET® Power MOSFET



V_{DSS}	55V
R_{DS(on)}	0.024Ω
I_D	31A



G	D	S
Gate	Drain	Source

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Full Pak eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heat sink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heat sink using a single clip or by a single screw fixing.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFIZ44NPbF	TO-220 Full-Pak	Tube	50	IRFIZ44NPbF

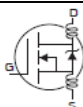
Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	31	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	22	
I _{DM}	Pulsed Drain Current ①⑥	160	
P _D @ T _C = 25°C	Maximum Power Dissipation	45	W
	Linear Derating Factor	0.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②⑥	210	mJ
I _{AR}	Avalanche Current ①⑥	25	A
E _{AR}	Repetitive Avalanche Energy ①	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt③⑥	5.0	V/ns
T _J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T _{STG}			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

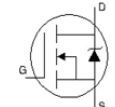
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	3.3	°C/W
R _{θJA}	Junction-to-Ambient	—	65	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

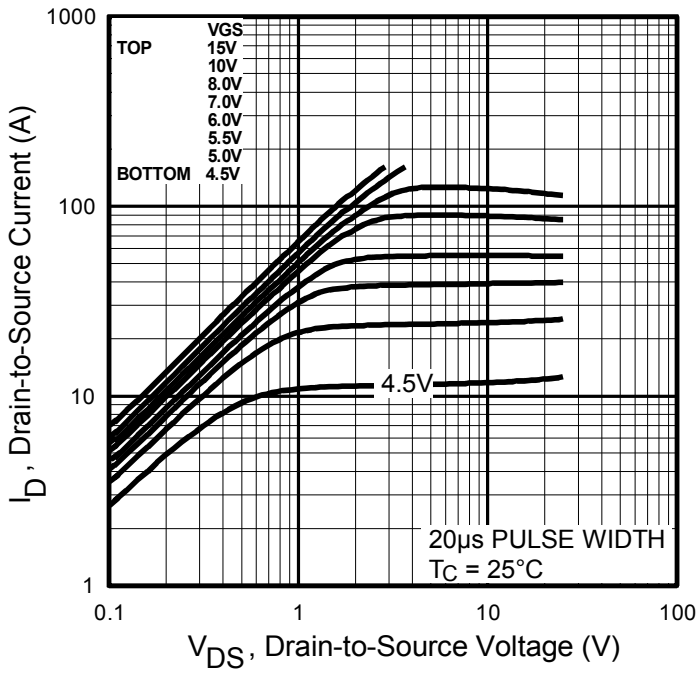
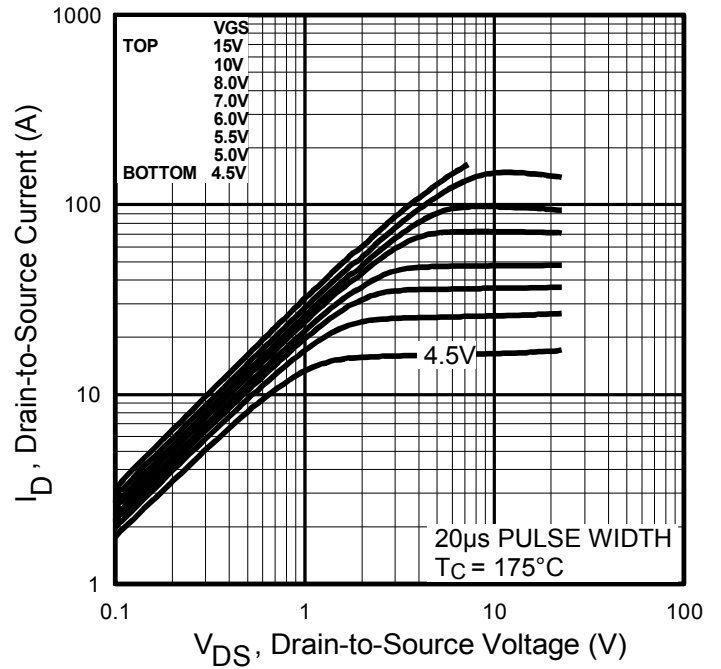
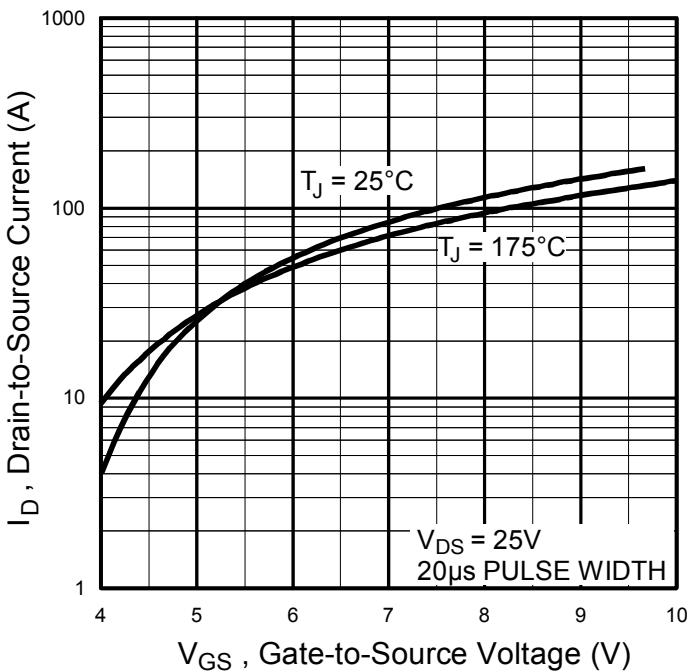
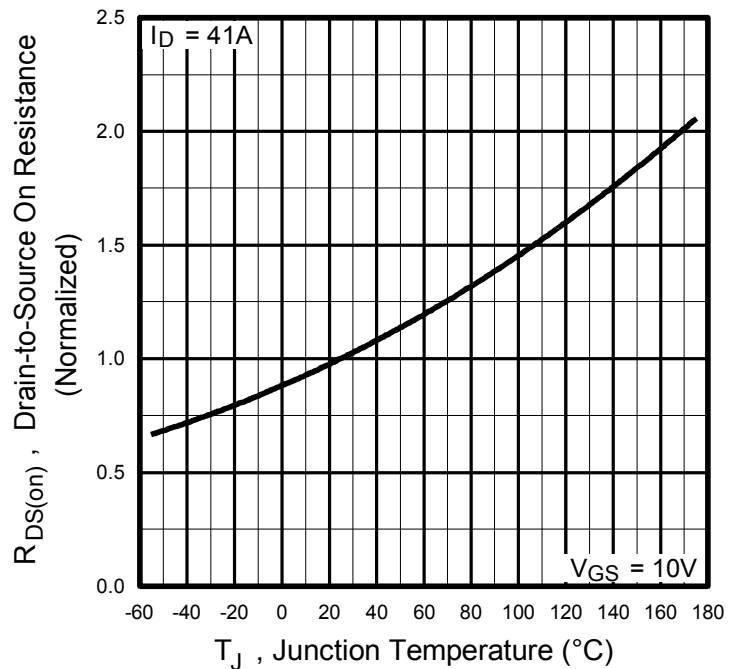
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.055	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.024	Ω	$V_{GS} = 10V, I_D = 17A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
g_{fs}	Forward Trans conductance	17	—	—	S	$V_{DS} = 25V, I_D = 25A$ ⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 55V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	65	nC	$I_D = 25A$
Q_{gs}	Gate-to-Source Charge	—	—	12		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain Charge	—	—	27		$V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑥
$t_{d(on)}$	Turn-On Delay Time	—	7.3	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	69	—		$I_D = 25A$
$t_{d(off)}$	Turn-Off Delay Time	—	47	—		$R_G = 12\Omega$
t_f	Fall Time	—	60	—		$R_D = 1.1\Omega$, See Fig. 10 ④ ⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	410	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	150	—		$f = 1.0\text{MHz}$, See Fig. 5 ⑥
C	Drain to Sink Capacitance	—	12	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	31	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	65	98	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
Q_{rr}	Reverse Recovery Charge	—	160	240	μC	$di/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② starting $T_J = 25^\circ\text{C}$, $L = 470\mu\text{H}$, $R_G = 25\Omega$, $I_{AS} = 25A$ (See fig. 12)
- ③ $I_{SD} \leq 25A$, $di/dt \leq 320\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ $t = 60\text{s}$, $f = 60\text{Hz}$
- ⑥ Uses IRFZ44N data and test conditions.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

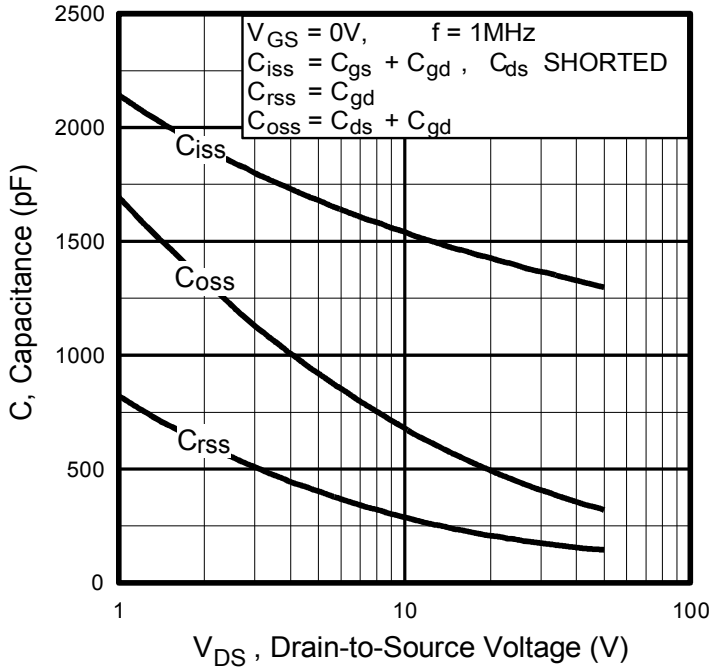


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

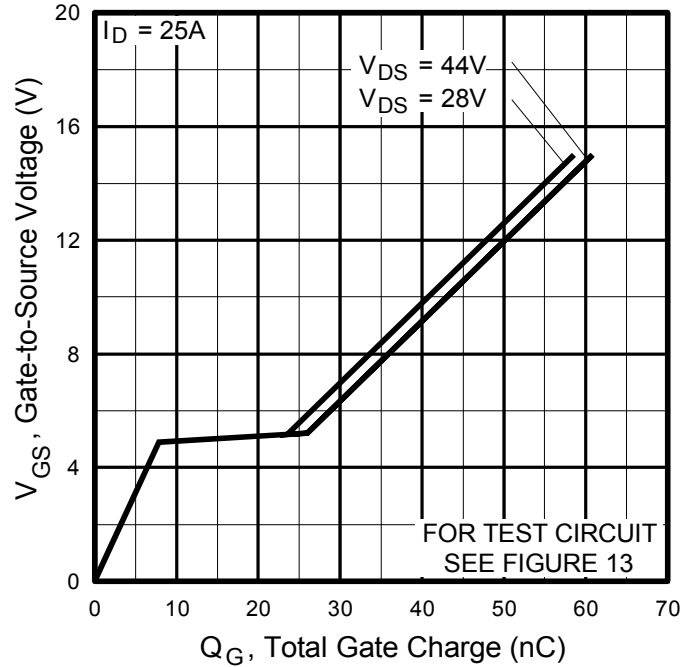


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

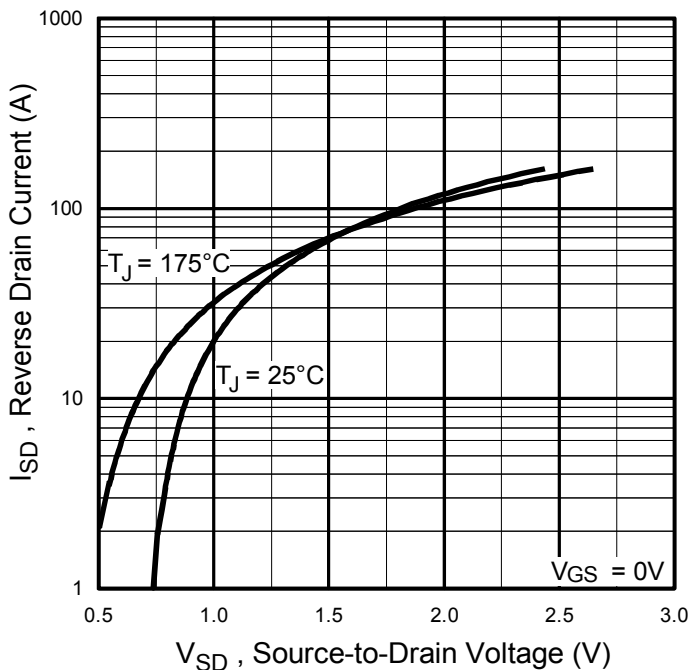


Fig 7. Typical Source-to-Drain Diode Forward Voltage

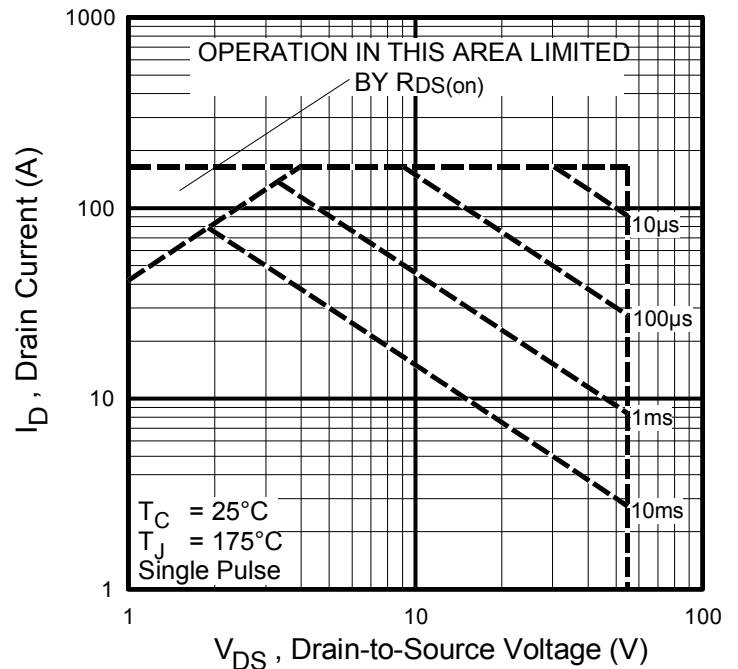


Fig 8. Maximum Safe Operating Area

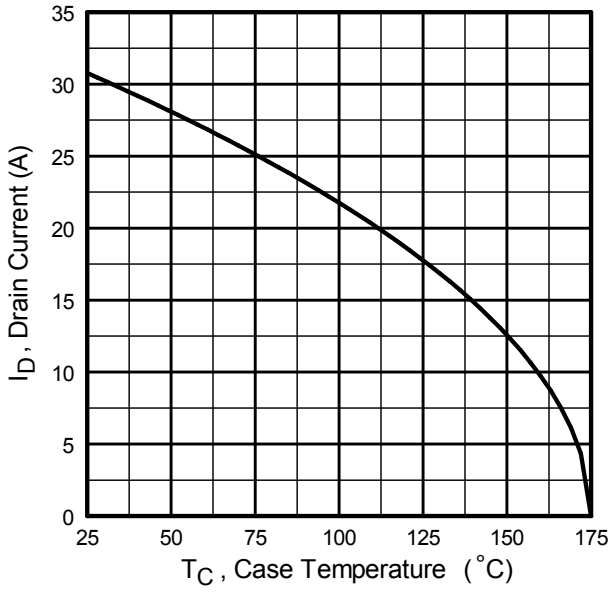
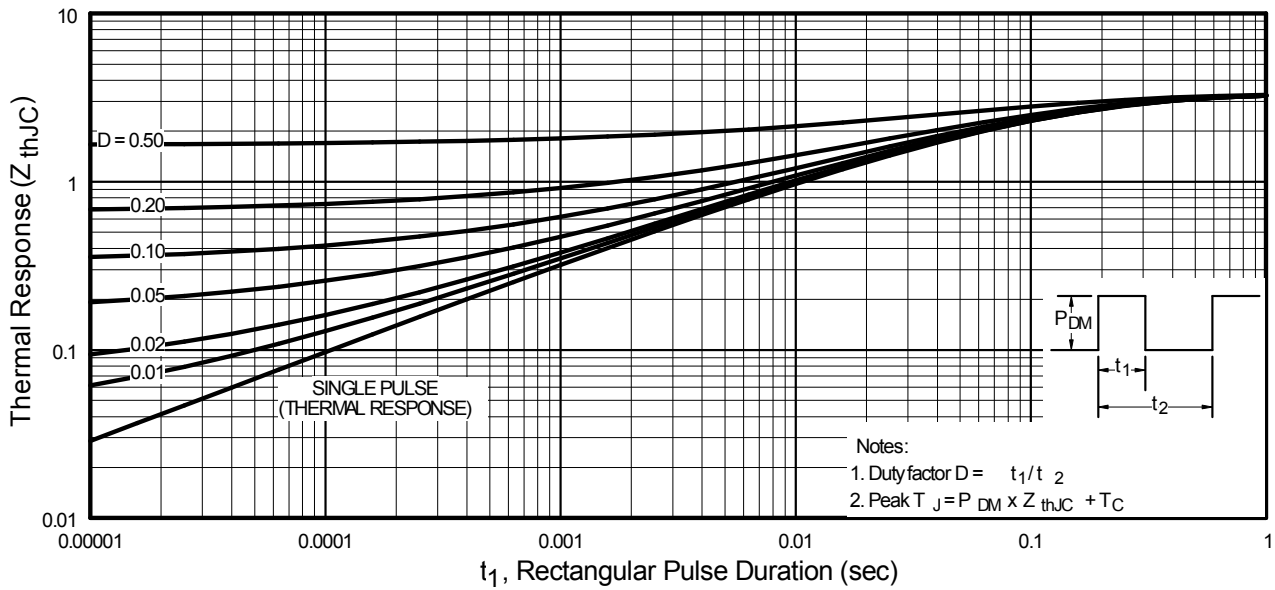

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

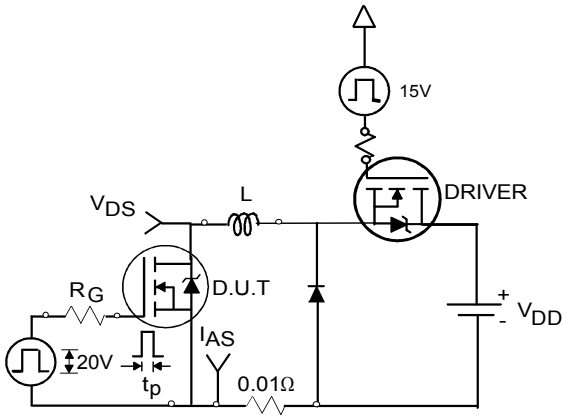
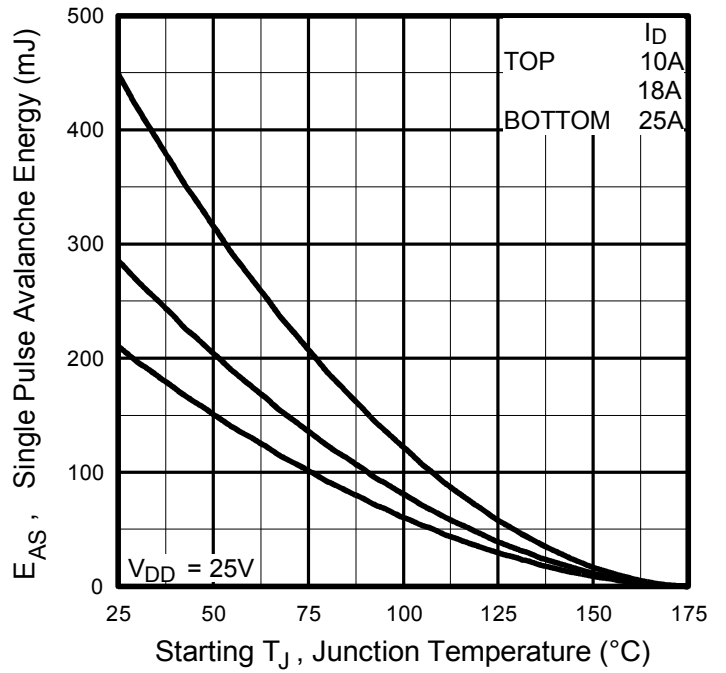
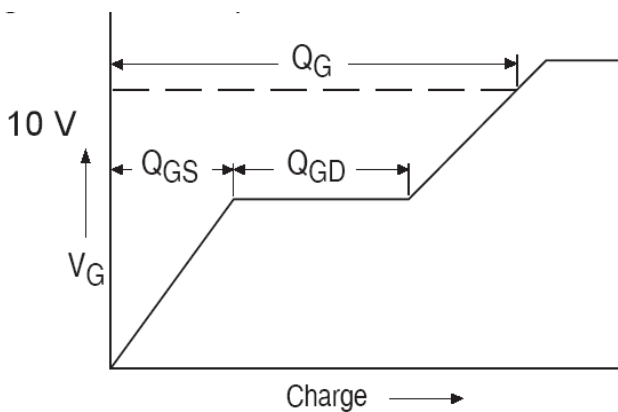
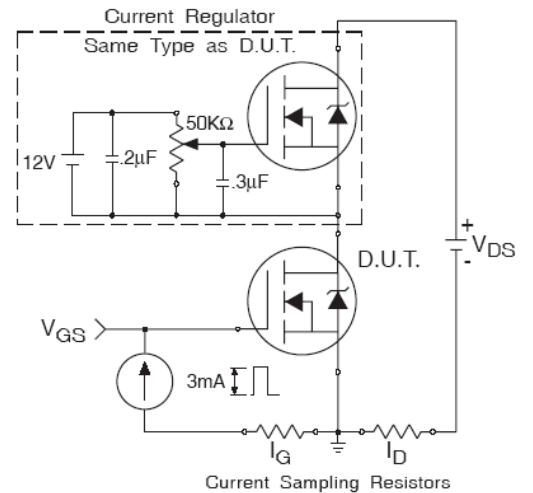
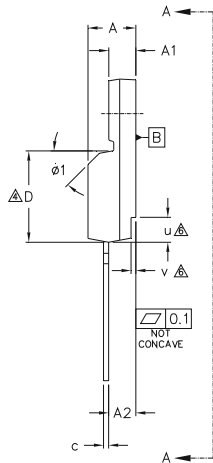
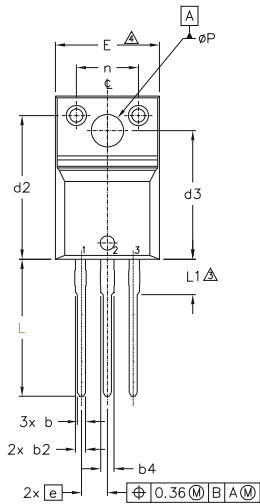

Fig 12a. Unclamped Inductive Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

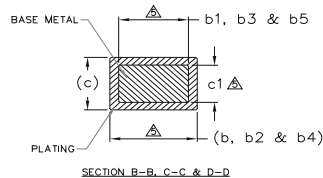
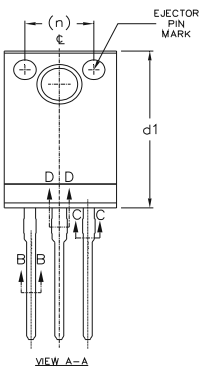
SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	.180	.190	LEAD ASSIGNMENTS HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE	
A1	2.57	2.82	.101	.111		
A2	2.51	2.92	.099	.115		
b	0.61	0.94	.024	.037		
b1	0.61	0.89	.024	.035		5
b2	0.76	1.27	.030	.050		5
b3	0.76	1.22	.030	.048		
b4	1.02	1.52	.040	.060		
b5	1.02	1.47	.040	.058		5
c	0.33	0.63	.013	.025		5
c1	0.33	0.58	.013	.023		
D	8.66	9.80	.341	.386	4	
d1	15.80	16.13	.622	.635	4	
d2	13.97	14.22	.550	.560		
d3	12.29	12.93	.484	.509		
E	9.63	10.74	.379	.423		
e	2.54	BSC	.100	BSC	4	
L	13.21	13.72	.520	.540		
L1	3.10	3.68	.122	.145	3	
n	6.05	6.60	.238	.260		
phiP	3.05	3.45	.120	.136	6	
u	2.39	2.49	.094	.098		
v	0.41	0.51	.016	.020	6	
phi1	-	45°	-	45°		

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

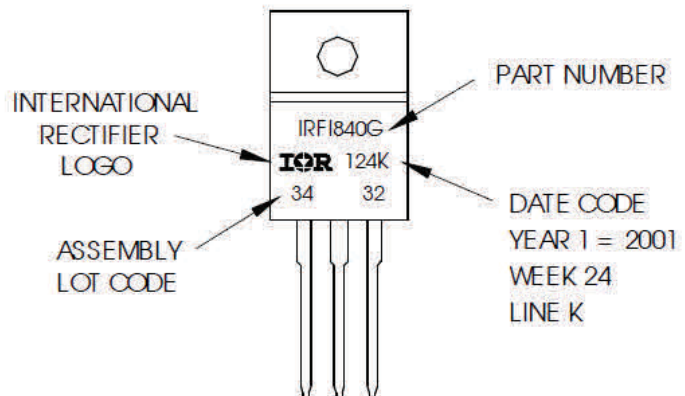
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER


TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW24, 2001
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
04/27/2017	<ul style="list-style-type: none"> Changed datasheet with Infineon logo - all pages. Corrected Package Outline on page 8. Added disclaimer on last page.

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