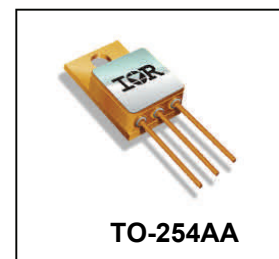


POWER MOSFET
THRU-HOLE (TO-254AA)
500V, N-CHANNEL
REF: MIL-PRF-19500/596
HEXFET MOSFET TECHNOLOGY
Product Summary

Part Number	$R_{DS(on)}$	I_D
IRFM440	0.85Ω	8.0A


Description

HEXFET MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high trans conductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heat sink. This improves thermal efficiency and reduces drain capacitance.

Features

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light Weight
- ESD Rating: Class 2 per MIL-STD-750, Method 1020

Absolute Maximum Ratings

	Parameter		Units
$I_D @ V_{GS} = 10V, T_C = 25^\circ C$	Continuous Drain Current	8.0	A
$I_D @ V_{GS} = 10V, T_C = 100^\circ C$	Continuous Drain Current	5.0	
I_{DM}	Pulsed Drain Current ①	32	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	700	mJ
I_{AR}	Avalanche Current ①	8.0	A
E_{AR}	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

For Footnotes refer to the page 2.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.78	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.85	Ω	$V_{GS} = 10V, I_D = 5.0A$ ④
		—	—	0.95		$V_{GS} = 10V, I_D = 8.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
G_{fs}	Forward Transconductance	4.7	—	—	S	$V_{DS} = 15V, I_D = 5.0A$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	68.5	nC	$I_D = 8.0A$
Q_{GS}	Gate-to-Source Charge	—	—	12.5		$V_{DS} = 250V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	42.4		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	—	21	ns	$V_{DD} = 250V$
t_r	Rise Time	—	—	73		$I_D = 8.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	—	72		$R_G = 9.1\Omega$
t_f	Fall Time	—	—	51		$V_{GS} = 10V$
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	310	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	120	—		$f = 1.0MHz$

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 8.0A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	—	700	ns	$T_J = 25^\circ\text{C}, I_F = 8.0A, V_{DD} \leq 50V$
Q_{rr}	Reverse Recovery Charge	—	—	8.9	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case -to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ\text{C}$, $L = 21.8mH$, Peak $I_L = 8.0A$, $V_{GS} = 10V$
- ③ $I_{SD} \leq 8.0A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq 500V$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$.

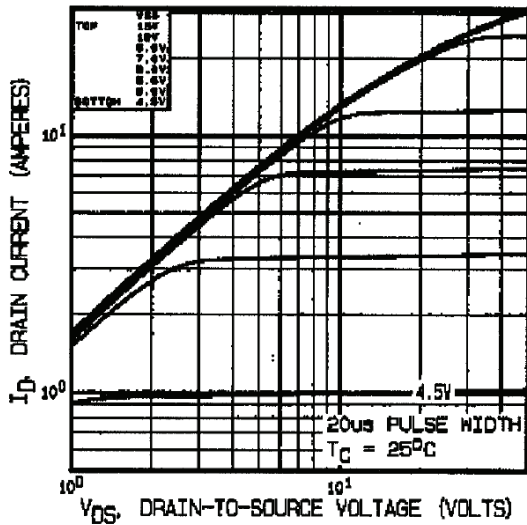


Fig 1. Typical Output Characteristics

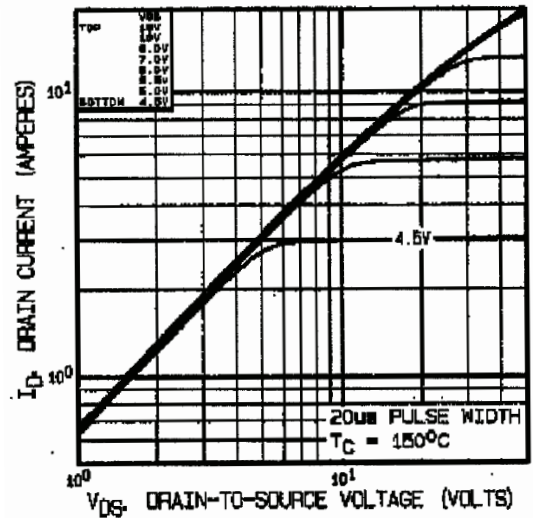


Fig 2. Typical Output Characteristics

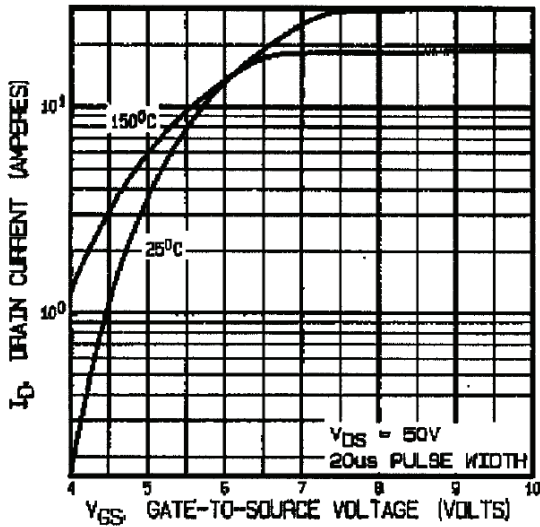


Fig 3. Typical Transfer Characteristics

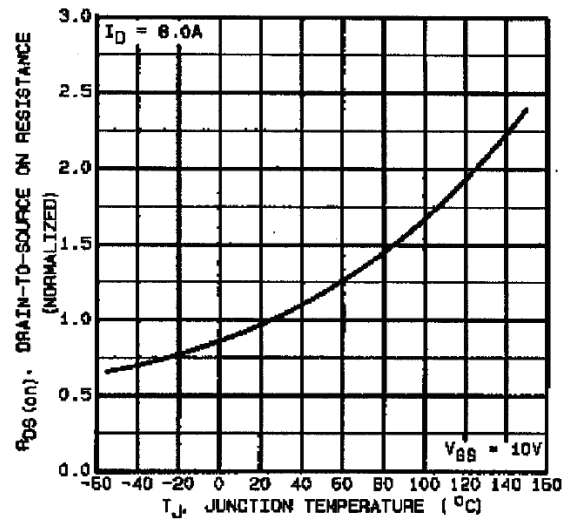


Fig 4. Normalized On-Resistance Vs. Temperature

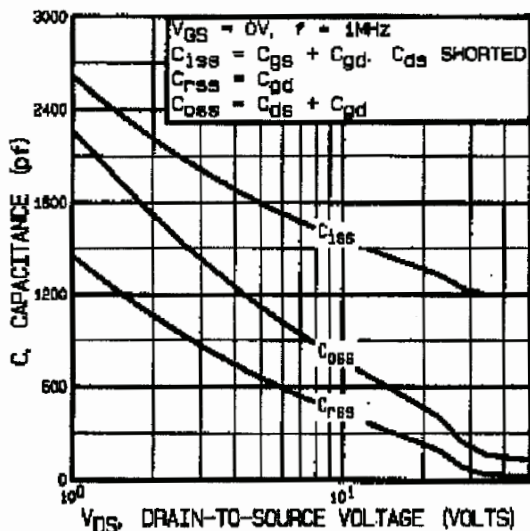


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

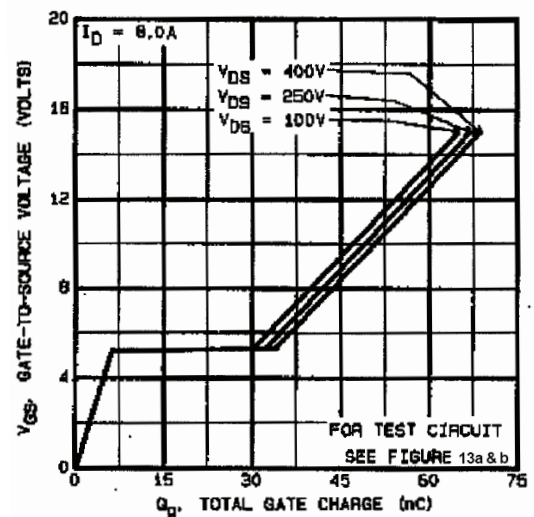


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

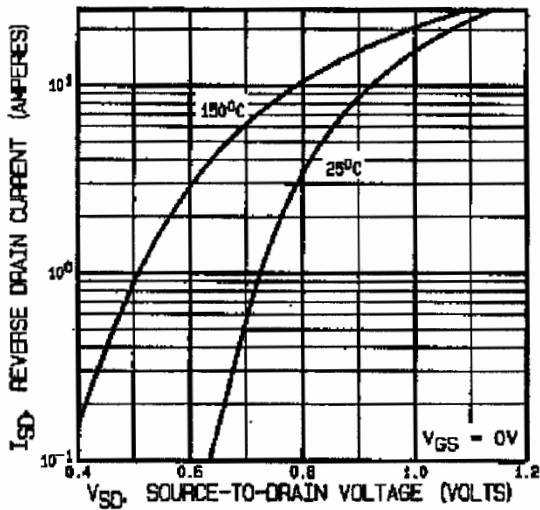


Fig 7. Typical Source-Drain Diode Forward Voltage

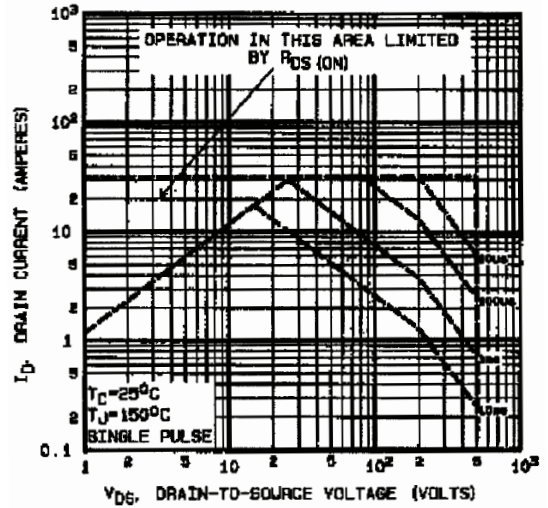


Fig 8. Maximum Safe Operating Area

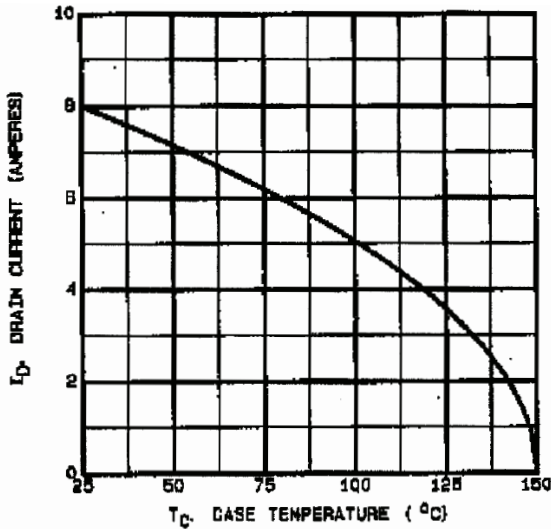


Fig 9. Maximum Drain Current Vs. Case Temperature

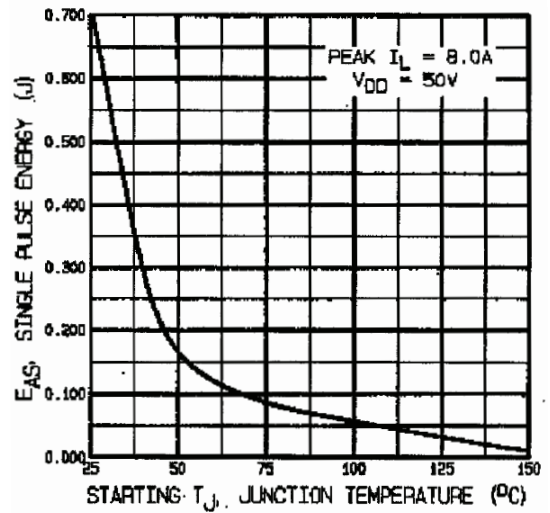


Fig 10. Maximum Avalanche Energy Vs. Drain Current

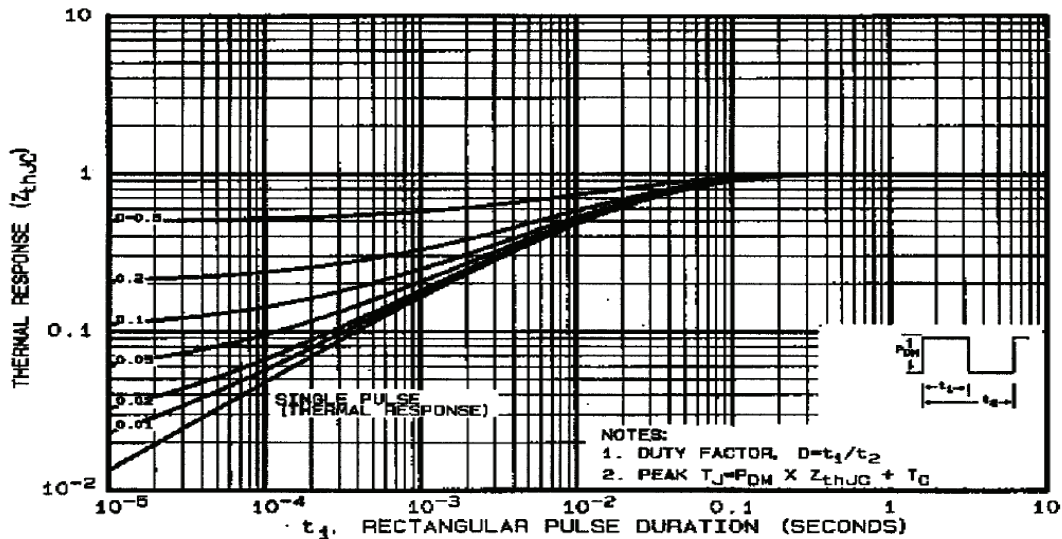


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

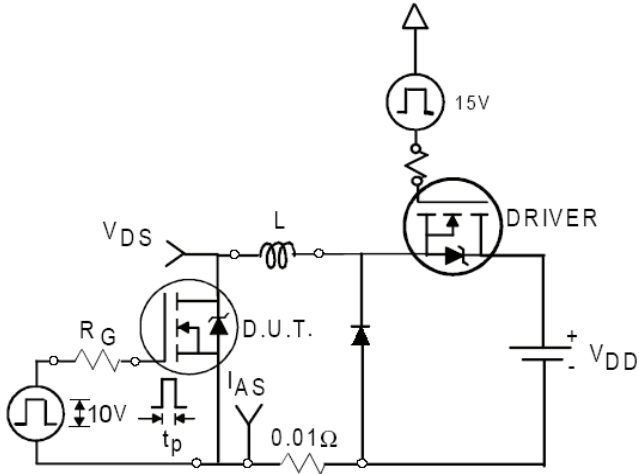


Fig 12a. Unclamped Inductive Test Circuit

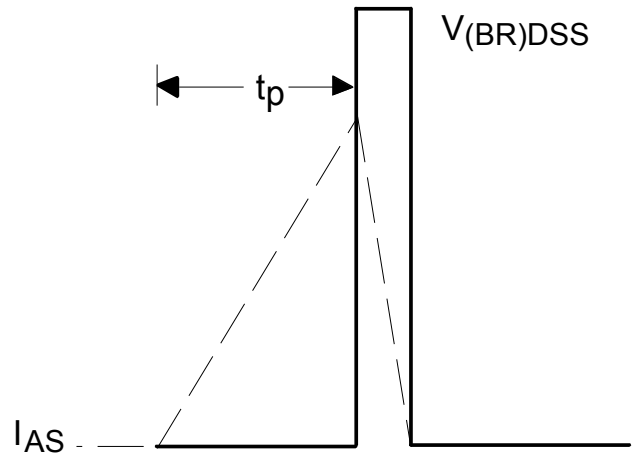


Fig 12b. Unclamped Inductive Waveforms

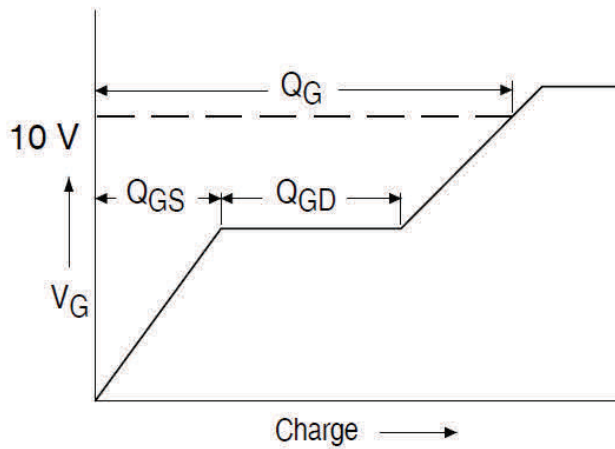


Fig 13a. Basic Gate Charge Waveform

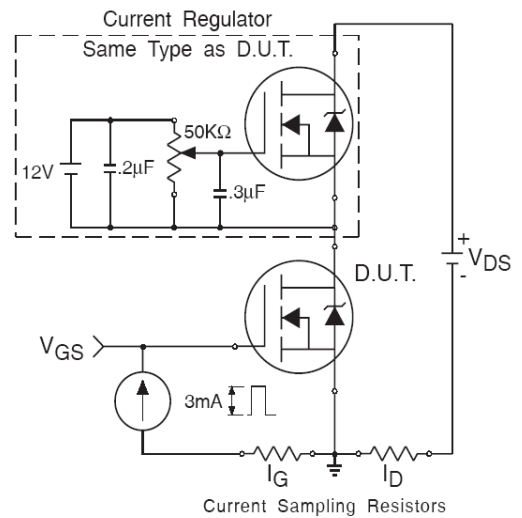


Fig 13b. Gate Charge Test Circuit

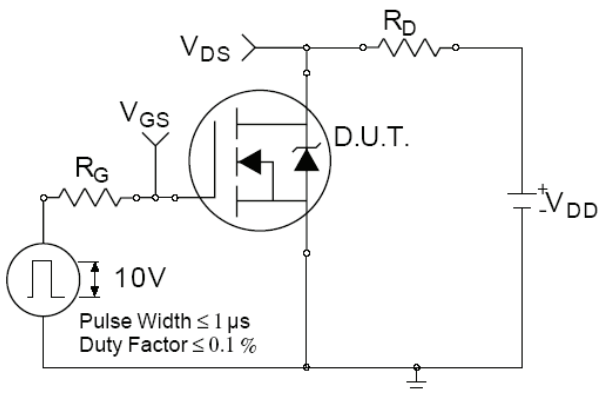


Fig 14a. Switching Time Test Circuit

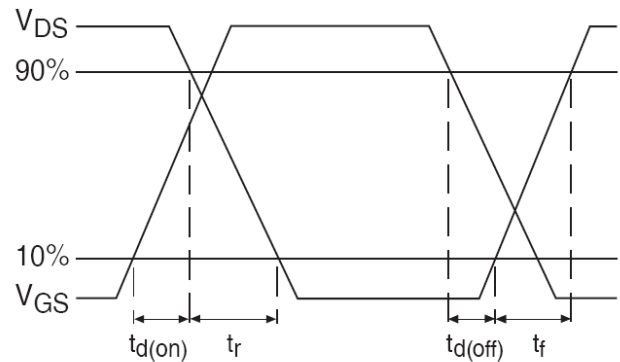
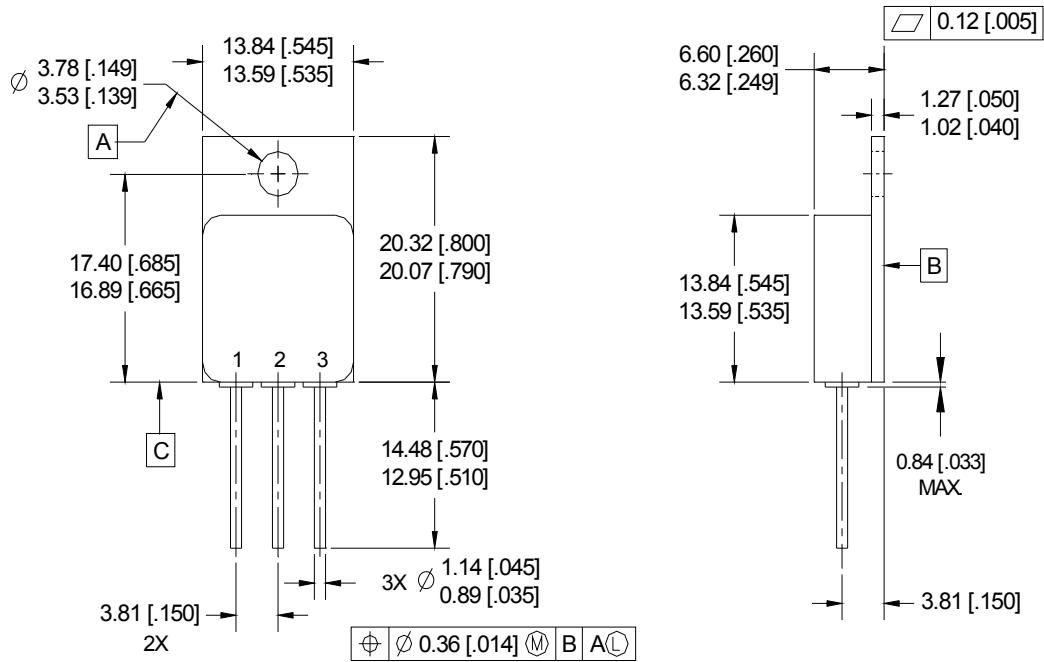


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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