# International Rectifier

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

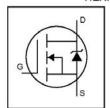
### Description

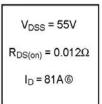
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

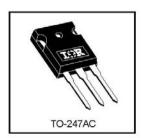
The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting

# IRFP054NPbF

HEXFET<sup>®</sup> Power MOSFET







### Absolute Maximum Ratings

	Parameter	Max.	Units	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	816		
@ T <sub>C</sub> = 100°C Continuous Drain Current, V <sub>GS</sub> @ 10V		57	Α	
I <sub>DM</sub>	Pulsed Drain Current ①⑤	290		
P <sub>D</sub> @T <sub>C</sub> = 25°C	Power Dissipation	170	W	
	Linear Derating Factor	1.1	W/°C	
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V	
EAS	Single Pulse Avalanche Energy 25	360	mJ	
l <sub>AR</sub>	Avalanche Current®	43	Α	
EAR	Repetitive Avalanche Energy®	17	mJ	
d∨/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns	
TJ	Operating Junction and	-55 to + 175		
T <sub>STG</sub>	Storage Temperature Range		℃	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )		
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)		

### Thermal Resistance

	Parameter	Тур.	Max.	Units
Reuc	Junction-to-Case	-	0.90	
R <sub>BCS</sub>	Case-to-Sink, Flat, Greased Surface	0.24		°CM
Reus	Junction-to-Ambient		40	

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### Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55			٧	$V_{GS} = 0V, I_{D} = 250 \mu A$
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient		0.06		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>⑤</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance			0.012	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 43A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
<b>g</b> fs	Forward Transconductance	30			S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 43A⑤
lacare	Drain-to-Source Leakage Current		60 0000	25	μA	$V_{DS}$ = 55V, $V_{GS}$ = 0V
DSS	Diamitio-Gaute Leakage Current	(1-1-1-1)	6	250	μΑ	$V_{DS} = 44V, V_{GS} = 0V, T_{J} = 150$ °C
l acore accor	Gate-to-Source Forward Leakage	-		100	n.A	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Reverse Leakage		621 - 21	-100	пА	V <sub>GS</sub> = -20V
Qg	Total Gate Charge	s <del>-2-</del> 3		130		I <sub>D</sub> = 43A
Q <sub>gs</sub>	Gate-to-Source Charge			23	nC	$V_{DS} = 44V$
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge		<u> </u>	53		V <sub>GS</sub> = 10V, See Fig. 6 and 13 <b>9 9</b>
t <sub>d(on)</sub>	Turn-On Delay Time		11			V <sub>DD</sub> = 28V
tr	Rise Time		66			I <sub>D</sub> = 43A
t <sub>d(off)</sub>	Turn-Off Delay Time		40		ns	$R_G = 3.6\Omega$
t <sub>f</sub>	FallTime		46			R <sub>D</sub> = 0.62Ω, See Fig. 10എ⑤
L <sub>D</sub>	Internal Drain Inductance	3 <del>-3-</del> 8	5.0		(1)	Between lead, 6mm (0.25in.)
L <sub>S</sub>	Internal Source Inductance	_	13		nΗ	from package and center of die contact
Ciss	Input Capacitance	7	2900			V <sub>GS</sub> = 0V
Coss	Output Capacitance		880		pF	V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance		330			f = 1.0MHz, See Fig. 5⑤

### Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
ls	Continuous Source Current (Body Diode)	1275 - 17		81®	Α	MOSFET symbol showing the
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①		_	290		integral reverse p-n junction diode.
V <sub>SD</sub>	Diode Forward Voltage		-	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 43A, V <sub>GS</sub> = 0V ④
trr	Reverse Recovery Time		81	120	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 43A
Q <sub>rr</sub>	Reverse RecoveryCharge		240	370	nC	di/dt = 100A/µs ④⑤

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{DD}$  = 25V, starting  $T_J$  = 25°C, L = 390 $\mu$ H  $R_G$  = 25 $\Omega$ ,  $I_{AS}$  = 43A. (See Figure 12)
- $\label{eq:loss_def} \begin{tabular}{ll} \begin{tabular}{ll} $I_{SD} \le 43A$, $di/dt \le 260A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, \\ $T_{,l} \le 175^{\circ}C$ \end{tabular}$
- 4 Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$ .
- © Uses IRF1010N data and test conditions
- © Caculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

# International TOR Rectifier

## IRFP054NPbF

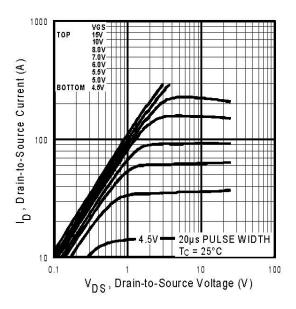


Fig 1. Typical Output Characteristics

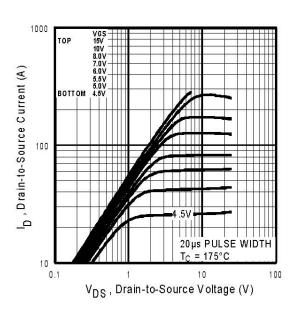


Fig 2. Typical Output Characteristics

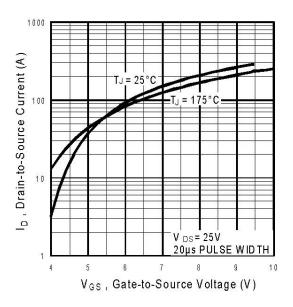


Fig 3. Typical Transfer Characteristics

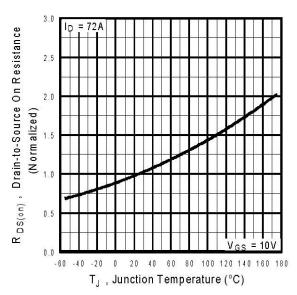
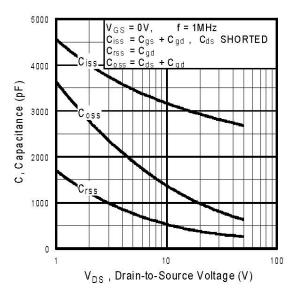


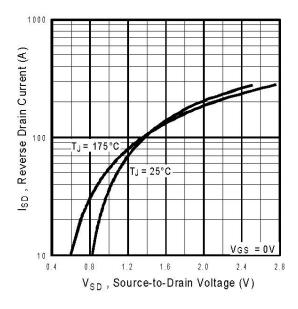
Fig 4. Normalized On-Resistance Vs. Temperature



20 D = 43A V<sub>DS</sub> = 44V V<sub>GS</sub>, Gate-to-Source Voltage (V) V<sub>DS</sub> = 28V 12 OR TEST CIRCUIT SEE FIGURE 13 0 20 40 60 80 100 0 Q<sub>G</sub>, Total Gate Charge (nC)

**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



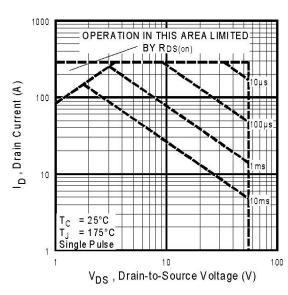
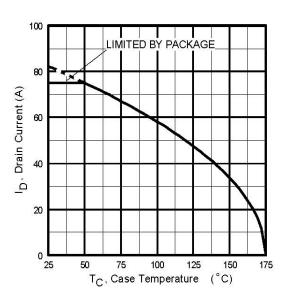


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

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**Fig 9.** Maximum Drain Current Vs. Case Temperature

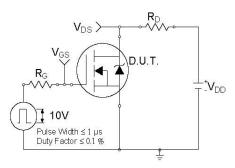


Fig 10a. Switching Time Test Circuit

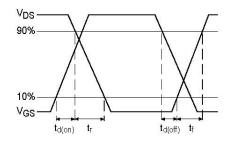
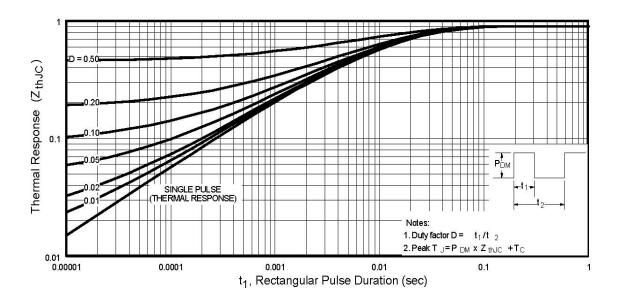


Fig 10b. Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case www.irf.com

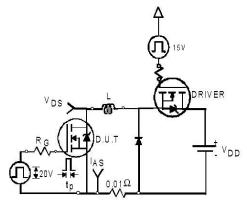


Fig 12a. Unclamped Inductive Test Circuit

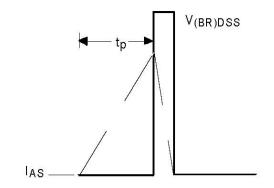


Fig 12b. Unclamped Inductive Waveforms

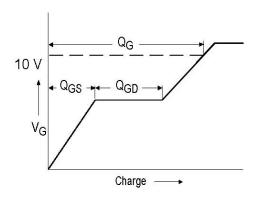
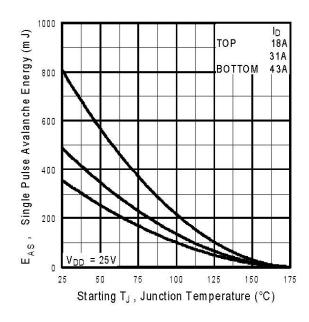


Fig 13a. Basic Gate Charge Waveform

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**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

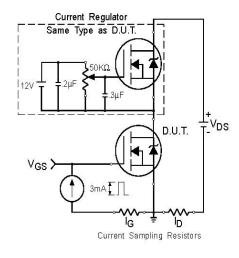
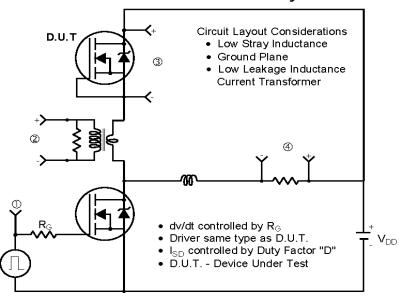


Fig 13b. Gate Charge Test Circuit

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### Peak Diode Recovery dv/dt Test Circuit



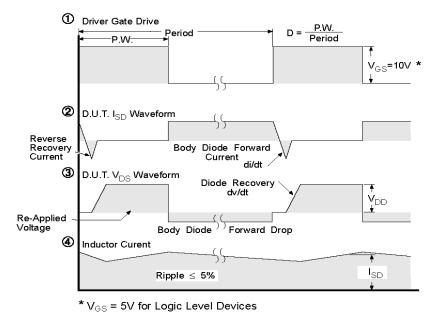


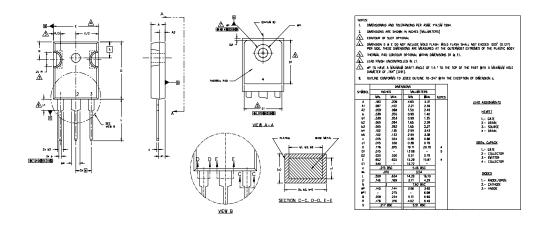
Fig 14. For N-Channel HEXFETS

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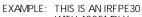
International IOR Rectifier

### TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



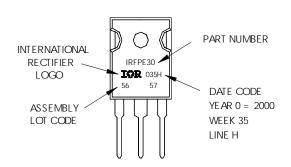
### TO-247AC Part Marking Information



WITH ASSEMBLY LOT CODE 5657

ASSEMBLED ON WW 35, 2000 IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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Note: For the most current drawings please refer to the IR website at: <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>

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