

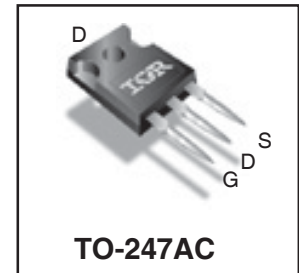
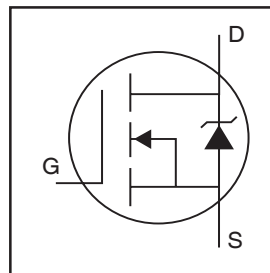
**PDP SWITCH**

**IRFP4227PbF**

**Features**

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $E_{PULSE}$  Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $Q_G$  for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
$V_{DS}$ max	200	V
$V_{DS}$ (Avalanche) typ.	240	V
$R_{DS(ON)}$ typ. @ 10V	21	mΩ
$I_{RP}$ max @ $T_C = 100^\circ\text{C}$	130	A
$T_J$ max	175	°C



G	D	S
Gate	Drain	Source

**Description**

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low  $E_{PULSE}$  rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	±30	V
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	65	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	46	
$I_{DM}$	Pulsed Drain Current ①	260	
$I_{RP}$ @ $T_C = 100^\circ\text{C}$	Repetitive Peak Current ⑤	130	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	W
$P_D$ @ $T_C = 100^\circ\text{C}$	Power Dissipation	190	
	Linear Derating Factor	2.2	W/°C
$T_J$	Operating Junction and	-40 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

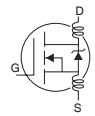
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ④	—	62	

Notes ① through ⑥ are on page 8

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	170	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	21	25	m $\Omega$	$V_{GS} = 10V, I_D = 46A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-13	—	mV/ $^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	49	—	—	S	$V_{DS} = 25V, I_D = 46A$
$Q_g$	Total Gate Charge	—	70	98	nC	$V_{DD} = 100V, I_D = 46A, V_{GS} = 10V$ ③
$Q_{gd}$	Gate-to-Drain Charge	—	23	—	nC	
$t_{d(on)}$	Turn-On Delay Time	—	33	—	ns	$V_{DD} = 100V, V_{GS} = 10V$ ③ $I_D = 46A$ $R_G = 2.5\Omega$ See Fig. 22
$t_r$	Rise Time	—	20	—		
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		
$t_f$	Fall Time	—	31	—		
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 160V, V_{GS} = 15V, R_G = 4.7\Omega$
$E_{PULSE}$	Energy per Pulse	—	570	—	$\mu J$	$L = 220\text{nH}, C = 0.4\mu F, V_{GS} = 15V$ $V_{DS} = 160V, R_G = 4.7\Omega, T_J = 25^\circ\text{C}$
		—	910	—		$L = 220\text{nH}, C = 0.4\mu F, V_{GS} = 15V$ $V_{DS} = 160V, R_G = 4.7\Omega, T_J = 100^\circ\text{C}$
$C_{iss}$	Input Capacitance	—	4600	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	460	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	91	—		$f = 1.0\text{MHz},$
$C_{oss\text{ eff.}}$	Effective Output Capacitance	—	360	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$
$L_D$	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	13	—		

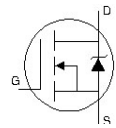


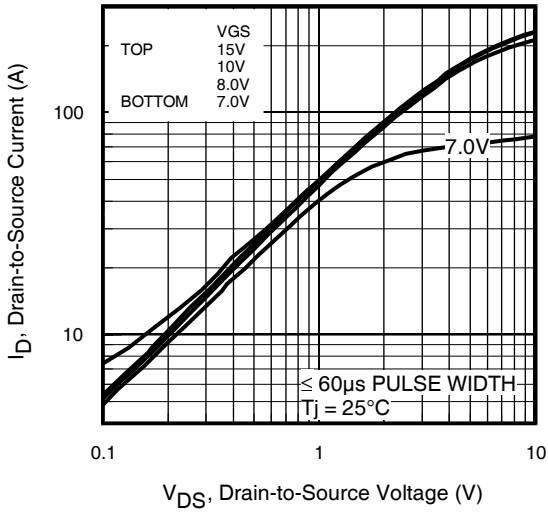
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	140	mJ
$E_{AR}$	Repetitive Avalanche Energy ①	—	33	mJ
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	240	—	V
$I_{AS}$	Avalanche Current ②	—	39	A

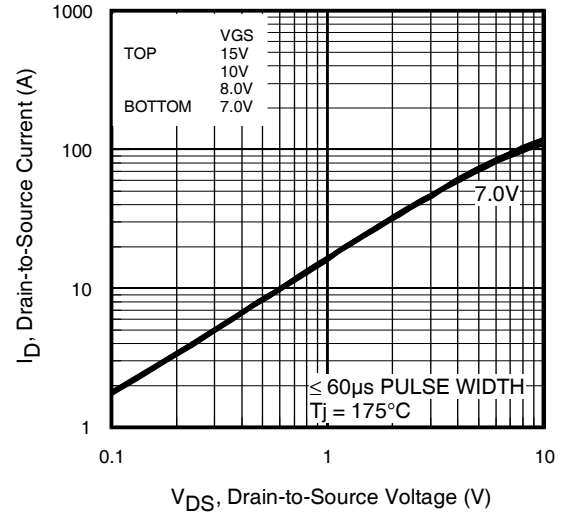
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	65	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	260		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 46A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ\text{C}, I_F = 46A, V_{DD} = 50V$
$Q_{rr}$	Reverse Recovery Charge	—	430	640	nC	$di/dt = 100A/\mu s$ ③

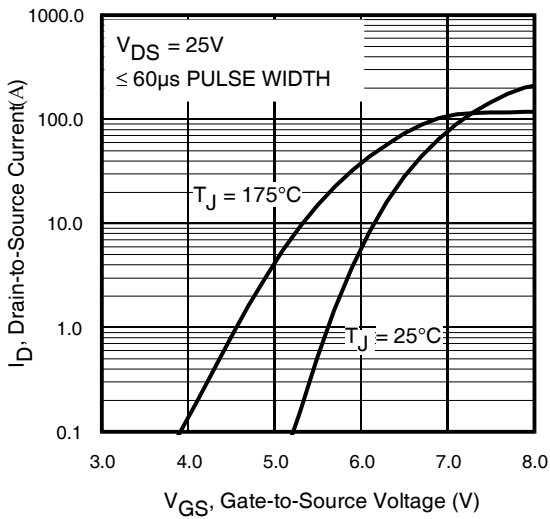




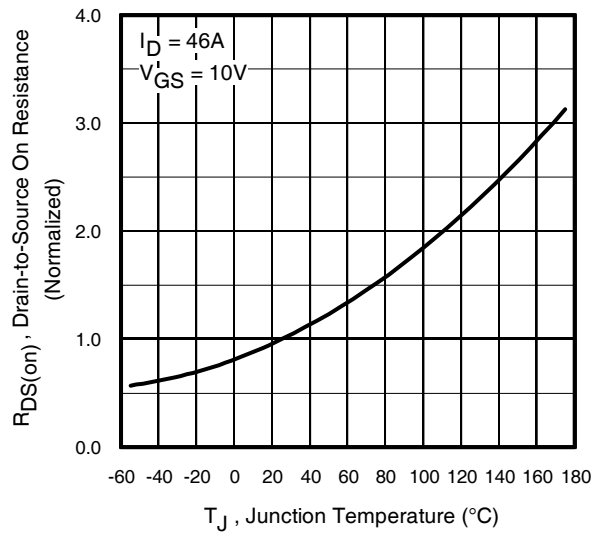
**Fig 1.** Typical Output Characteristics



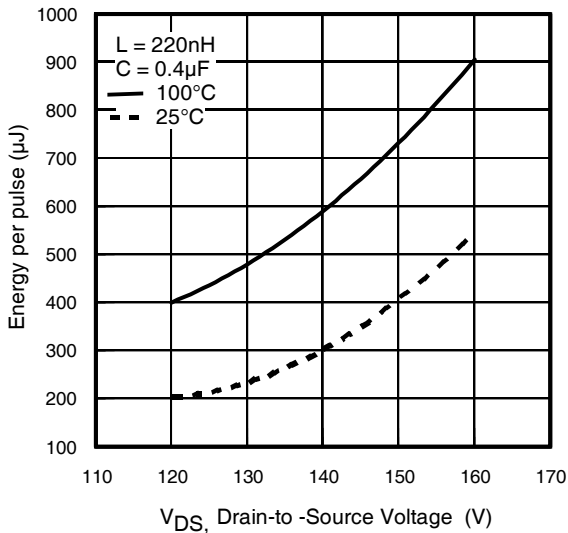
**Fig 2.** Typical Output Characteristics



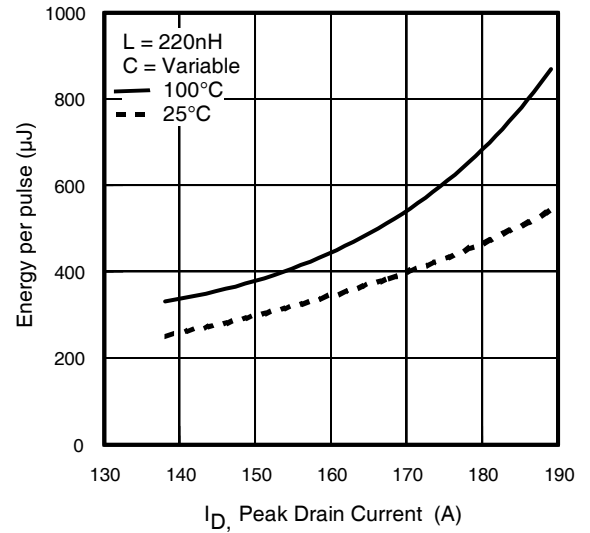
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance vs. Temperature

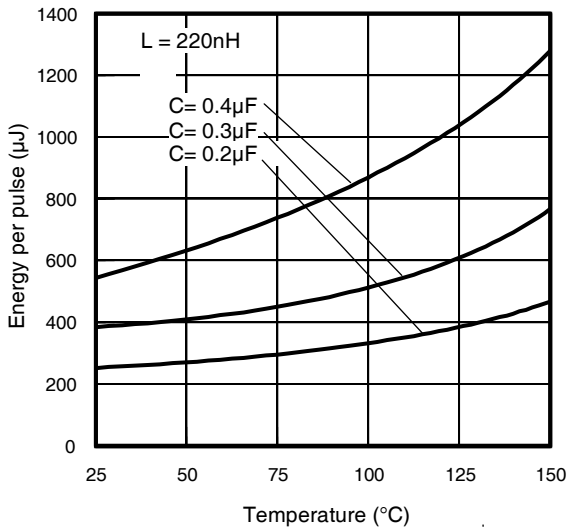


**Fig 5.** Typical  $E_{PULSE}$  vs. Drain-to-Source Voltage

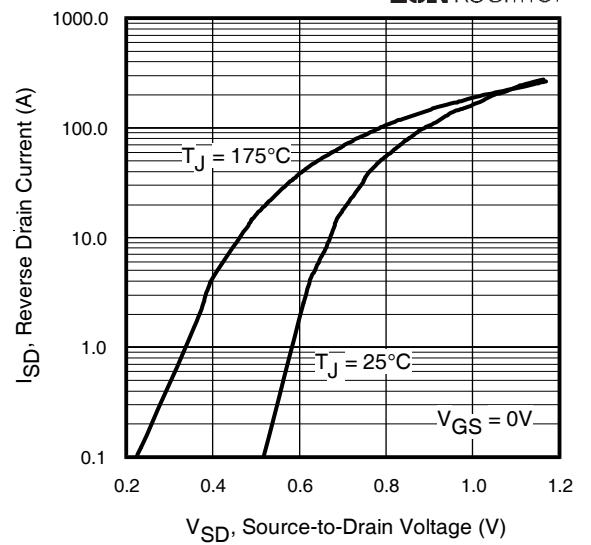


**Fig 6.** Typical  $E_{PULSE}$  vs. Drain Current

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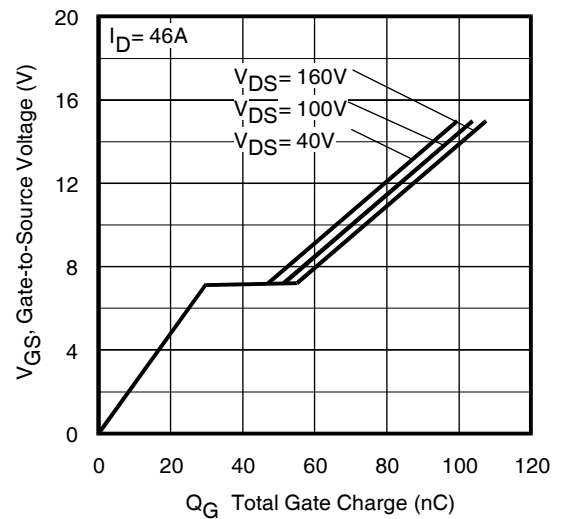
**Fig 7.** Typical  $E_{\text{PULSE}}$  vs. Temperature



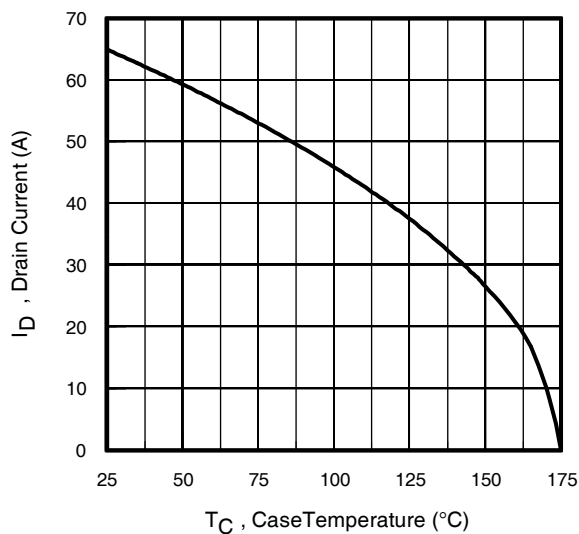
**Fig 8.** Typical Source-Drain Diode Forward Voltage



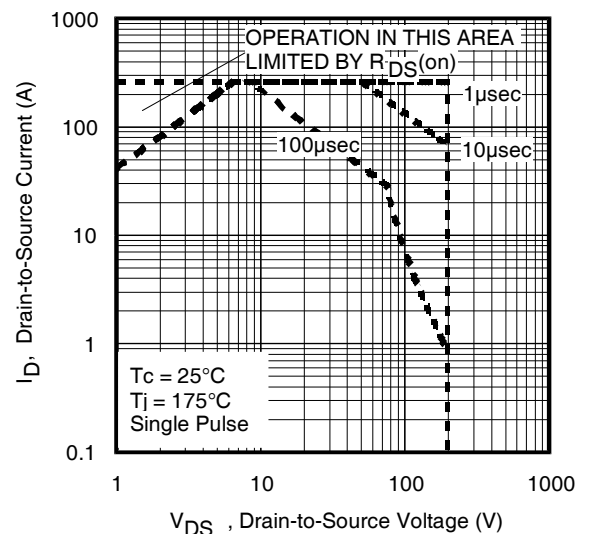
**Fig 9.** Typical Capacitance vs. Drain-to-Source Voltage



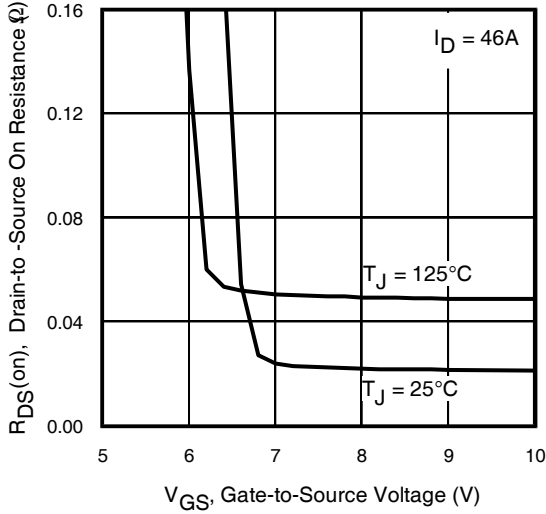
**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage



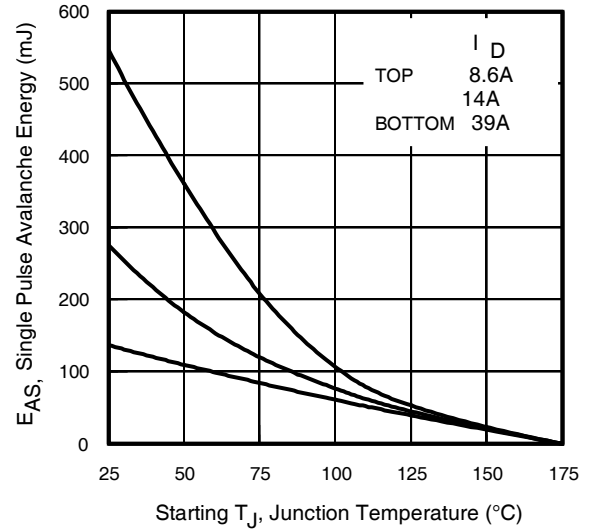
**Fig 11.** Maximum Drain Current vs. Case Temperature



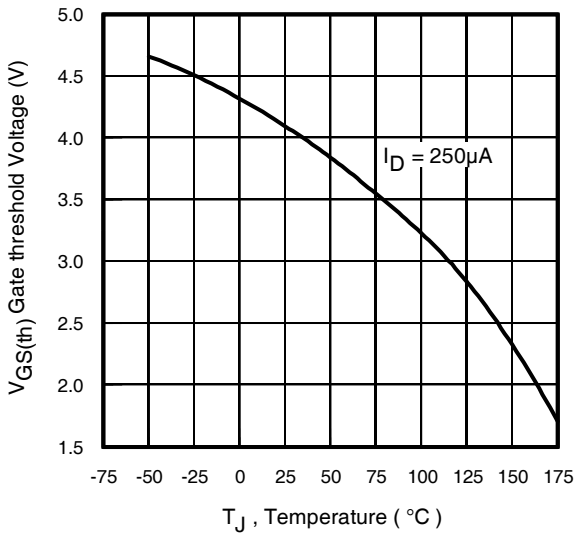
**Fig 12.** Maximum Safe Operating Area



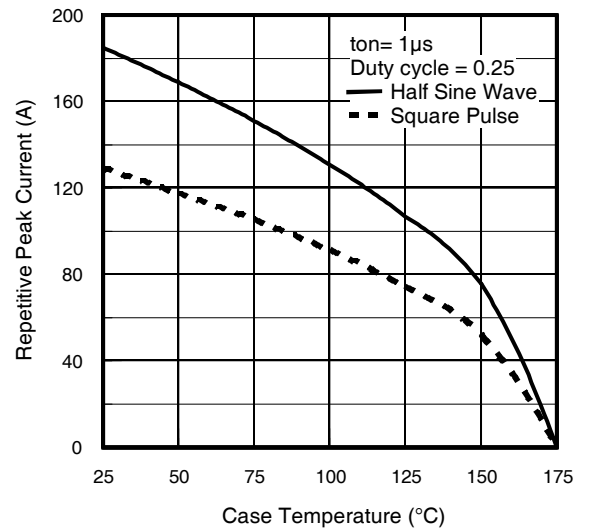
**Fig 13.** On-Resistance Vs. Gate Voltage



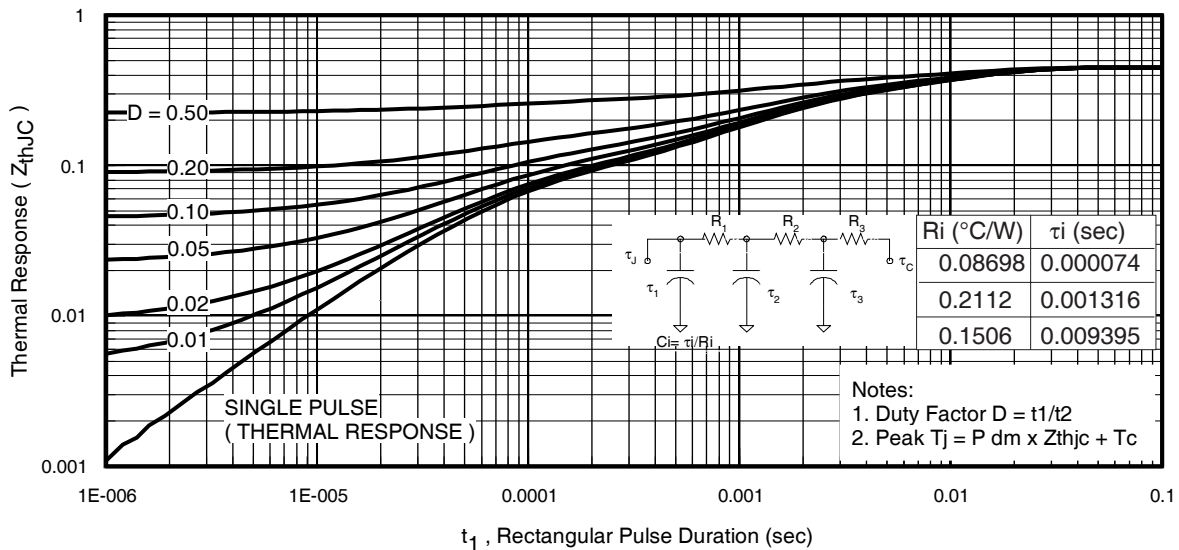
**Fig 14.** Maximum Avalanche Energy Vs. Temperature



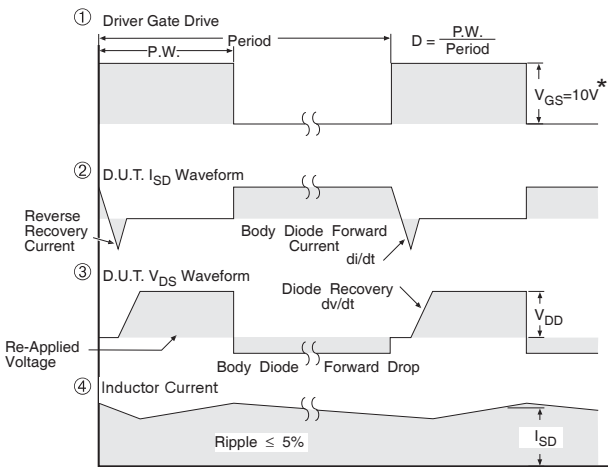
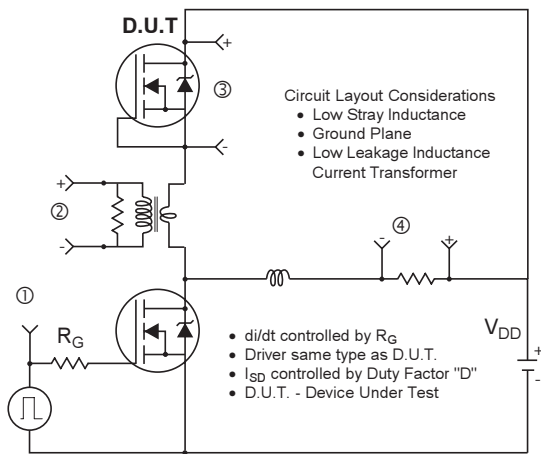
**Fig 15.** Threshold Voltage vs. Temperature



**Fig 16.** Typical Repetitive peak Current vs. Case temperature

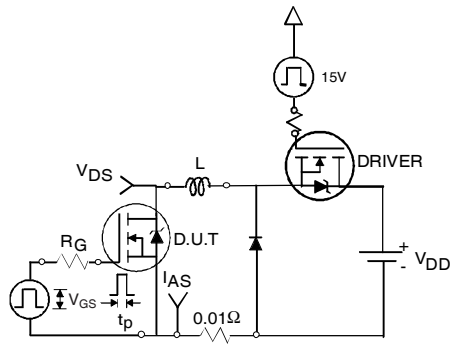


**Fig 17.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

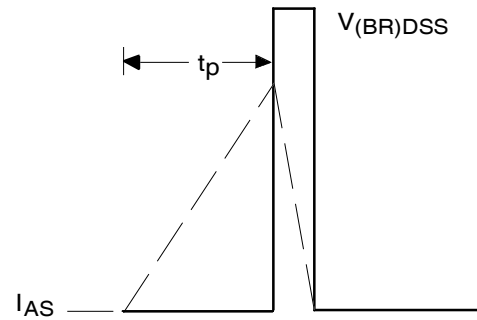


\*  $V_{GS} = 5V$  for Logic Level Devices

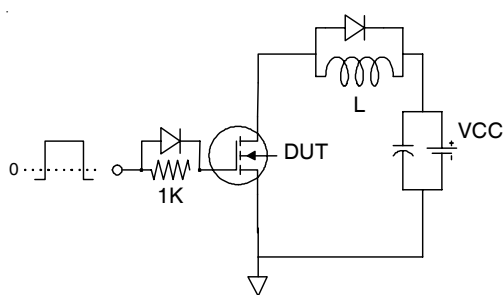
**Fig 18.** Diode Reverse Recovery Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs



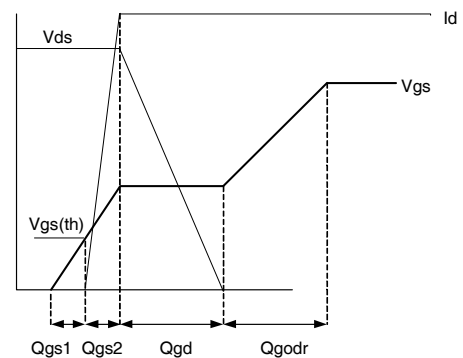
**Fig 19a.** Unclamped Inductive Test Circuit



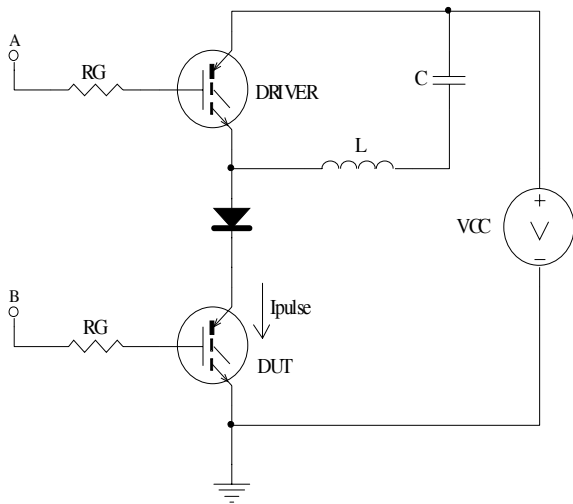
**Fig 19b.** Unclamped Inductive Waveforms



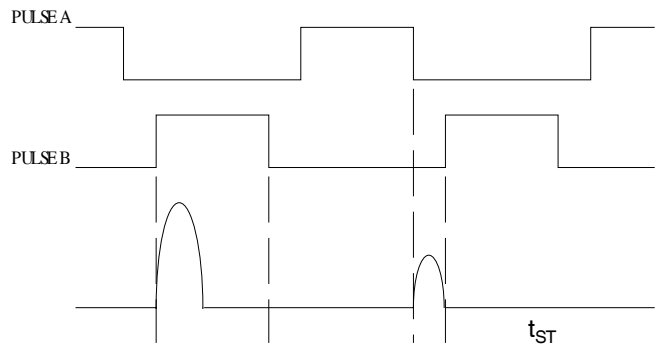
**Fig 20a.** Gate Charge Test Circuit



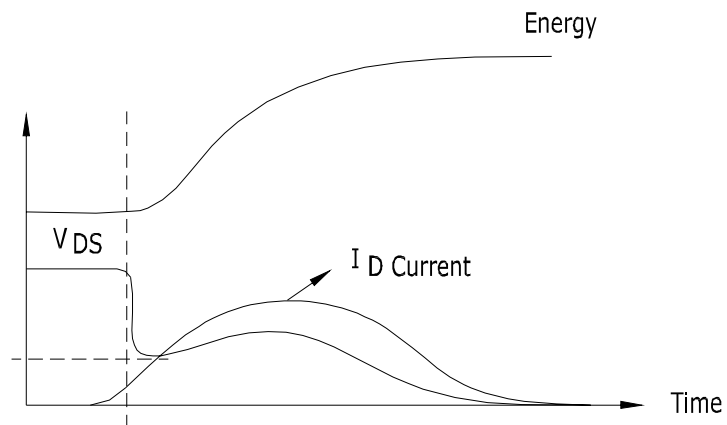
**Fig 20b.** Gate Charge Waveform



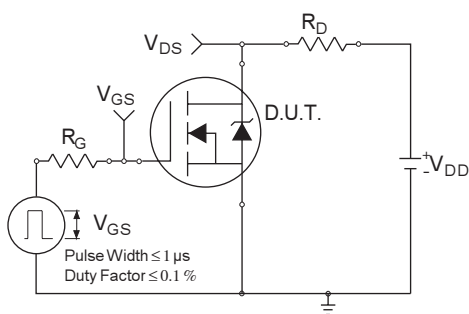
**Fig 21a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



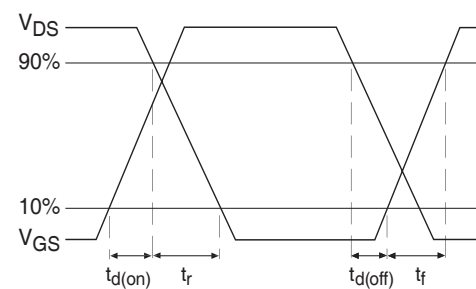
**Fig 21b.**  $t_{st}$  Test Waveforms



**Fig 21c.**  $E_{PULSE}$  Test Waveforms



**Fig 22a.** Switching Time Test Circuit

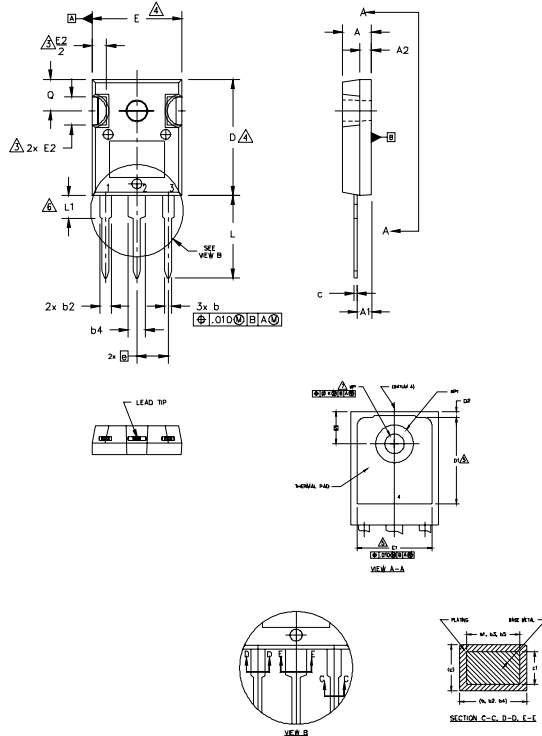


**Fig 22b.** Switching Time Waveforms

# IRFP4227PbF

## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
  2. DIMENSIONS ARE SHOWN IN INCHES.
  3. CONTOUR OF SLOT OPTIONAL.
  4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  6. LEAD FINISH UNCONTROLLED IN L1.
  7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
ek	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

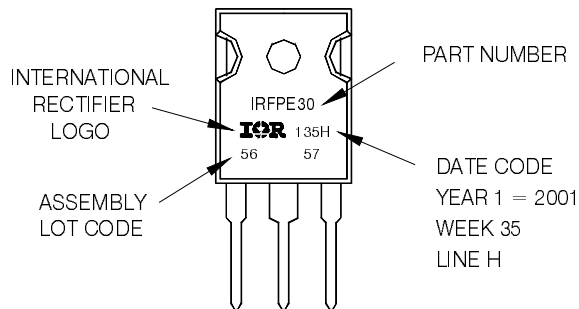
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



### TO-247AC package is not recommended for Surface Mount Application.

**Notes:**

1. Repetitive rating; pulse width limited by max. junction temperature.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.18\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 39\text{A}$ .
3. Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
4.  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
5. Half sine wave with duty cycle = 0.25,  $t_{on} = 1\mu\text{sec}$ .

**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.



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[SSM6P54TU,LF](#) [SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)