

IRFP90N20DPbF

HEXFET® Power MOSFET

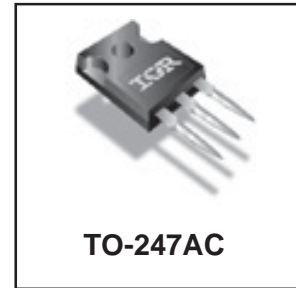
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DSS}	R_{DS(on) max}	I_D
200V	0.023Ω	94A[Ⓔ]

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	94 [Ⓔ]	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	66	
I _{DM}	Pulsed Drain Current [Ⓓ]	380	
P _D @ T _C = 25°C	Power Dissipation	580	W
	Linear Derating Factor	3.8	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt [Ⓢ]	6.7	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.26	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.24	—	
R _{θJA}	Junction-to-Ambient	—	40	

Notes [Ⓓ] through [Ⓔ] are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.24	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.023	Ω	V _{GS} = 10V, I _D = 56A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	250		V _{DS} = 160V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

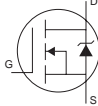
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	39	—	—	S	V _{DS} = 50V, I _D = 56A
Q _g	Total Gate Charge	—	180	270	nC	I _D = 56A V _{DS} = 160V V _{GS} = 10V, ④
Q _{gs}	Gate-to-Source Charge	—	45	67		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	87	130		
t _{d(on)}	Turn-On Delay Time	—	23	—	ns	V _{DD} = 100V I _D = 56A R _G = 1.2Ω V _{GS} = 10V ④
t _r	Rise Time	—	160	—		
t _{d(off)}	Turn-Off Delay Time	—	43	—		
t _f	Fall Time	—	79	—		
C _{iss}	Input Capacitance	—	6040	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	1070	—		
C _{rss}	Reverse Transfer Capacitance	—	170	—		
C _{oss}	Output Capacitance	—	8350	—		
C _{oss}	Output Capacitance	—	420	—		
C _{oss eff.}	Effective Output Capacitance	—	870	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	1010	mJ
I _{AR}	Avalanche Current①	—	56	A
E _{AR}	Repetitive Avalanche Energy①	—	58	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	94⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	380		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 56A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	230	340	ns	T _J = 25°C, I _F = 56A
Q _{rr}	Reverse Recovery Charge	—	1.9	2.8	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

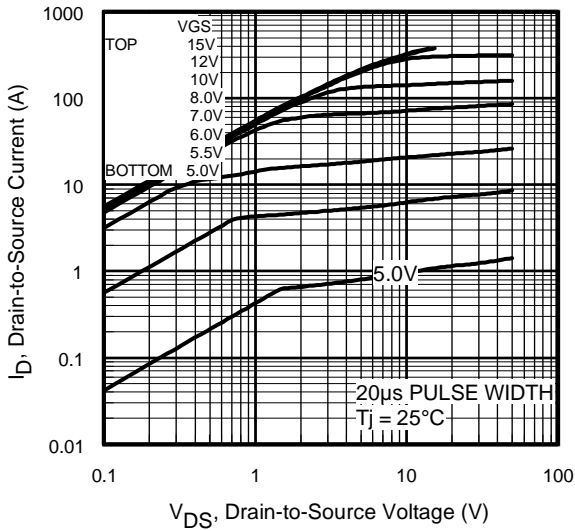


Fig 1. Typical Output Characteristics

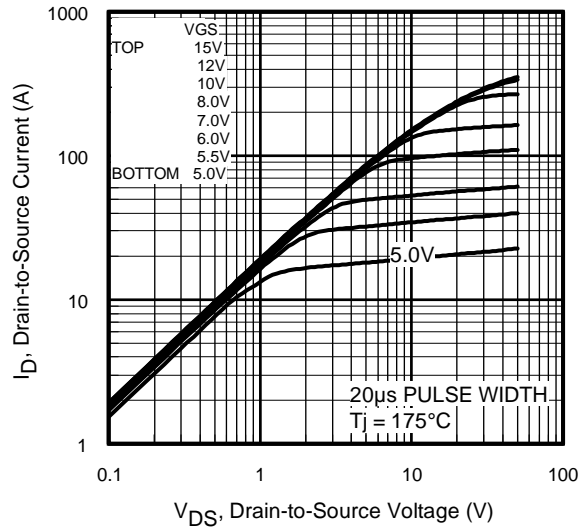


Fig 2. Typical Output Characteristics

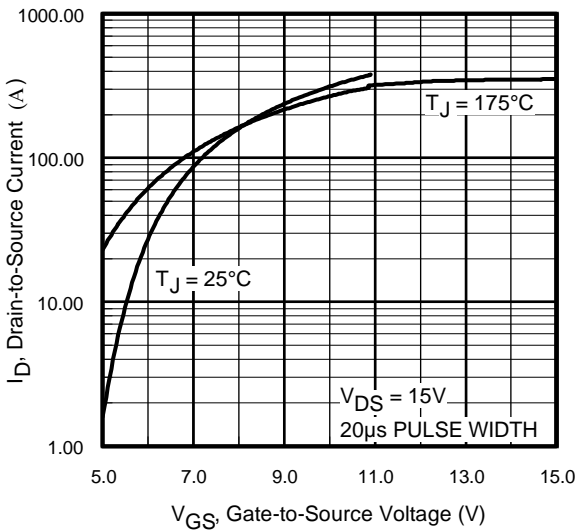


Fig 3. Typical Transfer Characteristics

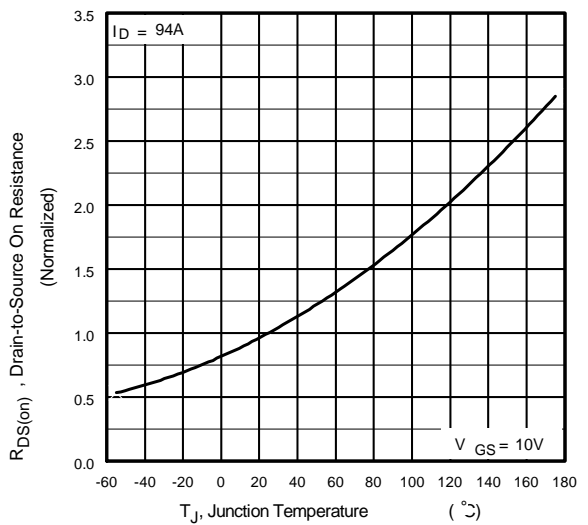


Fig 4. Normalized On-Resistance vs. Temperature

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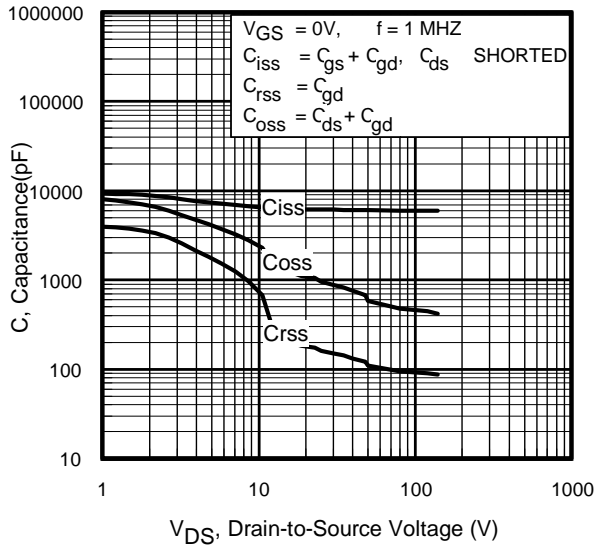


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

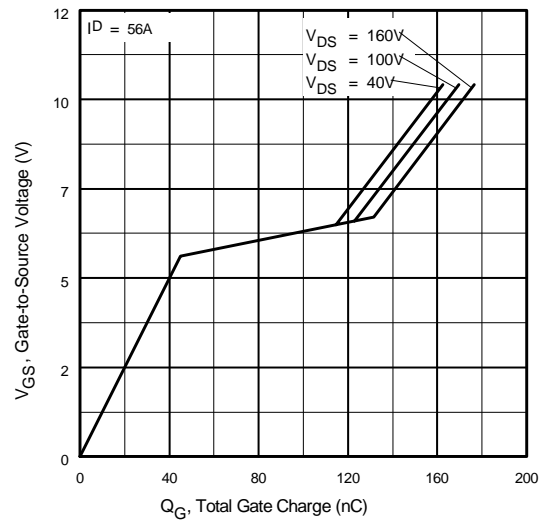


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

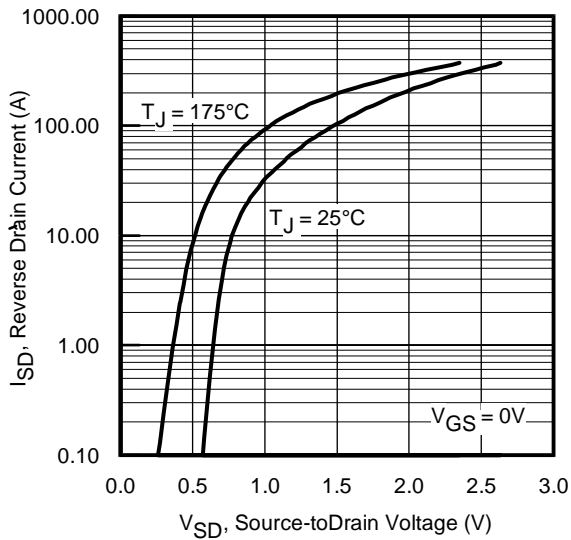


Fig 7. Typical Source-Drain Diode Forward Voltage

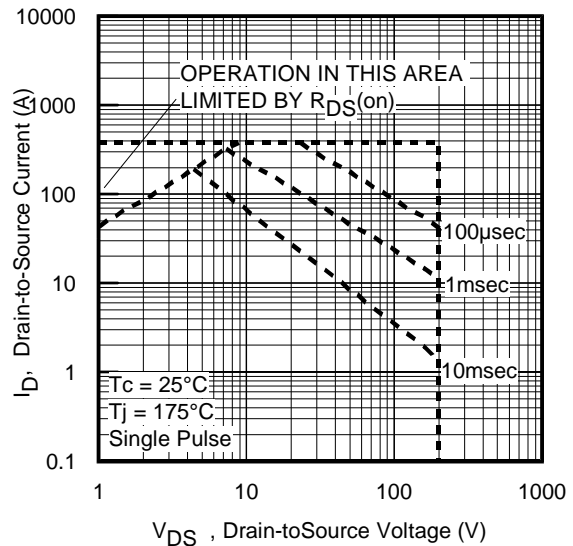


Fig 8. Maximum Safe Operating Area

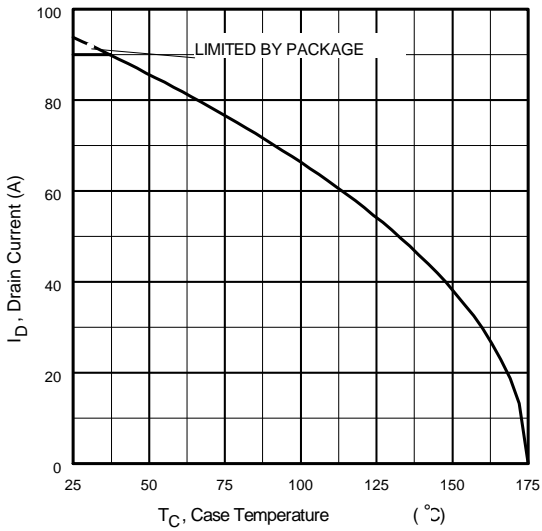


Fig 9. Maximum Drain Current vs. Case Temperature



Fig 10a. Switching Time Test Circuit

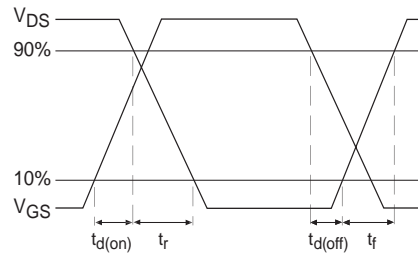


Fig 10b. Switching Time Waveforms

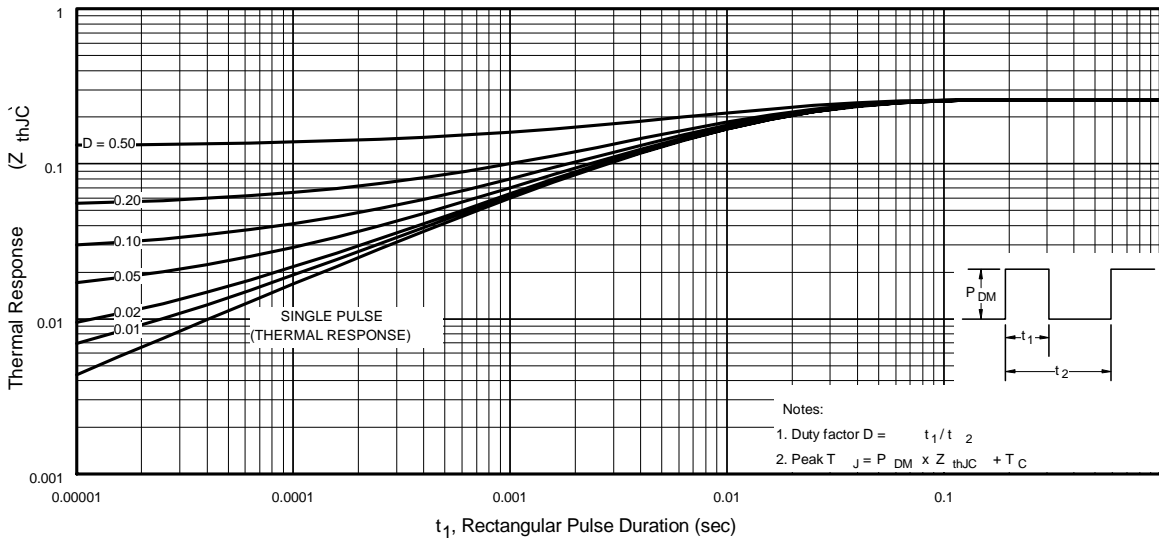


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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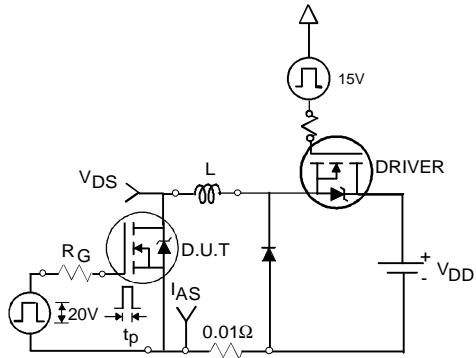


Fig 12a. Unclamped Inductive Test Circuit

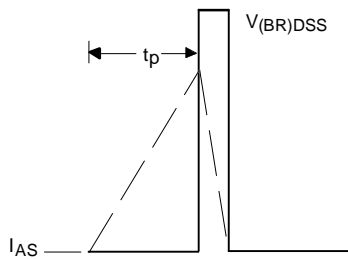


Fig 12b. Unclamped Inductive Waveforms

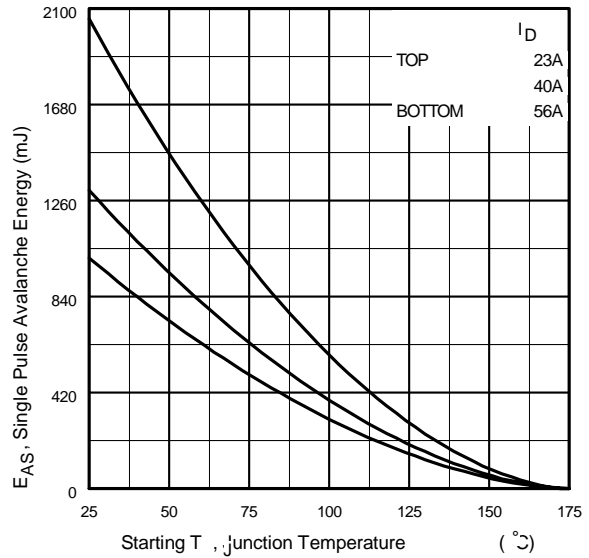


Fig 12c. Maximum Avalanche Energy vs. Drain Current

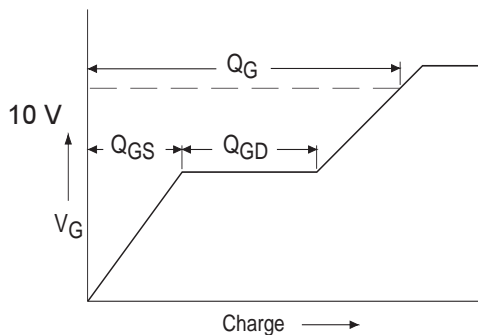


Fig 13a. Basic Gate Charge Waveform

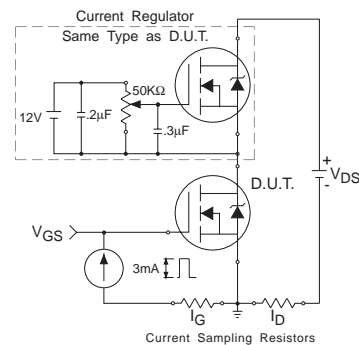
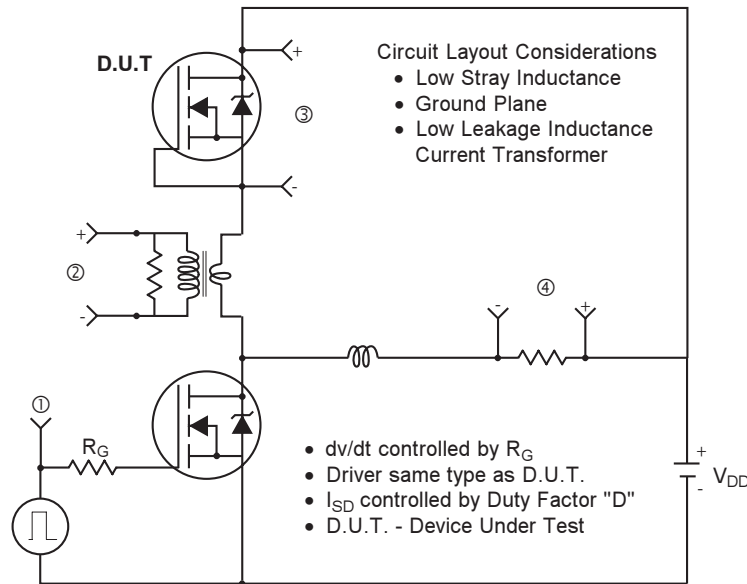


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



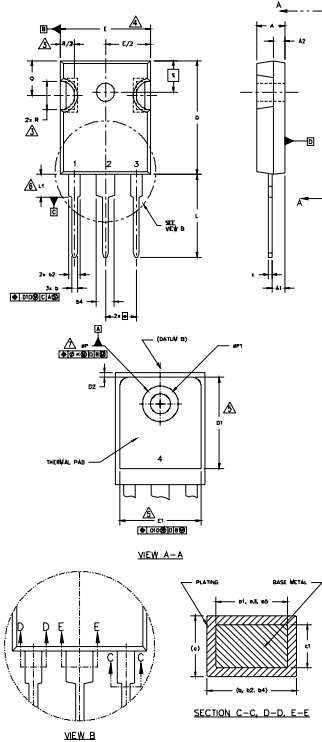
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)

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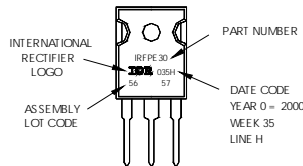
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- CONTOUR OF SLOT OPTIONAL.
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
- LEAD FINISH UNCONTROLLED IN LI.
- #P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91]
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

SYMBOL	INCHES		MILLIMETERS		NOTES	
	MIN.	MAX.	MIN.	MAX.		
A	.183	.209	4.65	5.31	LEAD ASSIGNMENTS HEXFET 1 - GATE 2 - DRAIN 3 - SOURCE 4 - DRAIN	
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		
b1	.039	.053	0.99	1.35		
b2	.065	.094	1.65	2.39		
b3	.065	.092	1.65	2.37		
b4	.102	.135	2.59	3.43		
b5	.102	.133	2.59	3.38		
c	.015	.034	0.38	0.86		
c1	.015	.030	0.38	0.76		
D	.776	.815	19.71	20.70		4
D1	.515	-	13.08	-		5
D2	.020	.030	0.51	0.76		4
E	.602	.625	15.29	15.87	4	
E1	.540	-	13.72	-		
e	215 BSC		5.46 BSC			
e1	.010		2.54			
L	.559	.634	14.20	16.10	DIODES 1 - ANODE/OPEN 2 - CATHODE 3 - ANODE	
L1	.146	.169	3.71	4.29		
N	3		7.62 BSC			
#P	.140	.144	3.56	3.66		
#P1	-	.275	-	6.98		
O	.209	.224	5.31	5.69		
R	.178	.216	4.52	5.49		
S	217 BSC		5.51 BSC			

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 5657 ASSEMBLED ON WW 35, 2000 IN THE ASSEMBLY LINE "H"
Note: "P" in assembly line position indicates "Lead-Free"



Notes:

- Repetitive rating; pulse width limited by max. junction temperature.
- Starting $T_J = 25^\circ\text{C}$, $L = 0.64\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 56\text{A}$.
- $I_{SD} \leq 56\text{A}$, $di/dt \leq 470\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 90A.
Data and specifications subject to change without notice.

This product has been designed and qualified for the Industrial market.

Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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