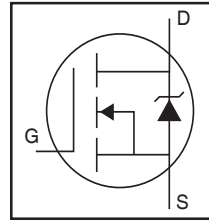


HEXFET® Power MOSFET

**Applications**

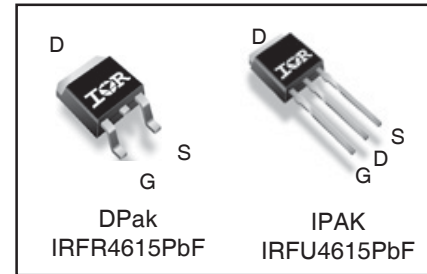
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



$V_{DSS}$		<b>150V</b>
$R_{DS(on)}$	typ.	<b>34mΩ</b>
	max.	<b>42mΩ</b>
$I_D$		<b>33A</b>

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFR4615PbF	D-PAK	Tube/Bulk	75	IRFR4615PbF
IRFR4615TRLPbF		Tape and Reel Left	3000	IRFR4615TRLPbF
IRFU4615PbF	I-PAK	Tube/Bulk	75	IRFU4615PbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	33	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	24	
$I_{DM}$	Pulsed Drain Current ①	140	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	144	W
	Linear Derating Factor	0.96	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	38	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	109	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ③	—	1.045	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ②	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes ① through ③ are on page 11

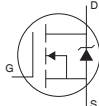
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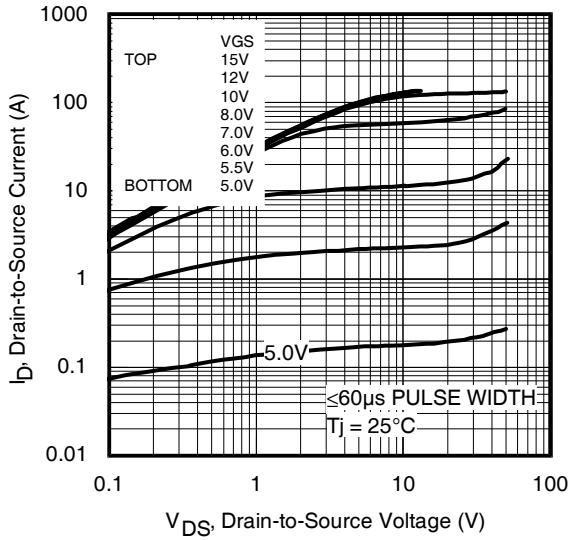
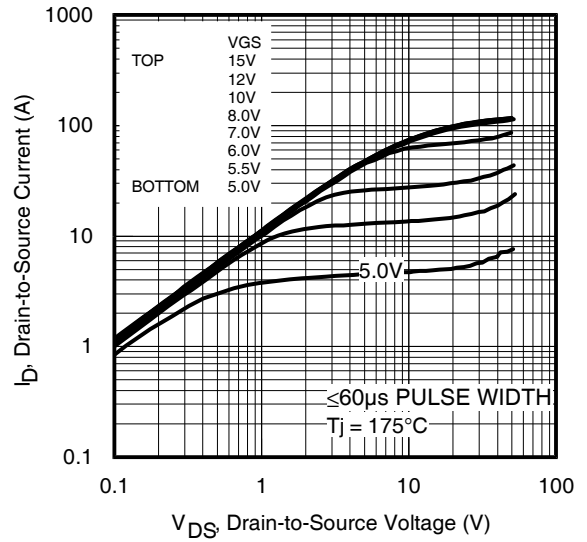
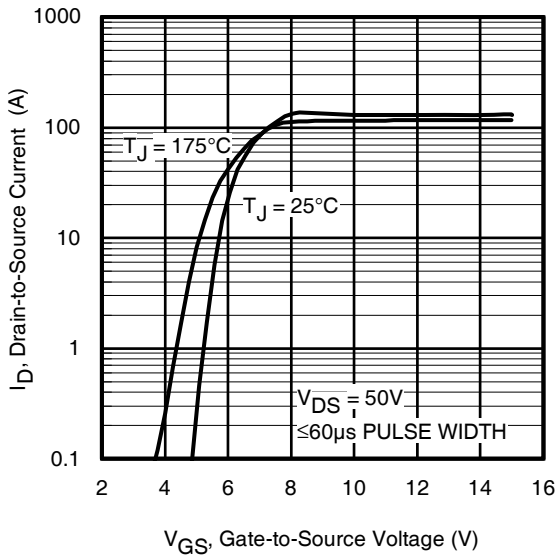
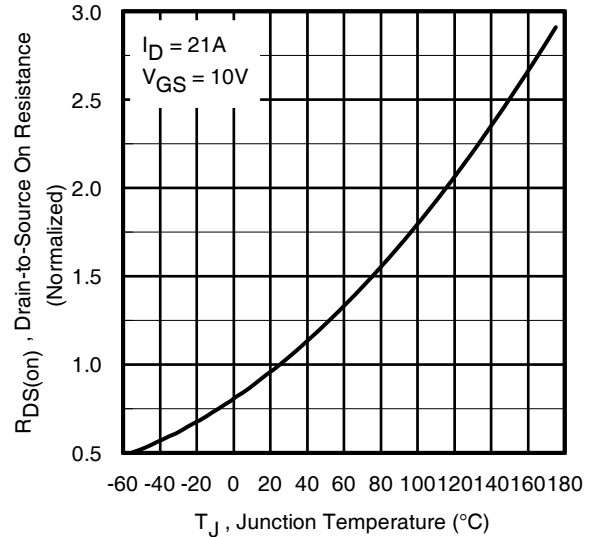
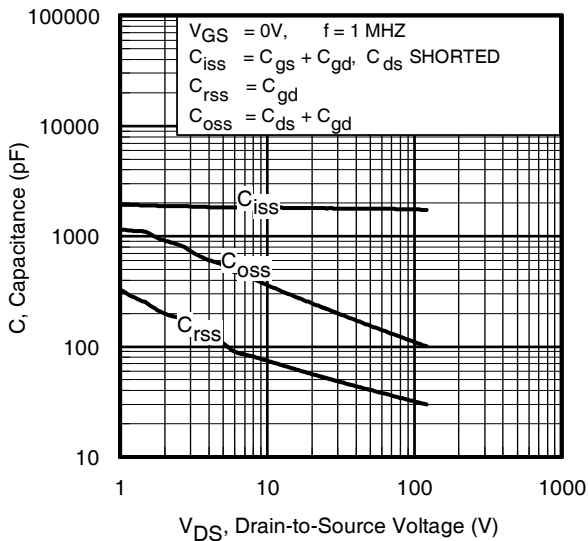
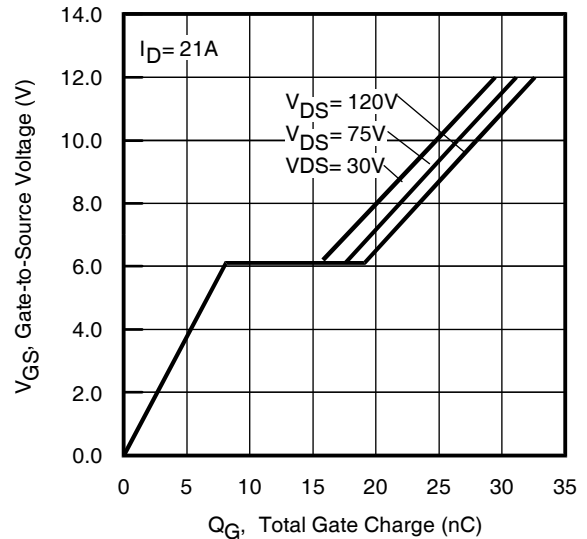
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.19	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	34	42	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 21A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G(int)</sub>	Internal Gate Resistance	—	2.7	—	Ω	

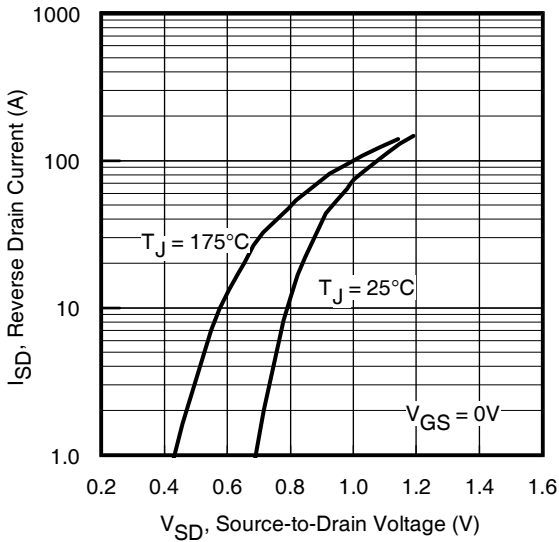
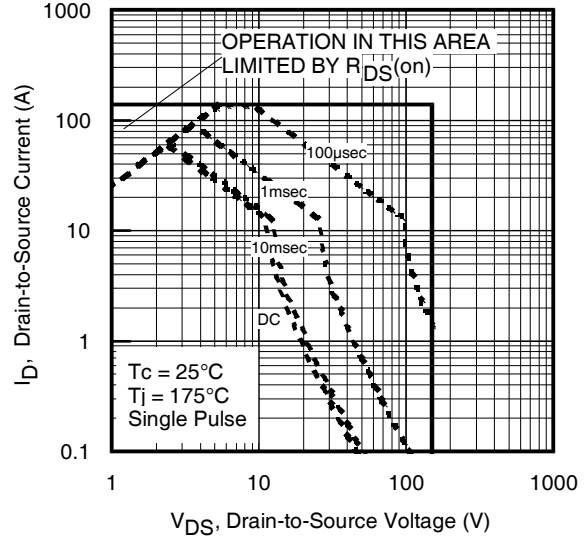
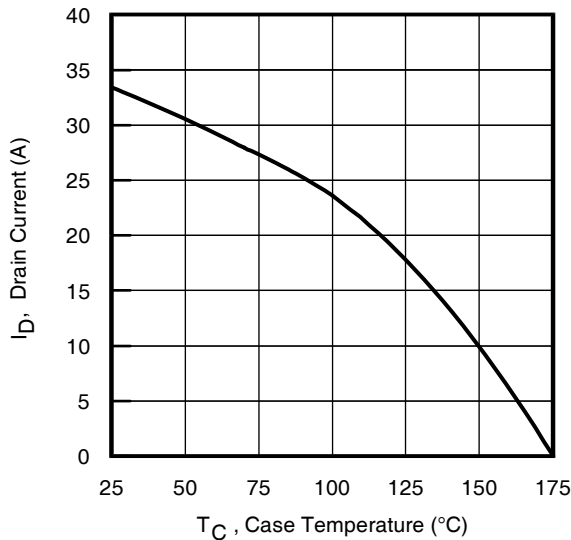
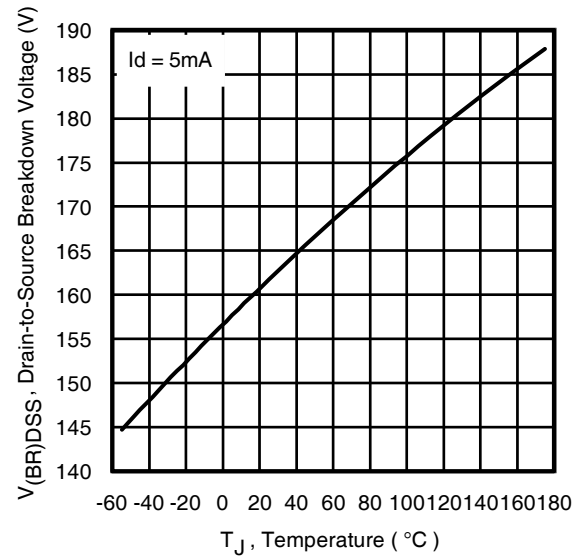
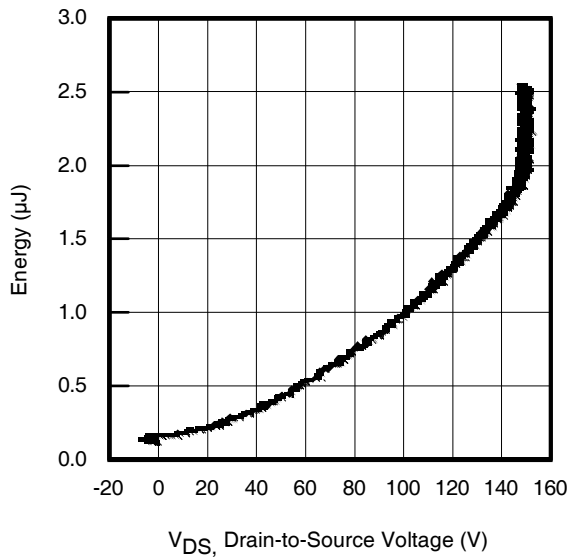
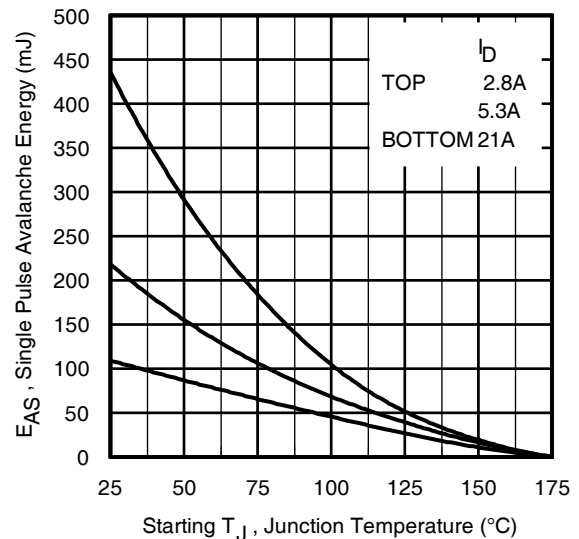
**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

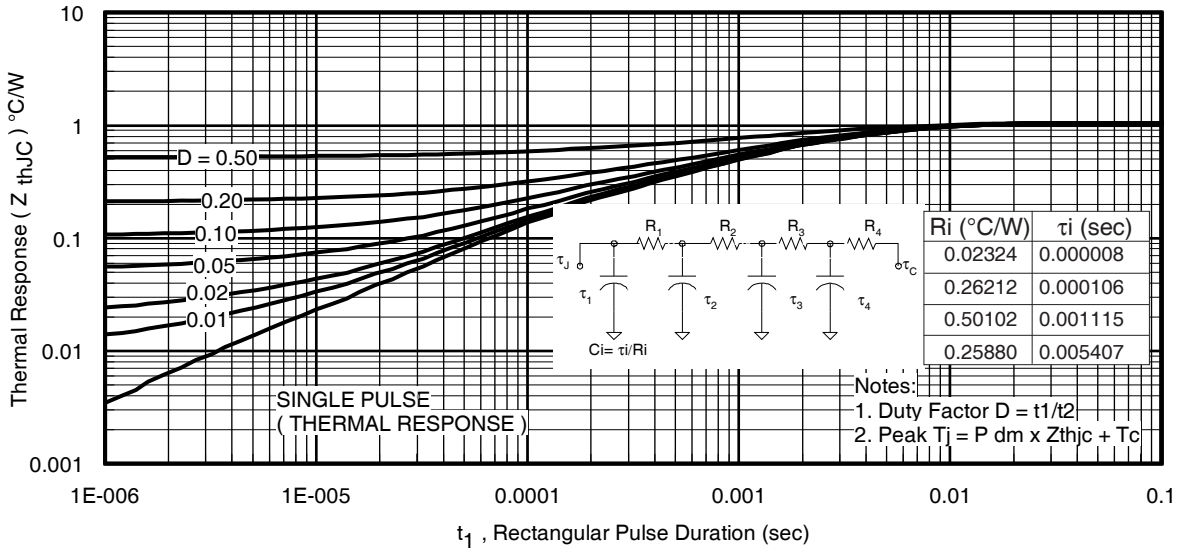
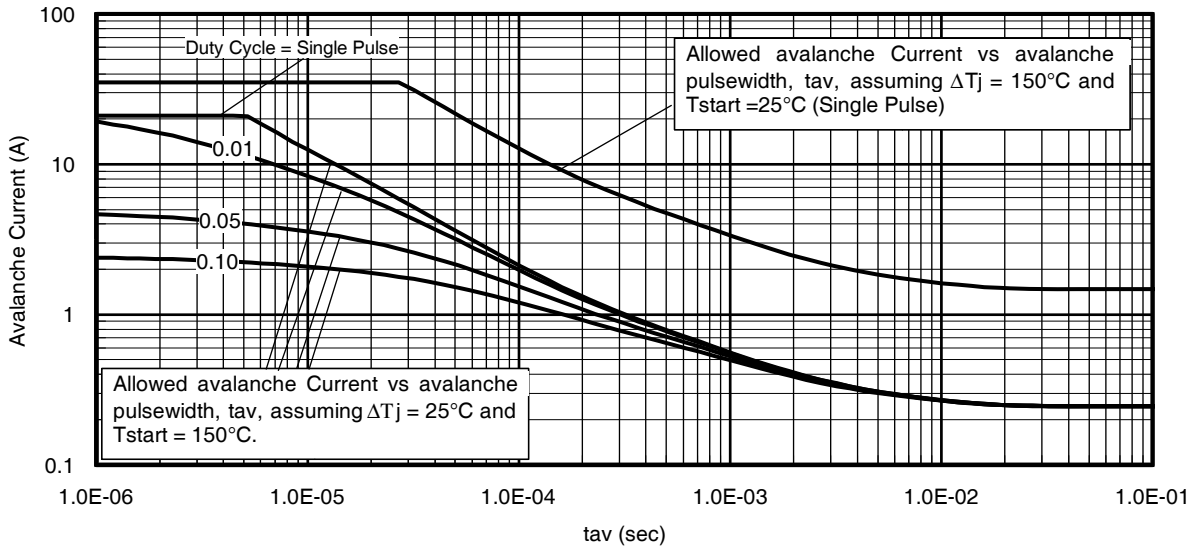
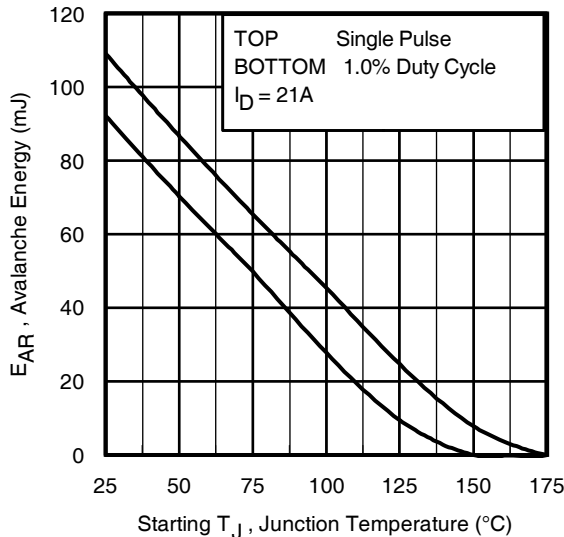
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	35	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 21A
Q <sub>g</sub>	Total Gate Charge	—	26	—	nC	I <sub>D</sub> = 21A
Q <sub>gs</sub>	Gate-to-Source Charge	—	8.6	—		V <sub>DS</sub> = 75V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	9.0	—		V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	17	—		I <sub>D</sub> = 21A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	15	—	ns	V <sub>DD</sub> = 98V
t <sub>r</sub>	Rise Time	—	35	—		I <sub>D</sub> = 21A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	25	—		R <sub>G</sub> = 7.3Ω
t <sub>f</sub>	Fall Time	—	20	—		V <sub>GS</sub> = 10V <sup>④</sup>
C <sub>iss</sub>	Input Capacitance	—	1750	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	155	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	40	—		f = 1.0MHz (See Fig.5)
C <sub>oss eff. (ER)</sub>	Effective Output Capacitance (Energy Related) <sup>⑥</sup>	—	179	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V <sup>⑥</sup> (See Fig.11)
C <sub>oss eff. (TR)</sub>	Effective Output Capacitance (Time Related) <sup>⑤</sup>	—	382	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V <sup>⑤</sup>

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	140		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 21A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	70	—	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 100V,
		—	83	—		T <sub>J</sub> = 125°C I <sub>F</sub> = 21A
Q <sub>rr</sub>	Reverse Recovery Charge	—	177	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>④</sup>
		—	247	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	4.9	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7. Typical Source-Drain Diode Forward Voltage**

**Fig 8. Maximum Safe Operating Area**

**Fig 9. Maximum Drain Current vs. Case Temperature**

**Fig 10. Drain-to-Source Breakdown Voltage**

**Fig 11. Typical  $C_{OSS}$  Stored Energy**

**Fig 12. Maximum Avalanche Energy vs. Drain Current**


**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulsewidth**

**Notes on Repetitive Avalanche Curves, Figures 14, 15:  
 (For further info, see AN-1005 at www.irf.com)**

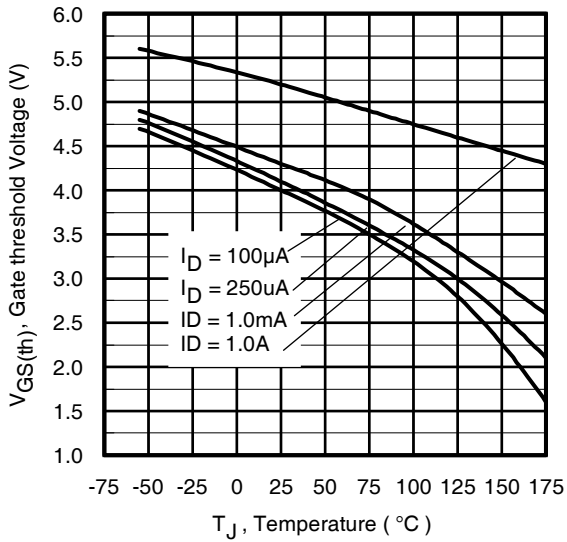
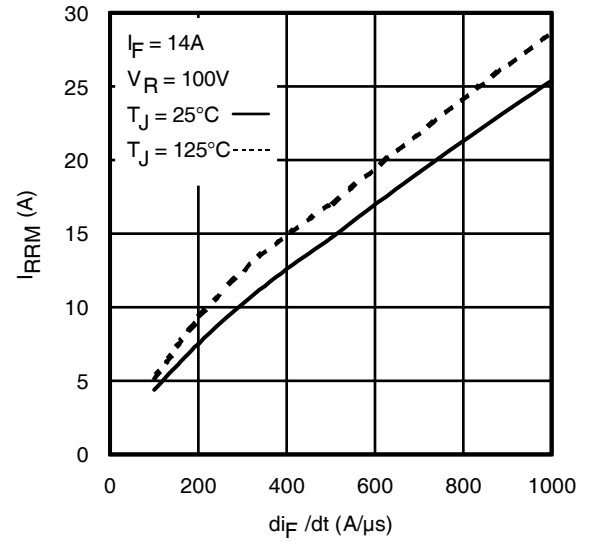
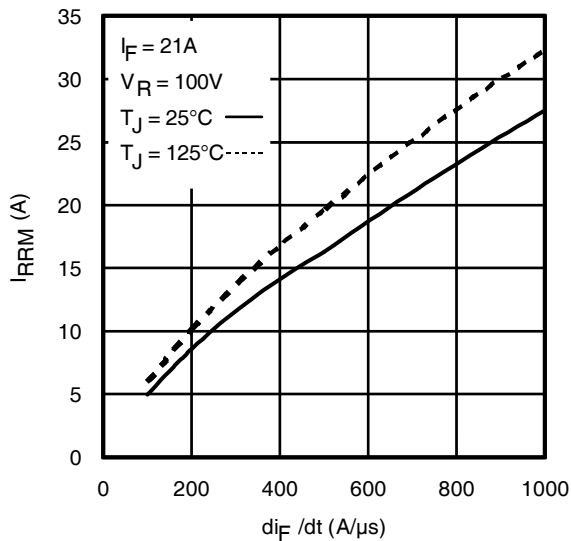
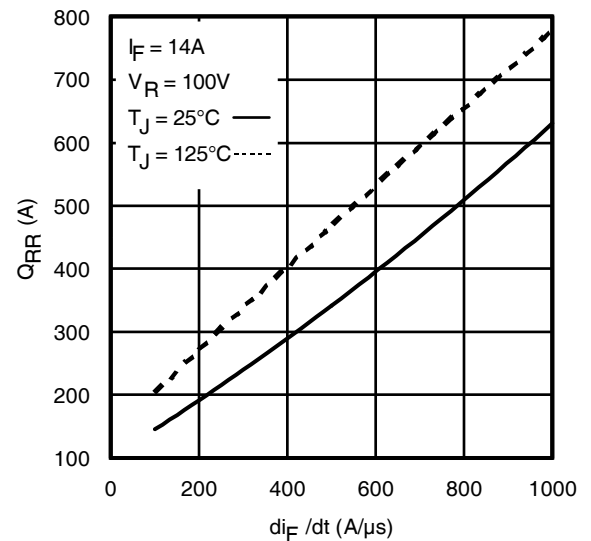
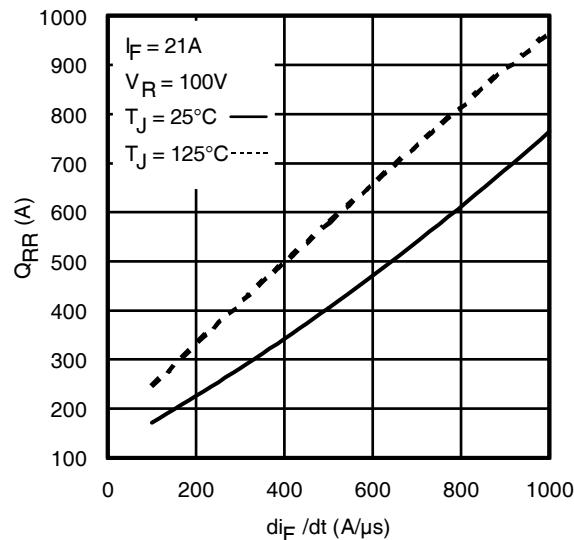
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

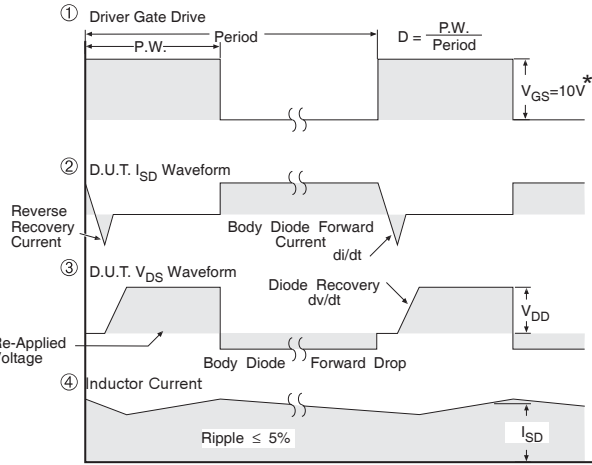
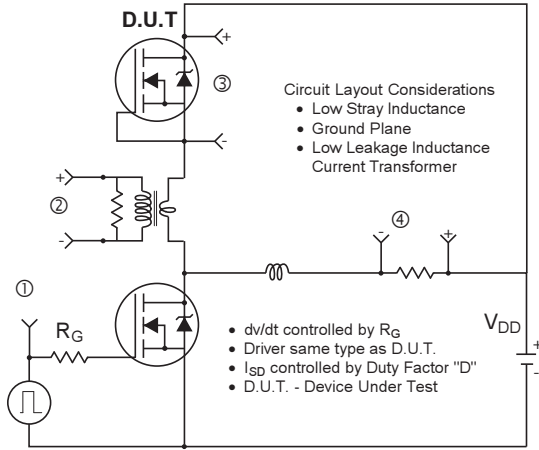
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

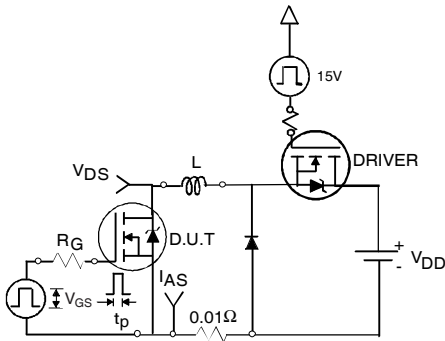
**Fig 15. Maximum Avalanche Energy vs. Temperature**


**Fig. 16.** Threshold Voltage vs. Temperature

**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 18 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 19 -** Typical Stored Charge vs.  $di_F/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$

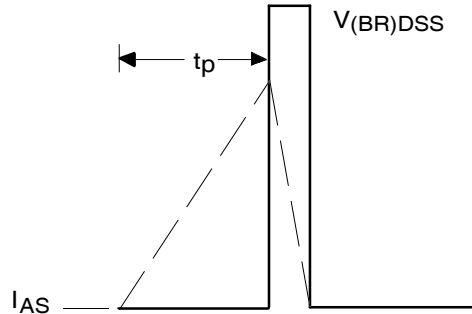


\*  $V_{GS} = 5V$  for Logic Level Devices

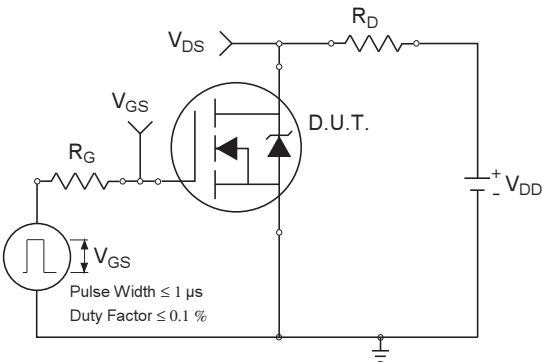
**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



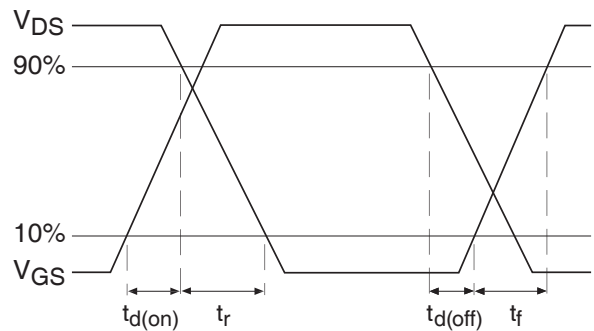
**Fig 22a. Unclamped Inductive Test Circuit**



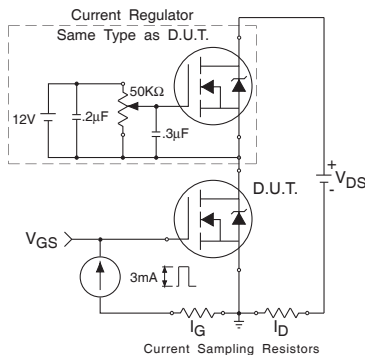
**Fig 22b. Unclamped Inductive Waveforms**



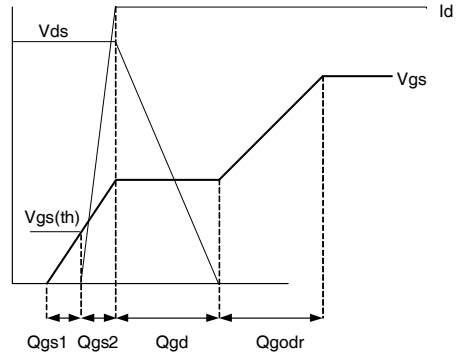
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



**Fig 24a. Gate Charge Test Circuit**



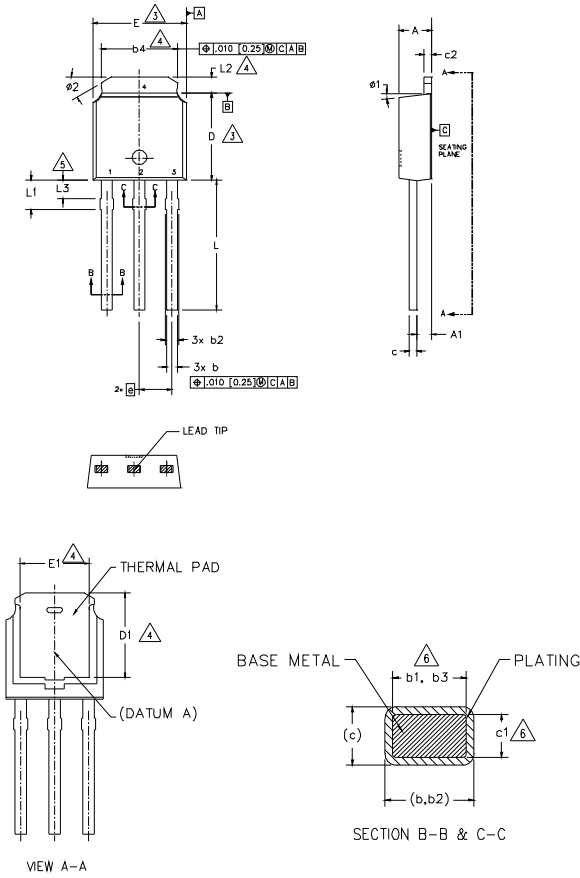
**Fig 24b. Gate Charge Waveform**





# I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5. LEAD DIMENSION UNCONTROLLED IN L3.
6. DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
ø1	0"	15"	0"	15"	
ø2	25*	35*	25*	35*	

**LEAD ASSIGNMENTS**

**HEXFET**

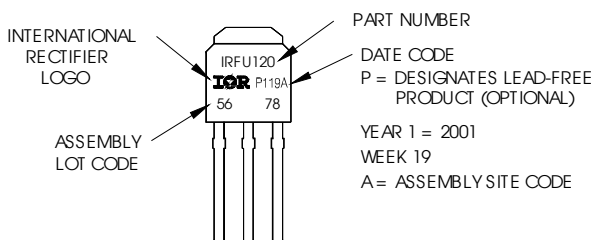
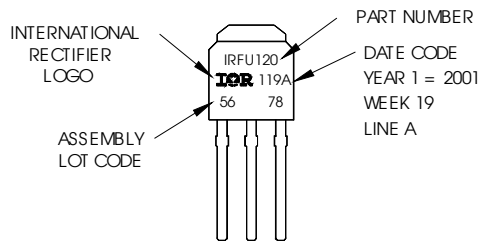
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

# I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW19, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates Lead-Free!

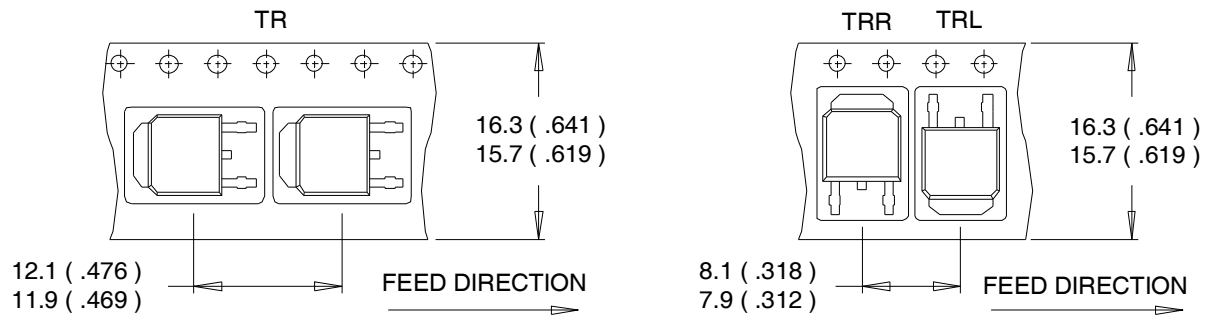
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

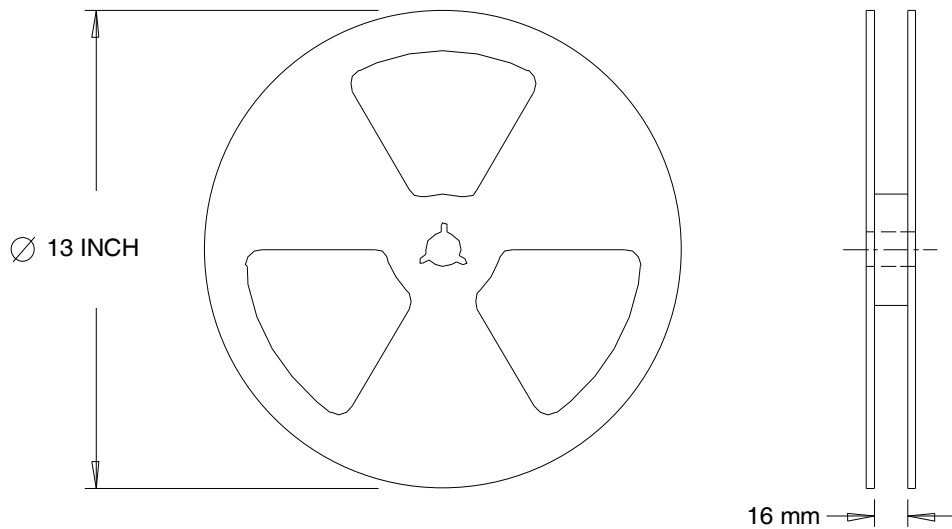
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information†**

Qualification level	Industrial (per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	D-PAK	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
	I-PAK	Not applicable
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.51\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 21\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 21\text{A}$ ,  $di/dt \leq 549\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{OSS}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$

**Revision History**

Date	Comments
5/16/2013	<ul style="list-style-type: none"> <li>• Updated datasheet to new IR corporate formatting template</li> <li>• Updated Orderable part number from "IRFR4615TRPbF" to "IRFR4615TRLpBf", on page 1</li> </ul>

## **IMPORTANT NOTICE**

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