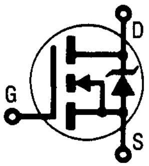
INTERNATIONAL RECTIFIER IOR

AVALANCHE ENERGY RATED AND dv/dt RATED

HEXFET® TRANSISTOR IRFV064



N-CHANNEL

60 Volt, 0.017 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies and virtually any application where military and/or high reliability is required.

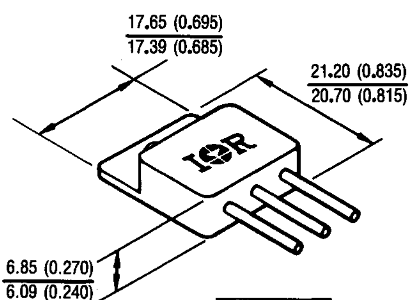
Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRFV064	60V	0.017Ω	45A*

FEATURES:

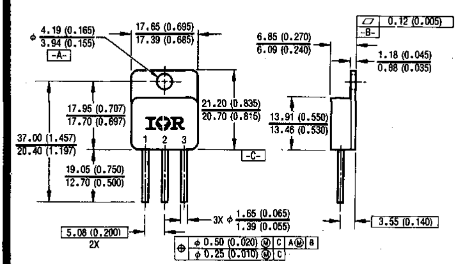
- Avalanche Energy Rating
- Isolated and Hermetically Sealed
- Alternative to TO-3 Package
- Simple Drive Requirements
- Ease of Paralleling
- Ceramic Eyelets

CASE STYLE AND DIMENSIONS



CAUTION

BERYLLIA WARNING PER MIL-S-19500
SEE PAGE I-454



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
2 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

LEGEND
1 DRAIN
2 SOURCE
3 GATE

*For optional leadforms see page I-454, fig. 15

Conforms to JEDEC Outline TO-258AA*
Dimensions in Millimeters and (Inches)

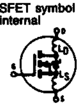
*I_D current limited by pin diameter

Absolute Maximum Ratings

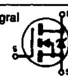
Parameter		IRFV064	Units
I_D @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	45*	A
I_D @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	45*	
I_{DM}	Pulsed Drain Current ①	400	
P_D @ T_C = 25°C	Max. Power Dissipation	300	W
	Linear Derating Factor	2.4	W/K ⑤
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	620	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.063 in. (1.6 mm) from case for 10s)	
	Weight	10.9 (typical)	g

*I_D current limited by pin diameter

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 1.0 mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.048	—	V/°C	Reference to 25°C, I_D = 1.0 mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.017	Ω	V_{GS} = 10V, I_D = 45A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance	21	—	—	S (℧)	V_{DS} ≥ 15V, I_{DS} = 45A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V
		—	—	250		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	240	nC	V_{GS} = 10V, I_D = 45A
Q_{gs}	Gate-to-Source Charge	—	—	53		V_{DS} = 0.5 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	78		See Fig. 6 and 14
$t_{d(on)}$	Turn-On Delay Time	—	—	27	ns	V_{DD} = 30V, I_D = 45A, R_G = 2.35Ω
t_r	Rise Time	—	—	120		
$t_{d(off)}$	Turn-Off Delay Time	—	—	76		See Fig. 11
t_f	Fall Time	—	—	93		
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	—	13	—		Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	—	7400	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	3200	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	—	540	—		See Fig. 5
C_{DC}	Drain-to-Case Capacitance	—	12	—		f = 1.0 MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	45*	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	3.0	V	T_J = 25°C, I_S = 45A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	220	nS	T_J = 25°C, I_F = 45A, dI/dt = ≤ 100 A/μs ④
Q_{RR}	Reverse Recovery Charge	—	—	1.1	μC	V_{DD} ≤ 50V
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

*I_S current limited by pin diameter

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.42	K/W ⑤	
R_{thCS}	Case-to-Sink	—	0.21	—		Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	30		Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 9) Refer to current HEXFET reliability report

② @ V_{DD} = 25V, Starting T_J = 25°C, L ≥ 79 mH, R_G = 25Ω, Peak I_L = 45A

③ I_{SD} ≤ 130A, dI/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ 125°C Suggested R_G = 2.35Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ K/W = °C/W W/K = W/°C

I

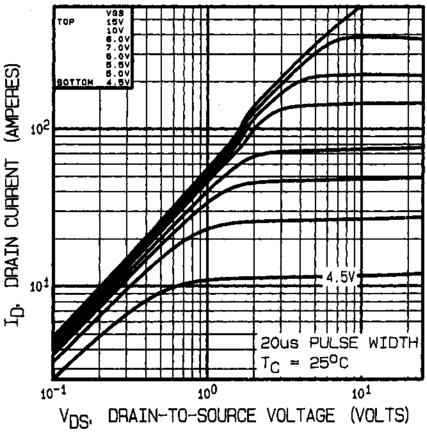


Fig. 1 — Typical Output Characteristics, T_C = 25°C

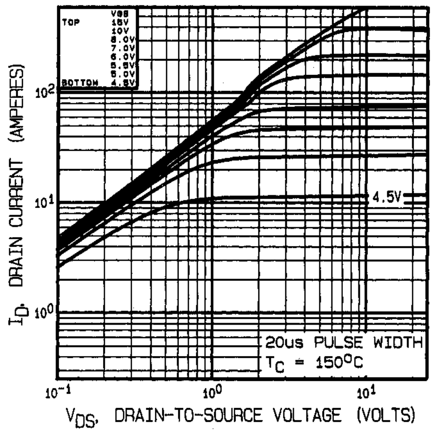


Fig. 2 — Typical Output Characteristics, T_C = 150°C

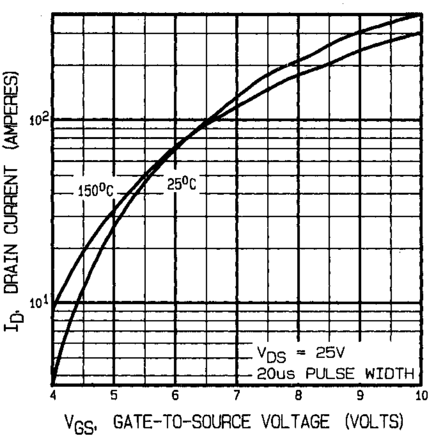


Fig. 3 — Typical Transfer Characteristics

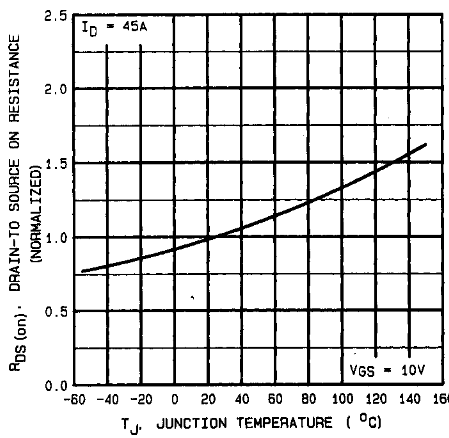


Fig. 4 — Normalized On-Resistance Vs. Temperature

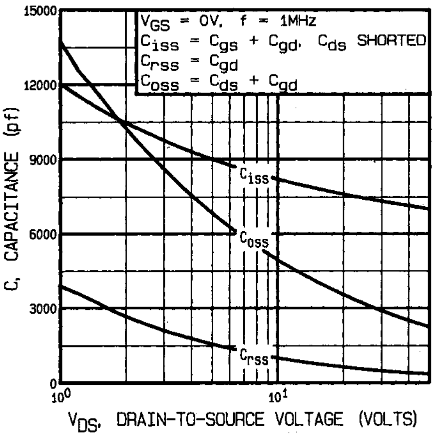


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

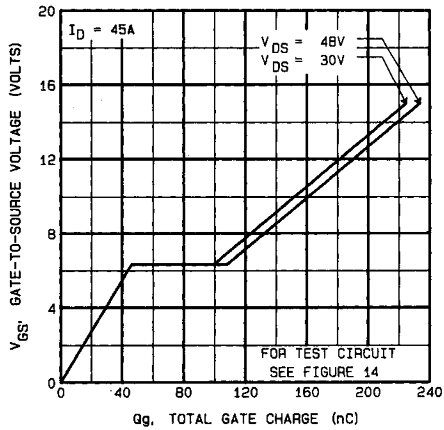


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

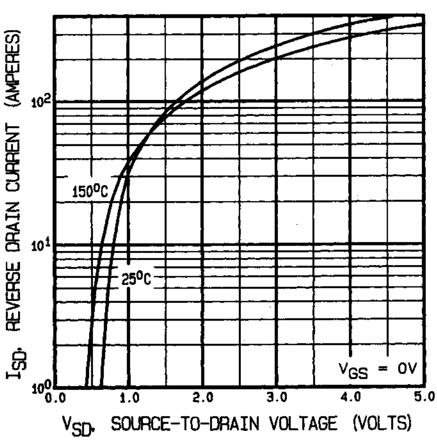


Fig. 7 — Typical Source-Drain Diode Forward Voltage

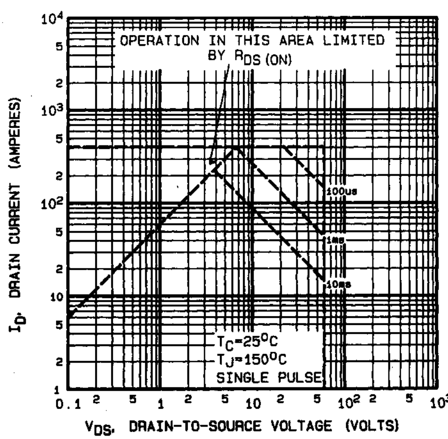


Fig. 8 — Maximum Safe Operating Area

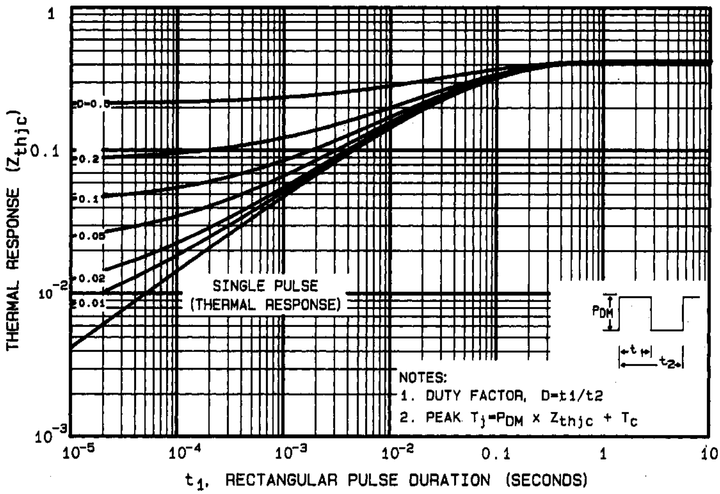


Fig. 9 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

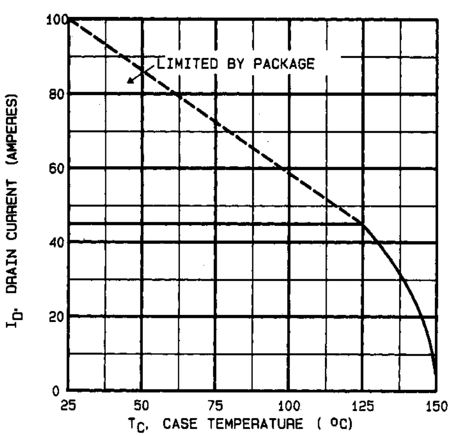


Fig. 10 — Maximum Drain Current Vs. Case Temperature

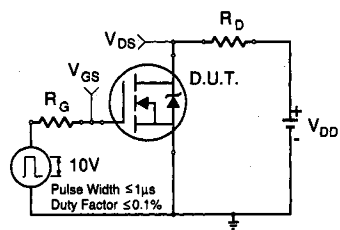


Fig. 11a — Switching Time Test Circuit

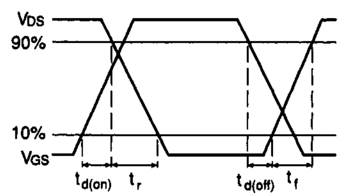


Fig. 11b — Switching Time Waveforms

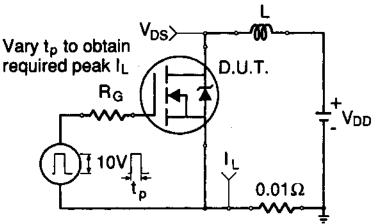


Fig. 12a — Unclamped Inductive Test Circuit

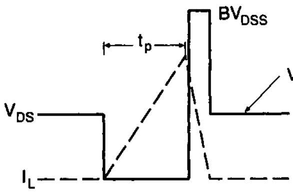


Fig. 12b — Unclamped Inductive Waveforms

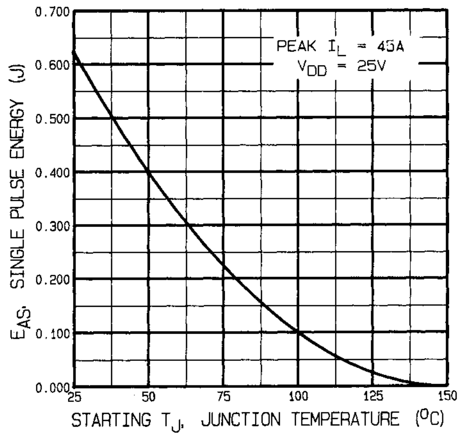
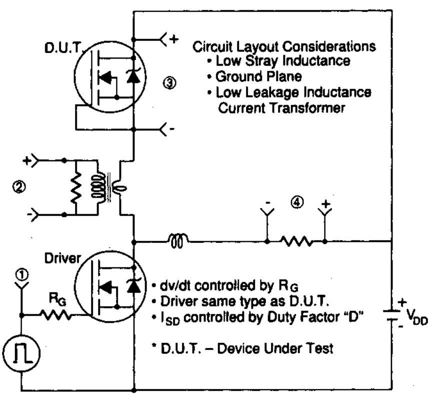
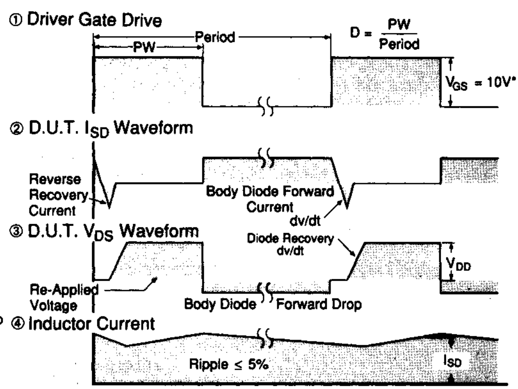


Fig. 12c — Maximum Avalanche Energy Vs. Starting Junction Temperature





*V_{GS} = 5V for Logic Level Devices

Fig. 13 — Peak Diode Recovery dv/dt Test Circuit

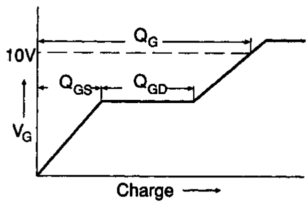


Fig. 14a — Basic Gate Charge Waveform

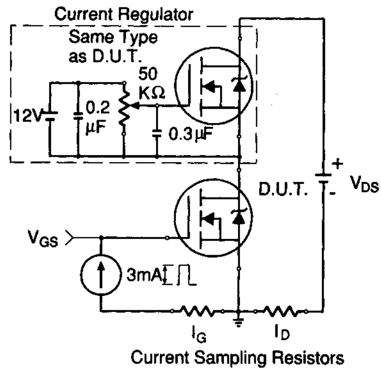
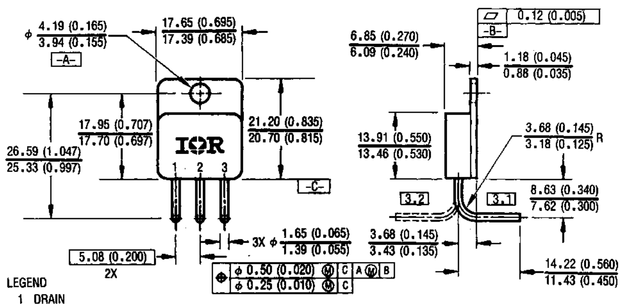


Fig. 14b — Gate Charge Test Circuit



LEGEND
1 DRAIN
2 SOURCE
3 GATE

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
2 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3 LEADFORM IS AVAILABLE IN EITHER ORIENTATION:
3.1 EXAMPLE: IRFV064D
3.2 EXAMPLE: IRFV064U

Fig. 15 – Optional Leadforms for Outline TO-258

BERYLLIA WARNING PER MIL-S-19500
Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.