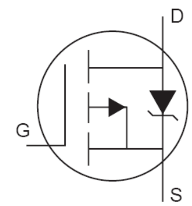
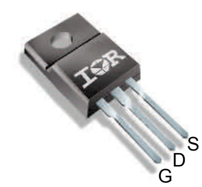
HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low R_{DSON} for Improved Efficiency
- Low Q_G and Q_{sw} for Better THD and Improved Efficiency
- Low Q_{rr} for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability
- Lead-Free

Key Parameters		
V_{DS}	-55	V
$R_{DS(ON)}$ typ. @ V_{GS} =-10V	93	mΩ
$R_{DS(ON)}$ typ. @ V_{GS} = -4.5V	150	mΩ
Q_g typ.	31	nC
T_J max	175	°C





TO-220 Full-Pak

G	D	S
Gate	Drain	Source

Description

This Digital Audio HEXFET® is specifically designed for Class-D audio amplifier applications. This MosFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MosFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MosFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLIB9343PbF	TO-220 Full-Pak	Tube	50	IRLIB9343PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-55	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-14	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-10	
I_{DM}	Pulsed Drain Current ①	-60	
P_D @T_C = 25°C	Maximum Power Dissipation	33	W
P_D @T_C = 100°C	Maximum Power Dissipation	20	
	Linear Derating Factor	0.26	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	——	3.84	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ④	——	65	

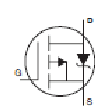
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	——	——	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	-52	——	mV/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	93	105	mΩ	V_{GS} = -10V, I_D = -3.4A
			150	170		V_{GS} = -4.5V, I_D = -2.7A
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	——	——	V	V_{DS} = V_{GS}, I_D = -250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	——	-3.7	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	-2.0	μA	V_{DS} = -55V, V_{GS} = 0V
		——	——	-25		V_{DS} = -55V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	——	——	100		V_{GS} = 20V
gfs	Forward Trans conductance	5.3	——	——	S	V_{DS} = -25V, I_D = -14A
Q_g	Total Gate Charge	——	31	47	nC	V_{DS} = -44V
Q_{gs}	Pre-Vth Gate-to-Source Charge	——	7.1	——		I_D = -14A,
Q_{gd}	Gate-to-Drain Charge	——	8.5	——		V_{GS} = -10V
Q_{godr}	Gate Charge Overdrive	——	15	——		See Fig. 6 and 19.
$t_{d(on)}$	Turn-On Delay Time	——	9.5	——	ns	V_{DD} = -28V, V_{GS} = -10V ③
t_r	Rise Time	——	24	——		I_D = -14A
$t_{d(off)}$	Turn-Off Delay Time	——	21	——		R_G= 2.5Ω
t_f	Fall Time	——	9.5	——		
C_{iss}	Input Capacitance	——	660	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	160	——		V_{DS} = -50V
C_{rss}	Reverse Transfer Capacitance	——	72	——		*ƒ* = 1.0MHz, See Fig. 5
C_{oss} eff.	Effective Output Capacitance	——	280	——		V_{GS} = 0V, V_{DS} = 0V to –44V
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	7.5	——		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	——	190	mJ
I_{AR}	Avalanche Current ⑤	See Fig. 14, 15, 17a, 17b		A
E_{AR}	Repetitive Avalanche Energy ⑤			mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S @ T_C = 25°C	Continuous Source Current (Body Diode)	——	——	-14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-60		
V_{SD}	Diode Forward Voltage	——	——	-1.2	V	T_J = 25°C,I_S = -14A,V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	57	86	ns	T_J = 25°C ,I_F = -14A
Q_{rr}	Reverse Recovery Charge	——	120	180	nC	di/dt = 100A/μs ③

Notes:
① Repetitive rating; pulse width limited by max. junction temperature.
② starting T_J = 25°C, L = 3.89mH, R_G = 25Ω, I_{AS} = -10A.
③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
④ R_θ is measured at T_J of approximately 90°C.
⑤ Limited by T_{jmax}. See Figs. 14, 15, 17a, 17b for repetitive avalanche information

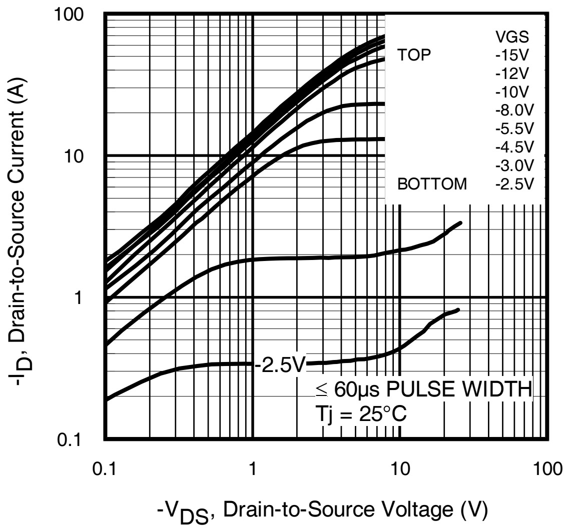


Fig. 1 Typical Output Characteristics

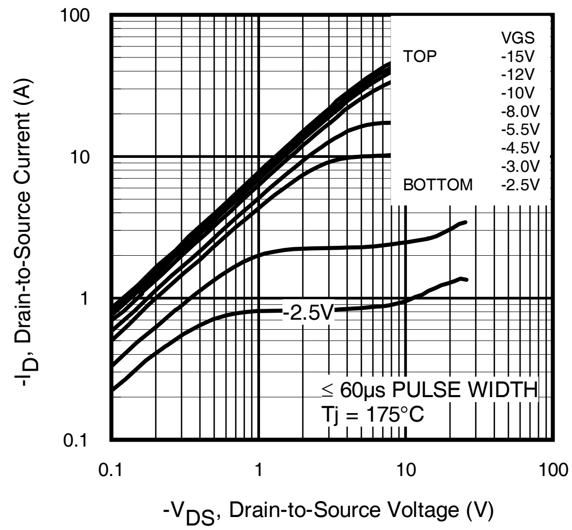


Fig. 2 Typical Output Characteristics

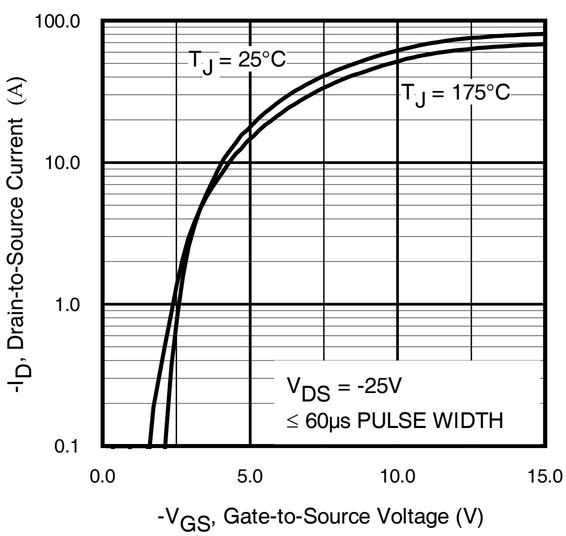


Fig. 3 Typical Transfer Characteristics

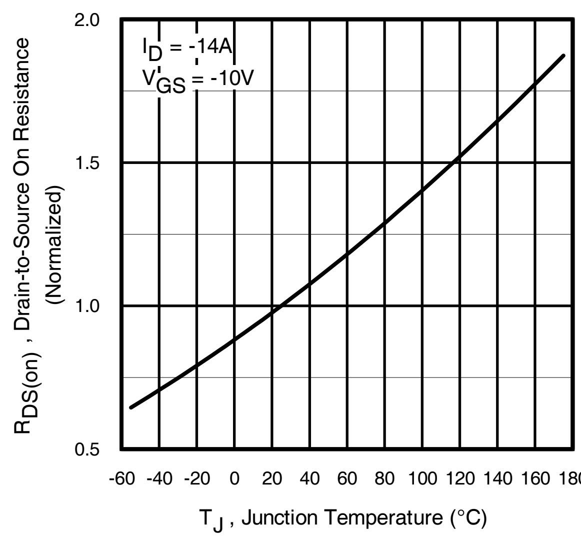


Fig. 4 Normalized On-Resistance vs. Temperature

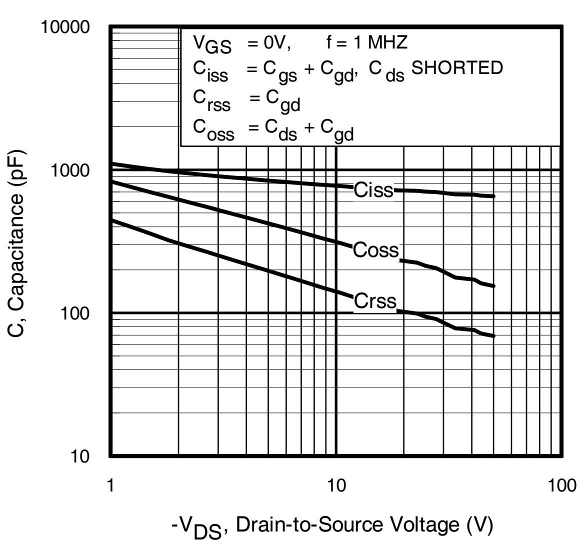


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

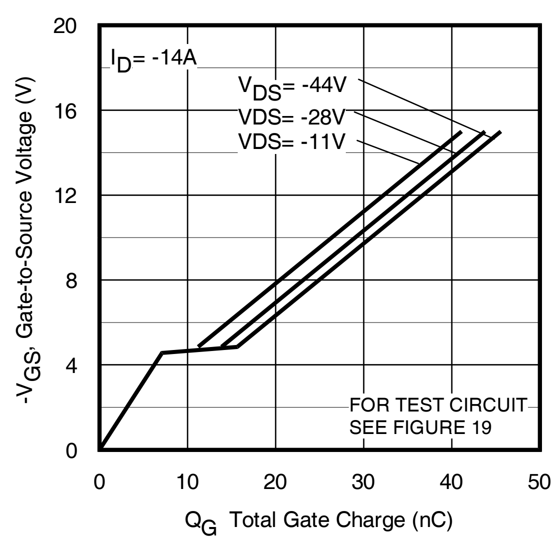


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

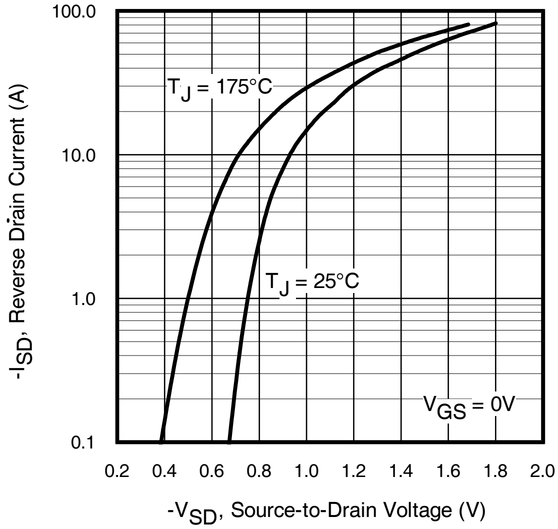


Fig. 7 Typical Source-to-Drain Diode

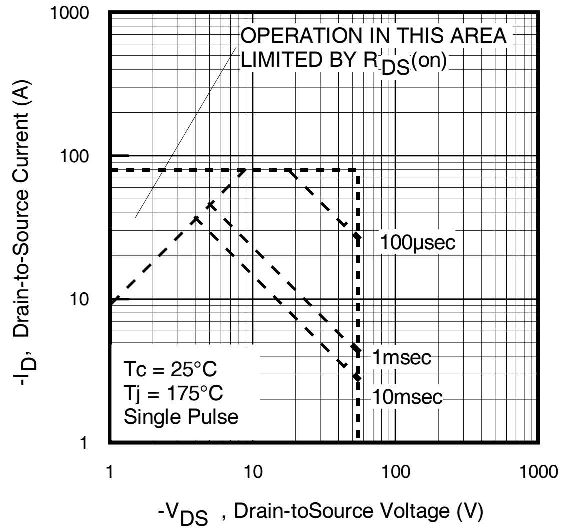


Fig 8. Maximum Safe Operating Area

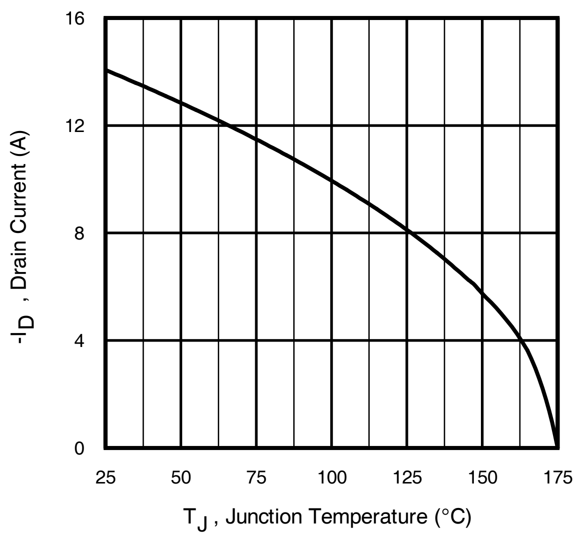


Fig 9. Maximum Drain Current vs. Case Temperature

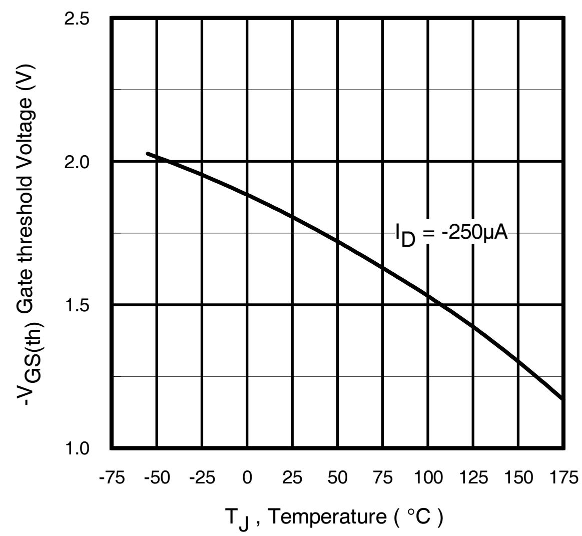
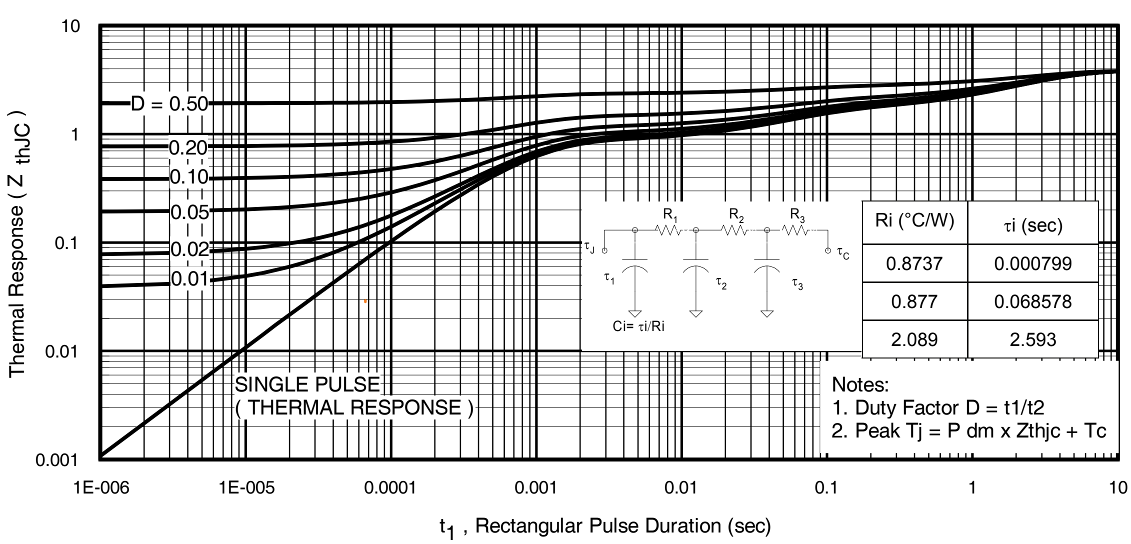


Fig 10. Threshold Voltage vs. Temperature



Ri (°C/W)	τi (sec)
0.8737	0.000799
0.877	0.068578
2.089	2.593

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

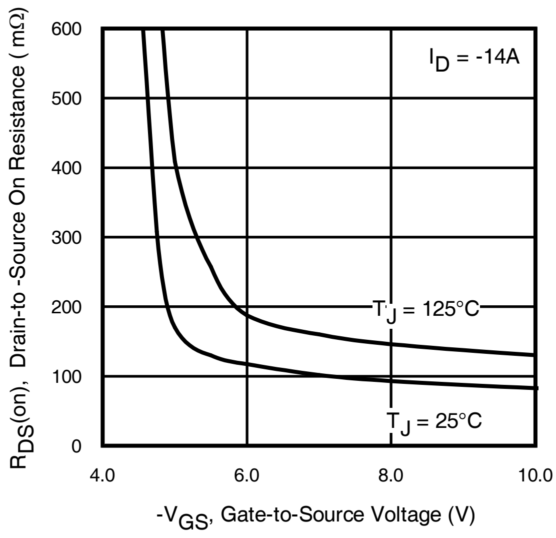


Fig 12. On-Resistance Vs. Gate Voltage

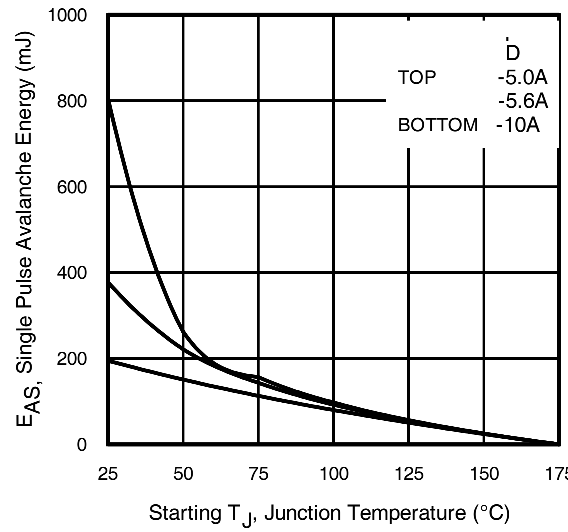


Fig 13. Maximum Avalanche Energy Vs. Drain Current

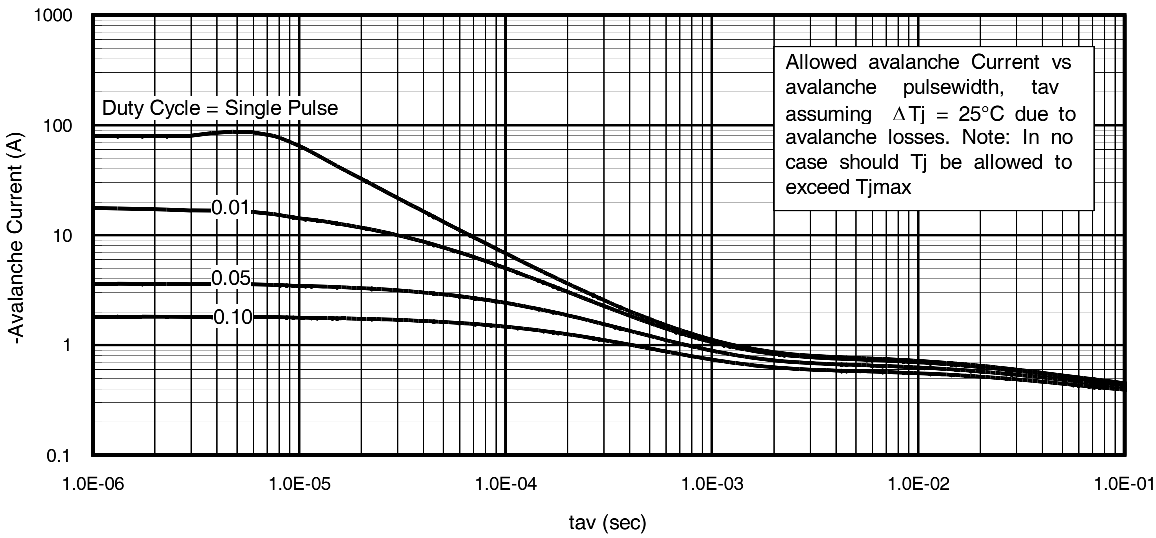


Fig 14. Typical Avalanche Current vs. Pulse width

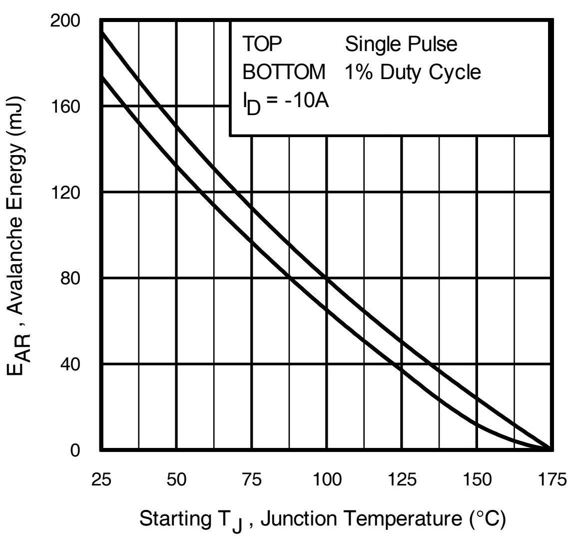


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

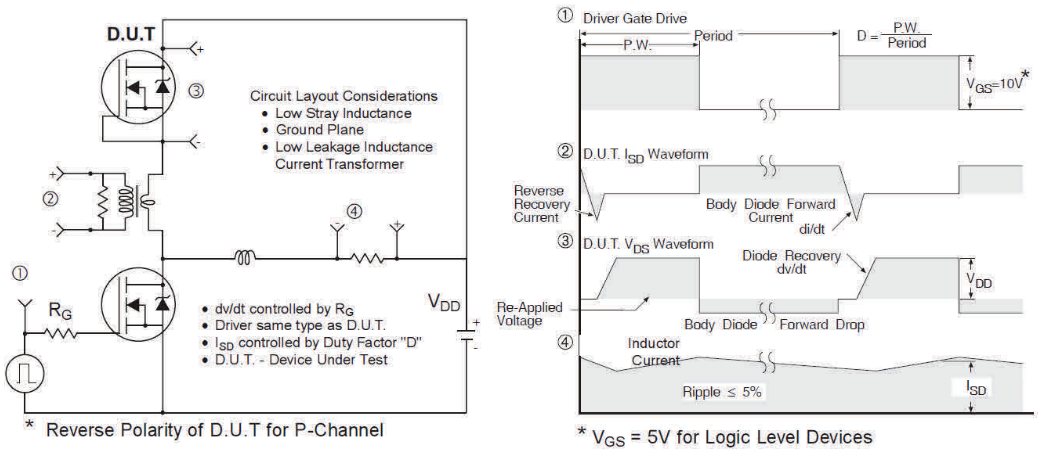


Fig 16. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs

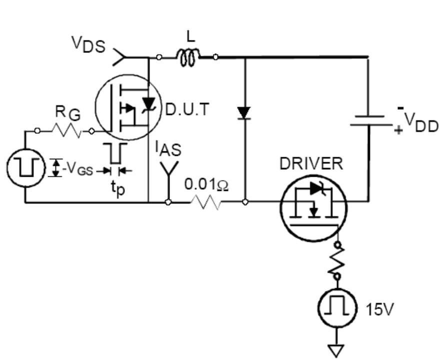


Fig 17a. Unclamped Inductive Test Circuit

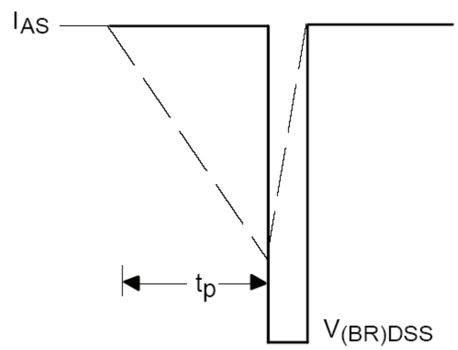


Fig 17b. Unclamped Inductive Waveforms

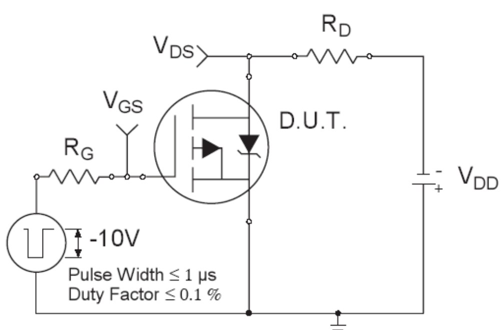


Fig 18a. Switching Time Test Circuit

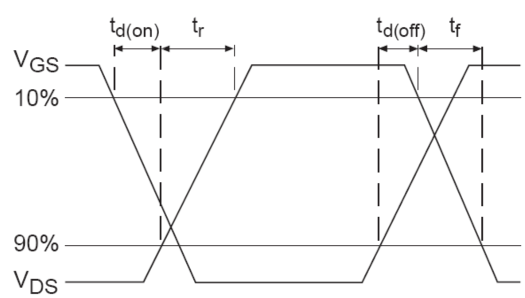


Fig 18b. Switching Time Waveforms

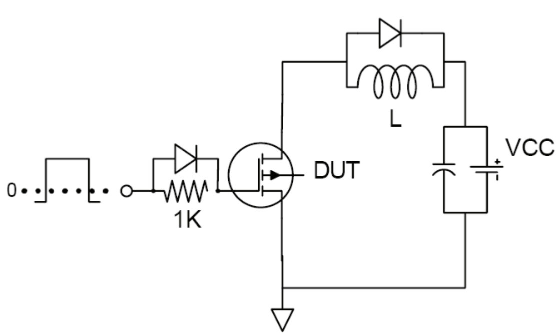


Fig 19a. Gate Charge Test Circuit

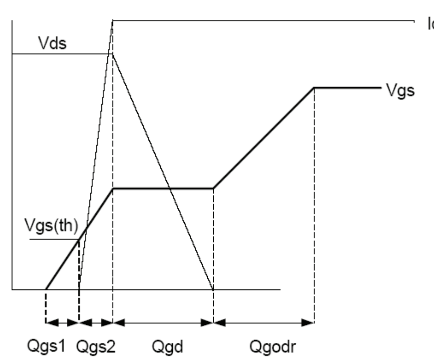
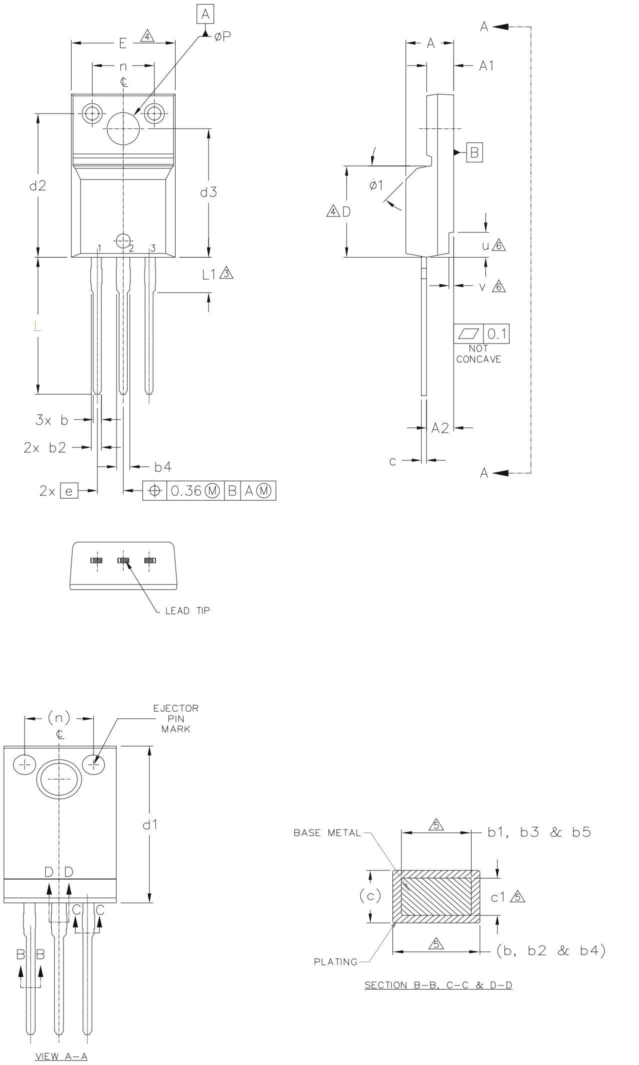


Fig 19b. Gate Charge Waveform

TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.

2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.

4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.

5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.

6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.

7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	5
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	5
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	5
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	4
e	2.54 BSC		.100 BSC		
L	13.21	13.72	.520	.540	
L1	3.10	3.68	.122	.145	3
n	6.05	6.60	.238	.260	
øP	3.05	3.45	.120	.136	
u	2.39	2.49	.094	.098	6
v	0.41	0.51	.016	.020	6
ø1	–	45°	–	45°	

LEAD ASSIGNMENTS

HEXFET

1.– GATE

2.– DRAIN

3.– SOURCE

IGBTs, CoPACK

1.– GATE

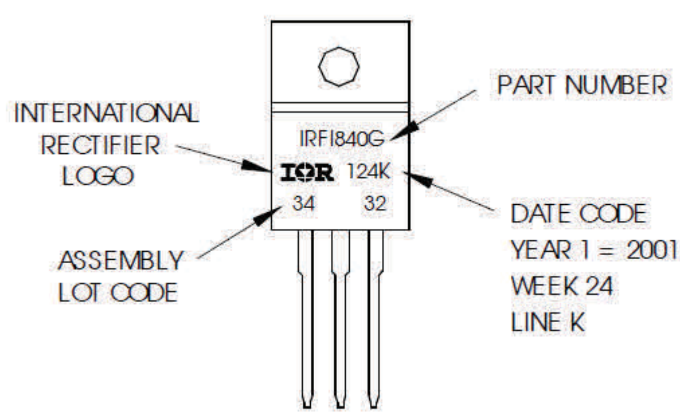
2.– COLLECTOR

3.– EMITTER

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24, 2001
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification information

Qualification level	Industrial (per JEDEC JESD47F †guidelines)	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A (per JEDEC J-STD-020D†)
RoHS compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
04/27/2017	• Changed datasheet with Infineon logo - all pages. • Corrected Package Outline on page 7. • Added disclaimer on last page.

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Document reference
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