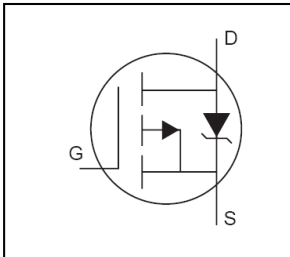


HEXFET® Power MOSFET

**Features**

- Advanced Process Technology
- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low R<sub>DS(ON)</sub> for Improved Efficiency
- Low Q<sub>G</sub> and Q<sub>sw</sub> for Better THD and Improved Efficiency
- Low Q<sub>rr</sub> for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability
- Lead-Free

Key Parameters		
V <sub>DS</sub>	-55	V
R <sub>DS(ON)</sub> typ. @ V <sub>GS</sub> = -10V	93	mΩ
R <sub>DS(ON)</sub> typ. @ V <sub>GS</sub> = -4.5V	150	mΩ
Q <sub>G</sub> typ.	31	nC
T <sub>J</sub> max	175	°C



G	D	S
Gate	Drain	Source

**Description**

This Digital Audio HEXFET® is specifically designed for Class-D audio amplifier applications. This MosFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MosFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MosFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLIB9343PbF	TO-220 Full-Pak	Tube	50	IRLIB9343PbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	-55	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ -10V	-14	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V	-10	
I <sub>DM</sub>	Pulsed Drain Current ①	-60	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	33	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation	20	
	Linear Derating Factor	0.26	W/°C
T <sub>J</sub>	Operating Junction and	-40 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb•in (1.1N•m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ④	—	3.84	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) ④	—	65	


**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-52	—	mV/°C	Reference to 25°C, I <sub>D</sub> = -1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	93	105	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -3.4A
			150	170		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2.7A
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	—	—	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Temp. Coefficient	—	-3.7	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-2.0	μA	V <sub>DS</sub> = -55V, V <sub>GS</sub> = 0V
				-25		V <sub>DS</sub> = -55V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V
g <sub>fs</sub>	Forward Trans conductance	5.3	—	—	S	V <sub>DS</sub> = -25V, I <sub>D</sub> = -14A
Q <sub>g</sub>	Total Gate Charge	—	31	47	nC	V <sub>DS</sub> = -44V
Q <sub>gs</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	7.1	—		I <sub>D</sub> = -14A,
Q <sub>gd</sub>	Gate-to-Drain Charge	—	8.5	—		V <sub>GS</sub> = -10V
Q <sub>godr</sub>	Gate Charge Overdrive	—	15	—		See Fig. 6 and 19.
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.5	—	ns	V <sub>DD</sub> = -28V, V <sub>GS</sub> = -10V ③
t <sub>r</sub>	Rise Time	—	24	—		I <sub>D</sub> = -14A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	21	—		R <sub>G</sub> = 2.5Ω
t <sub>f</sub>	Fall Time	—	9.5	—		
C <sub>iss</sub>	Input Capacitance	—	660	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	160	—		V <sub>DS</sub> = -50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	72	—		f = 1.0MHz, See Fig. 5
C <sub>oss eff.</sub>	Effective Output Capacitance	—	280	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to -44V
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		

**Avalanche Characteristics**

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	190	mJ
I <sub>AR</sub>	Avalanche Current ⑤	See Fig. 14, 15, 17a, 17b		A
E <sub>AR</sub>	Repetitive Avalanche Energy ⑤			mJ

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub> @ T <sub>C</sub> = 25°C	Continuous Source Current (Body Diode)	—	—	-14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-60		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -14A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	57	86	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -14A
Q <sub>rr</sub>	Reverse Recovery Charge	—	120	180	nC	di/dt = 100A/μs ③

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting T<sub>J</sub> = 25°C, L = 3.89mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -10A.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.
- ⑤ Limited by T<sub>Jmax</sub>. See Figs. 14, 15, 17a, 17b for repetitive avalanche information

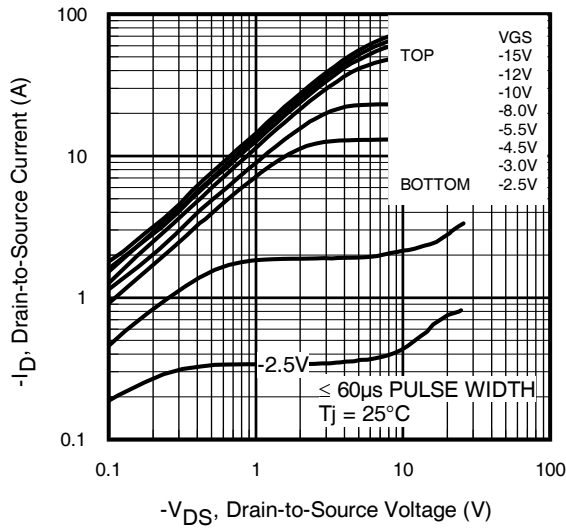


Fig. 1 Typical Output Characteristics

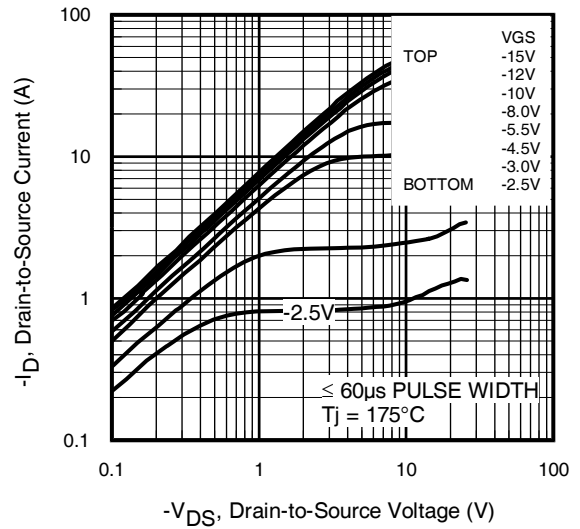


Fig. 2 Typical Output Characteristics

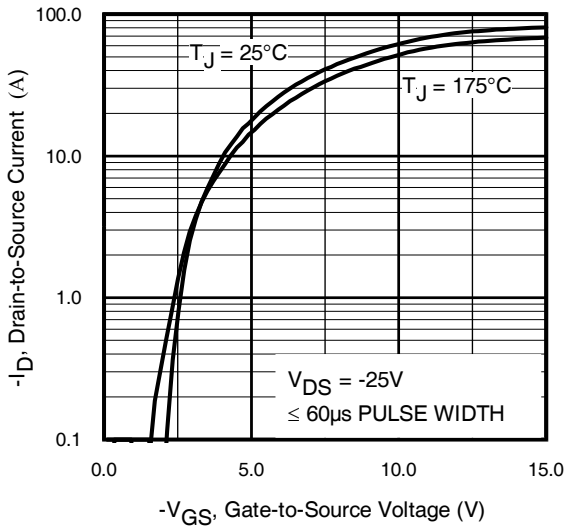


Fig. 3 Typical Transfer Characteristics

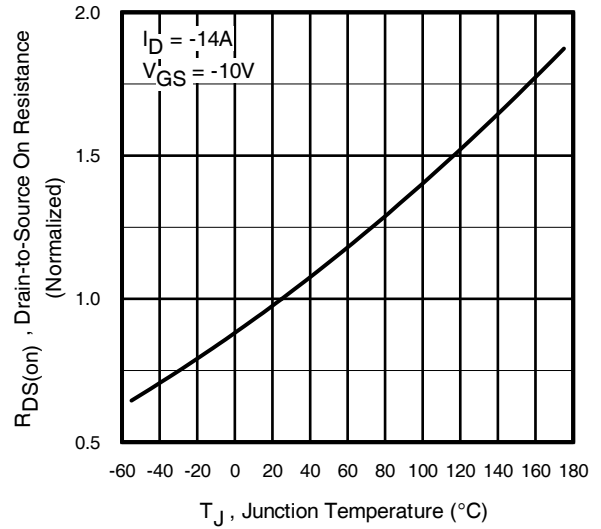


Fig. 4 Normalized On-Resistance vs. Temperature

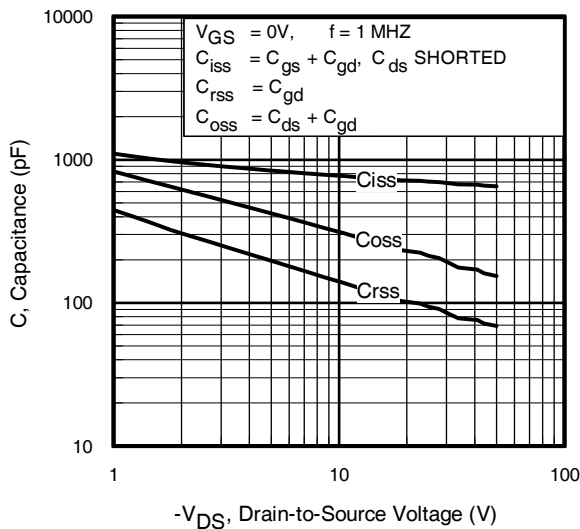


Fig. 5. Typical Capacitance vs. Drain-to-Source Voltage

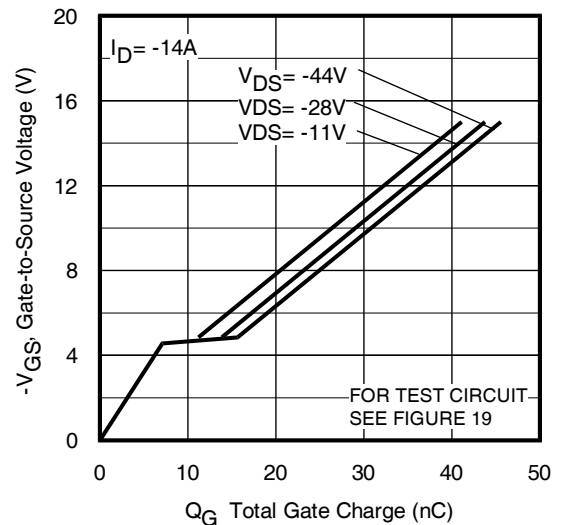
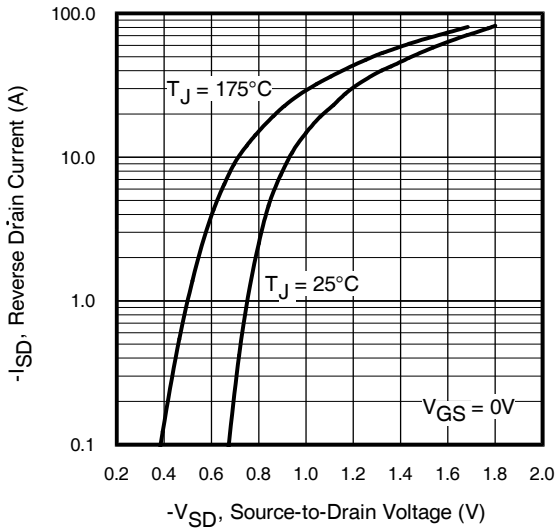
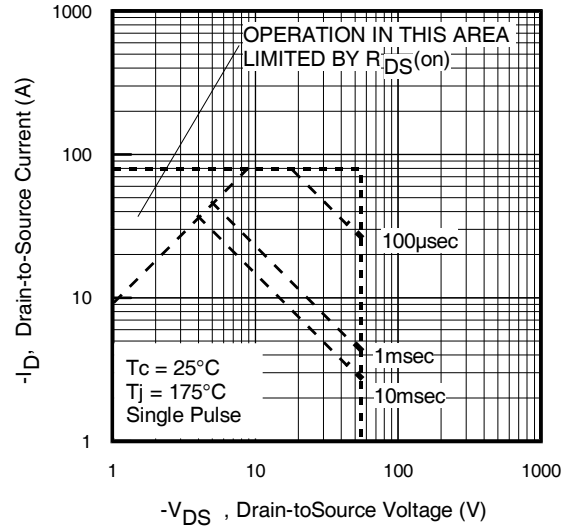
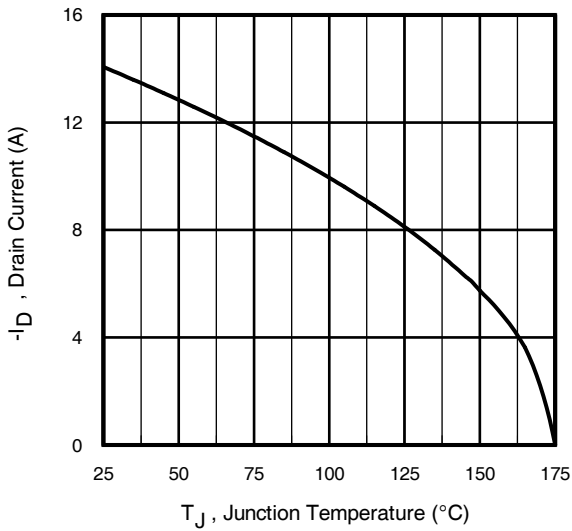
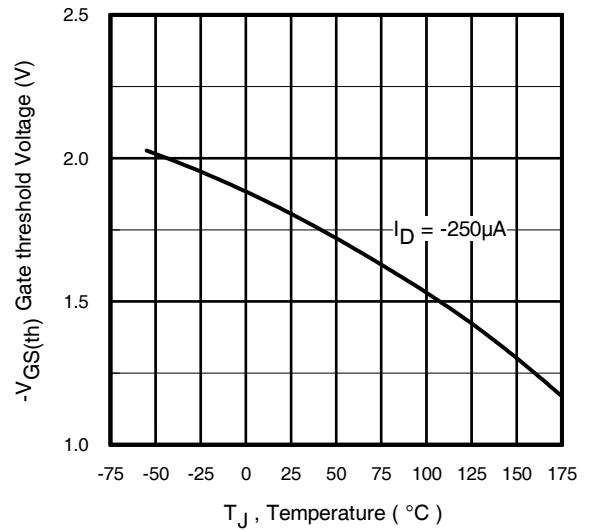
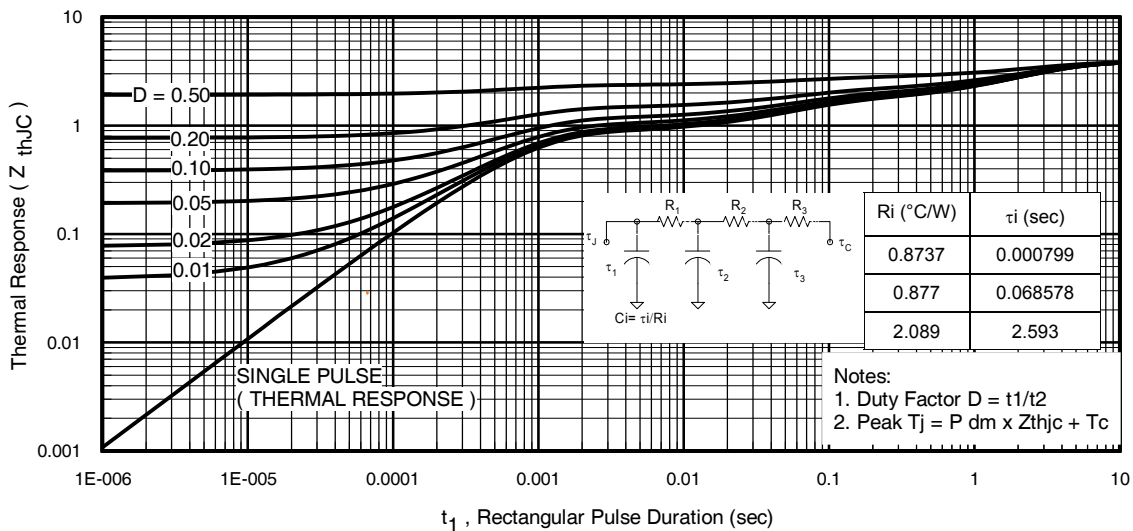
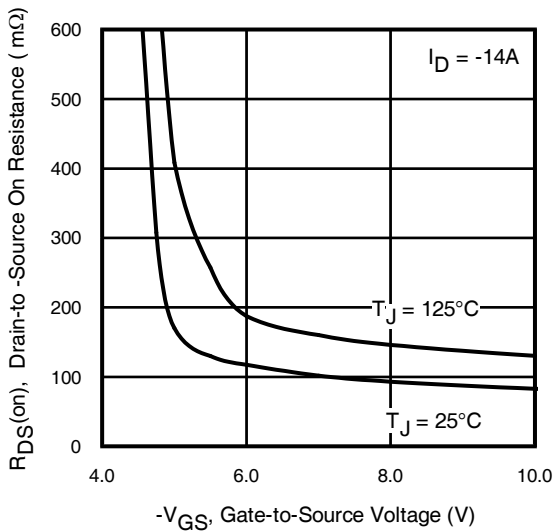
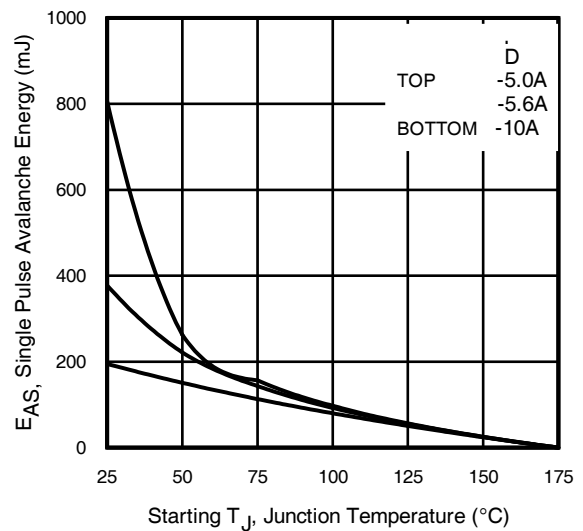
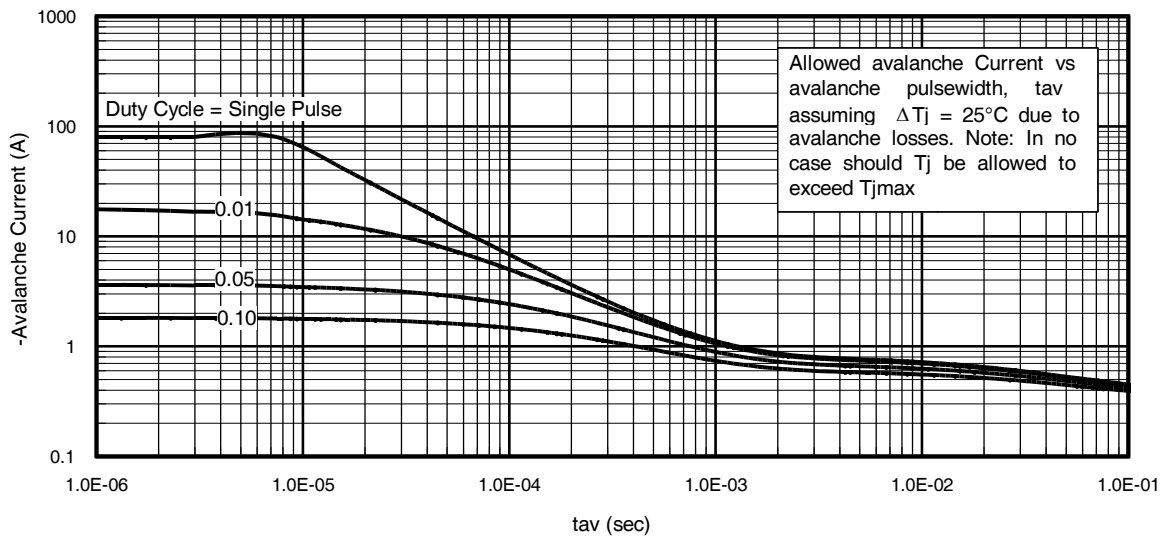
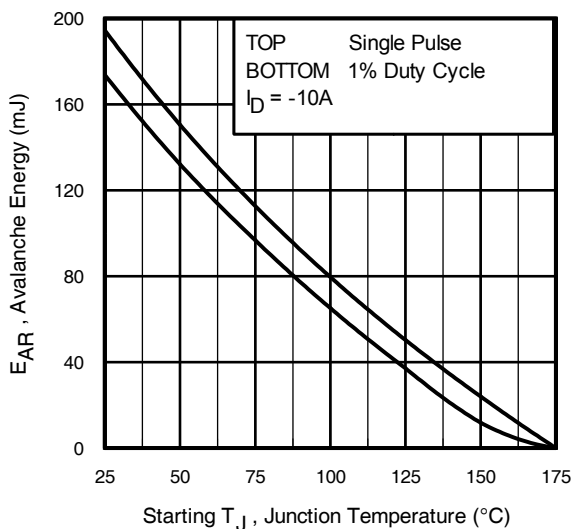


Fig. 6. Typical Gate Charge vs. Gate-to-Source Voltage


**Fig. 7 Typical Source-to-Drain Diode**

**Fig. 8. Maximum Safe Operating Area**

**Fig 9. Maximum Drain Current vs. Case Temperature**

**Fig 10. Threshold Voltage vs. Temperature**

**Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

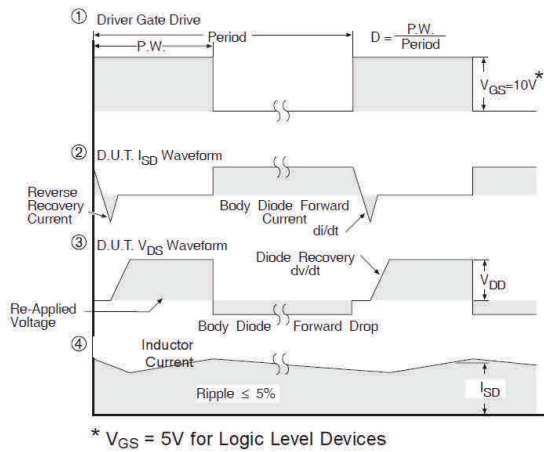
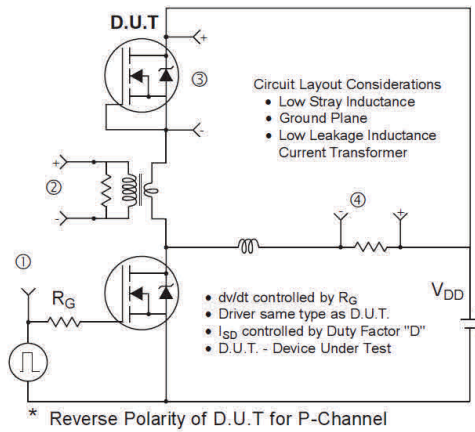
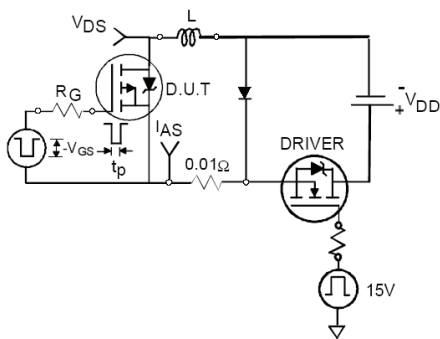
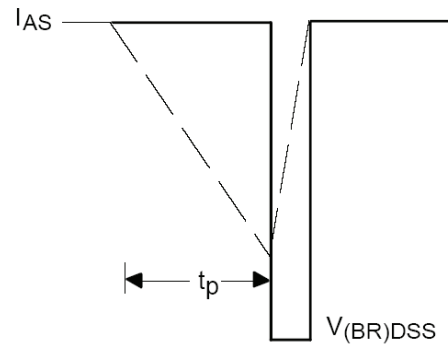
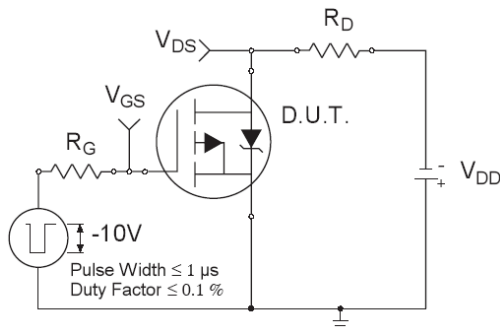
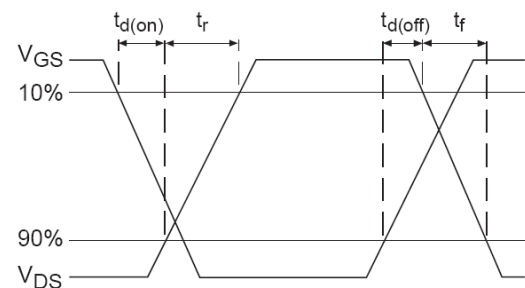
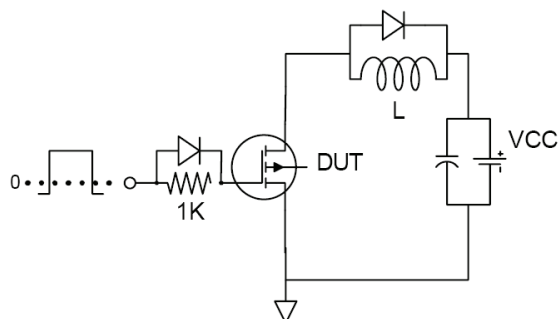
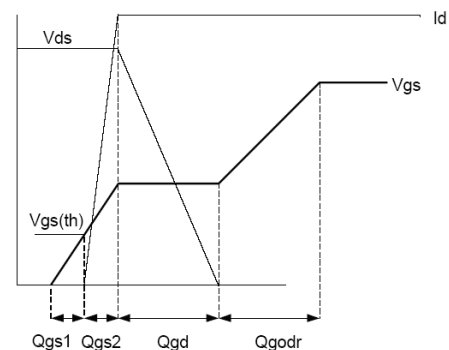

**Fig 12. On-Resistance Vs. Gate Voltage**

**Fig 13. Maximum Avalanche Energy Vs. Drain Current**

**Fig 14. Typical Avalanche Current vs. Pulse width**

**Fig 15. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at [www.inf.com](http://www.inf.com))**

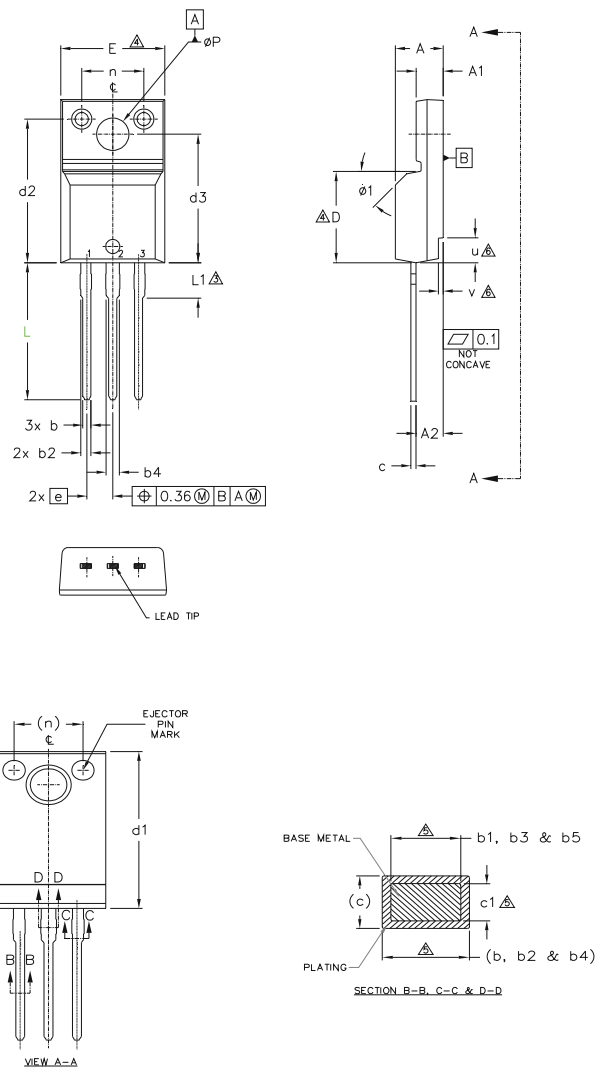
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig 16. Peak Diode Recovery  $dv/dt$  Test Circuit for P-Channel HEXFET® Power MOSFETs**

**Fig 17a. Unclamped Inductive Test Circuit**

**Fig 17b. Unclamped Inductive Waveforms**

**Fig 18a. Switching Time Test Circuit**

**Fig 18b. Switching Time Waveforms**

**Fig 19a. Gate Charge Test Circuit**

**Fig 19b. Gate Charge Waveform**

**TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

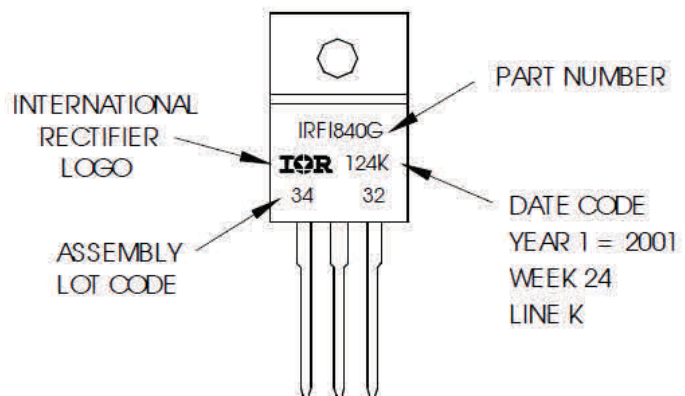
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	.180	.190	LEAD ASSIGNMENTS  HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE	
A1	2.57	2.82	.101	.111		
A2	2.51	2.92	.099	.115		
b	0.61	0.94	.024	.037		
b1	0.61	0.89	.024	.035		
b2	0.76	1.27	.030	.050		
b3	0.76	1.22	.030	.048		
b4	1.02	1.52	.040	.060		
b5	1.02	1.47	.040	.058		
c	0.33	0.63	.013	.025		
c1	0.33	0.58	.013	.023	5	
D	8.66	9.80	.341	.386	4	
d1	15.80	16.13	.622	.635	IGBTs, CoPACK 1.- GATE 2.- COLLECTOR 3.- EMITTER	
d2	13.97	14.22	.550	.560		
d3	12.29	12.93	.484	.509		
E	9.63	10.74	.379	.423		
e	2.54	BSC	.100	BSC		
L	13.21	13.72	.520	.540		
L1	3.10	3.68	.122	.145		3
n	6.05	6.60	.238	.260		
phi P	3.05	3.45	.120	.136		
u	2.39	2.49	.094	.098		
v	0.41	0.51	.016	.020	6	
phi 1	-	45°	-	45°	6	

**TO-220 Full-Pak Part Marking Information**

EXAMPLE: THIS IS AN IRF1840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24, 2001  
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**Qualification information**

Qualification level	Industrial	
	(per JEDEC JESD47F † guidelines )	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A
		(per JEDEC J-STD-020D †)
RoHS compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
04/27/2017	<ul style="list-style-type: none"> <li>• Changed datasheet with Infineon logo - all pages.</li> <li>• Corrected Package Outline on page 7.</li> <li>• Added disclaimer on last page.</li> </ul>

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[SSM6P54TU,LF](#) [SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)