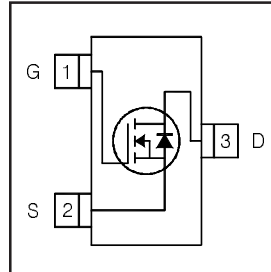


IRLML6346TRPbF

HEXFET® Power MOSFET

V_{DS}	30	V
V_{GS Max}	± 12	V
R_{DS(on) max} (@ V _{GS} = 4.5V)	63	mΩ
R_{DS(on) max} (@ V _{GS} = 2.5V)	80	mΩ



Application(s)

- Load/ System Switch

Features and Benefits

Features

Industry-standard SOT-23 Package
RoHS compliant containing no lead, no bromide and no halogen
MSL1, Consumer Qualification

results in



Benefits

Multi-vendor compatibility
Environmentally friendly
Increased Reliability

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	30	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	3.4	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	2.7	
I _{DM}	Pulsed Drain Current	17	
P _D @ T _A = 25°C	Maximum Power Dissipation	1.3	W
P _D @ T _A = 70°C	Maximum Power Dissipation	0.8	
	Linear Derating Factor	0.01	W/°C
V _{GS}	Gate-to-Source Voltage	± 12	V
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJA}	Junction-to-Ambient ③	—	100	°C/W
R _{θJA}	Junction-to-Ambient (t<10s) ④	—	99	

ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

Notes ① through ④ are on page 10

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Electric Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	46	63	mΩ	V _{GS} = 4.5V, I _D = 3.4A ②
		—	59	80		V _{GS} = 2.5V, I _D = 2.7A ②
V _{GS(th)}	Gate Threshold Voltage	0.5	0.8	1.1	V	V _{DS} = V _{GS} , I _D = 10μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -12V
R _G	Internal Gate Resistance	—	3.9	—	Ω	
g _{fs}	Forward Transconductance	9.5	—	—	S	V _{DS} = 10V, I _D = 3.4A
Q _g	Total Gate Charge	—	2.9	—	nC	I _D = 3.4A
Q _{gs}	Gate-to-Source Charge	—	0.13	—		V _{DS} = 15V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	1.1	—		V _{GS} = 4.5V ②
t _{d(on)}	Turn-On Delay Time	—	3.3	—	ns	V _{DD} = 15V ②
t _r	Rise Time	—	4.0	—		I _D = 1.0A
t _{d(off)}	Turn-Off Delay Time	—	12	—		R _G = 6.8Ω
t _f	Fall Time	—	4.9	—		V _{GS} = 4.5V
C _{iss}	Input Capacitance	—	270	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	32	—		V _{DS} = 24V
C _{rss}	Reverse Transfer Capacitance	—	21	—		f = 1.0MHz

Source - Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	17		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 3.4A, V _{GS} = 0V ②
t _{rr}	Reverse Recovery Time	—	8.8	13	ns	T _J = 25°C, V _R = 24V, I _F = 1.3A
Q _{rr}	Reverse Recovery Charge	—	2.7	4.1	nC	di/dt = 100A/μs ②

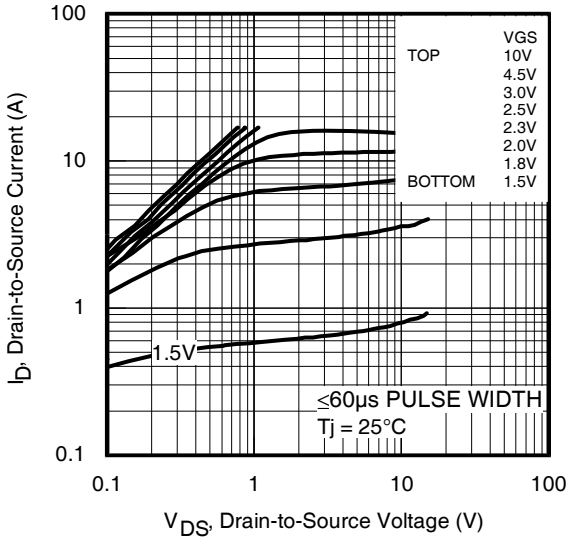


Fig 1. Typical Output Characteristics

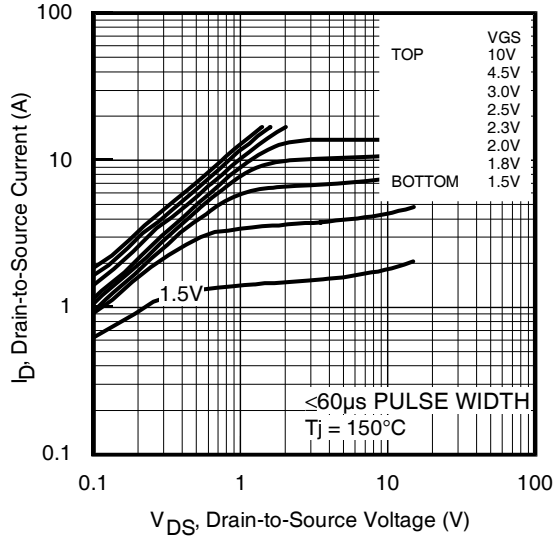


Fig 2. Typical Output Characteristics

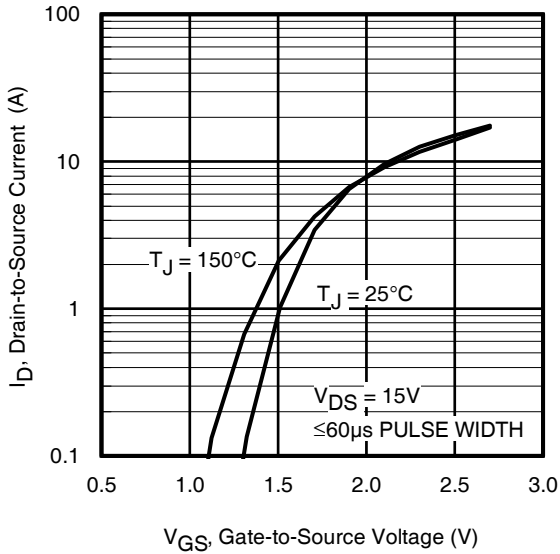


Fig 3. Typical Transfer Characteristics

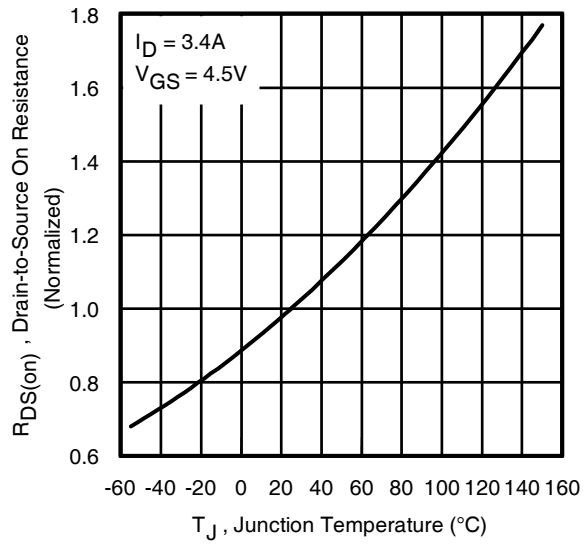


Fig 4. Normalized On-Resistance vs. Temperature

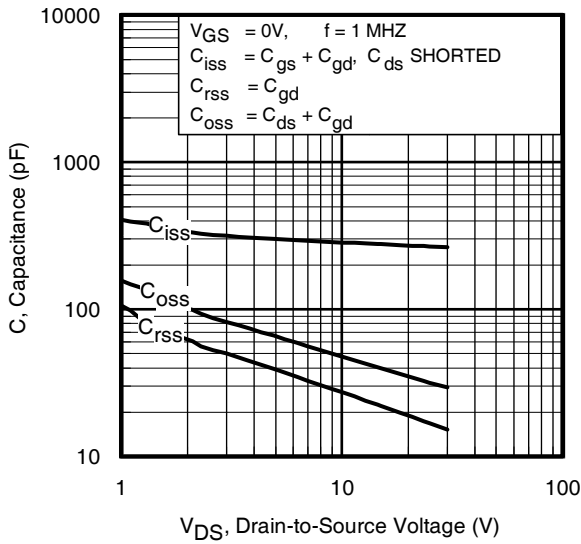


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

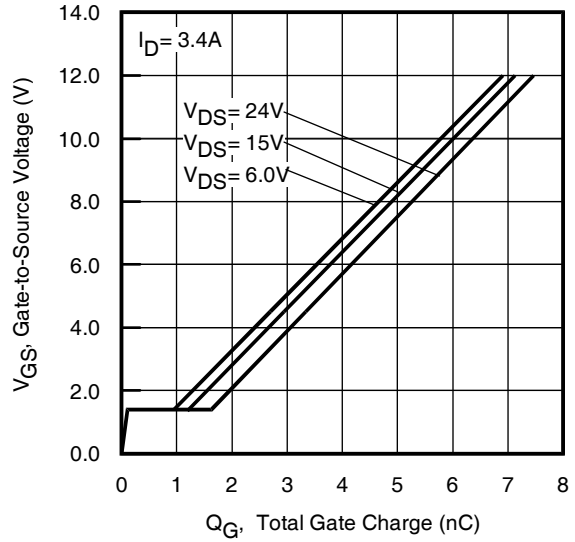


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

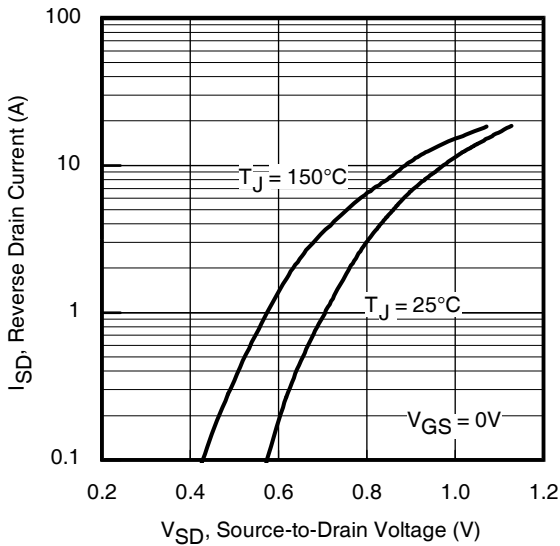


Fig 7. Typical Source-Drain Diode Forward Voltage

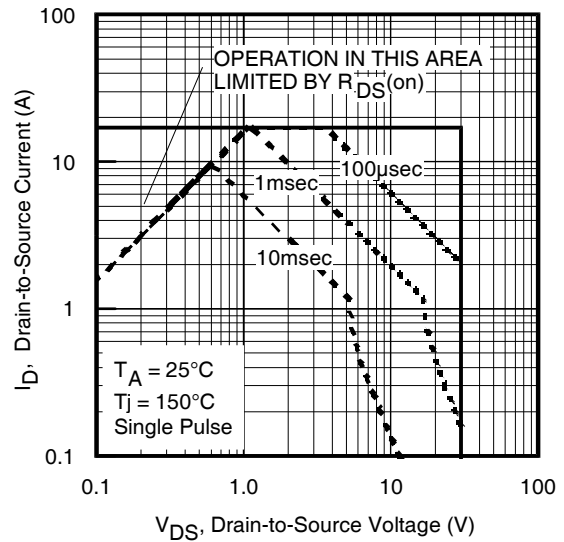


Fig 8. Maximum Safe Operating Area

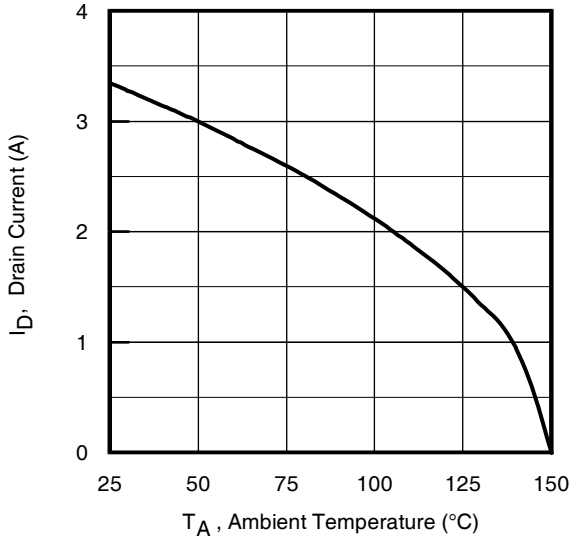


Fig 9. Maximum Drain Current vs. Ambient Temperature

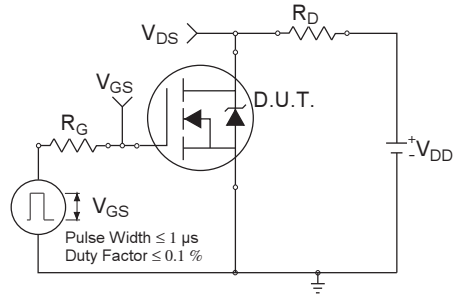


Fig 10a. Switching Time Test Circuit

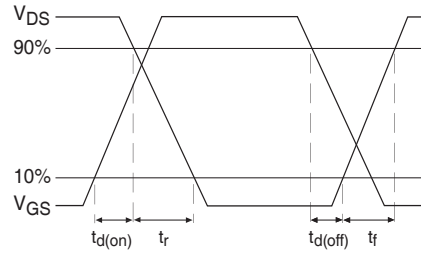


Fig 10b. Switching Time Waveforms

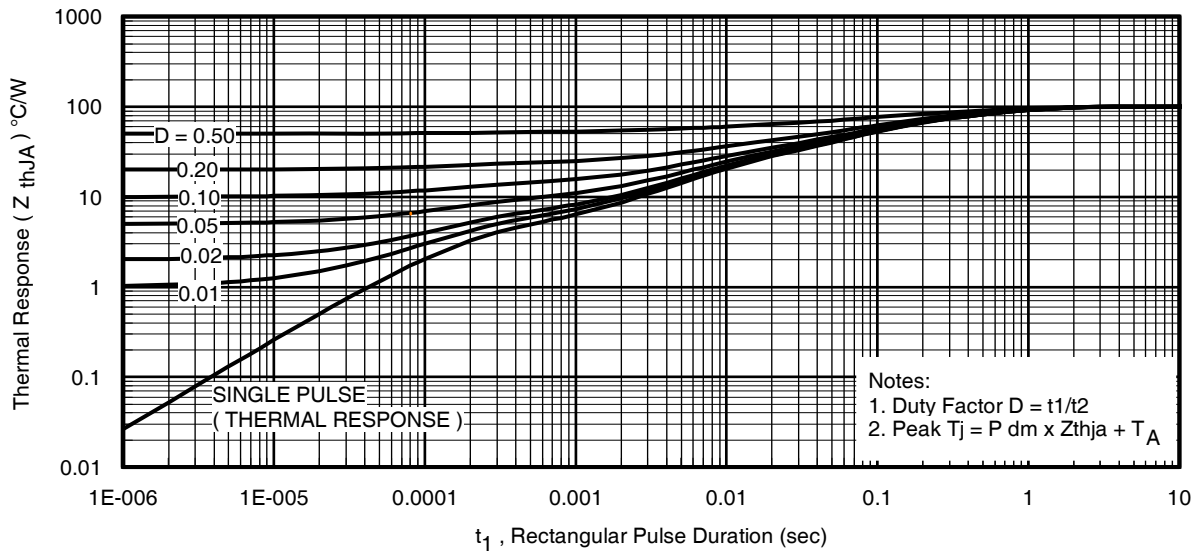


Fig 11. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

IRLML6346TRPbF

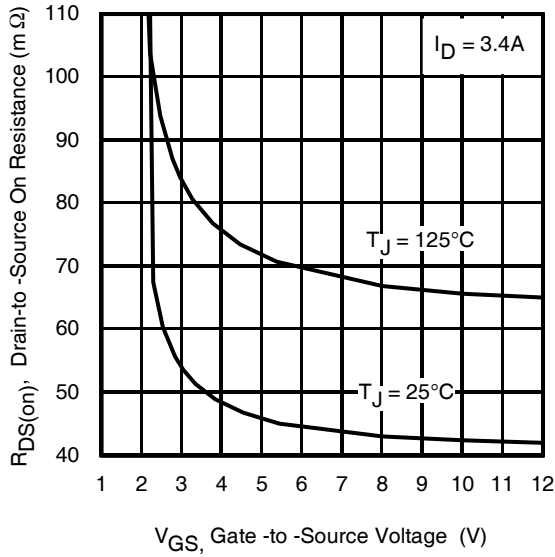


Fig 12. Typical On-Resistance vs. Gate Voltage

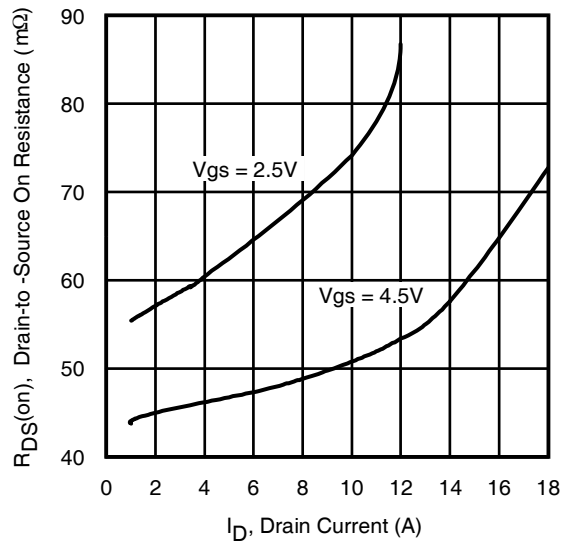


Fig 13. Typical On-Resistance vs. Drain Current

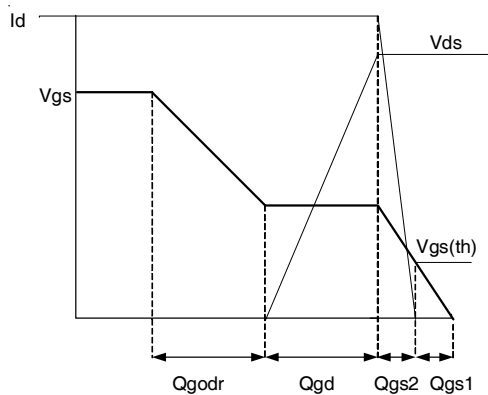


Fig 14a. Basic Gate Charge Waveform

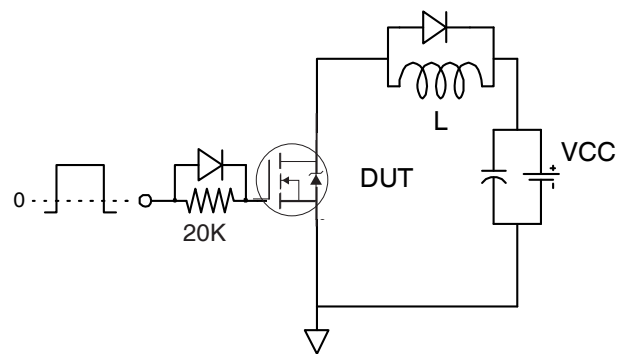


Fig 14b. Gate Charge Test Circuit

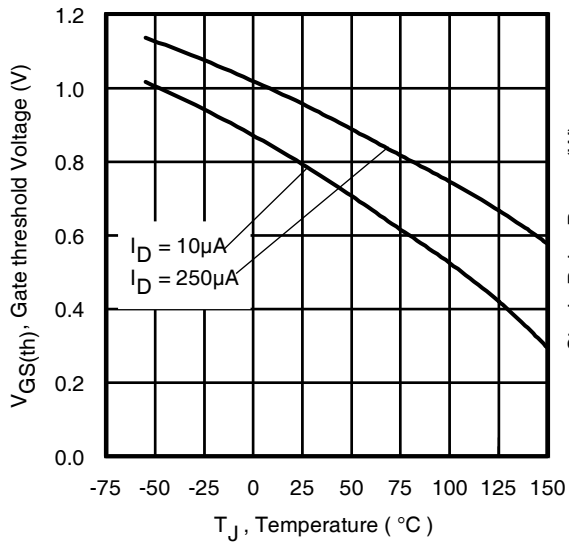


Fig 15. Typical Threshold Voltage vs. Junction Temperature

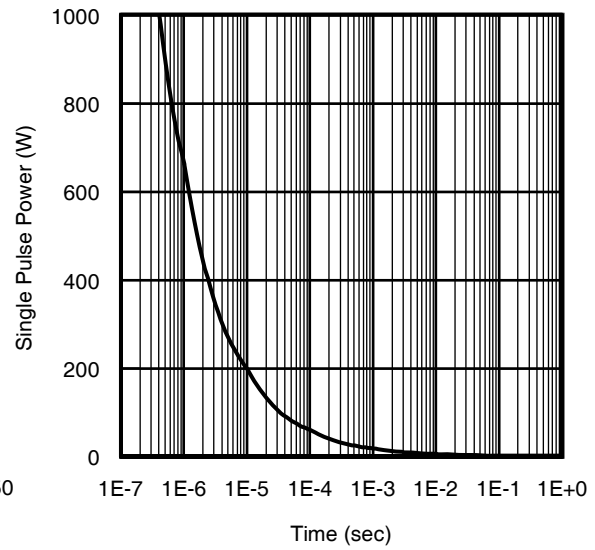


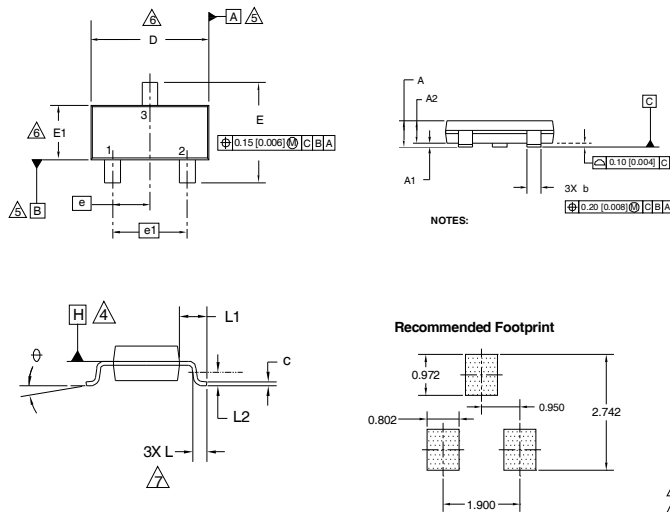
Fig 16. Typical Power vs. Time

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Micro3™(SOT-23) Package Outline

Dimensions are shown in millimeters (inches)

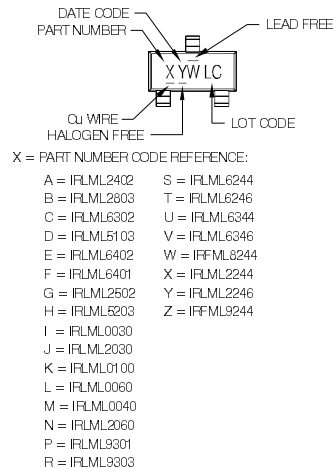


DIMENSIONS				
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.89	1.12	0.035	0.044
A1	0.01	0.10	0.0004	0.004
A2	0.88	1.02	0.035	0.040
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E1	1.20	1.40	0.047	0.055
e	0.95	BSC	0.037	BSC
e1	1.90	BSC	0.075	BSC
L	0.40	0.60	0.016	0.024
L1	0.54	REF	0.021	REF
L2	0.25	BSC	0.010	BSC
⌀	0	8	0	8

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
3. CONTROLLING DIMENSION: MILLIMETER
4. DATUM PLANE H IS LOCATED AT THE MOLD PARTING LINE
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H. DIMENSIONS DOES NOT INCLUDE MOLD PROTRUSIONS OR INTERLEAD FLASH. MOLD PROTRUSIONS OR INTERLEAD FLASH SHALL NOT EXCEED 0.25 MM (0.010 INCH) PER SIDE
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-236 AB.

Micro3™(SOT-23) Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001



Note: A line above the work week (as shown here) indicates Lead-Free.

DATE CODE MARKING INSTRUCTIONS

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2011	2001	1	01
2012	2002	2	02
2013	2003	3	03
2014	2004	4	04
2015	2005	5	
2016	2006	6	
2017	2007	7	
2018	2008	8	
2019	2009	9	
2020	2010	0	24
			25
			26
			Z

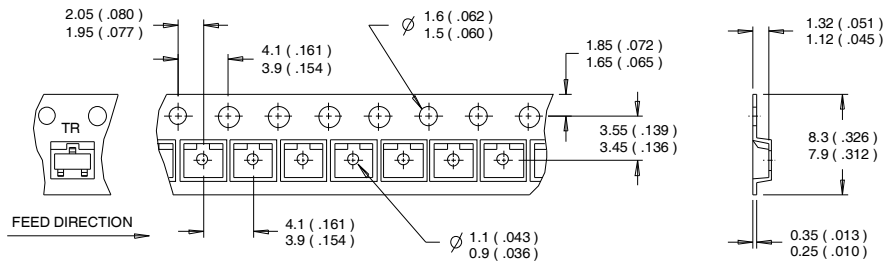
WW = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2011	2001	A	27
2012	2002	B	28
2013	2003	C	29
2014	2004	D	30
2015	2005	E	
2016	2006	F	
2017	2007	G	
2018	2008	H	
2019	2009	J	
2020	2010	K	50
			51
			52
			Z

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Micro3™(SOT-23) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
 1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

IRLML6346TRPbF

International
IOR Rectifier

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLML6346TRPbF	Micro3™(SOT-23)	Tape and Reel	3000	

Qualification information[†]

Qualification level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)		
Moisture Sensitivity Level	Micro3™(SOT-23)	MSL1 (per IPC/JEDEC J-STD-020D ^{†††})	
RoHS compliant	Yes		

† Qualification standards can be found at International Rectifier's web site
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.
Please contact your International Rectifier sales representative for further information:
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width ≤ 400µs; duty cycle ≤ 2%.
- ③ Surface mounted on 1 in square Cu board.
- ④ Refer to [application note #AN-994](#).

Data and specifications subject to change without notice.

International
IOR Rectifier

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#)