International IOR Rectifier

May 14, 2012

IRS2001MPBF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +200V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Leadfree, RoHS compliant

Product Summary

Topology	General Driver
V_{OFFSET}	≤ 200V
V_{OUT}	10V – 20V
I_{o+} & I_{o-} (typical)	290mA & 600mA
t_{on} & t_{off} (typical)	160ns & 150ns
Delay Matching (Max.)	50ns

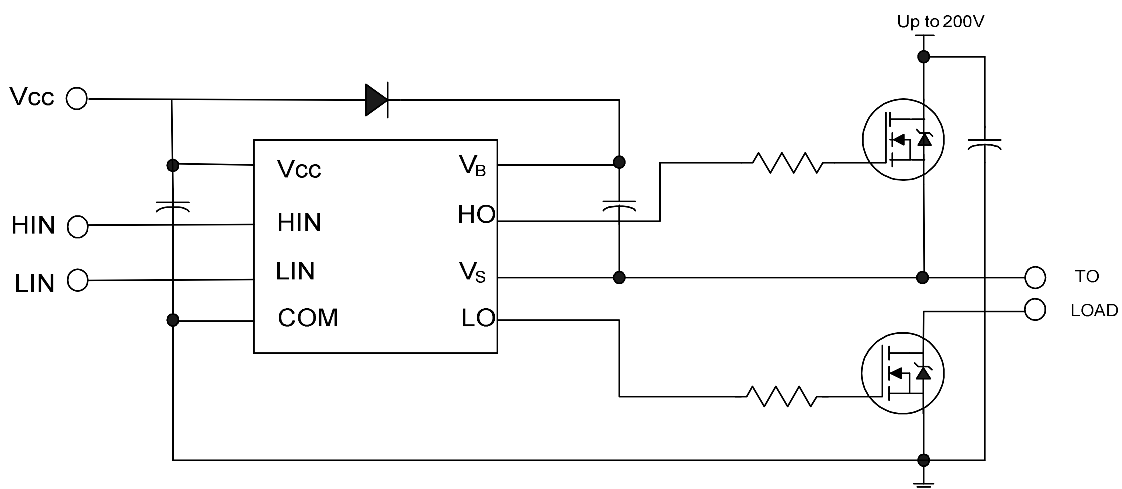
Description

The IRS2001 is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200V.

Package Options

MLPQ4x4 - 16 Leads
(Without 2 leads)

Typical Connection



(Refer to Lead Assignments for correct pin configuration) This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

* Qualification standards can be found on IR’s web site www.irf.com

Qualification Information†

Qualification Level		Industrial†† (per JEDEC JESD 47)	
		Comments: This IC has passed JEDEC’s Industrial qualification. IR’s Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		MLPQ4x4 14L	MSL2††† (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (+/-200V) (per JEDEC standard JESD22-A115A)	
	Human Body Model	Class 1C (+/-2000V) (per JEDEC standard JESD22-A114F)	
	Charged Device Model	Class III (+/-1000V) (per JEDEC standard JESD22-C101D)	
IC Latch-Up Test		Class II, Level B (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier’s web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating absolute voltage	-0.3	225	V
V_S	High side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	—	2.08	W
Rth_{JA}	Thermal resistance, junction to ambient	—	36	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	†	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Logic operational for V_S of -5V to +200V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

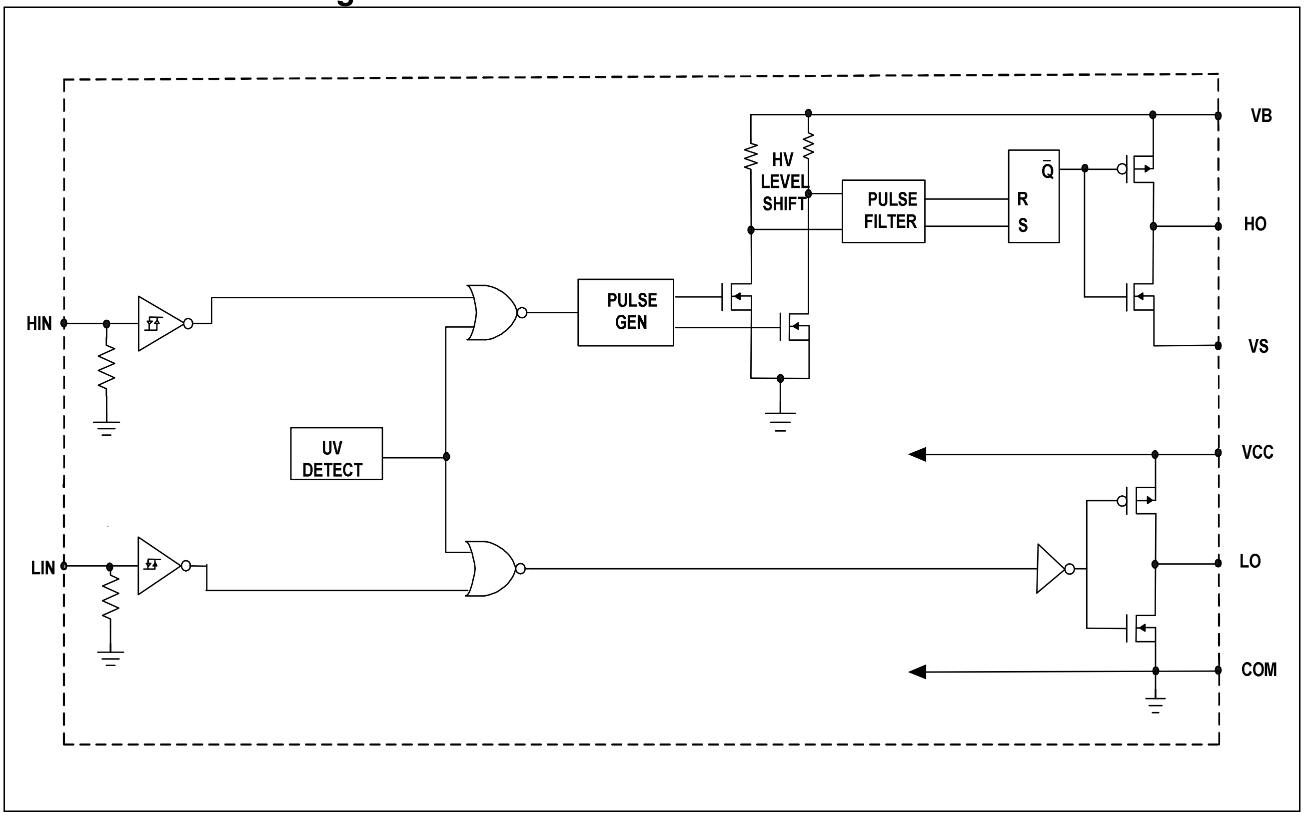
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	160	220	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 200V
t_r	Turn-on rise time	—	70	170		
t_f	Turn-off fall time	—	35	90		
MT	Delay Matching, HS & LS turn-on/off	—	—	50		

Static Electrical Characteristics

V_{BIAS}(V_{CC}, V_{BS})= 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 200V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		
I_{IN+}	Logic "1" input bias current	—	3	10		V_{IN} = 5V
I_{IN-}	Logic "0" input bias current	—	—	5		V_{IN} = 0V
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9.0		
I_{O+}	Output high short circuit pulsed current	200	290	—	mA	V_O = 0V, V_{IN} = Logic "1" PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	420	600	—		V_O = 15V, V_{IN} = Logic "0" PW ≤ 10 µs

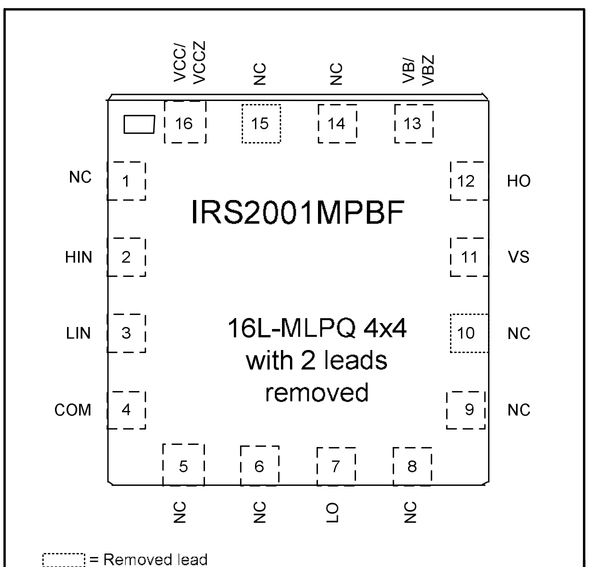
Functional Block Diagram



Lead Definitions

PIN	Symbol	Description
1	NC	No connection
2	HIN	Logic input for high side gate driver output (HO), in phase
3	LIN	Logic input for low side driver output (LO), in phase
4	COM	Low side return
5	NC	No Connection
6	NC	No Connection
7	LO	Low side gate drive output
8	NC	No Connection
9	NC	No Connection
10	NC	No Connection (pin removed)
11	V_S	High side floating supply return
12	HO	High side gate drive output
13	V_B/V_{BZ}	High side floating supply
14	NC	No Connection
15	NC	No Connection (pin removed)
16	V_{CC}/V_{CCZ}	Low side and logic fixed supply

Lead Assignments



IRS2001MPbF

Application Information and Additional Details

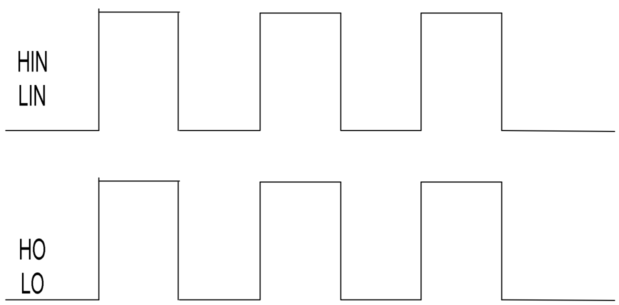


Figure 1: Input/Output Timing Diagram

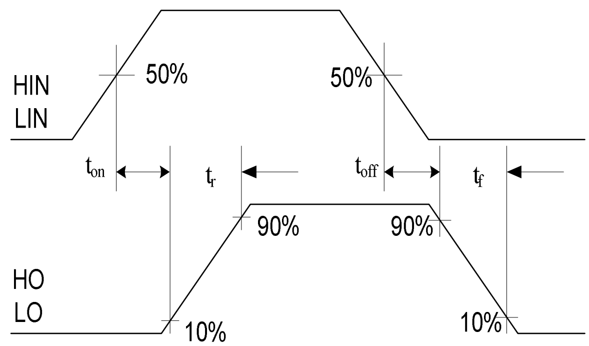


Figure 2: Switching Time Waveform Definitions

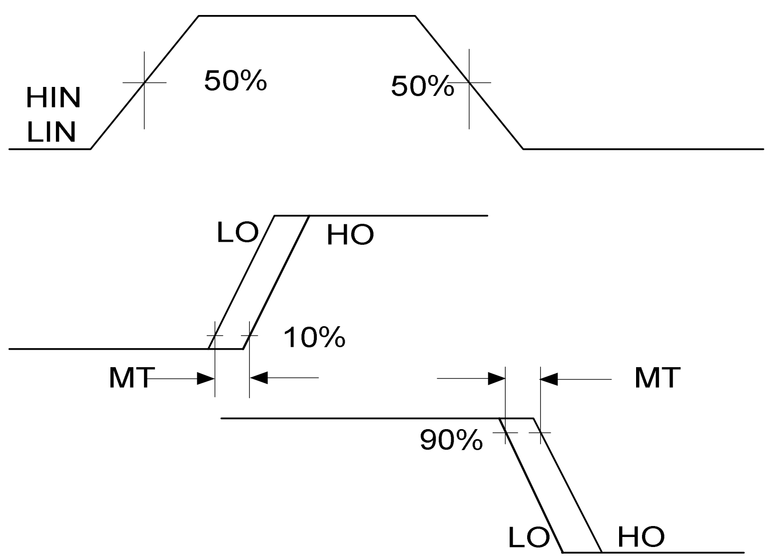


Figure 3: Delay Matching Waveform Definitions

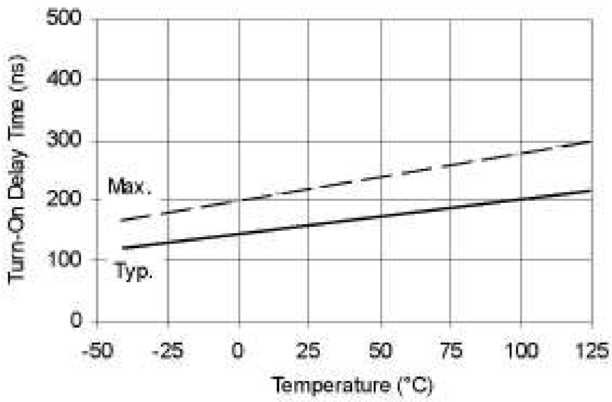


Figure 6A. Turn-On Time vs. Temperature

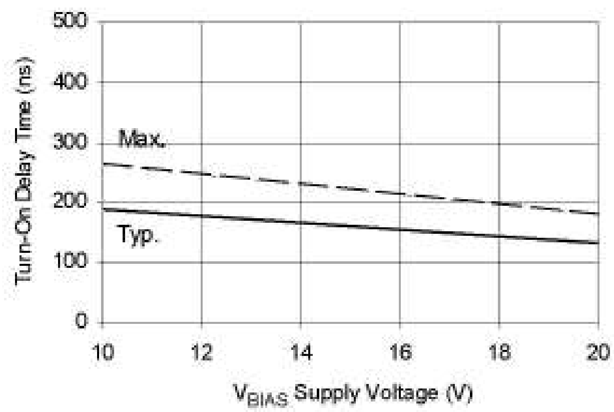


Figure 6B. Turn-On Time vs. Supply Voltage

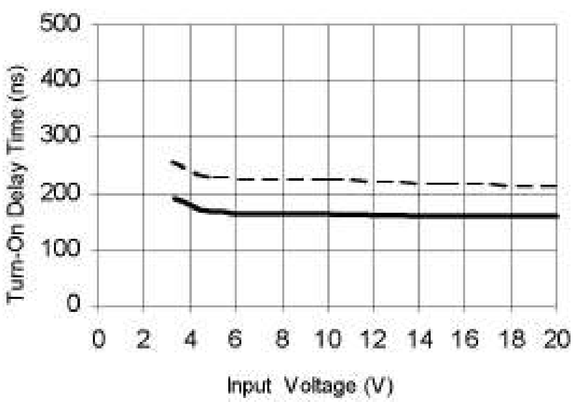


Figure 6C. Turn-On Time vs. Input Voltage

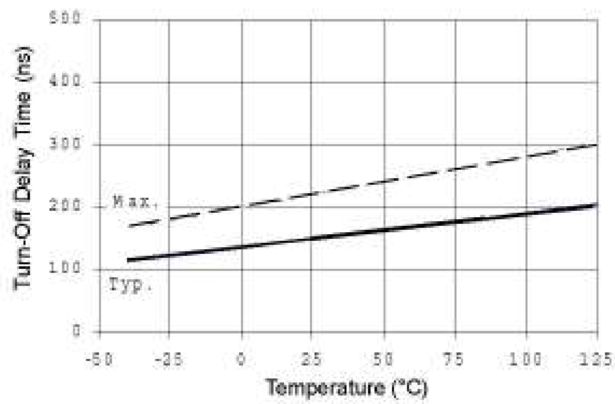


Figure 7A. Turn-Off Time vs. Temperature

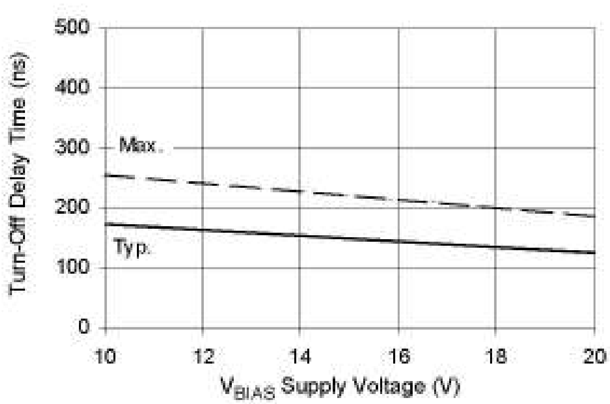


Figure 7B. Turn-Off Time vs. Supply Voltage

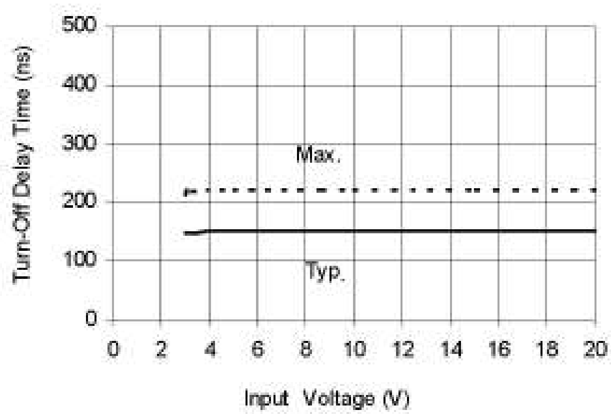


Figure 7C. Turn-Off Time vs. Input Voltage

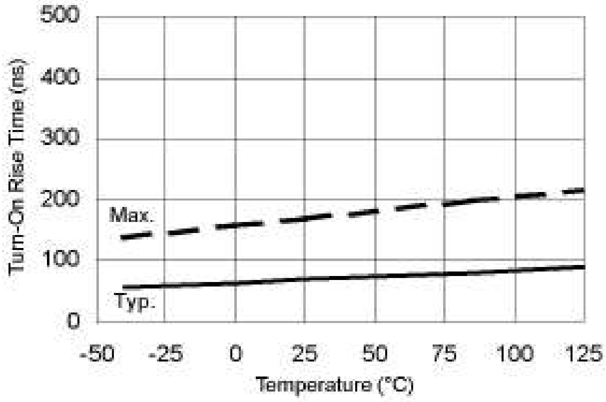


Figure 9A. Turn-On Rise Time vs. Temperature

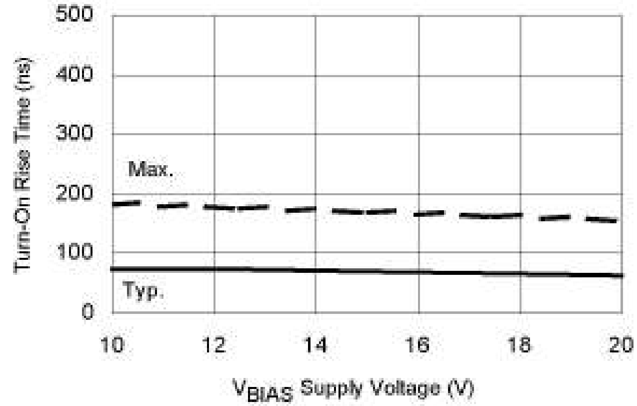


Figure 9B. Turn-On Rise Time vs. Voltage

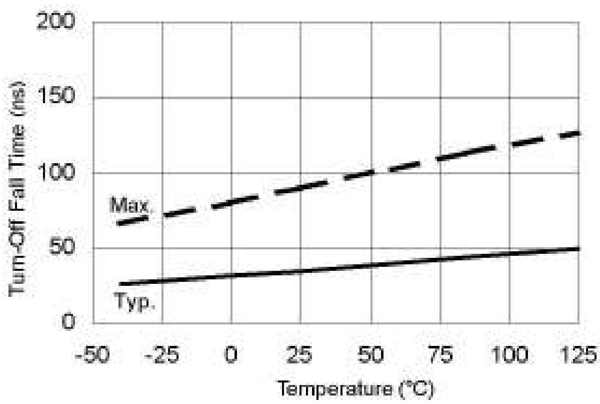


Figure 10A. Turn-Off Fall Time vs. Temperature

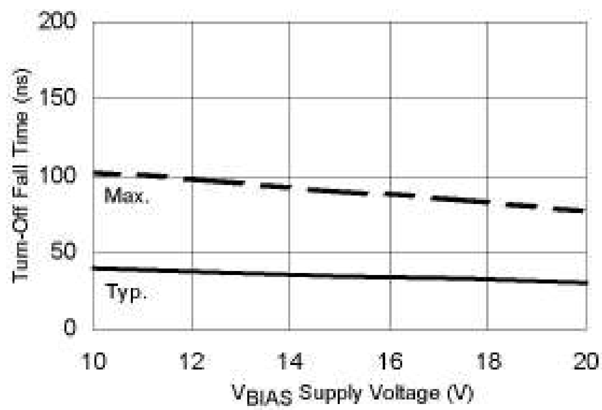


Figure 10B. Turn-Off Fall Time vs. Voltage

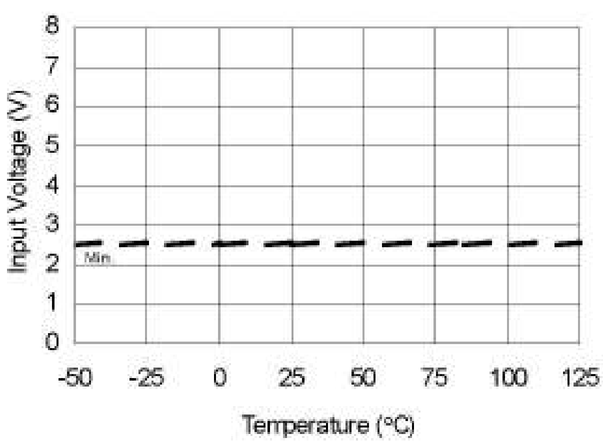


Figure 12A. Logic "1" Input Voltage vs. Temperature

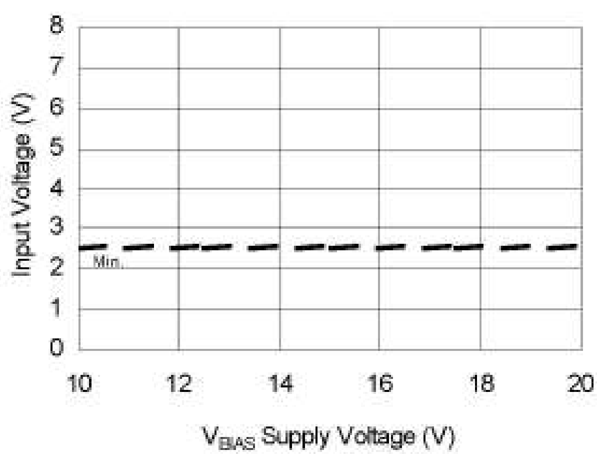


Figure 12B. Logic "1" Input Voltage vs. Voltage

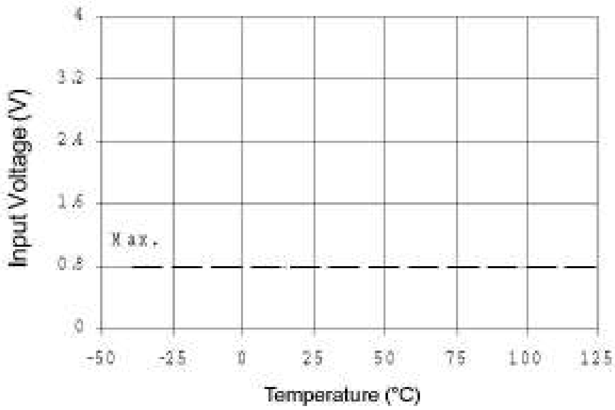


Figure 13A. Logic "0" Input Voltage vs. Temperature

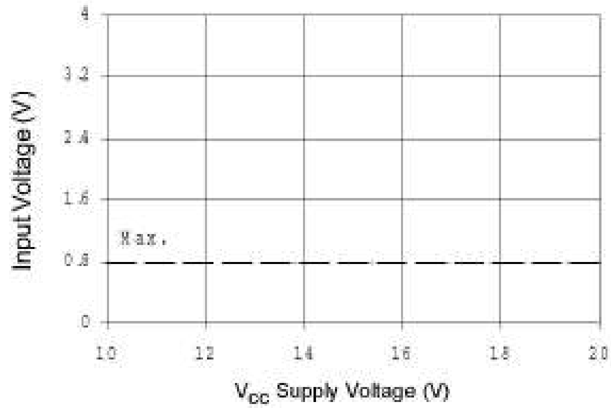


Figure 13B. Logic "0" Input Voltage vs. Supply Voltage

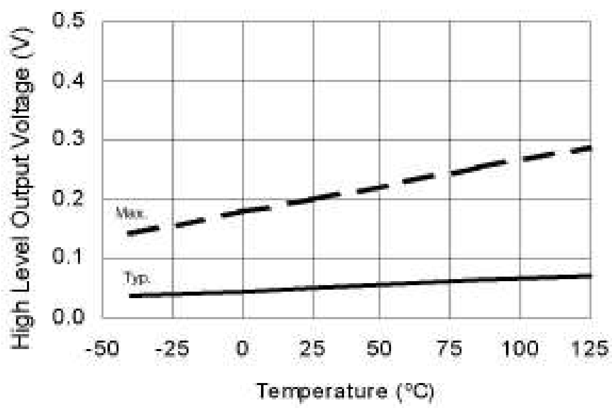


Figure 14A. High Level Output Voltage vs. Temperature

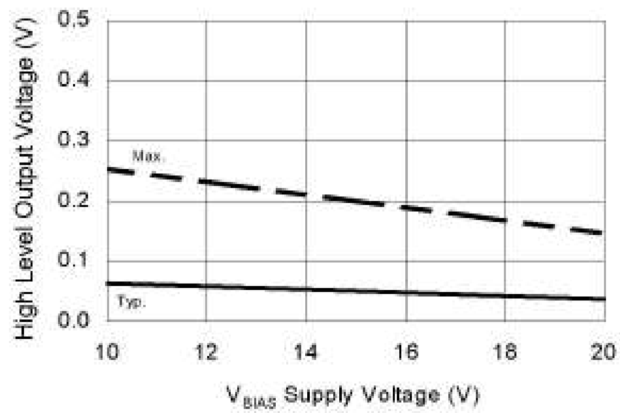


Figure 14B. High Level Output vs. Supply Voltage

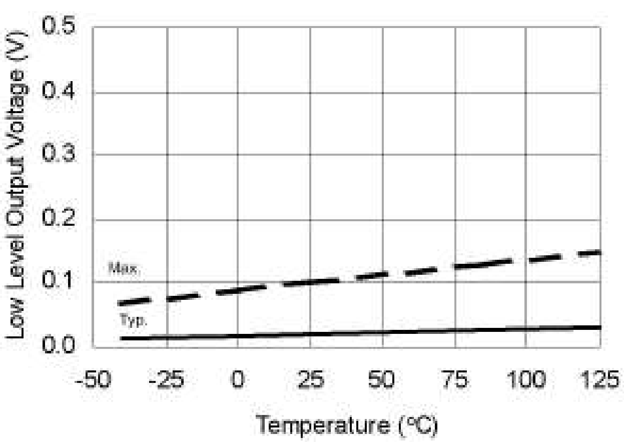


Figure 15A. Low Level Output Voltage vs. Temperature

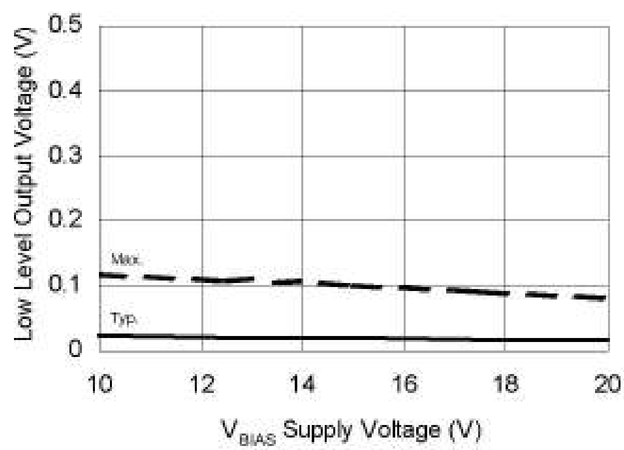


Figure 15B. Low level Output vs.Supply Voltage

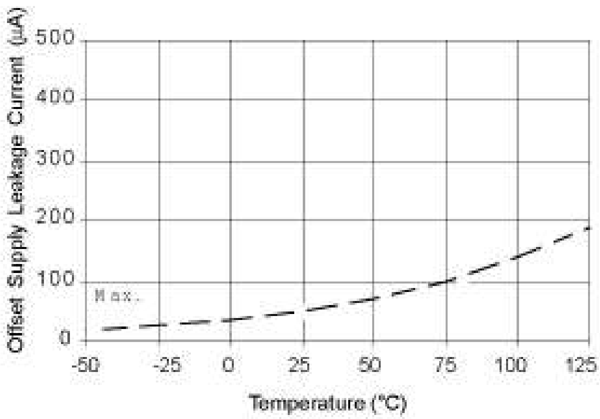


Figure 16A. Offset Supply Current vs. Temperature

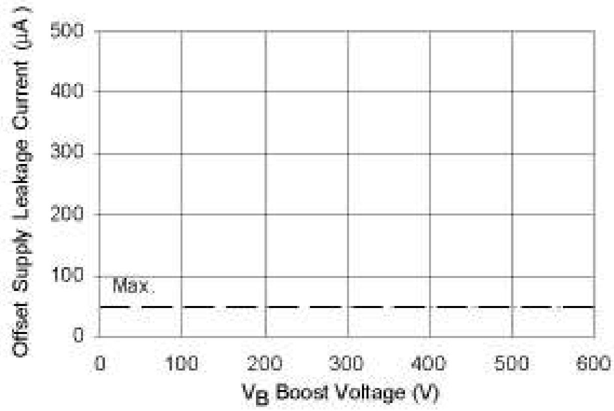


Figure 16B. Offset Supply Current vs. Voltage

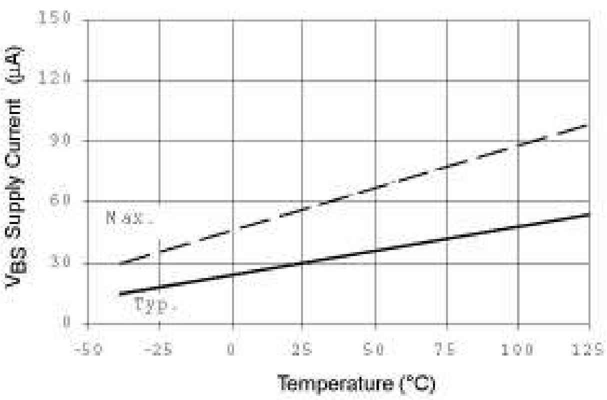


Figure 17A. V_{BS} Supply Current vs. Temperature

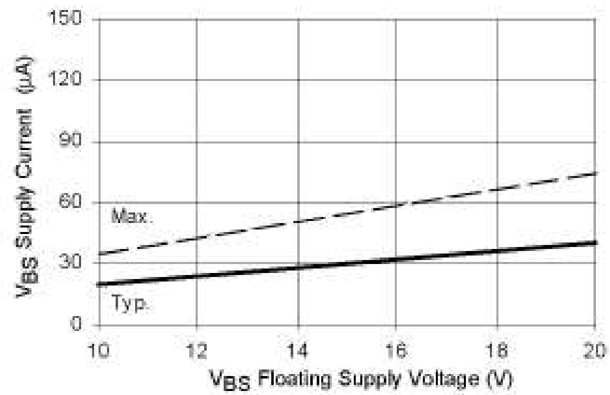


Figure 17B. V_{BS} Supply Current vs. Voltage

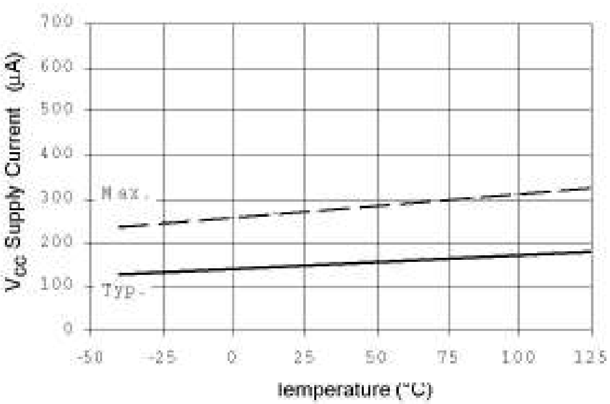


Figure 18A. V_{CC} Supply Current vs. Temperature

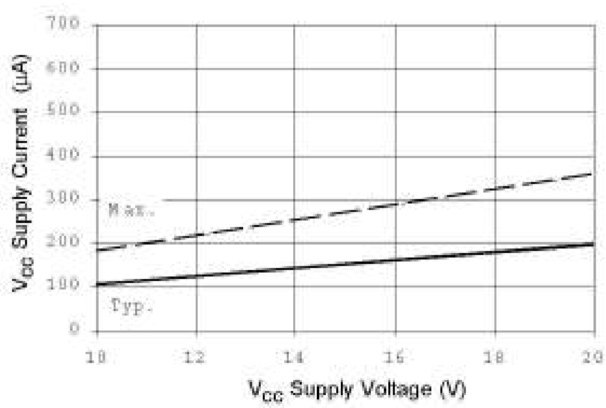


Figure 18B. V_{CC} Supply Current vs. Voltage

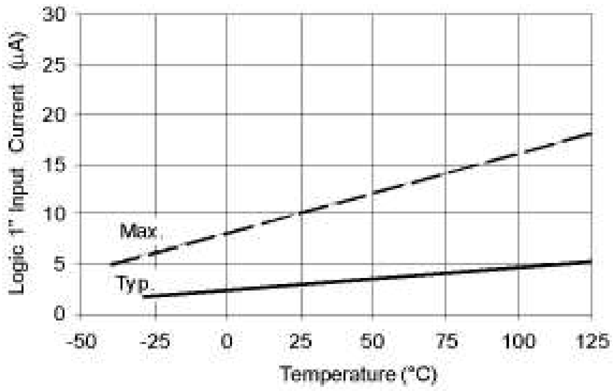


Figure 19A. Logic"1" Input Current vs. Temperature

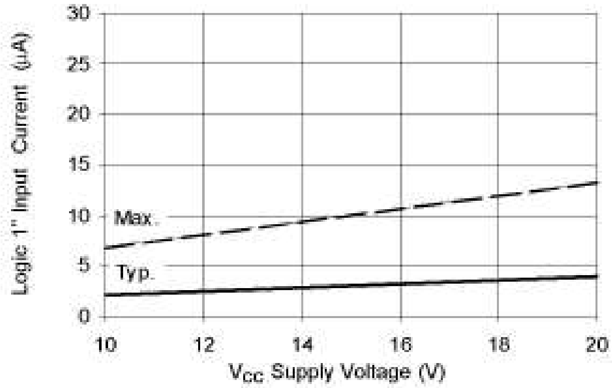


Figure 19B. Logic"1" Input Current vs. Voltage

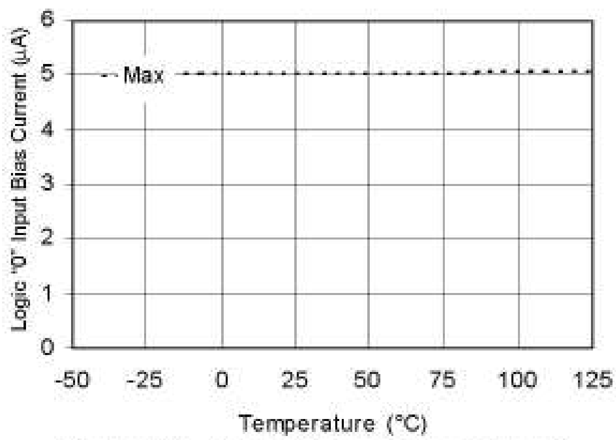


Figure 20A. Logic "0" Input Bias Current vs. Temperature

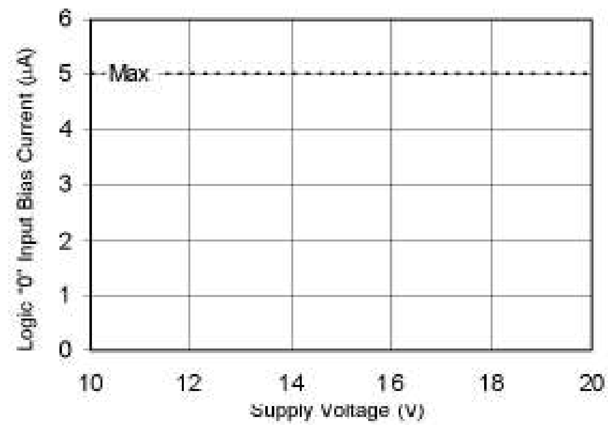


Figure 20B. Logic "0" Input Bias Current vs. Voltage

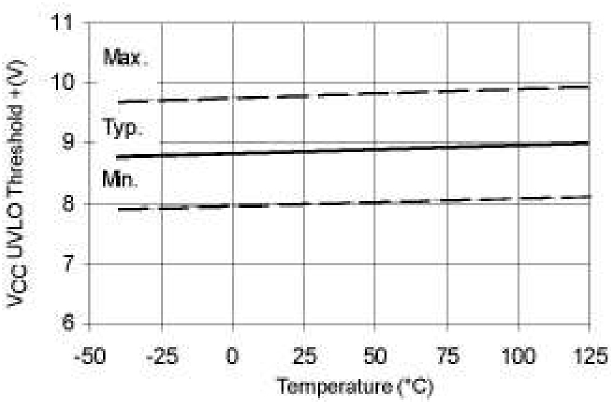


Figure 21A. V_{CC} Undervoltage Threshold(+) vs. Temperature

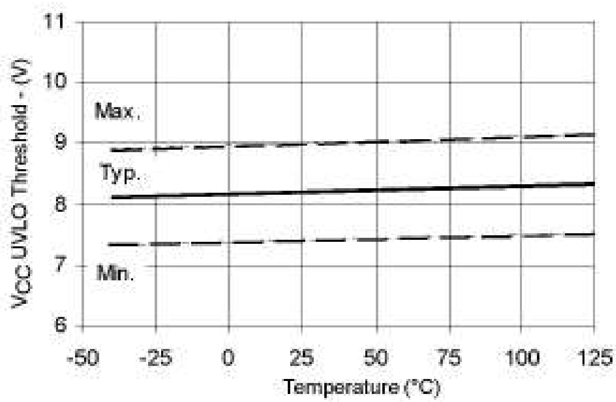


Figure 21B. V_{CC} Undervoltage Threshold(-) vs. Temperature

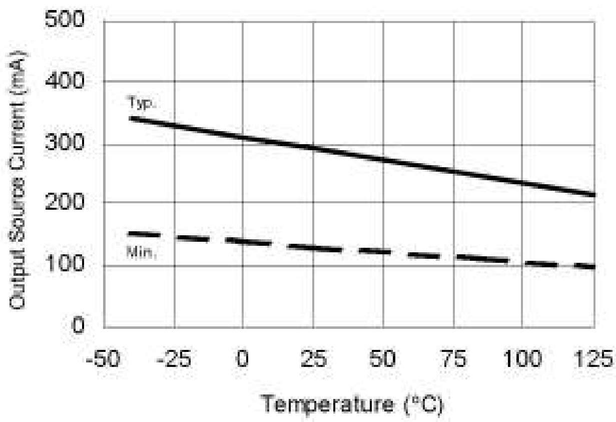


Figure 22A. Output Source Current vs. Temperature

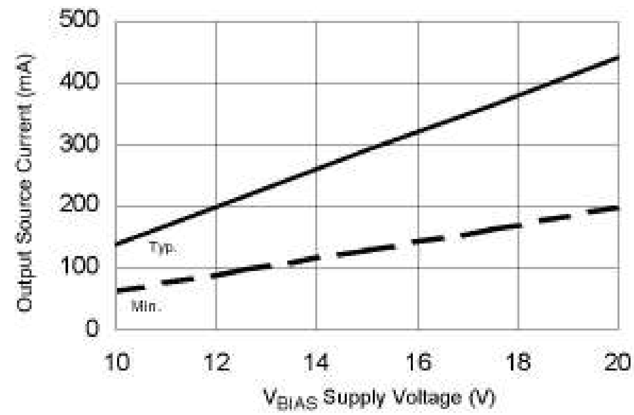


Figure 22B. Output Source Current vs. Supply Voltage

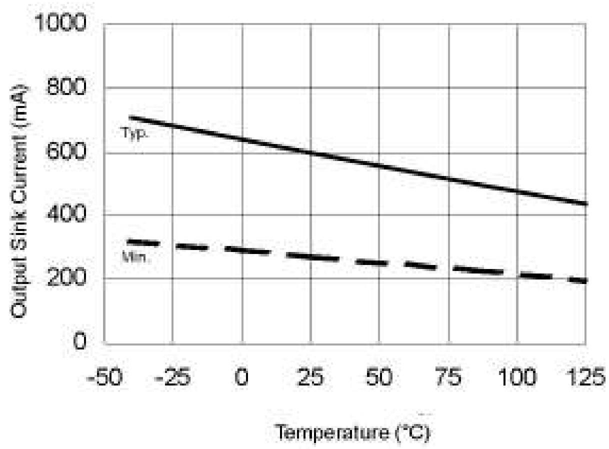


Figure 23A. Output Sink Current vs. Temperature

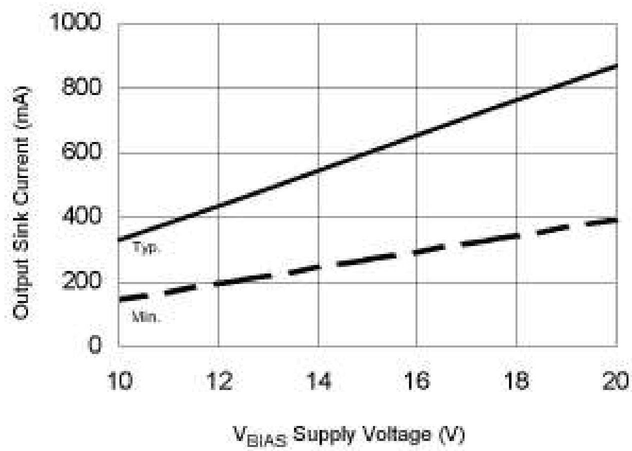
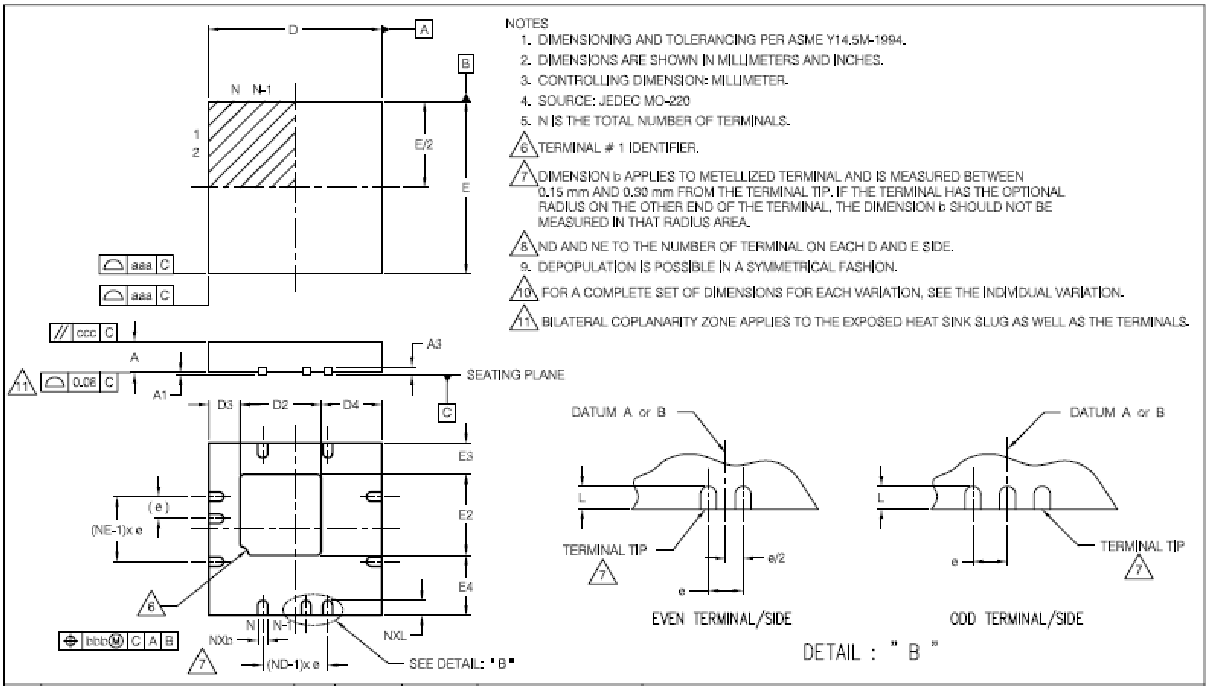


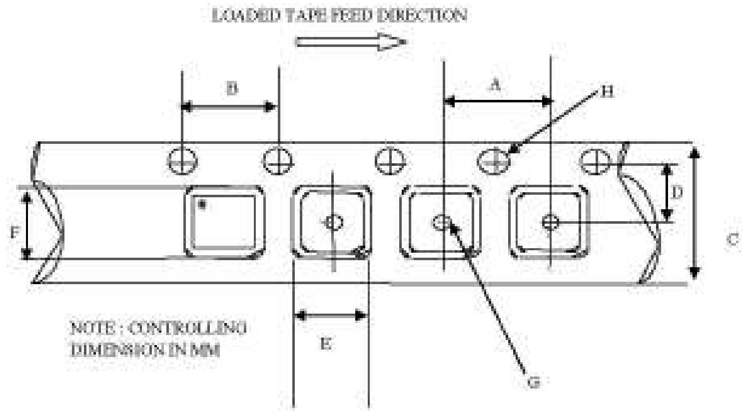
Figure 23B. Output Sink Current vs. Supply Voltage

Package Details: MLPQ 4x4 -14L



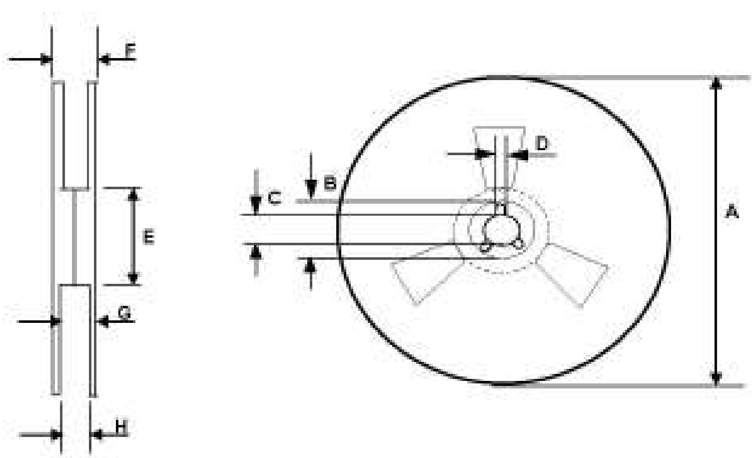
SYMBOL	VGGD-10					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.007	.010	.012
D2	1.78	1.88	1.98	.070	.074	.078
D3	0.73 REF			.029 REF		
D4	1.40 REF			.055 REF		
D	4.00 BSC			.157 BSC		
E	4.00 BSC			.157 BSC		
E4	1.40 REF			.055 REF		
E3	0.73 REF			.029 REF		
E2	1.78	1.88	1.98	.070	.074	.078
L	0.30	0.40	0.50	.012	.016	.020
e	0.50 PITCH			.020 PITCH		
N	16			16		
ND	4			4		
NE	4			4		
aaa	0.15			.0059		
bbb	0.10			.0039		
ccc	0.10			.0039		
ddd	0.05			.0019		

Tape and Reel Details: MLPQ 4x4 - 14L



CARRIER TAPE DIMENSION FOR MLPQ4X4V

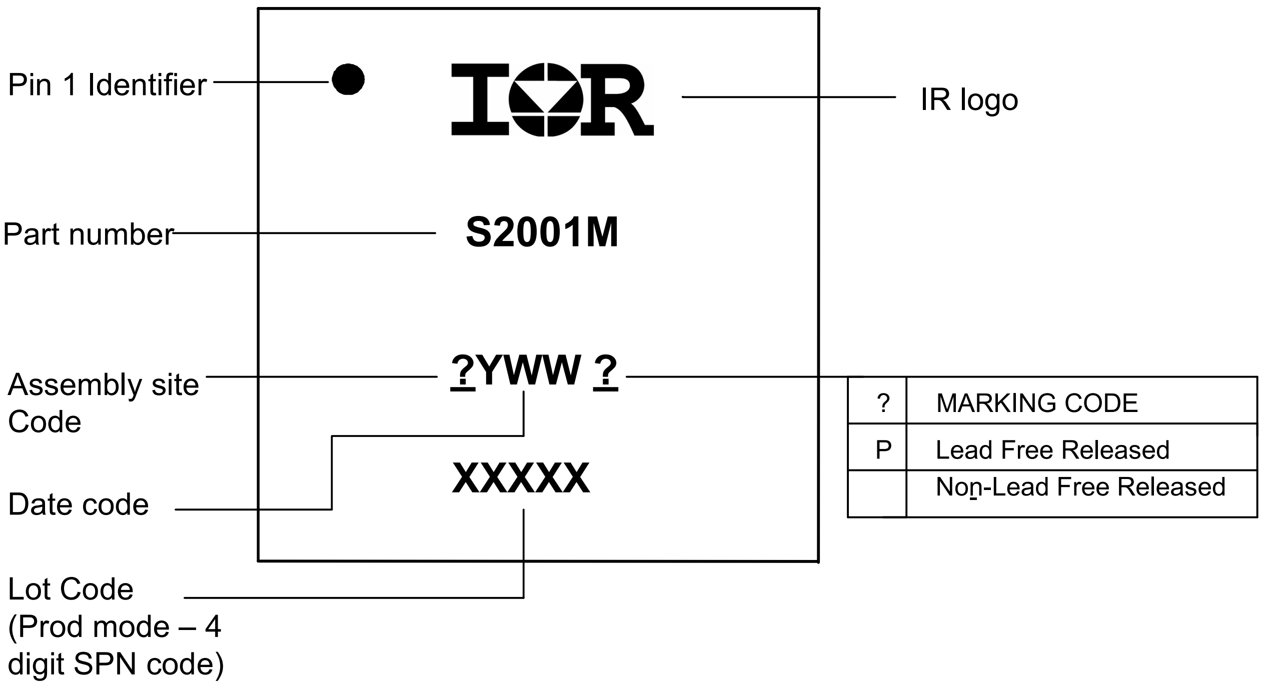
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.358
B	3.90	4.10	0.154	0.161
C	11.70	12.30	0.461	0.484
D	5.45	5.55	0.215	0.219
E	4.25	4.45	0.168	0.176
F	4.25	4.45	0.168	0.176
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.063



REEL DIMENSIONS FOR MLPQ4X4V

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2001	MLPQ 4x4-14L	Tube/Bulk	92	IRS2001MPBF
		Tape and Reel	3,000	IRS2001MTRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Revision History

Date	Comment
9/15/09	Initial draft converted from SO8 data sheet
06/18/2010	Included Qual Info Page
05/14/2012	Io+/- minspec modification