

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage,  $dV/dt$  immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower  $di/dt$  gate driver for better noise immunity
- Output source/sink current capability (min) 1.4 A/1.8 A
- Leadfree, RoHS compliant

### Product Summary

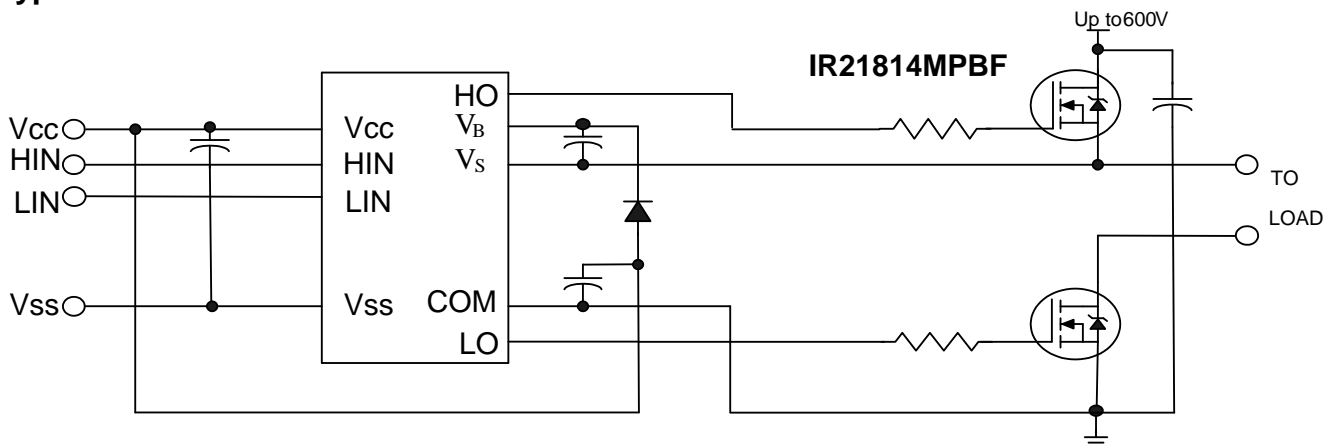
Topology	High and Low Side Driver
$V_{\text{OFFSET}}$	$\leq 600$ V
$V_{\text{OUT}}$	10 V – 20 V
$I_{o+}$ & $I_{o-}$ (typical)	1.9 A & 2.3 A
$t_{\text{ON}}$ & $t_{\text{OFF}}$ (typical)	180 ns & 220 ns

### Package Options



MLPQ4x4 16- Leads  
(Without 2 leads)

### Typical Connection



(Refer to Lead Assignments for correct pin configuration) This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

**Description**

The IRS21814MPBF is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

**Feature Comparison: IRS2181(4)/IRS2183(4)/IRS2184(4)**

Part	Input Logic	Cross-Conduction Prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				V <sub>SS</sub> /COM	
2183	HIN/LIN	yes	Internal 500ns	COM	180/220 ns
21834			Programmable 0.4 – 5 us	V <sub>SS</sub> /COM	
2184	IN/SD	yes	Internal 500ns	COM	680/270 ns
21844			Programmable 0.4 – 5 us	V <sub>SS</sub> /COM	

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup> (per JEDEC JESD 47)
		Comments: This IC has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
<b>Moisture Sensitivity Level</b>		MLPQ4x4 14L      MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class A (+/-150V) (per JEDEC standard JESD22-A115)
	Human Body Model	Class 1B (+/-1000V) (per EIA/JEDEC standard EIA/JESD22-A114)
	Charged Device Model	Class III (+/-1000V) (per JEDEC standard JESD22-C101)
<b>IC Latch-Up Test</b>		Class II, Level A (per JESD78A)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
$V_B$	High-side floating absolute voltage	-0.3	625	V
$V_S$	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
$V_{HO}$	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{CC}$	Low-side and logic fixed supply voltage	-0.3	20 †	
$V_{LO}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{IN}$	Logic input voltage (HIN & LIN)	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
$V_{SS}$	Logic ground	$V_{CC} - 20$	$V_{CC} + 0.3$	
$dV_S/dt$	Allowable offset supply voltage transient	—	50	V/ns
$P_D$	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	—	2.08	W
$R_{thJA}$	Thermal resistance, junction to ambient	—	36	$^\circ\text{C}/\text{W}$
$T_J$	Junction temperature	—	150	$^\circ\text{C}$
$T_S$	Storage temperature	-50	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply

### Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min	Max	Units
$V_B$	High-side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High-side floating supply offset voltage	††	600	
$V_{HO}$	High-side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low-side and logic fixed supply voltage	10	20	
$V_{LO}$	Low-side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage	$V_{SS}$	$V_{CC}$	
$V_{SS}$	Logic ground	-5	5	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

†† Logic operational for  $V_S$  of -5 V to +600 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

### Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM,  $C_L$  = 1000 pF,  $T_A$  = 25°C unless otherwise specified.

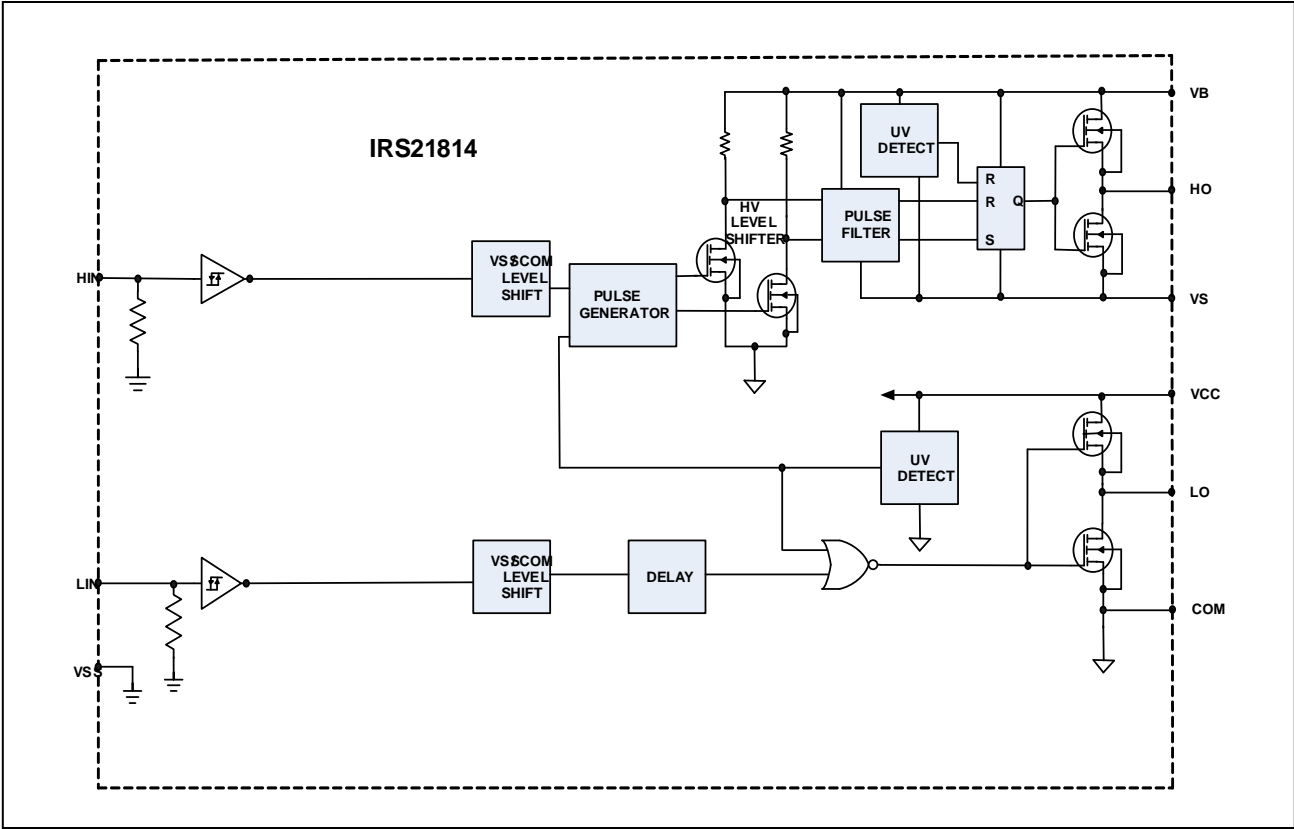
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	180	270	ns	$V_S = 0$ V
$t_{off}$	Turn-off propagation delay	—	220	330		$V_S = 0$ V or 600 V
MT	Delay matching, HS & LS turn-on/off	—	—	35		
$t_r$	Turn-on rise time	—	40	60		
$t_f$	Turn-off fall time	—	20	35		$V_S = 0$ V

### Static Electrical Characteristics

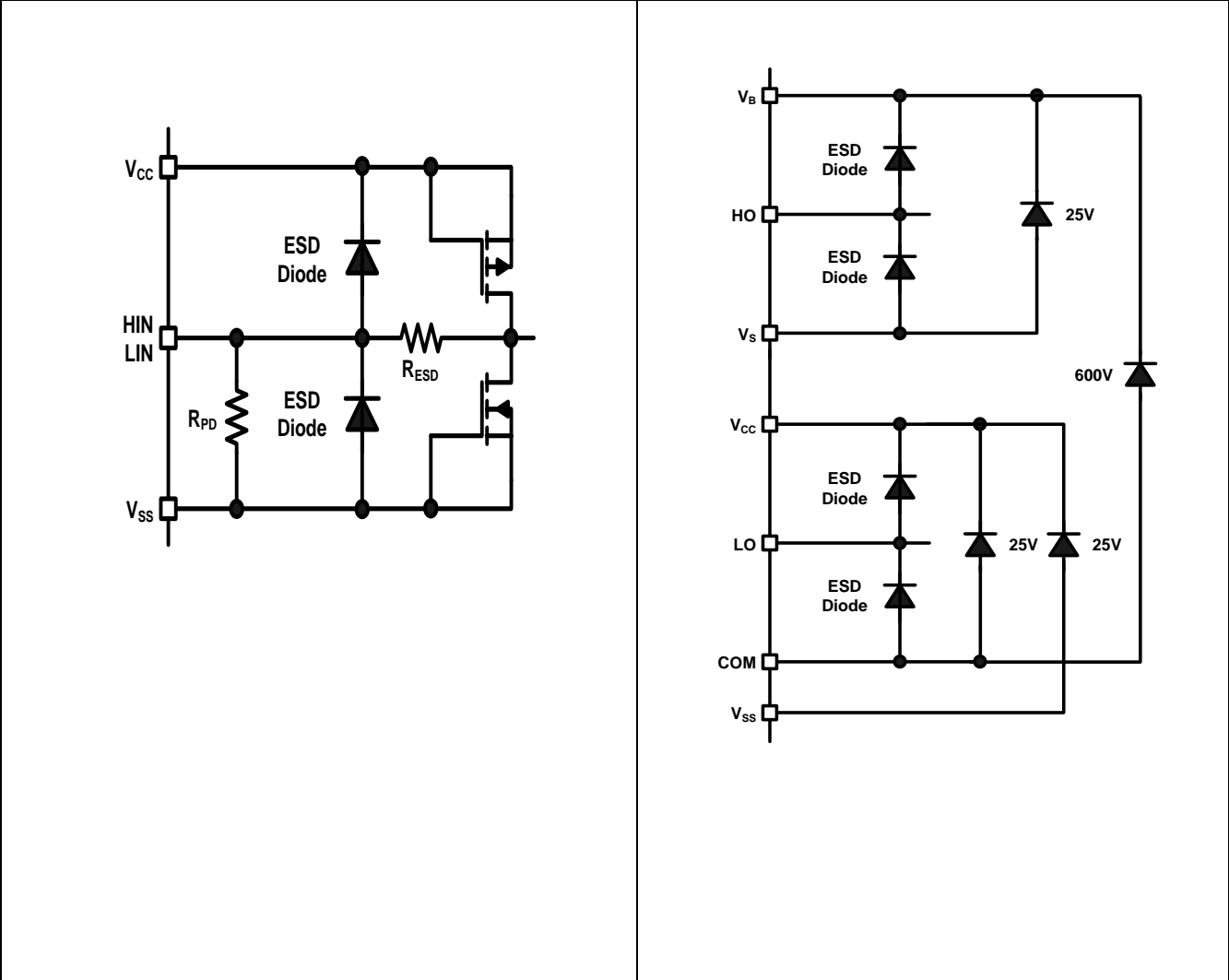
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM,  $T_A$  = 25°C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}/COM$  and are applicable to the respective input leads: HIN and LIN. The  $V_O$ ,  $I_O$  and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	2.5	—	—	V	$V_{CC} = 10$ V to 20 V
$V_{IL}$	Logic "0" input voltage	—	—	0.8		$V_{CC} = 10$ V to 20 V
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4		$I_O = 0$ mA
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.2		$I_O = 20$ mA
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu$ A	$V_B = V_S = 600$ V
$I_{QBS}$	Quiescent $V_{BS}$ supply current	20	60	150		$V_{IN} = 0$ V or 5 V
$I_{QCC}$	Quiescent $V_{CC}$ supply current	50	120	240		
$I_{IN+}$	Logic "1" input bias current	—	25	60		$V_{IN} = 5$ V
$I_{IN-}$	Logic "0" input bias current	—	—	1.0		$V_{IN} = 0$ V
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$V_{CCUVH}$ $V_{BSUVH}$	$V_{CC}$ and $V_{BS}$ supply undervoltage Hysteresis	0.3	0.7	—		
$I_{O+}$	Output high short circuit pulsed current	1.4	1.9	—	A	$V_O = 0$ V, $PW \leq 10$ $\mu$ s
$I_{O-}$	Output low short circuit pulsed current	1.8	2.3	—		$V_O = 15$ V, $PW \leq 10$ $\mu$ s

**Functional Block Diagrams: IRS21814**



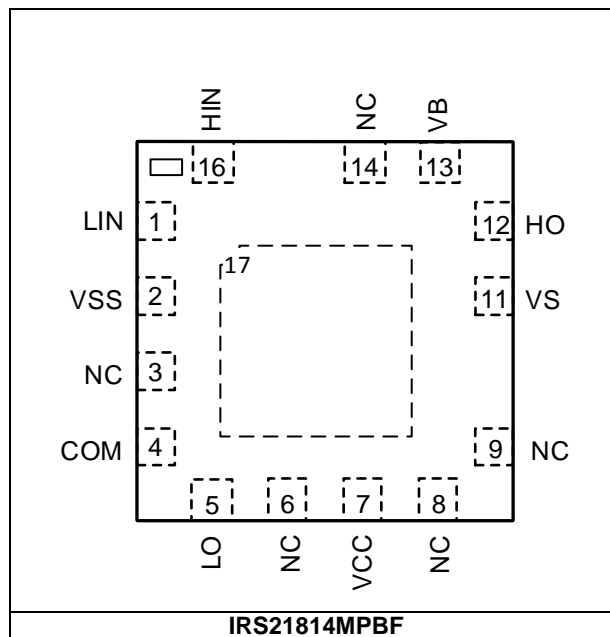
**Input/Output Pin Equivalent Circuit Diagrams: IRS21814**



**Lead Definitions: IRS21814MPBF**

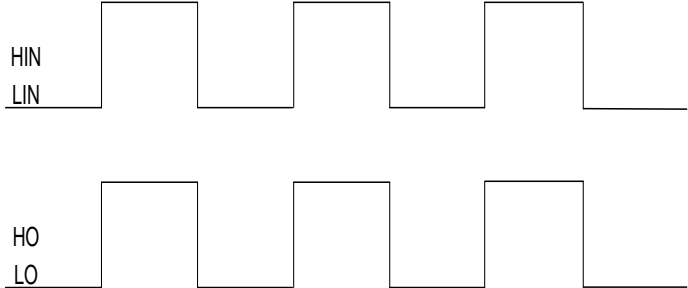
PIN	Symbol	Description
1	LIN	Logic input for low-side driver output (LO), in phase
2	V <sub>SS</sub>	Logic ground
3	NC	No Connection
4	COM	Low-side return
5	LO	Low-side gate drive output
6	NC	No Connection
7	V <sub>CC</sub>	Low-side and logic fixed supply
8	NC	No Connection
9	NC	No Connection
10	NC	No Connection (removed lead)
11	V <sub>S</sub>	High-side floating supply return
12	HO	High-side gate drive output
13	V <sub>B</sub>	High-side floating supply
14	NC	No Connection
15	NC	No Connection (removed lead)
16	HIN	Logic input for high-side gate driver output (HO), in phase

**Lead Assignments:**

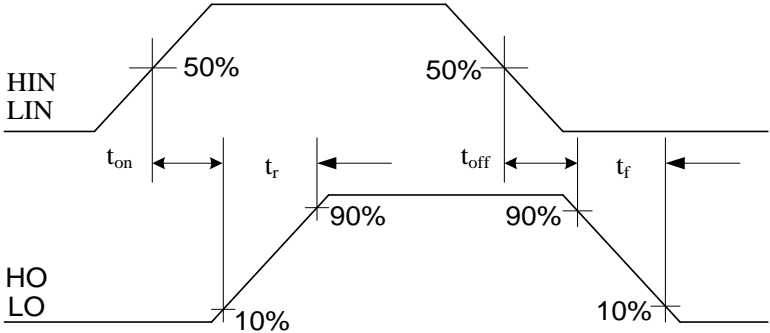


Central exposed pad (17) has to be connected to COM for better electrical performance.

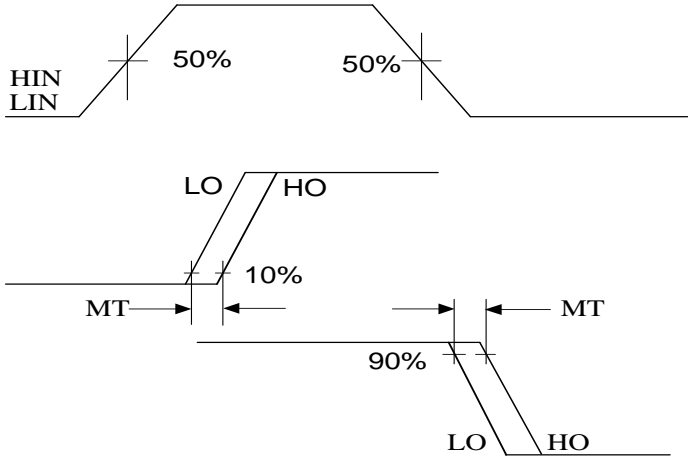
**Application Information and Additional Details**



**Figure 1. Input/Output Timing Diagram**



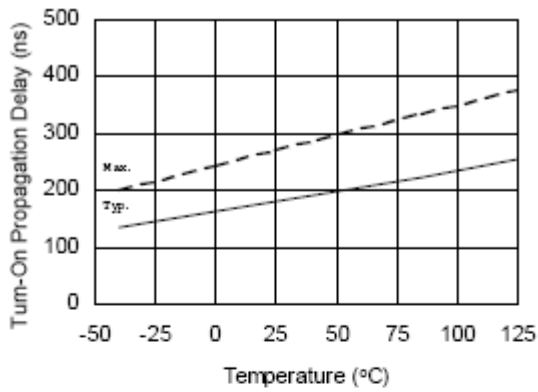
**Figure 2. Switching Time Waveform Definitions**



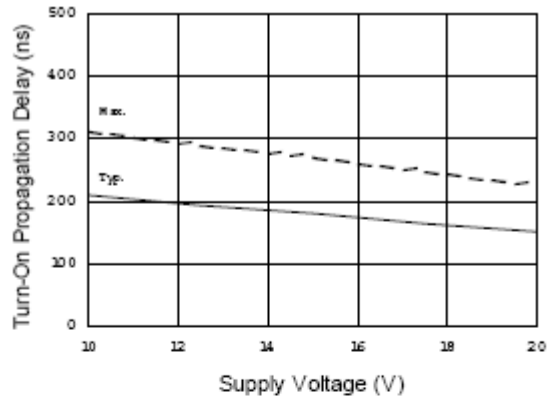
**Figure 3. Delay Matching Waveform Definitions**



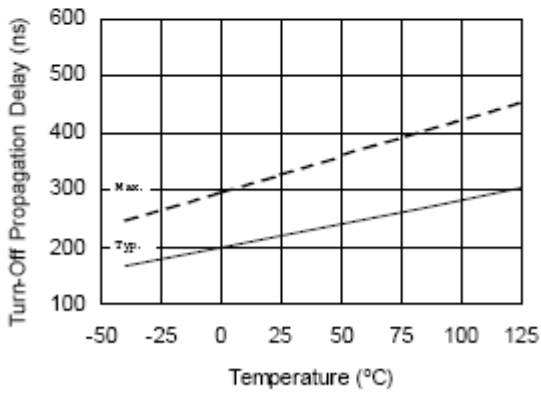
**Parameter Temperature Trends**



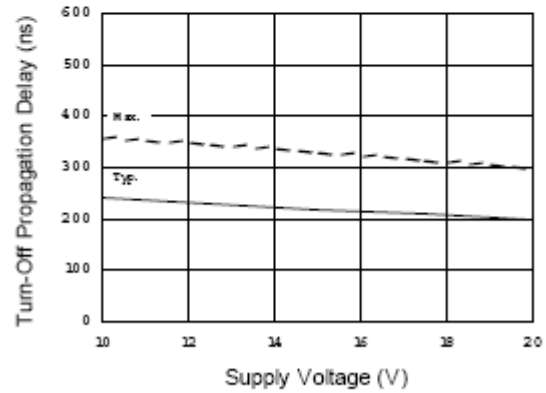
**Figure 4A. Turn-On Propagation Delay vs. Temperature**



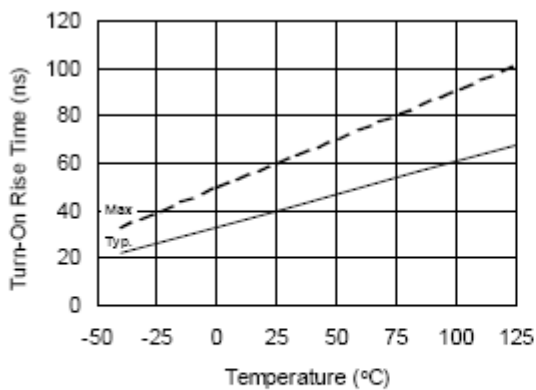
**Figure 4B. Turn-On Propagation Delay vs. Supply Voltage**



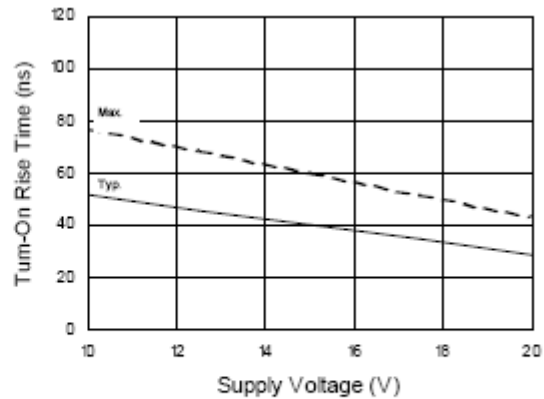
**Figure 5A. Turn-Off Propagation Delay vs. Temperature**



**Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage**



**Figure 6A. Turn-On Rise Time vs. Temperature**



**Figure 6B. Turn-On Rise Time vs. Supply Voltage**

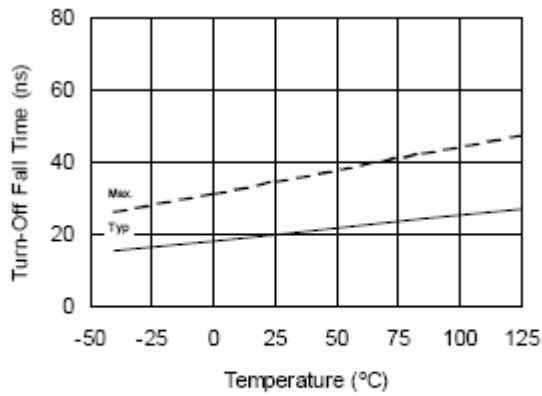


Figure 7A. Turn-Off Fall Time vs. Temperature

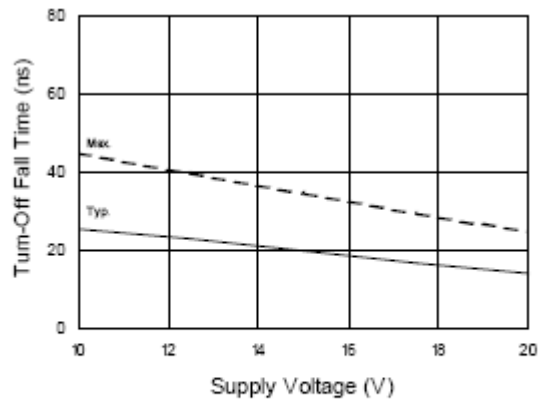


Figure 7B. Turn-Off Fall Time vs. Supply Voltage

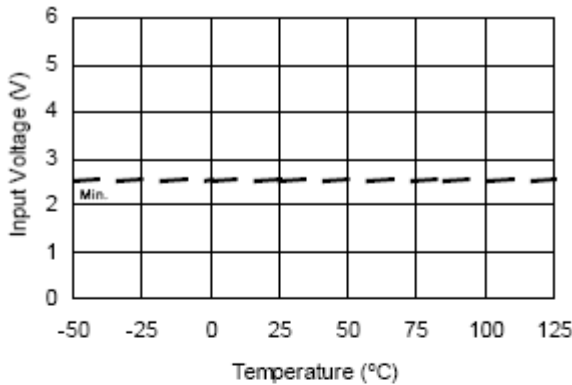


Figure 8A. Logic "1" Input Voltage vs. Temperature

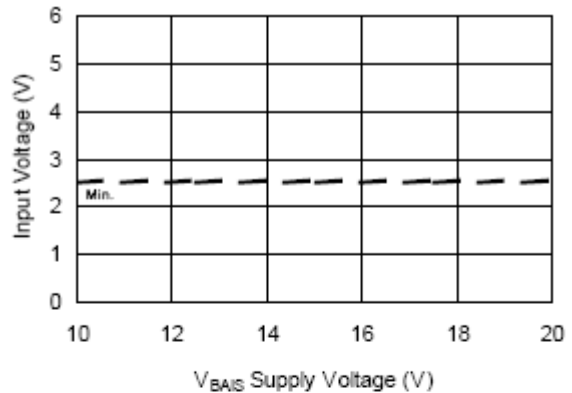


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

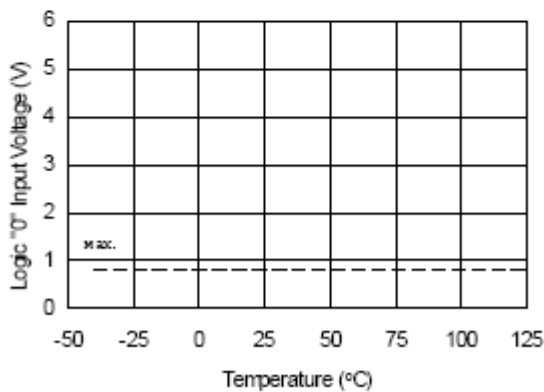


Figure 9A. Logic "0" Input Voltage vs. Temperature

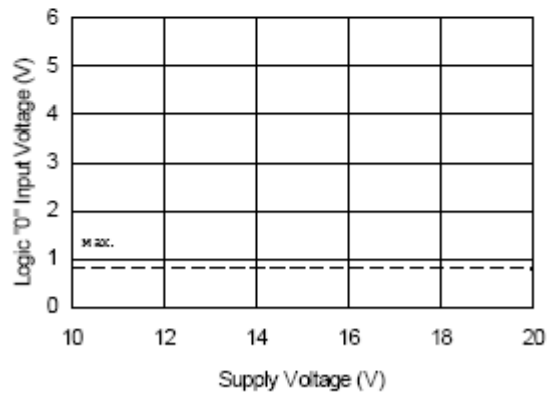
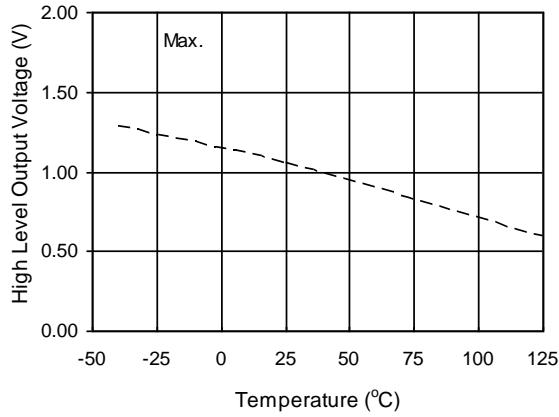
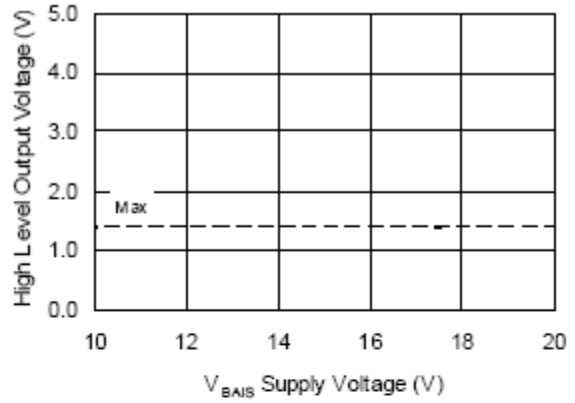


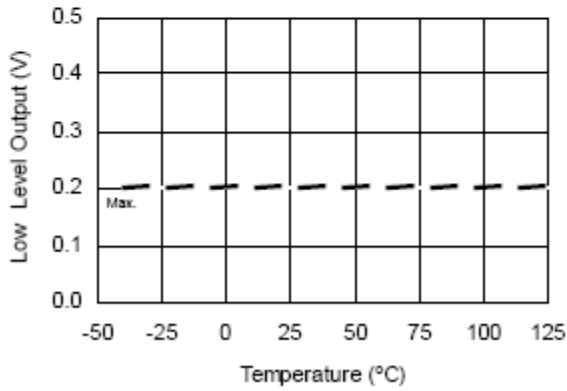
Figure 9B. Logic "0" Input Voltage vs. Supply Voltage



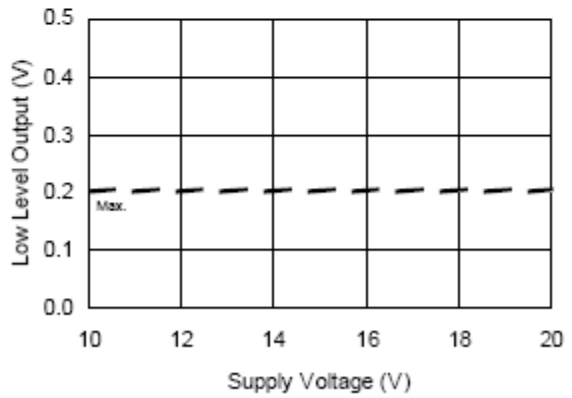
**Figure 10A. High Level Output Voltage vs. Temperature ( $I_O = 0$  mA)**



**Figure 10B. High Level Output Voltage vs. Supply Voltage ( $I_O = 0$  mA)**



**Figure 11A. Low Level Output vs. Temperature**



**Figure 11B. Low Level Output vs. Supply Voltage**

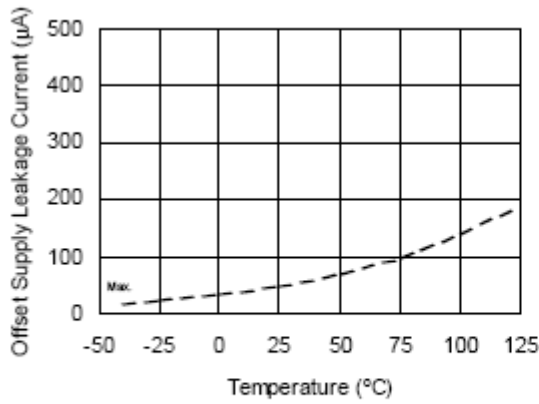


Figure 12A. Offset Supply Leakage Current vs. Temperature

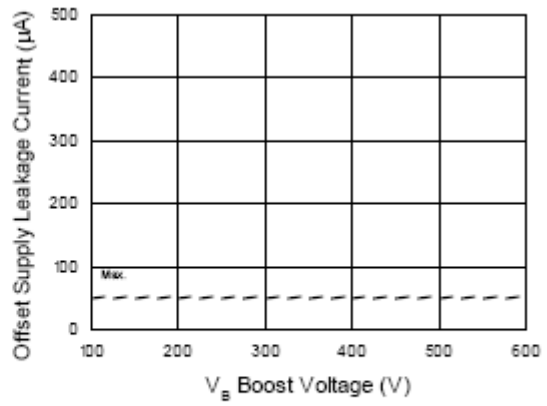


Figure 12B. Offset Supply Leakage Current vs. V<sub>B</sub> Boost Voltage

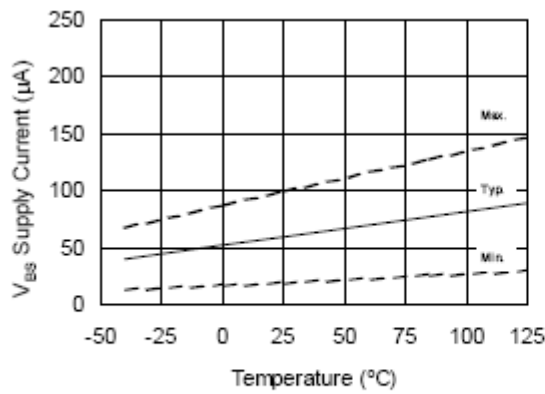


Figure 13A. V<sub>BS</sub> Supply Current vs. Temperature

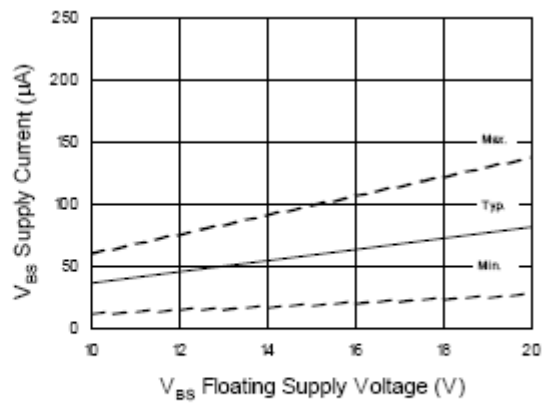


Figure 13B. V<sub>BS</sub> Supply Current vs. V<sub>BS</sub> Floating Supply Voltage

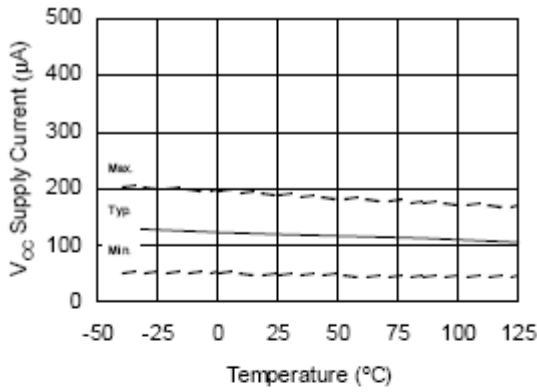


Figure 14A.  $V_{CC}$  Supply Current vs.  $V_{CC}$  Temperature

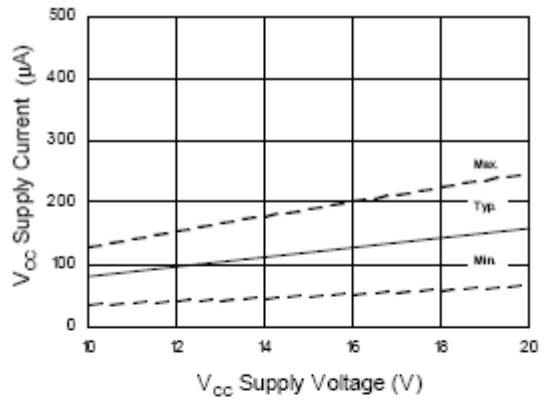


Figure 14B.  $V_{CC}$  Supply Current vs.  $V_{CC}$  Supply Voltage

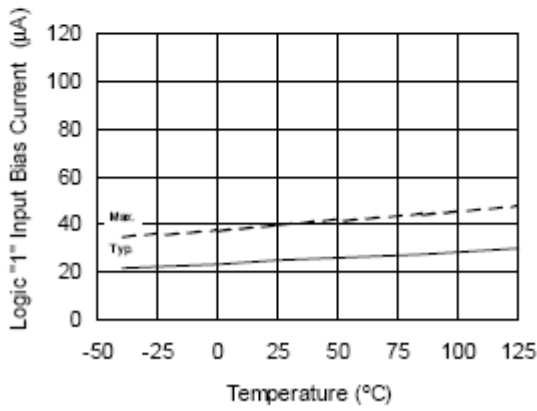


Figure 15A. Logic "1" Input Bias Current vs. Temperature

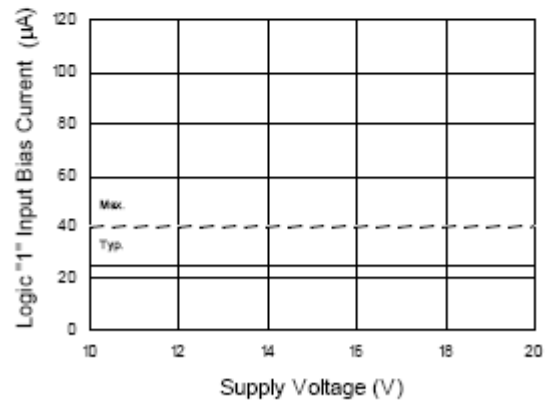
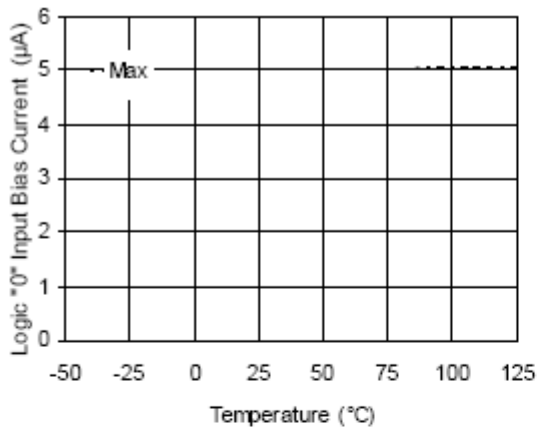
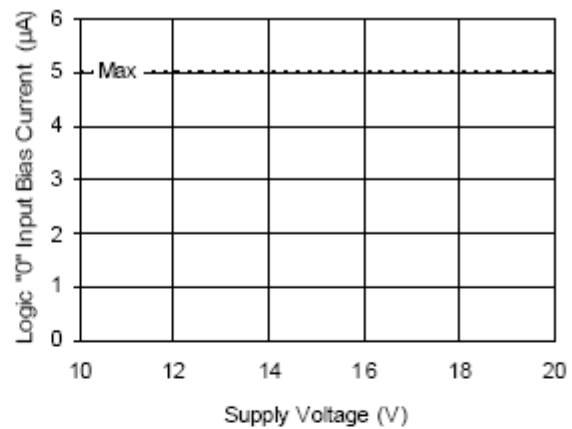


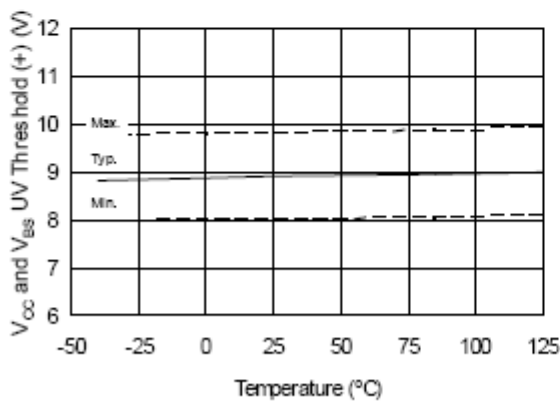
Figure 15B. Logic "1" Input Bias Current vs. Supply Voltage



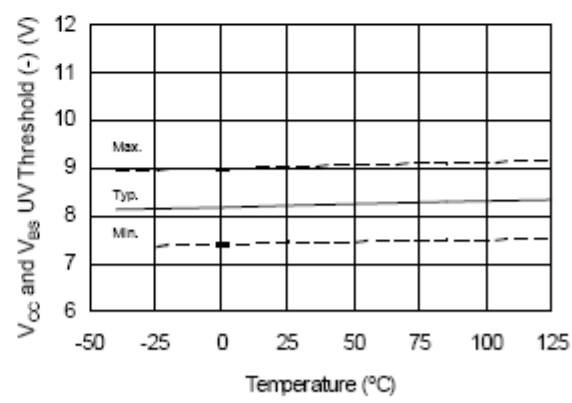
**Figure 16A. Logic "0" Input Bias Current vs. Temperature**



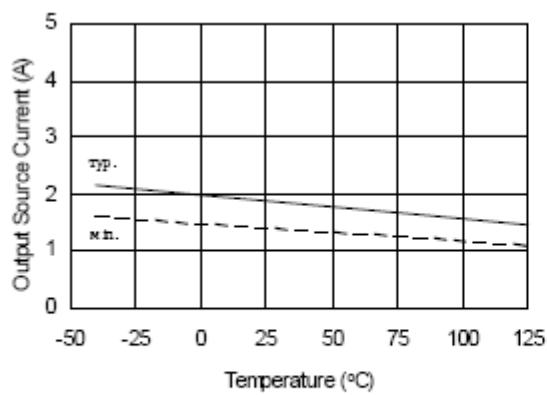
**Figure 16B. Logic "0" Input Bias Current vs. Voltage**



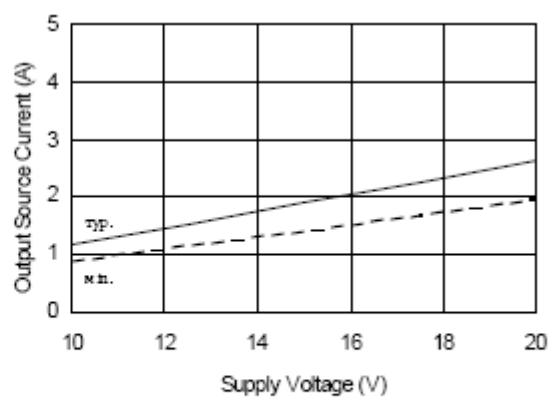
**Figure 17.  $V_{CC}$  and  $V_{SS}$  Undervoltage Threshold (+) vs. Temperature**



**Figure 18.  $V_{CC}$  and  $V_{SS}$  Undervoltage Threshold (-) vs. Temperature**



**Figure 19A. Output Source Current vs. Temperature**



**Figure 19B. Output Source Current vs. Supply Voltage**

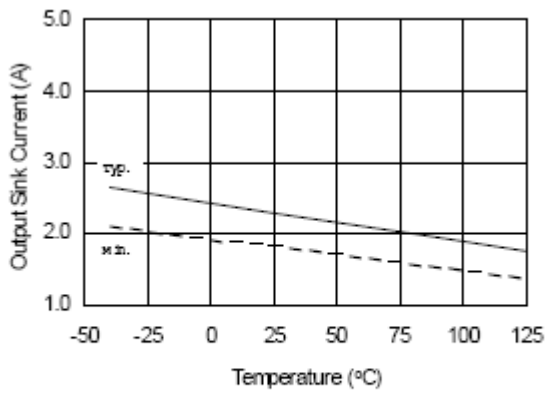


Figure 20A. Output Sink Current vs. Temperature

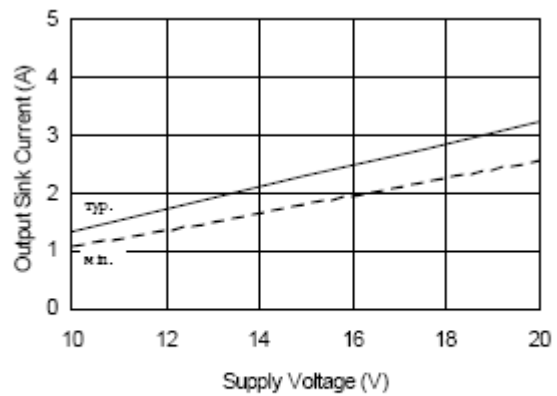


Figure 20B. Output Sink Current vs. Supply Voltage

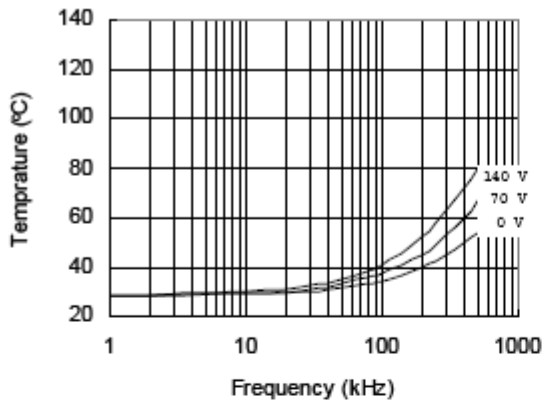


Figure 21. IRS2181 vs. Frequency (IRFBC20),  $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$

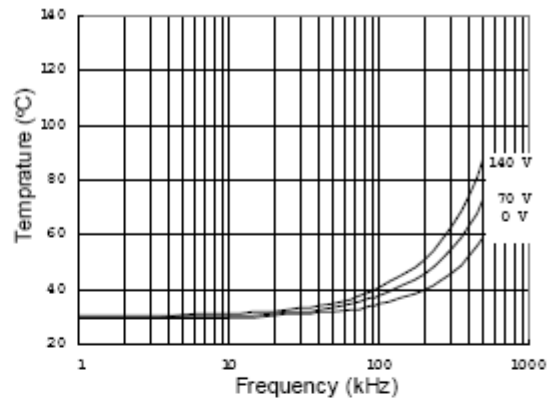


Figure 22. IRS2181 vs. Frequency (IRFBC30),  $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$

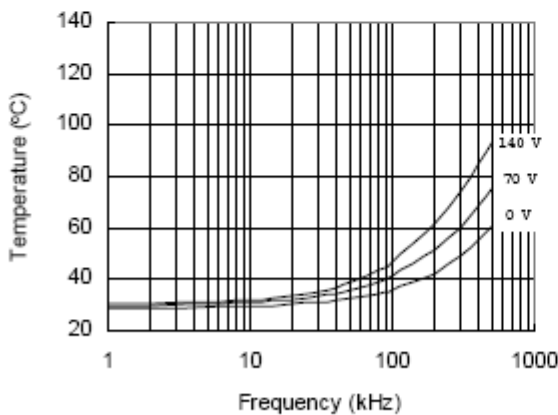


Figure 23. IRS2181 vs. Frequency (IRFBC40),  $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$

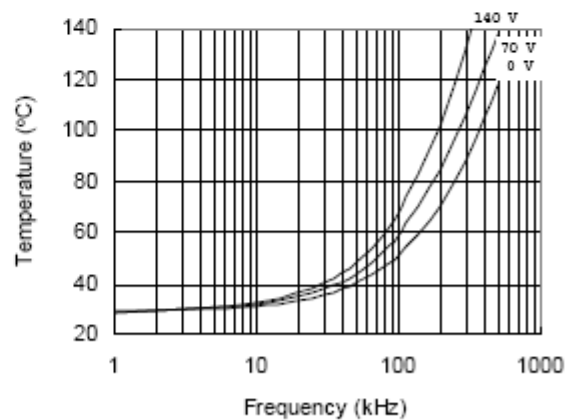


Figure 24. IRS2181 vs. Frequency (IRFPE50),  $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$

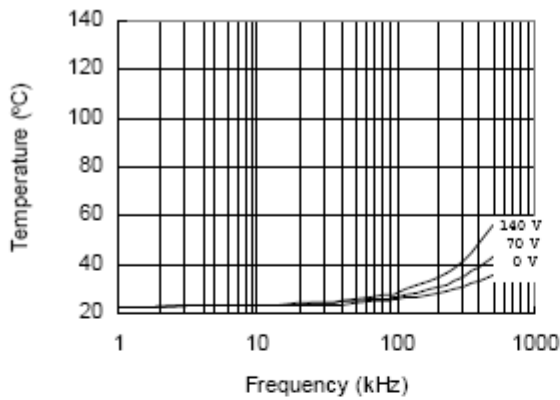


Figure 25. IRS21814 vs. Frequency (IRFBC20),  
 $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$

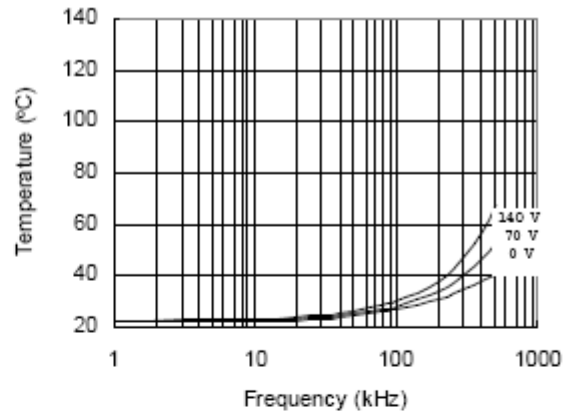


Figure 26. IRS21814 vs. Frequency (IRFBC30),  
 $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$

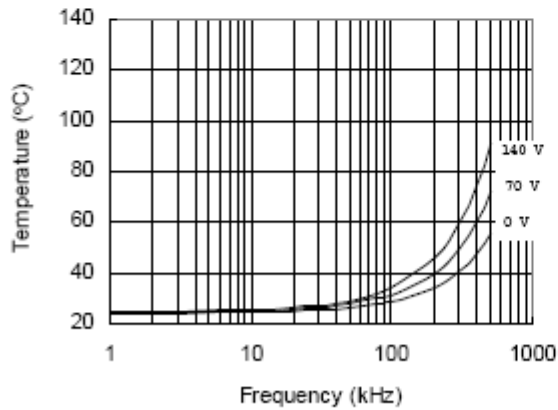


Figure 27. IRS21814 vs. Frequency (IRFBC40),  
 $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$

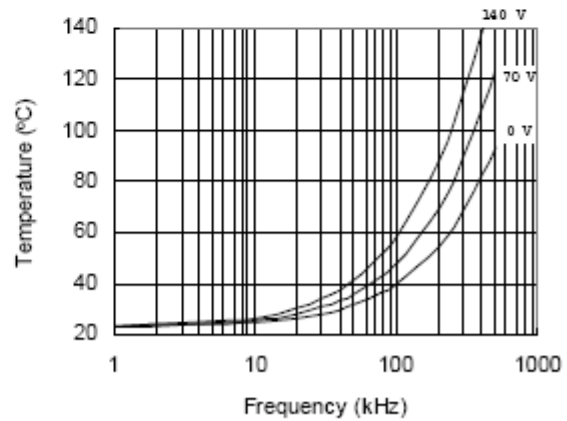


Figure 28. IRS21814 vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$

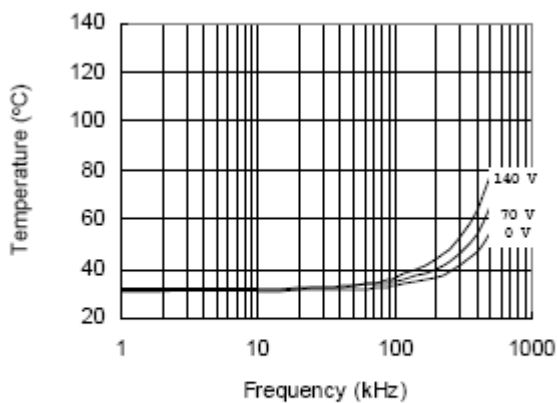


Figure 29. IRS2181S vs. Frequency (IRFBC20),  
 $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$

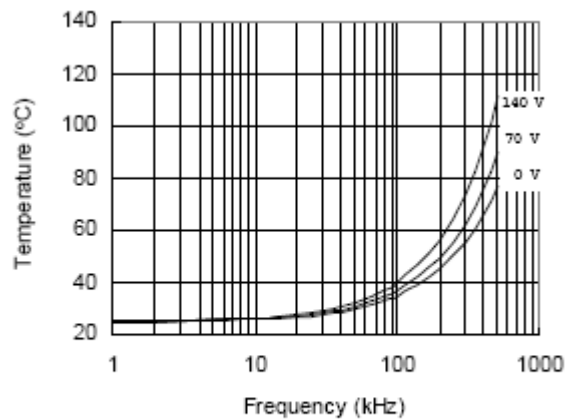


Figure 30. IRS2181S vs. Frequency (IRFBC30),  
 $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$



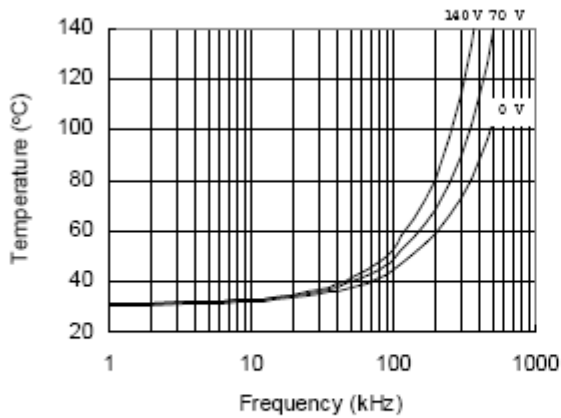


Figure 31. IRS2181S vs. Frequency (IRFBC40),  
 $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$

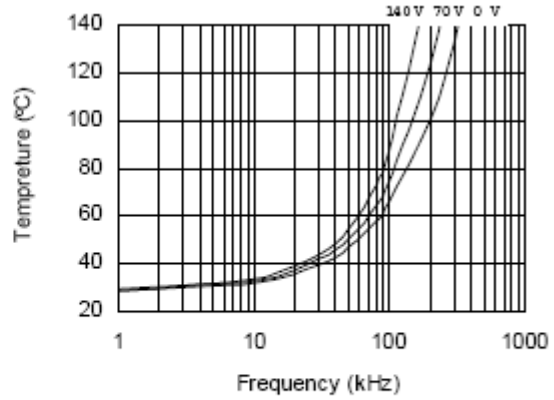


Figure 32. IRS2181S vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$

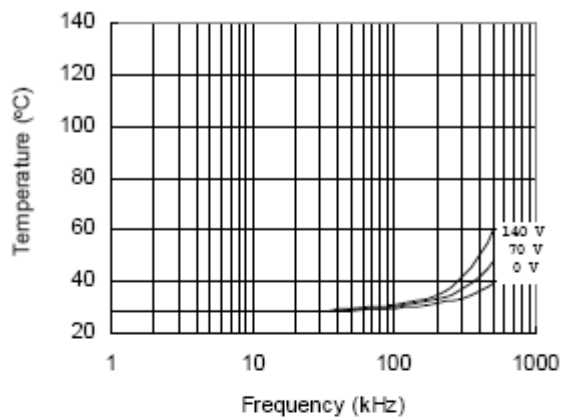


Figure 33. IRS21814S vs. Frequency (IRFBC20),  
 $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$

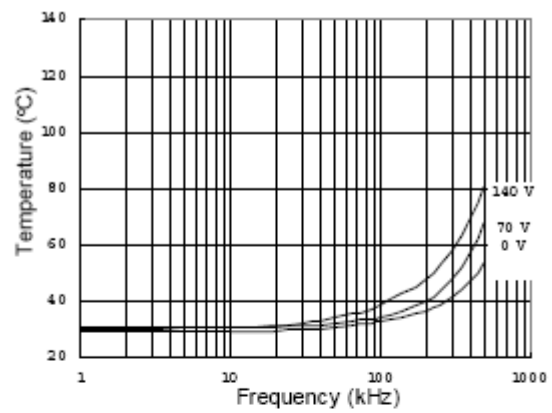


Figure 34. IRS21814S vs. Frequency (IRFBC30),  
 $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$

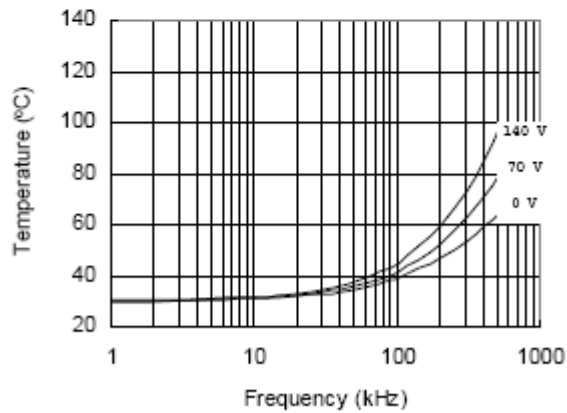


Figure 35. IRS21814S vs. Frequency (IRFBC40),  
 $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$

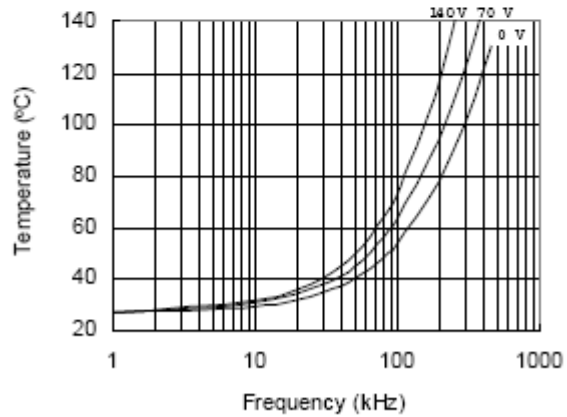
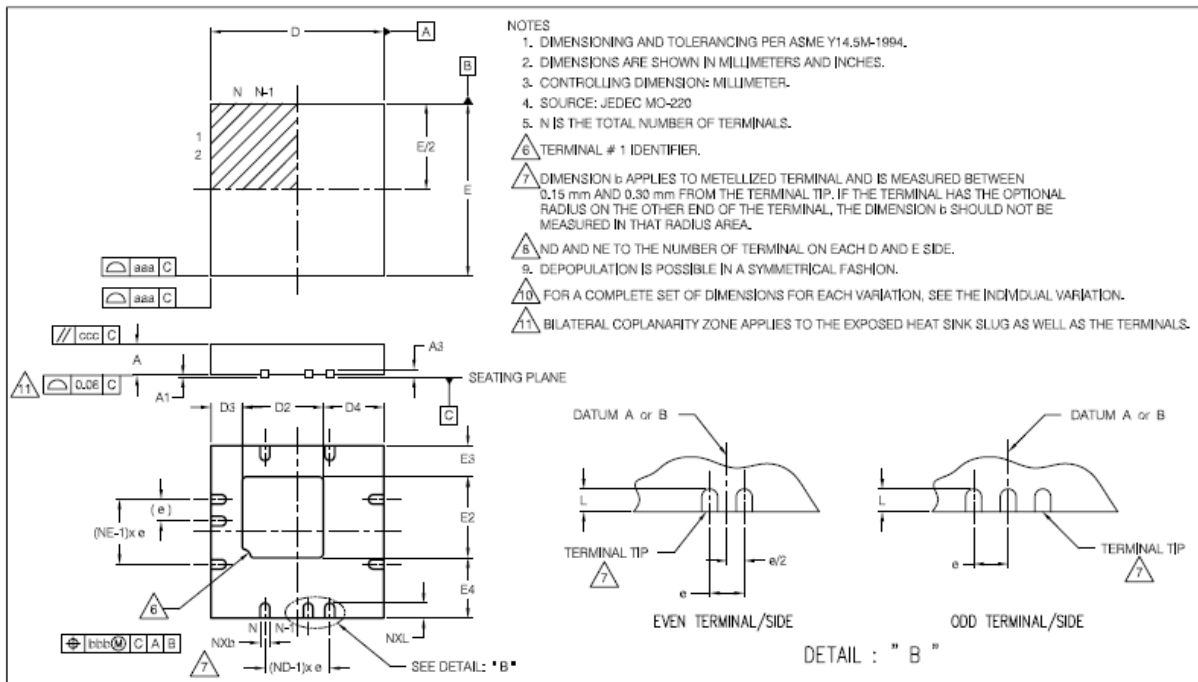


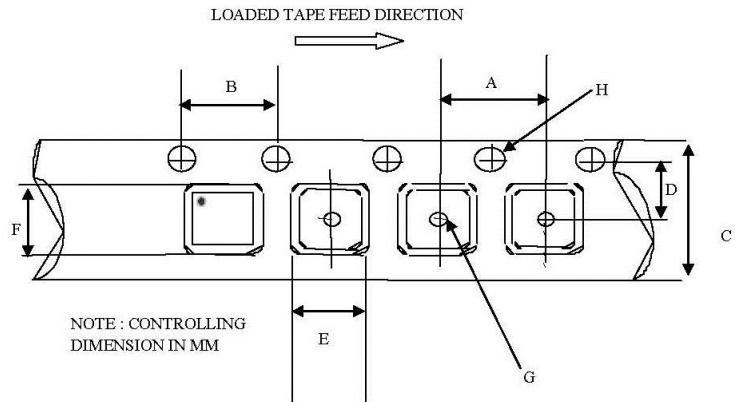
Figure 36. IRS21814S vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$

**Package Details: MLPQ 4x4 -16L**



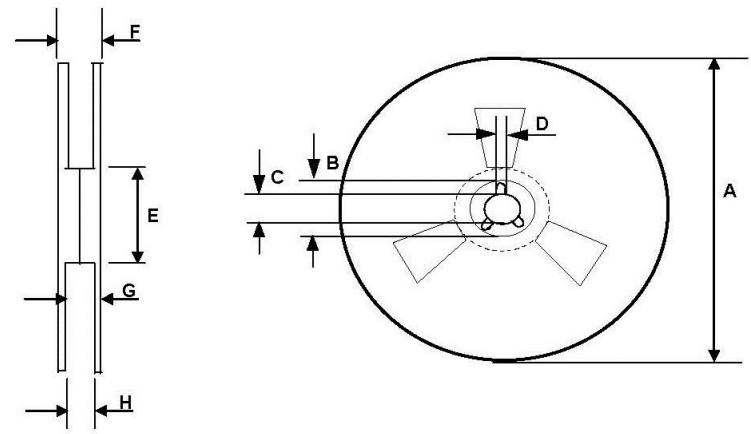
SYMBOL	VGGD-10					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.007	.010	.012
D2	1.78	1.88	1.98	.070	.074	.078
D3	0.73 REF			.029 REF		
D4	1.40 REF			.055 REF		
D	4.00 BSC			.157 BSC		
E	4.00 BSC			.157 BSC		
E4	1.40 REF			.055 REF		
E3	0.73 REF			.029 REF		
E2	1.78	1.88	1.98	.070	.074	.078
L	0.30	0.40	0.50	.012	.016	.020
e	0.50 PITCH			.020 PITCH		
N	16			16		
ND	4			4		
NE	4			4		
aaa	0.15			.0059		
bbb	0.10			.0039		
ccc	0.10			.0039		
ddd	0.05			.0019		

**Tape and Reel Details: MLPQ 4x4**



CARRIER TAPE DIMENSION FOR MLPQ4X4V

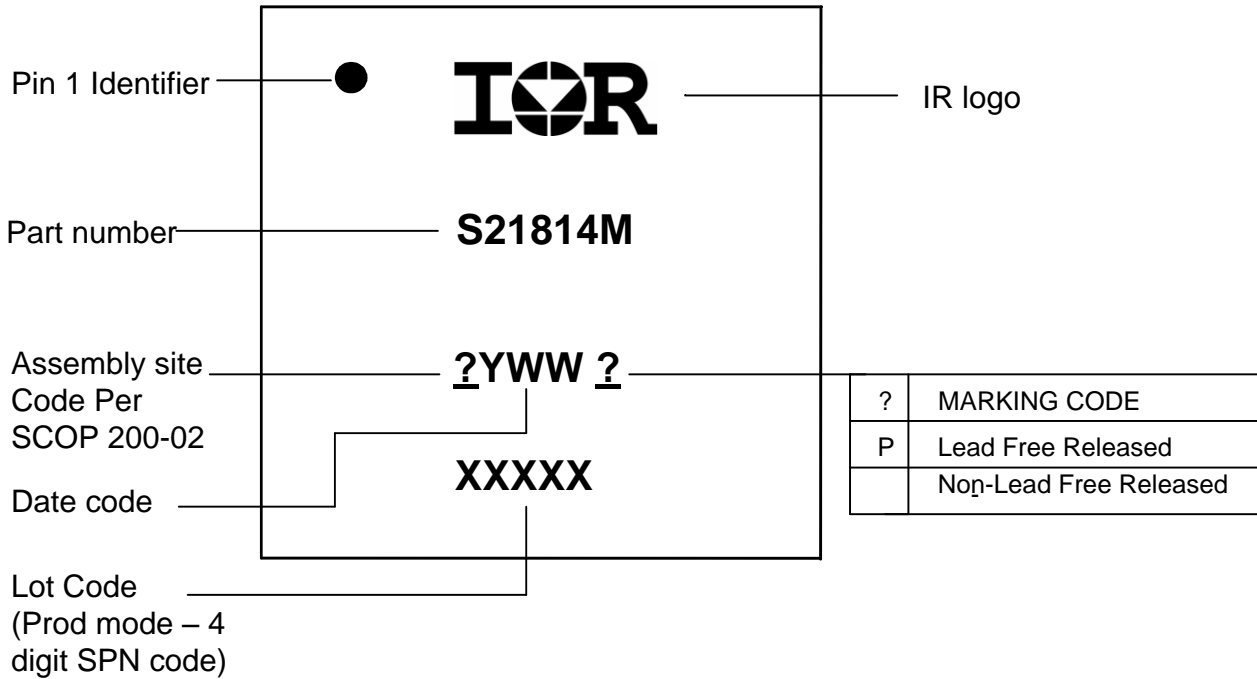
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.358
B	3.90	4.10	0.154	0.161
C	11.70	12.30	0.461	0.484
D	5.45	5.55	0.215	0.219
E	4.25	4.45	0.168	0.176
F	4.25	4.45	0.168	0.176
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.063



REEL DIMENSIONS FOR MLPQ4X4V

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS21814	MLPQ 4x4-16L	Tube/Bulk	92	IRS21814MPBF
		Tape and Reel	3,000	IRS21814MTRPBF

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<http://www.irf.com/technical-info/>

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**Revision History**

<b>Date</b>	<b>Comment</b>
09/24/09	Converted from existing data sheet; changing only package information
03/24/2010	Included Qual Info Page
6/9/2016	Add note regarding exposed pad, Fix typo

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