Class D Audio

Class D Audio IC IRS2452AM

Features

- 2 channel integrated analog input Class D audio amplifier driver
- Differential or single-ended input
- Versatile protection control enabling latched, non-latched, or host controlled shutdown function
- Programmable over current protection
- Programmable dead-time generation
- External thermal sensor input
- Click noise reduction
- Under voltage protection
- High noise immunity

Product Summary

Topology	Half-Bridge/Full-Bridge
$V_{OFFSET\ (max)}$	+/- 200 V
I_{O+} & I_{O-} (typical)	0.5 A & 0.6 A
Selectable deadtime	45/65/85/105 ns
DC offset	<18 mV
OC protection delay	500 ns (max)
Shutdown propagation delay	250 ns (max)
Error amplifier open loop gain	>60 dB

Package Options

MLPQ 7X7mm 32L (0.50 mm pitch)

Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2452AM	MLPQ 32 7x7	Tape and Reel	3000	IRS2452AM

Description

The IRS2452AM integrates two channels of high voltage, high performance Class D audio amplifier drivers with PWM modulators and protections. In conjunction with external MOSFET, the IRS2452AM forms a complete 2 channel Class D audio amplifier. The IRS2452AM is designed with floating analog inputs and protection control interface pins convenient for half bridge applications. High and low side MOSFET are protected from over current conditions by a programmable over current protection. Essential elements of PWM modulator section allow flexible system design. A small MLPQ 7x7mm package enhances the benefit of smaller size of Class D topology. The IRS2452AM is a lead-free, ROHS compliant.

Qualification Information†

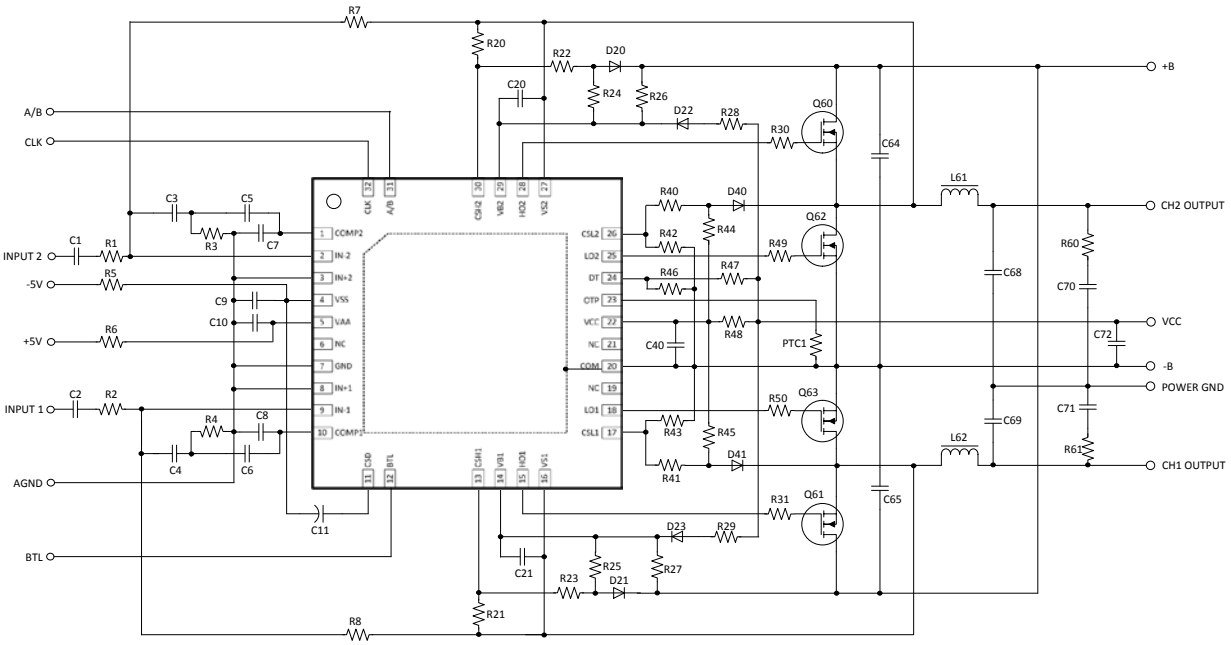
Qualification Level		Industrial††
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2†††, 260°C (per IPC/JEDEC J-STD-020)
ESD	**Machine Model**	Class B (per JEDEC standard EIA/JESD22-A115)
	Human Body Model	Class 1B (per EIA/JEDEC standard JESD22-A114)
	Charge Device Model	Class 0B (per EIA/JEDEC standard JESD22-C101)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at Infineon web site http://www.infineon.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon Technology sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon Technology sales representative for further information.

Typical Connection Diagram



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{Bn}	High side floating supply voltage	-0.3	415	V
V_{Sn}	High side floating supply voltage††, n=1-2	V_{Bn} -15	V_{Bn} +0.3	V
V_{Hon}	High side floating output voltage, n=1-2	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CSHn}	CSH pin input voltage, n=1-2	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CC}	V_{CC} low side fixed supply voltage††	-0.3	15.5	V
V_{Lon}	Low side output voltage, n=1-2	-0.3	V_{CC} +0.3	V
V_{AA}	Floating input positive supply voltage††	(See I_{AAZ})	210	V
V_{SS}	Floating input negative supply voltage††	-1 (See I_{SSZ})	V_{AA} +0.3	V
V_{GND}	Floating input supply ground voltage	V_{SS} -0.3	V_{AA} +0.3	V
I_{IN-n}	Inverting input current †, n=1-2	-	±3	mA
V_{CSD}	SD pin input voltage	V_{GND} -0.3	V_{AA} +0.3	V
V_{COMPn}	COMP pin input voltage, n=1-2	V_{SS} -0.3	V_{AA} +0.3	V
V_{CLK}	CLK pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{BTL}	BTL pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{AB}	A/B pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	V
V_{OTP}	OTP pin input voltage	-0.3	V_{CC} +0.3	V
V_{CSLn}	CSL pin input voltage, n=1-2	-0.3	V_{CC} +0.3	V
I_{AAZ}	Floating input positive supply zener clamp current††	-	10	mA
I_{CCZ}	Low side V_{CC} supply zener clamp current††	-	10	mA
I_{BSZn}	Floating supply zener clamp current††, n=1-2	-	10	mA
dV_{Sn}/dt	Allowable Vs voltage slew rate, n=1-2	-	50	V/ns
dV_{SS}/dt	Allowable Vss voltage slew rate†††	-	50	V/ms

Absolute Maximum Ratings (Cont'd)

Symbol	Definition	Min.	Max.	Units
Pd	Maximum power dissipation @ $T_A \leq +25°C$ ††††	-	6	W
Rth_{JA}	Thermal resistance, Junction to ambient ††††	-	20	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead temperature (Soldering, 10 seconds)	-	300	°C

† IN-1 and IN-2 contain clamping diode to GND.
†† VAA-VSS, VCC-COM, VB1-VS1 and VB2-VS2 contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.
††† For the rising and falling edges of step signal of 10V. VSS=15V to 200V.
†††† According to JESD51-5. JEDEC still air chamber.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at V_{AA}-V_{SS}=10V, V_{CC} =12V, COM2=COM and V_B-V_S=12V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition	Min.	Max.	Units
V_{Bn}	High side floating supply absolute voltage, n=1-2	V_{Sn} +10	V_{Sn} +14	V
V_{Sn}	High side floating supply offset voltage	(Note1)	400	V
V_{AA}	Floating input supply voltage	V_{SS} + 4.5	V_{SS} + 15	V
I_{AAZ}	Floating input positive supply zener clamp current	1	11	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{Hon}	High side floating output voltage, n=1-2	Vs	V_B	V
V_{CC}	Low side fixed supply voltage	10	14	V
V_{Lon}	Low side output voltage, n=1-2	0	V_{CC}	V
V_{GND}	GND pin input voltage	V_{SS} (Note2)	V_{AA} (Note2)	V
V_{IN-n}	Inverting input voltage, n=1-2	V_{GND} -0.5 (Note2)	V_{GND} +0.5 (Note2)	V
V_{CSD}	CSD pin input voltage	V_{GND}	V_{AA}	V
V_{COMPn}	COMP pin input voltage, n=1-2	V_{SS}	V_{AA}	V
C_{COMPn}	COMP pin phase compensation capacitor to GND, n=1-2	2.2	-	nF
V_{CLK}	CLK pin input voltage	V_{GND}	V_{AA}	V
V_{BTL}	BTL pin input voltage	V_{SS}	V_{AA}	V
V_{AB}	A/B pin input voltage	V_{SS}	V_{AA}	V
V_{DT}	DT pin input voltage	0	V_{CC}	V
V_{OTP}	OTP pin input voltage	0	V_{CC}	V
V_{CSHn}	CSH pin input voltage, n=1-2	V_{Sn}	V_{Bn}	V
V_{CSLn}	CSL pin input voltage, n=1-2	0	V_{CC}	V
dV_{SS}/dt	Allowable V_{SS} voltage slew rate upon power-up (Note3)	-	50	V/ms
f_{SW}	Switching frequency	-	800	kHz
f_{CLK}	CLK frequency (Note4)	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

(Note 1) Logic operational for Vsn equal to –5V to +400V. Logic state held for Vsn equal to –5V to –VBSn.
(Note 2) GND input voltage is limited by IIN-n.
(Note 3) Vss ramps up from 0V to 200V.
(Note 4) The CLK input frequency needs to be within +/-10% of self-oscillating frequency in order to synchronize PWM in a typical self-oscillating application.

Electrical Characteristics

V_{CC}= V_{BS1}=V_{BS2} =V_{DT}=12V, V_{SS}=V_{S1}=V_{S2}=COM =0V, V_{GND}=5V, V_{AA}=V_{BTL}=V_{AB}=10V, C_L=1nF and T_A=25°C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	6	mA	V_{DT}=V_{CC}
V_{CLAMPL}	Low side zener diode clamp voltage	14.7	15.3	16.2	V	I_{CC}=5mA
High Side Floating Supply						
UV_{BS+n}	High side well UVLO positive threshold, n=1-2	8.0	8.5	9.0	V	
UV_{BS-n}	High side well UVLO negative threshold, n=1-2	7.8	8.3	8.8	V	
UV_{BSHYSn}	UV_{BS} hysteresis, n=1-2	-	0.2	-	V	
I_{QBSn}	High side quiescent current, n=1-2	-	-	1	mA	
I_{LKHn}	High to Low side leakage current, n=1-2	-	-	50	µA	V_{Bn}=V_{Sn} =400V
$V_{CLAMPHn}$	High side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I_{BSn}=5mA
Floating Input Supply						
UV_{AA+}	V_{AA} floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	GND pin floating
UV_{AA-}	V_{AA} floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7	V	GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	GND pin floating
I_{QAASD}	Floating Input positive quiescent supply current in shutdown mode	-	2.5	4	mA	V_{CSD} =V_{GND}
I_{QAA0}	Floating Input positive quiescent supply current, positive input	-	8	11	mA	V_{IN-} = VSS+5.2V
I_{QAA1}	Floating Input positive quiescent supply current, negative input	-	5	8	mA	V_{IN-} = VSS+4.8V
I_{QAAST}	Floating Input positive quiescent supply current in start-up mode	-	6	8	mA	V_{CSD} = V_{GND}+2.5V
I_{QAABTL}	Floating Input positive quiescent supply current, negative input	-	5	8	mA	V_{IN-} = VSS+4.8V, VBTL=GND
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100V
V_{CLAMPM}	Floating supply zener diode clamp voltage	14.7	15.3	16.2	V	I_{AA}=5mA, V_{CSD} =V_{GND}

Electrical Characteristics (Cont'd)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Audio Input (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_{S1}=V_{S2}=CSH1=CSH2=-5V, DT=-5V)						
V_{Osn}	CHn input offset voltage, n=1-2	-18	0	18	mV	
I_{BINn}	CHn input bias current, n=1-2	-	-	40	nA	
GBWn	CHn small signal bandwidth, n=1-2	-	5 Note 1	-	MHz	C_{COMPn}=2.2nF, Rfn=10k, Note 1
V_{COMPn}	CHn OTA Output voltage, n=1-2	V_{AA}-1	-	V_{SS}+1	V	
g_{mn}	CHn OTA transconductance, n=1-2	80	200	260	mS	V_{IN-n}=10mV
G_{Vn}	CHn OTA gain, n=1-2	60	-	-	dB	
V_{Nrmsn}	CHn OTA input noise voltage, n=1-2	-	250	-	mVrms	BW=20kHz, Resolution BW=22Hz Fig.5
SRn	CHn slew rate, n=1-2	-	±5	-	V/us	C_{COMPn}=2.2nF
CMRRn	CHn common-mode rejection ratio, n=1-2	-	60	-	dB	
PSRRn	CHn supply voltage rejection ratio, n=1-2	-	65	-	dB	
PWM Comparator						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA} – V_{SS})/2	-	V	
f_{OTAn}	CHn COMP pin star-up local oscillation frequency, n=1-3	-	0.6	-	MHz	V_{CSD} =V_{GND}+2.5V
Clock Input (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_{S1}=V_{S2}=CSH1=CSH2=-5V, DT=-5V)						
V_{IHCLK}	CLK high level input threshold	8		-	V	
V_{ILCLK}	CLK low level input threshold	-		2	V	
I_{IHCLK+}	CLK high level input bias current	-35		35	µA	V_{CLK}=V_{AA}
I_{ILCLK-}	CLK low level input bias current	-45		45	µA	V_{CLK}=V_{SS}
V_{THAB}	AB high level input threshold	0.40x (V_{AA}-GND)	0.50x (V_{AA}-GND)	0.60x (V_{AA}-GND)	V	
I_{IHAB+}	AB high level input bias current	-35		35	µA	V_{AB}=V_{AA}
I_{ILAB-}	AB high level input bias current	-45		45	µA	V_{AB}=GND
BTL Mode (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_{S1}=V_{S2}=CSH1=CSH2=-5V, DT=-5V)						
V_{THBTL}	BTL high level input threshold	0.40x (V_{AA}-GND)	0.50x (V_{AA}-GND)	0.60x (V_{AA}-GND)	V	
I_{IHBTL+}	BTL high level input bias current	-35		35	µA	V_{BTL}=V_{AA}
I_{ILBTL-}	BTL high level input bias current	-45		45	µA	V_{BTL}=GND

Electrical Characteristics (Cont'd)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Protection						
Vth_{OCLn}	CHn low side OC threshold in V_{CSLn}, n=1-2	1.1	1.2	1.3	V	
Vth_{OCHn}	CHn high side OC threshold in V_{CSHn}, n=1-2	1.1+ Vs	1.2+ Vs	1.3+ Vs	V	Vs=400V
Vth1	CSD pin shutdown release threshold	$0.52xV_{AA-GND}$	$0.68xV_{AA-GND}$	$0.84xV_{AA-GND}$	V	
Vth2	CSD pin self reset threshold	$0.26xV_{AA-GND}$	$0.30xV_{AA-GND}$	$0.34xV_{AA-GND}$	V	
I_{CSD+}	CSD pin discharge current	70	100	130	µA	$V_{CSD} = V_{GND} + 2.4V$
I_{CSD-}	CSD pin charge current	70	100	130	µA	$V_{CSD} = V_{GND} + 2.4V$
t_{SSDn}	CHn shutdown propagation delay from $V_{CSD} < V_{GND}$+ Vth1 to Shutdown, n=1-2	-	140	250	ns	
t_{OCHn}	CHn propagation delay time from $V_{CSHn} > Vth_{OCHn}$ to Shutdown, n=1-2	-	400	500	ns	
t_{OCLn}	CHn propagation delay time from Vsn> Vth_{OCL} to Shutdown, n=1-2	-	270	350	ns	
V_{OTP}	OTP pin input threshold	-	2.8	-	V	
I_{OTP}	OTP bias sourcing current	-	0.6	-	mA	OTPn=0V

Electrical Characteristics (Cont'd)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver						
Io+n	CHn output high short circuit current (Source) , n=1-2	-	0.5	-	A	Vo=0V, PW≤10µS, Note 1
Io-n	CHn output low short circuit current (Sink) , n=1-2	-	0.6	-	A	Vo=12V, PW≤10µS, Note 1
V_{OLn}	CHn low level out put voltage LO – COM, HO - VS, n=1-2	-	-	0.1	V	Io=0A
V_{OHn}	CHn high level out put voltage VCC – LO, VB - HO, n=1-2	-	-	1.4	V	
Ton0n	CHn high and low side turn-on propagation delay, n=1-2	-	385	-	ns	$V_{DT} = V_{CC}$
Toff0n	CHn high and low side turn-off propagation delay, n=1-2	270	340	410	ns	
Toffskwn	CHn Toff skew, Toffhon – Tofflon, n=1-2	-30	0	30	ns	
tr	Turn-on rise time	-	12	25	ns	
tf	Turn-off fall time	-	12	25	ns	
DT1n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LnO turn-on (DT_{HO-LO})	30	45	65	ns	$V_{DT}>V_{DT1}$, V_{DTM}=COM
DT2n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	45	65	85	ns	$V_{DT1}>V_{DT}> V_{DT2}$, V_{DTM}=COM
DT3n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	60	85	110	ns	$V_{DT2}>V_{DT}> V_{DT3}$, V_{DTM}=COM
DT4n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HO turn-off to LOn turn-on (DT_{HO-LO})$V_{DT}= V_{DT4}$	80	105	145	ns	$V_{DT}<V_{DT3}$, V_{DTM}=COM
V_{DT1}	DT mode select threshold 1	0.51xVcc	0.57xVcc	0.63xVcc	V	V_{DTM}=COM
V_{DT2}	DT mode select threshold 2	0.32xVcc	0.36xVcc	0.40xVcc	V	
V_{DT3}	DT mode select threshold 3	0.21xVcc	0.23xVcc	0.25xVcc	V	

Note 1 Guaranteed by design, but not tested in production.

Waveform Definitions

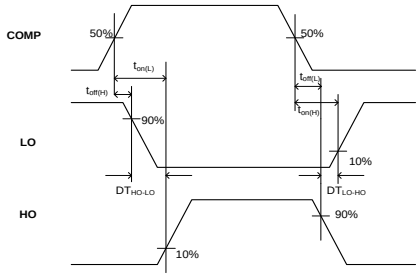


Figure 1 Switching Time Waveform Definitions

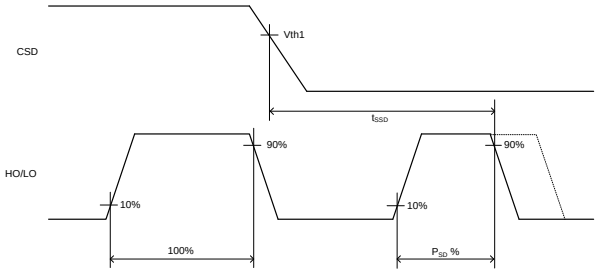


Figure 2 CSD to Shutdown Waveform Definitions

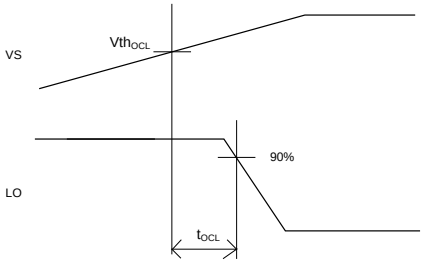


Figure 3 V_S > Vth_{OCL} to Shutdown Waveform

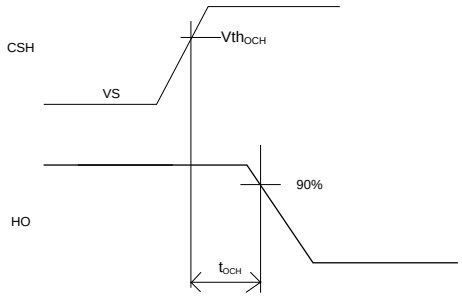


Figure 4 V_{CSH} > Vth_{OCH} to Shutdown Waveform

Waveform Definitions (Cont'd)

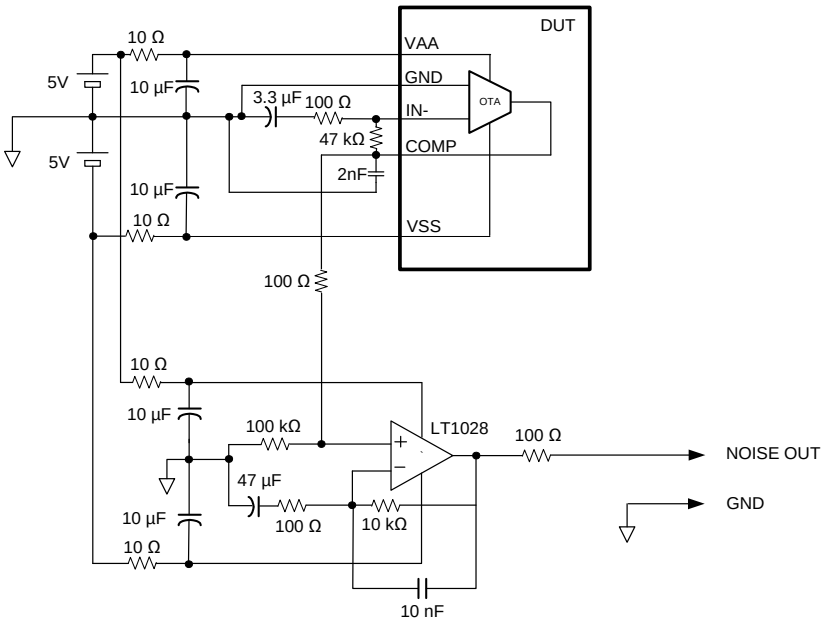
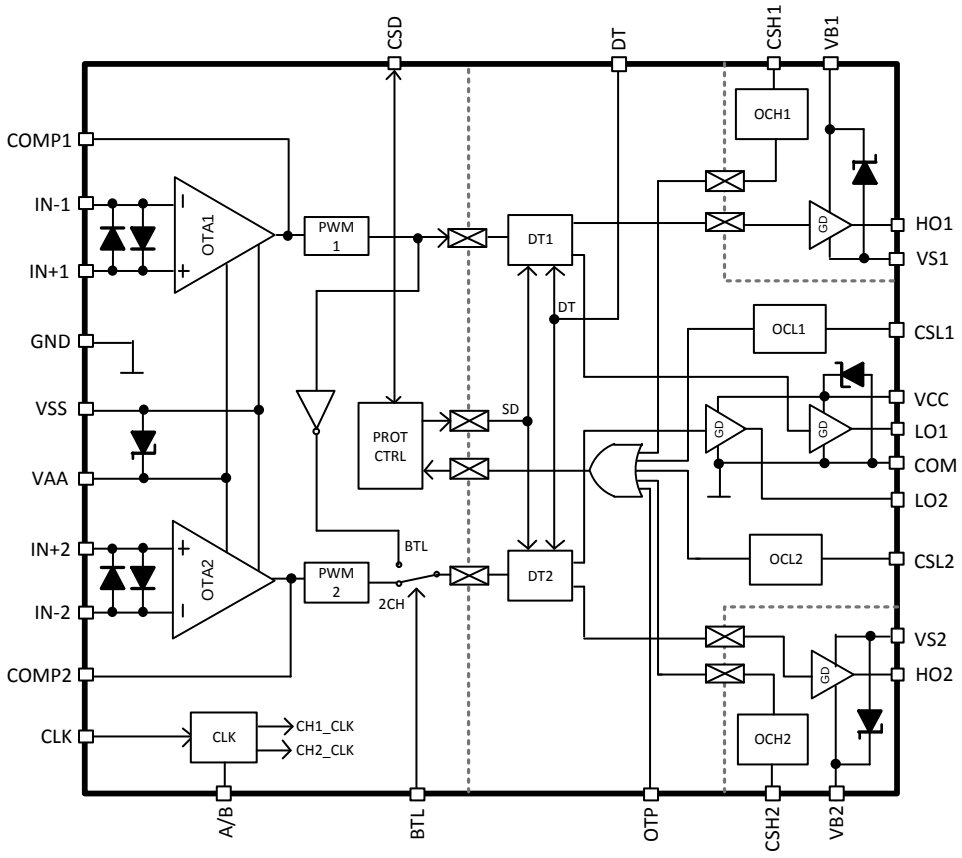
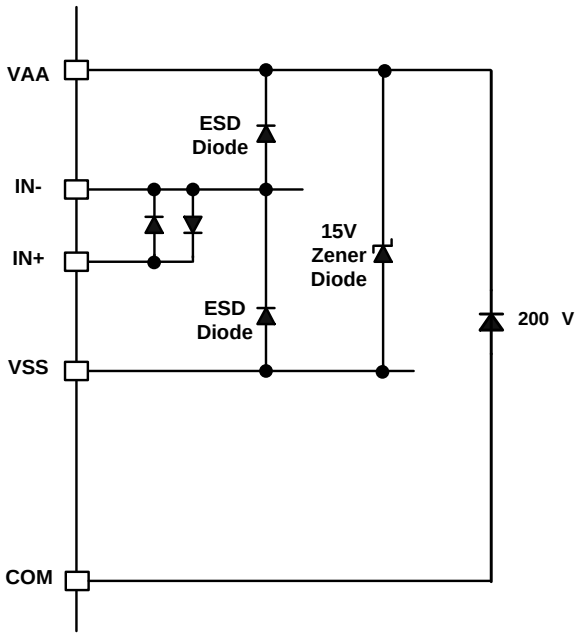


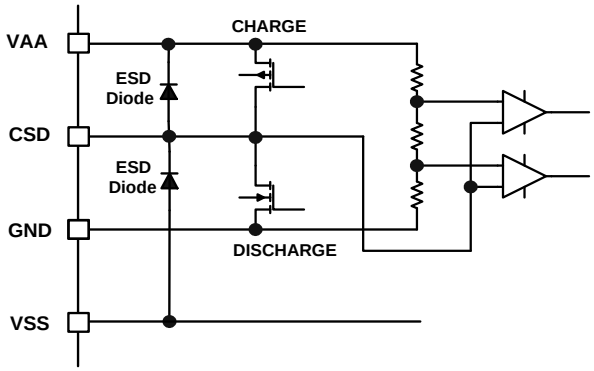
Figure 5: OTA input noise voltage mesurent circuit

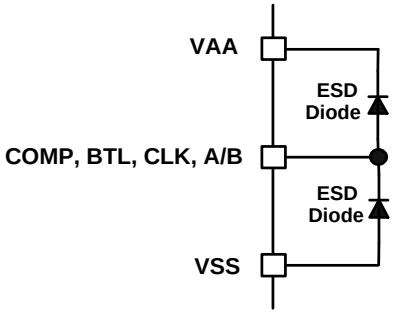
Functional Block Diagram

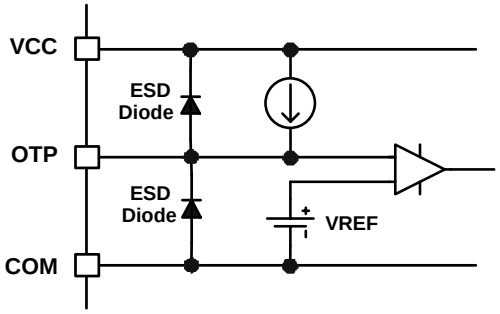


Input/Output Pin Equivalent Circuit Diagrams

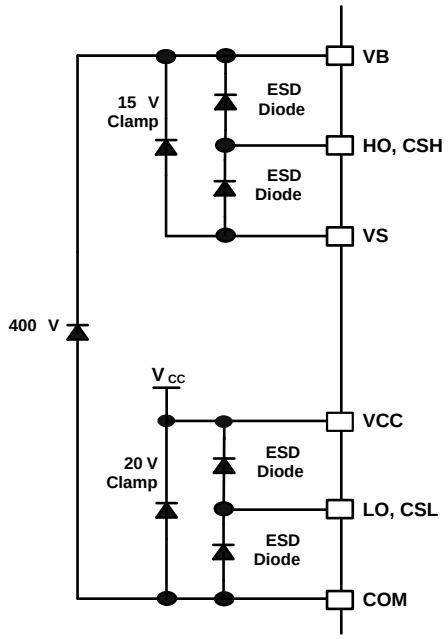








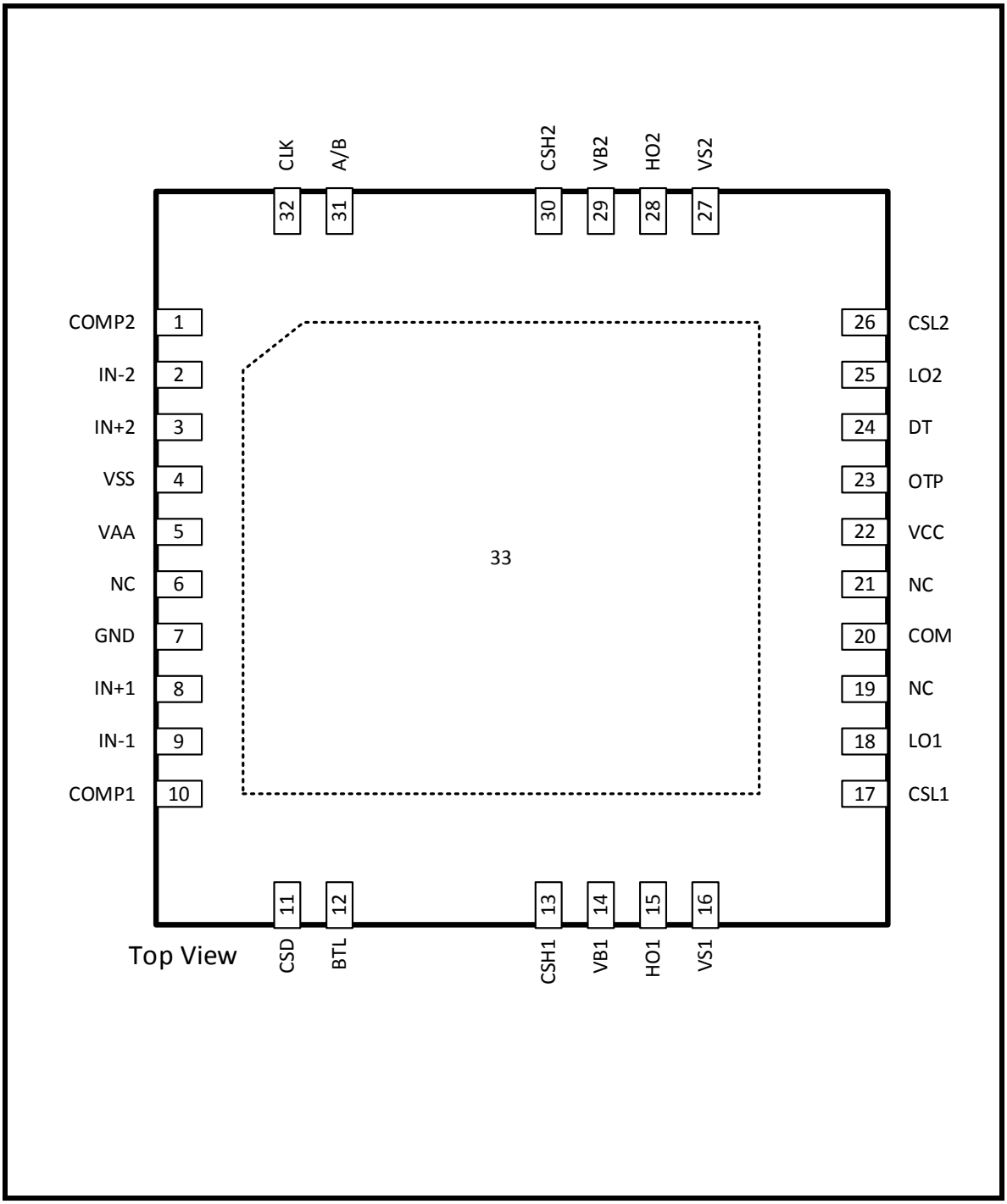
Input/Output Pin Equivalent Circuit Diagrams (Cont'd)



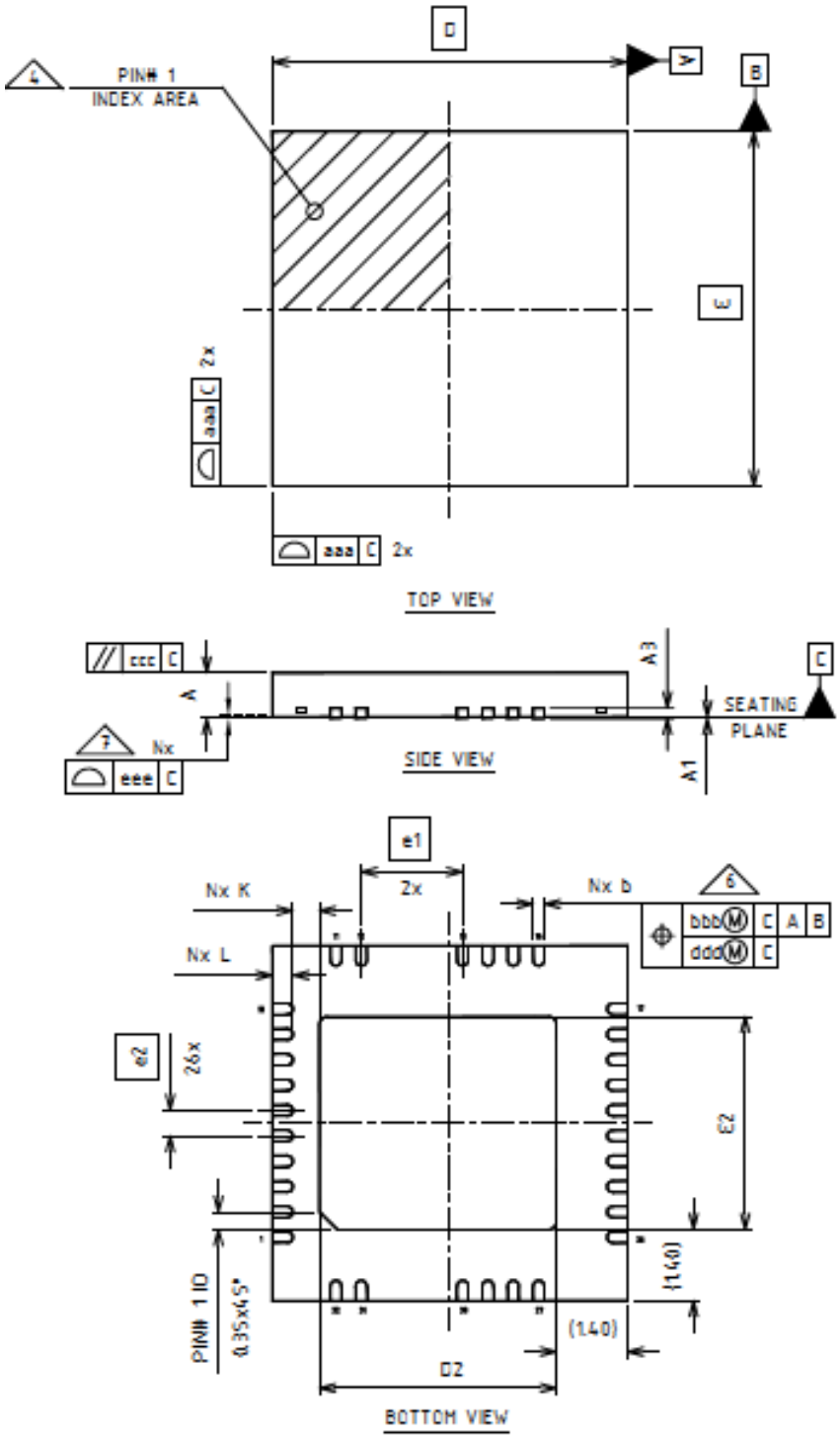
Lead Definitions

Pin #	Symbol	I/O	Description
1	COMP2	O	CH2 PWM comparator input
2	IN-2	I	CH2 inverting analog input
3	IN+2	I	CH2 non-inverting analog input
4	VSS	I	Floating input negative supply
5	VAA	I	Floating input positive supply
6	NC		
7	GND	I	Input reference GND
8	IN+1	I	CH1 non-inverting analog input
9	IN-1	I	CH1 inverting analog input
10	COMP1	O	CH1 PWM comparator input
11	CSD	I/O	Protection control
12	BTL	I	BTL mode select (VAA: 2CH mode, GND-VSS: BTL mode)
13	CSH1	I	CH1 High side over current sensing input, referenced to VS1
14	VB1	I	CH1 High side floating supply
15	HO1	O	CH1 High side output
16	VS1	I	CH1 High side floating supply return
17	CSL1	I	CH1 Low side over current sensing input, referenced to COM
18	LO1	O	CH1 Low side output
19	NC		
20	COM	I	Low side gate drive supply return
21	NC		
22	VCC	I	Low side gate drive supply
23	OTP	I	OTP sensor input
24	DT	I	Deadtime program, reference to COM
25	LO2	O	CH2 Low side output
26	CSL2	I	CH2 Low side over current sensing input, referenced to COM
27	VS2	I	CH2 High side floating supply return
28	HO2	O	CH2 High side output
29	VB2	I	CH2 High side floating supply
30	CSH2	I	CH2 High side over current sensing input, referenced to VS2
31	A/B	I	Clock phase select (VAA: In-phase, VSS: Out-of-phase)
32	CLK	I	Clock input, reference to GND
33	SUB	I	Internally connected to COM (Do not use as supply return)

Lead Assignments (MLPQ_7x7mm_32L)



Package Details:



Dimension Table				
Thickness / Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.203 Ref	---	
b	0.18	0.25	0.30	6
D	7.00 BSC			
E	7.00 BSC			
e1	2.00 BSC			
e2	0.50 BSC			
D2	4.525	4.675	4.775	
E2	4.05	4.20	4.30	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	32			3
ND	6			5
NE	10			5
NOTES	1, 2			
LF DWG NO.	B-4396			
REV.	1			

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

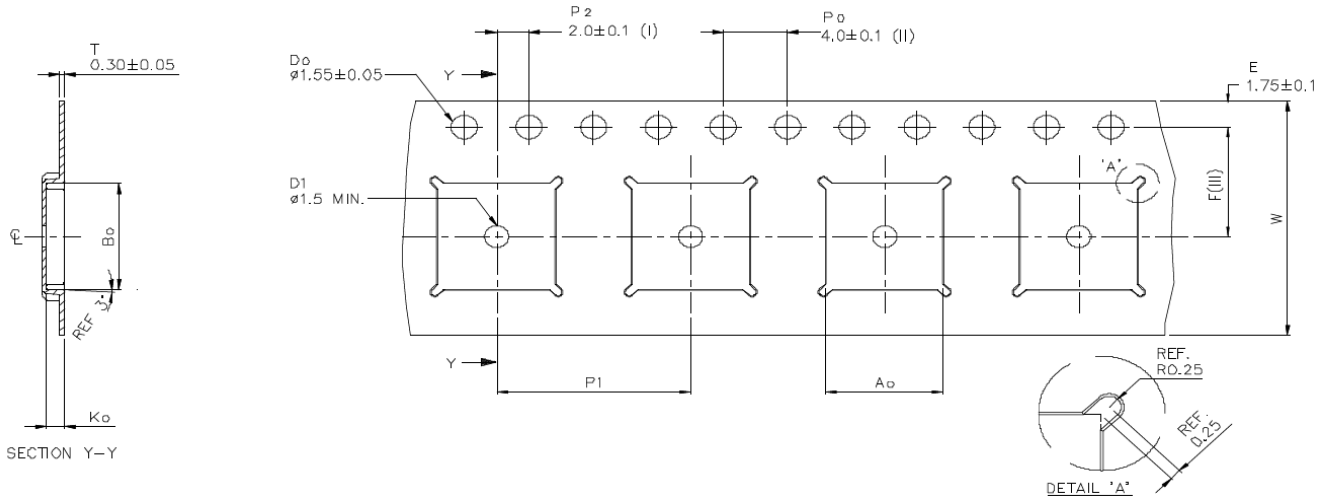
4. The location of the marked terminal #1 identifier is within the hatched area.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

7. Coplanarity applies to the terminals and all other bottom surface metallization.

Tape and Reel Details:



Ao	7.25 +/−0.1
Bo	7.25 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

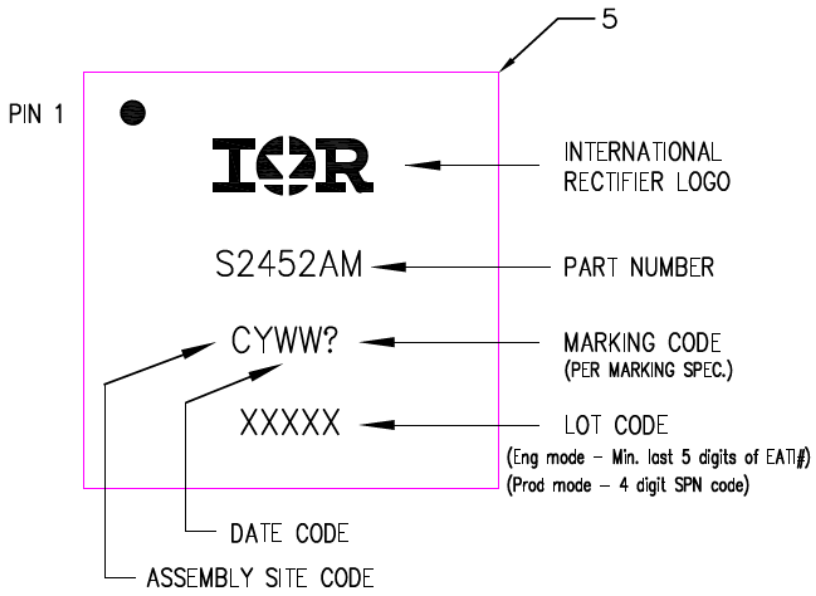
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^9 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Board Mounting Information

Reliability of products in PQFN package is subject to board mounting process. Soldering process is critical. Refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application Note for specific soldering methods.

Part Marking Information



TOP MARKING (LASER)

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