MOSFET

OptiMOS™ Small Signal Transistor, -60 V

SOT-23

Features

- P-Channel
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Logic Level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

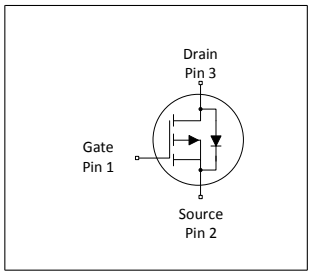


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-60	V
$R_{DS(on),max}$	1.7	Ω
I_D	-0.3	A

Type / Ordering Code	Package	Marking	Related Links
ISS17EP06LM	PG-SOT23	DL	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	-	-	-0.30	A	V_{GS}=-10 V, T_A=25 °C
Continuous drain current[1]	I_D	- - -	- - -	-0.21 -0.29 -0.18	A	V_{GS}=-10 V, T_A=100 °C V_{GS}=-4.5 V, T_A=25 °C V_{GS}=-4.5 V, T_A=100 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	-1.2	A	T_A=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	25	mJ	I_D=-0.3 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	0.36	W	T_A=25 °C, R_{THJA}=350 °C/W
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - soldering point, bottom	R_{thJS}	-	-	120	°C/W	-
Device on PCB, minimum footprint[1]	R_{thJA}	-	-	350	°C/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick), minimum footprint. PCB is vertical in still air.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	V_{GS}=0 V, I_D=-250 µA
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2	V	V_{DS}=V_{GS}, I_D=-34 µA
Zero gate voltage drain current	I_{DSS}	- -	-0.1 -10	-1 -100	µA	V_{DS}=-60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1356 1634	1700 2200	mΩ	V_{GS}=-10 V, I_D=-0.3 A V_{GS}=-4.5 V, I_D=-0.29 A
Gate resistance	R_G	-	67	-	Ω	-
Transconductance	g_{fs}	-	0.64	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=-0.3 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	55	-	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Output capacitance	C_{oss}	-	9	-	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	3	-	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-0.3 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	3	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-0.3 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-0.3 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	9	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-0.3 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-0.16	-	nC	V_{DD}=-30 V, I_D=-0.3 A, V_{GS}=0 to -10 V
Gate charge at threshold	$Q_{g(th)}$	-	-0.08	-	nC	V_{DD}=-30 V, I_D=-0.3 A, V_{GS}=0 to -10 V
Gate to drain charge	Q_{gd}	-	-0.45	-	nC	V_{DD}=-30 V, I_D=-0.3 A, V_{GS}=0 to -10 V
Switching charge	Q_{sw}	-	-0.53	-	nC	V_{DD}=-30 V, I_D=-0.3 A, V_{GS}=0 to -10 V
Gate charge total	Q_g	-	-1.79	-	nC	V_{DD}=-30 V, I_D=-0.3 A, V_{GS}=0 to -10 V
Gate plateau voltage	$V_{plateau}$	-	-3.00	-	V	V_{DD}=-30 V, I_D=-0.3 A, V_{GS}=0 to -10 V
Output charge	Q_{oss}	-	-0.58	-	nC	V_{DD}=-30 V, V_{GS}=0 V

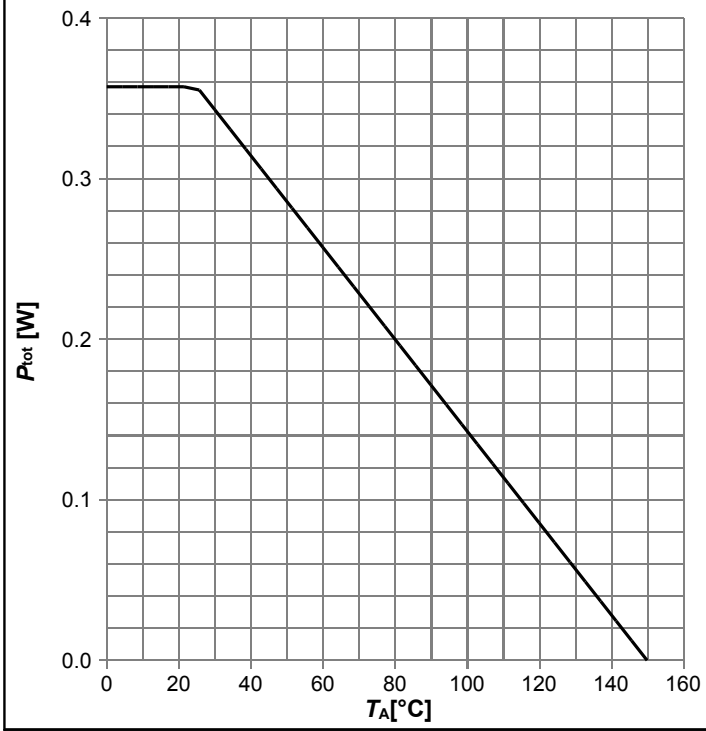
[1)] See diagram ,Gate charge waveforms, for gate charge parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-0.3	A	T_A=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-1.2	A	T_A=25 °C
Diode forward voltage	V_{SD}	-	-0.8	-1.2	V	V_{GS}=0 V, I_F=-0.3 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	14	-	ns	V_R=-30 V, I_F=-0.3 A, di_F/dt=-100 A/µs
Reverse recovery charge	Q_{rr}	-	-10	-	nC	V_R=-30 V, I_F=-0.3 A, di_F/dt=-100 A/µs

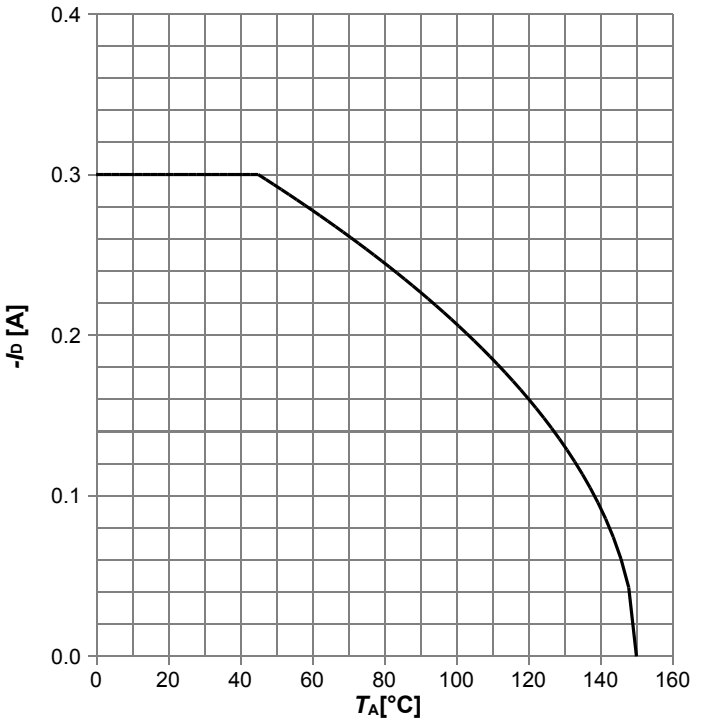
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



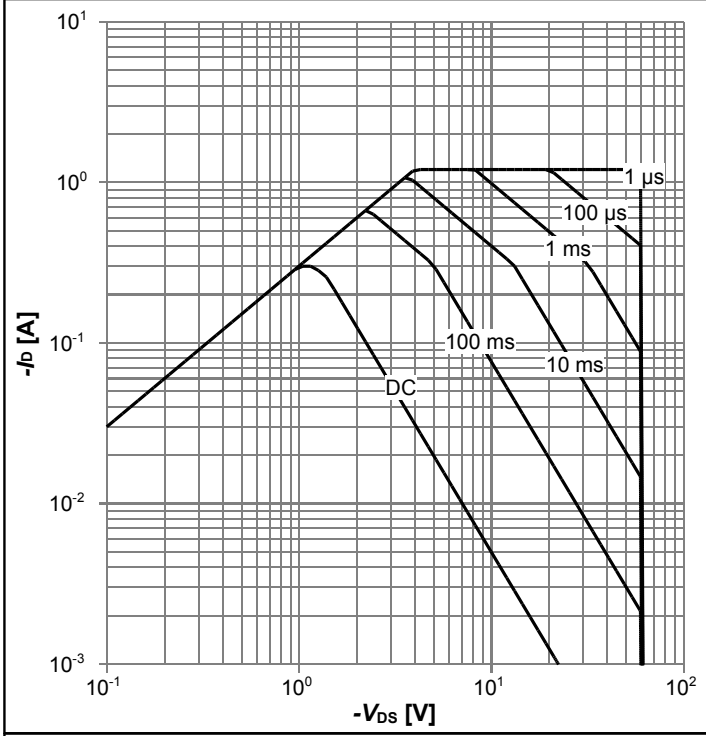
P_{tot}=f(T_A)

Diagram 2: Drain current



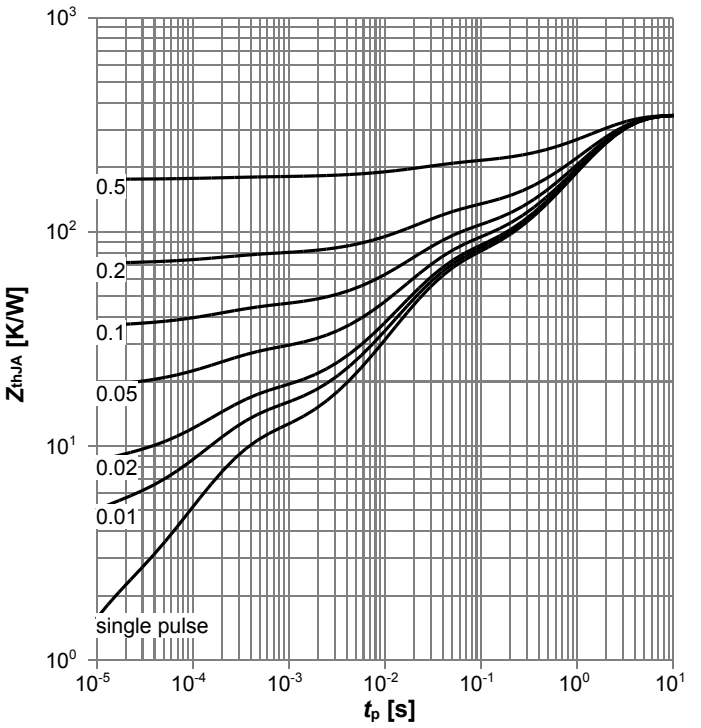
I_D=f(T_A); |V_{GS}|≥10 V

Diagram 3: Safe operating area



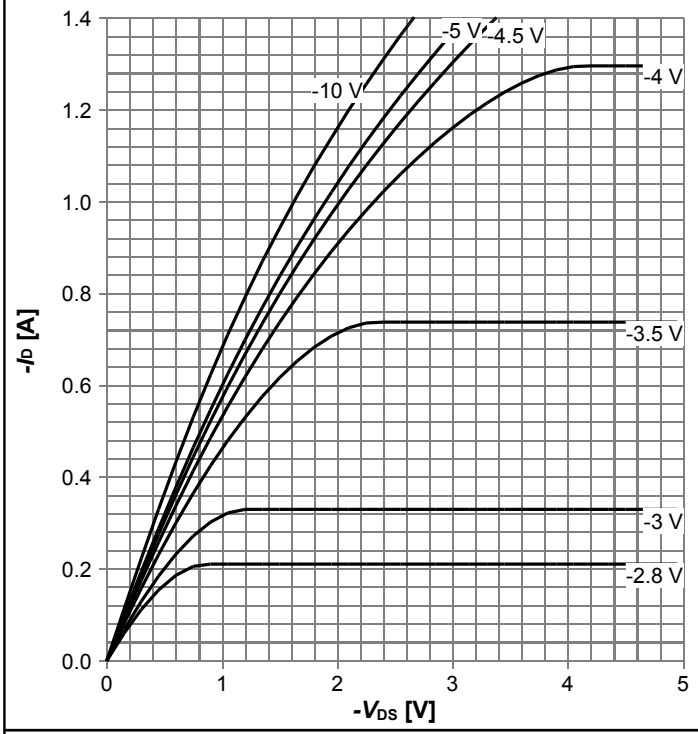
I_D=f(V_{DS}); T_A=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



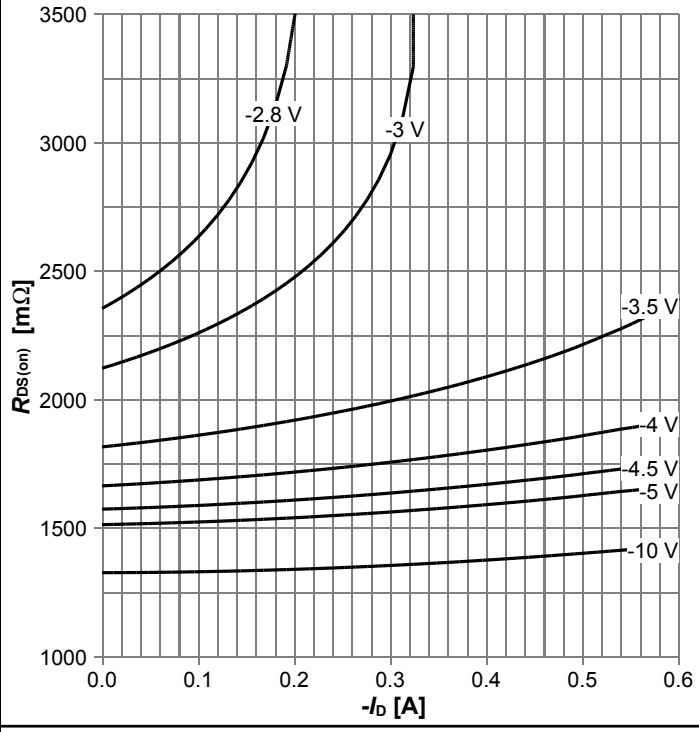
Z_{thJA}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



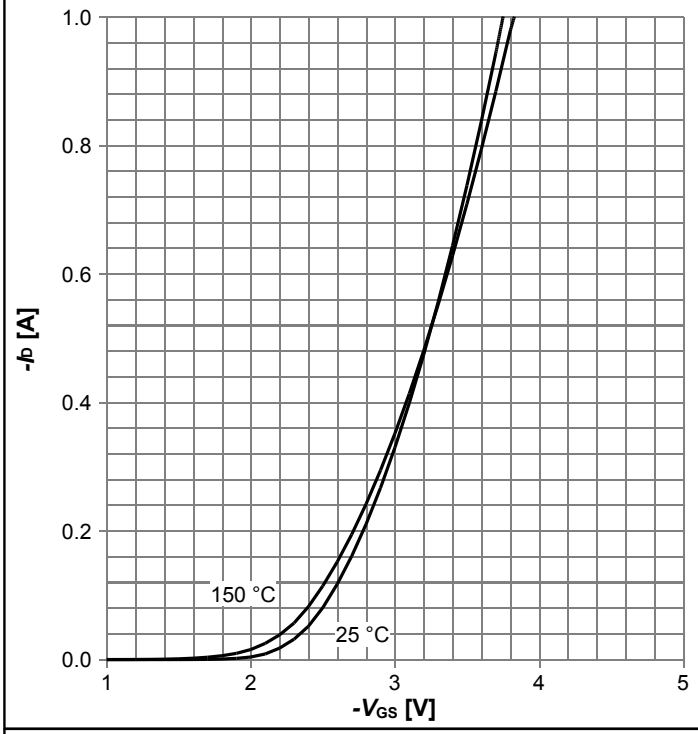
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



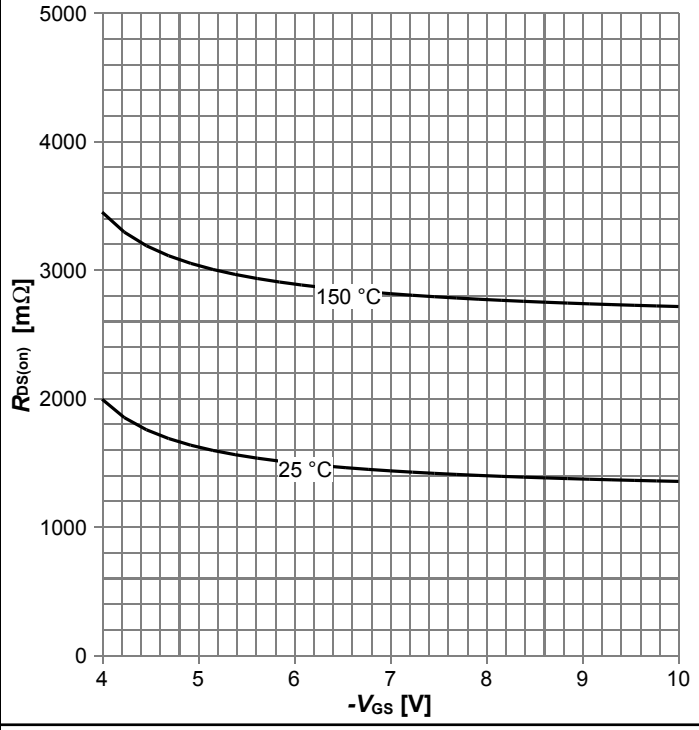
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



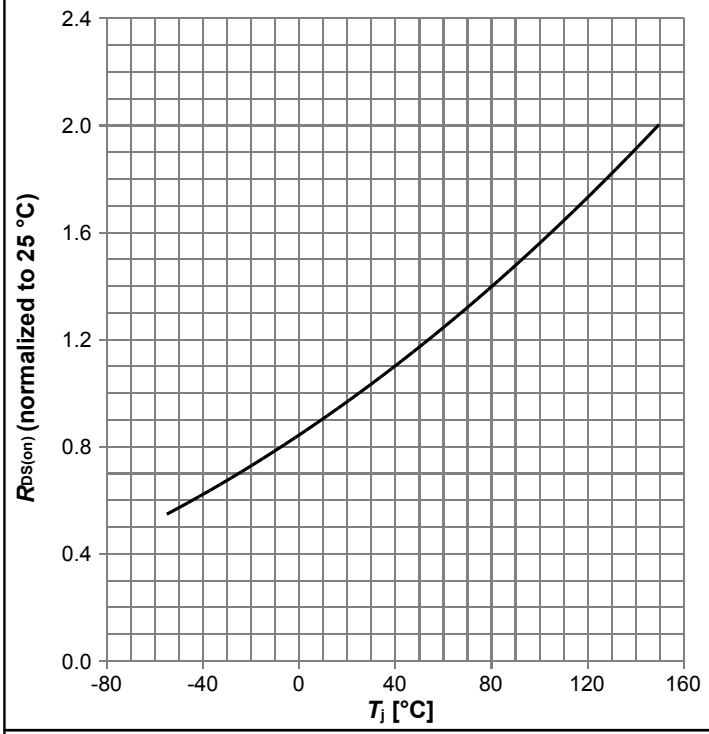
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



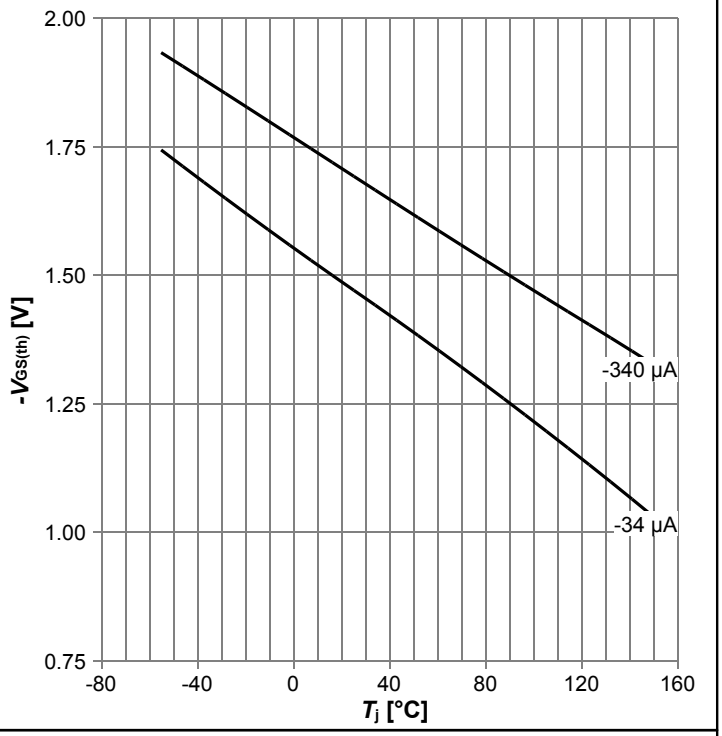
$R_{DS(on)}=f(V_{GS})$, $I_D=-0.3$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



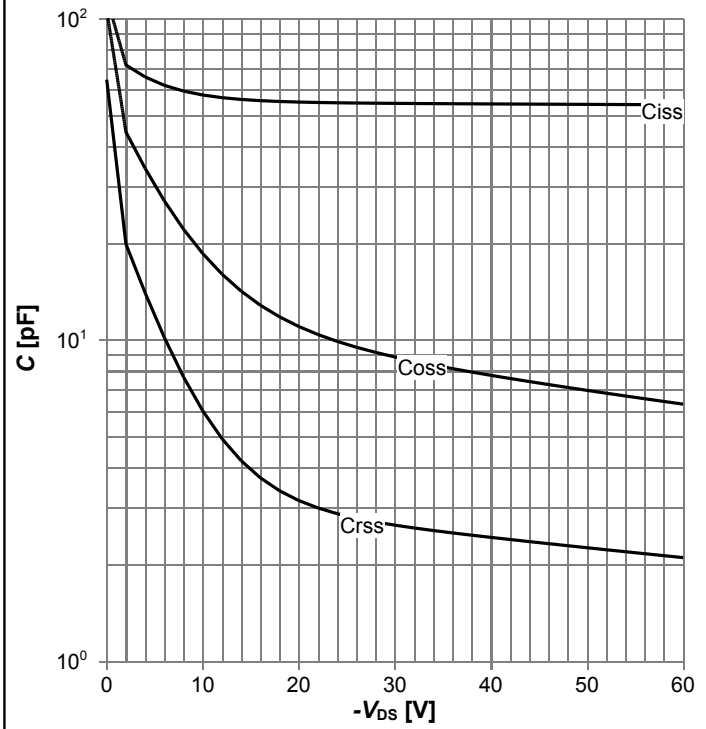
$R_{DS(on)}$=f(T_j), I_D=-0.3 A, V_{GS}=-10 V

Diagram 10: Typ. gate threshold voltage



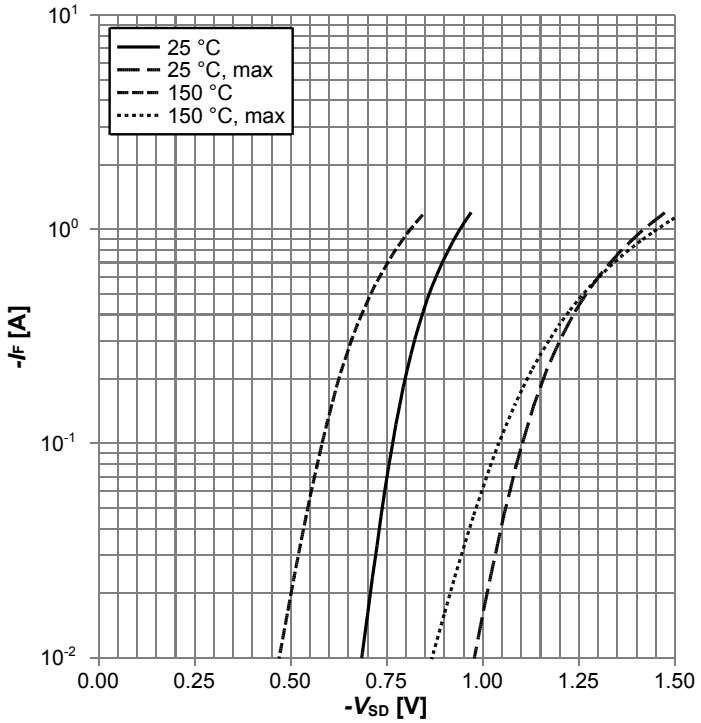
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



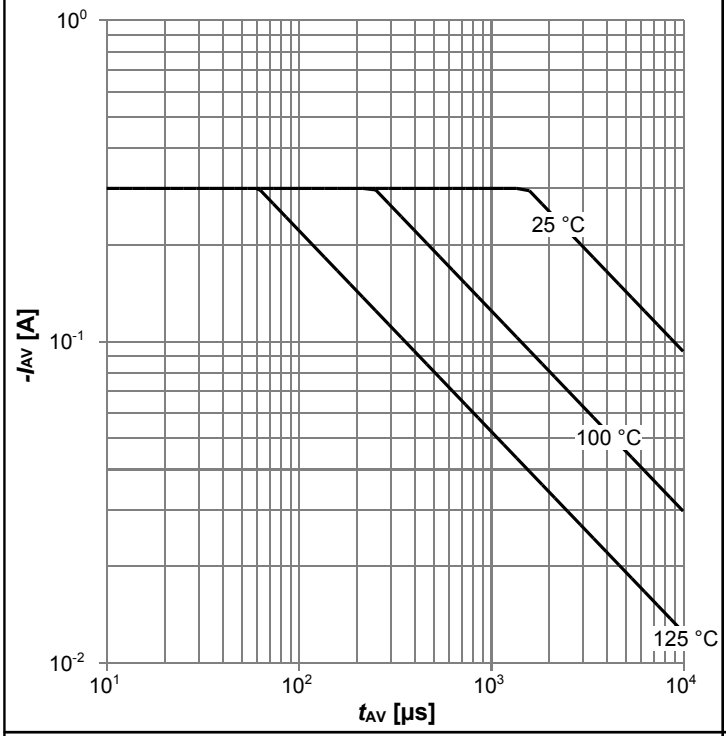
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



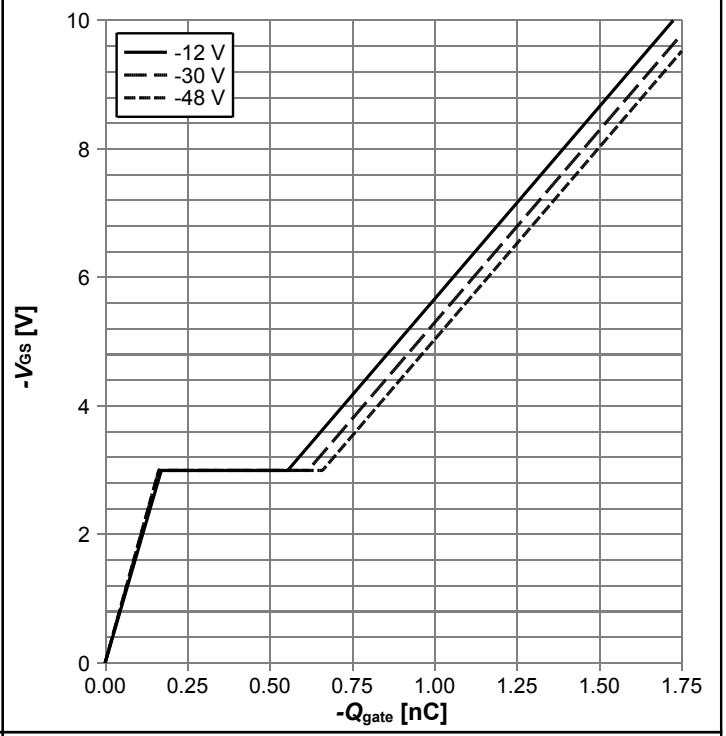
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



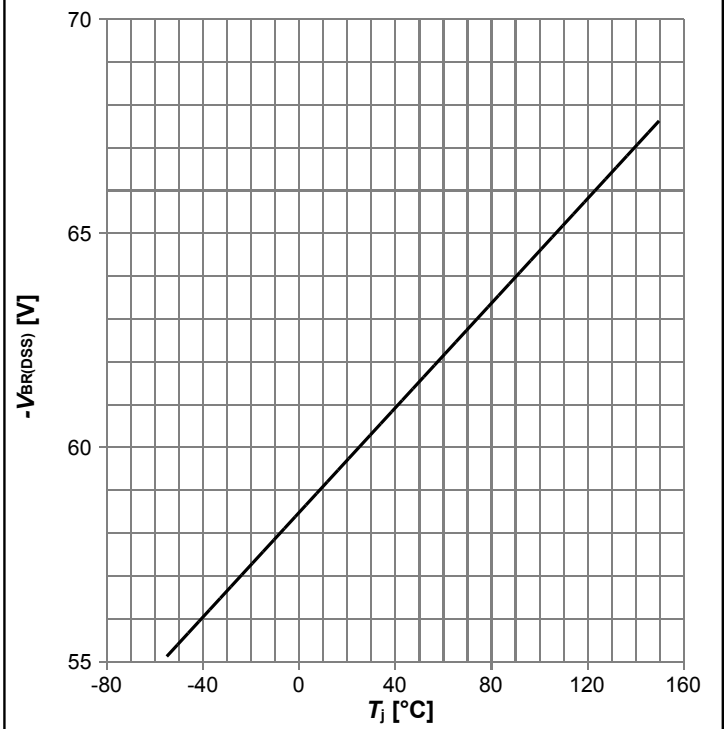
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



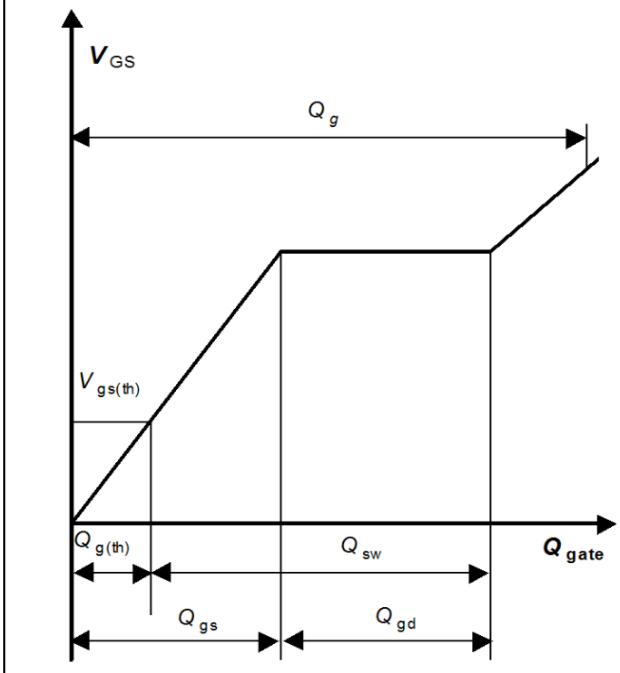
V_{GS}=f(Q_{gate}), I_D=-0.3 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



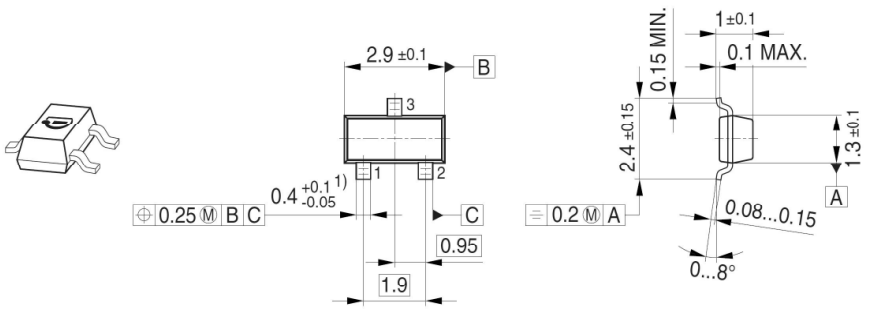
$V_{BR(DSS)}$=f(T_j); I_D=-250 µA

Diagram Gate charge waveforms



5 Package Outlines

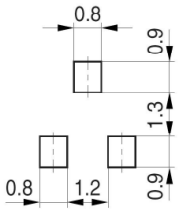
Package Outline



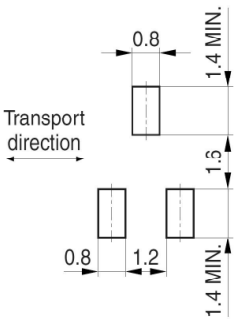
1) Lead width can be 0.6 max. in dambar area

Foot Print

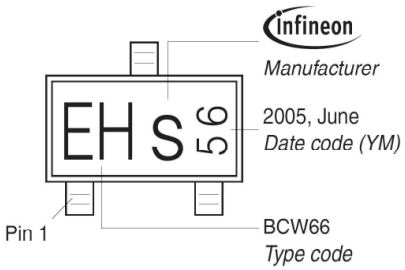
Soldering Type: Reflow Soldering



Soldering Type: Wave Soldering



Marking Layout (Example)



Tape and Reel

Reel ø180 mm: 3.000 Pieces/Reel
Reels/Box: 1 x 3.000 = 3.000
Reels/Box: 10 x 3.000 = 30.000

Reel ø330 mm: 10.000 Pieces/Reel
Reels/Box: 1 x 10.000 = 10.000

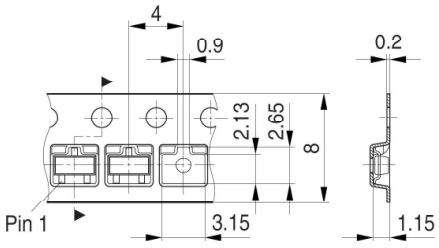


Figure 1 Outline PG-SOT23, dimensions in mm

Revision History

ISS17EP06LM

Revision: 2019-03-25, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2019-03-25	Release of final version

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