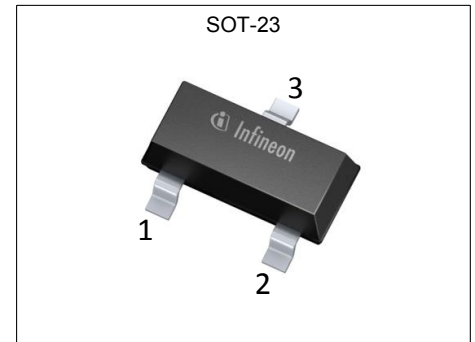


MOSFET

OptiMOS™ Small Signal Transistor, -60 V

Features

- P-Channel
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5$ V
- 100% avalanche tested
- Logic Level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

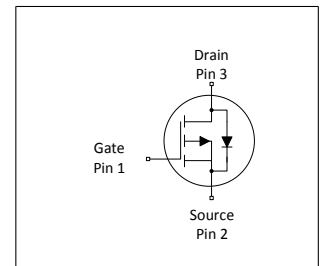


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-60	V
$R_{DS(on),max}$	5.5	Ω
I_D	-0.18	A



Type / Ordering Code	Package	Marking	Related Links
ISS55EP06LM	PG-SOT23	CL	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-0.18	A	$V_{GS}=-10\text{ V}$, $T_A=25\text{ °C}$
Continuous drain current ¹⁾	I_D	-	-	-0.12 -0.16 -0.10	A	$V_{GS}=-10\text{ V}$, $T_A=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_A=25\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_A=100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	-0.72	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	4.3	mJ	$I_D=-0.18\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	0.4	W	$T_A=25\text{ °C}$, $R_{thJA}=350\text{ °C/W}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - soldering point	R_{thJS}	-	-	130	°C/W	-
Device on PCB, minimum footprint ¹⁾	R_{thJA}	-	-	350	°C/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 (one layer, 70 µm thick), minimum footprint. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2	V	$V_{DS}=V_{GS}$, $I_D=-11\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1 -100	μA	$V_{DS}=-60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	4344 5240	5500 7000	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-0.18\text{ A}$ $V_{GS}=-4.5\text{ V}$, $I_D=-0.16\text{ A}$
Gate resistance	R_G	-	45	-	Ω	-
Transconductance	g_{fs}	-	0.28	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=-0.18\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	18	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	3.4	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	1.2	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	1.0	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.18\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	1.4	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.18\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	4.9	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.18\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	1.2	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.18\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-0.06	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-0.18\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-0.03	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-0.18\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate to drain charge	Q_{gd}	-	-0.17	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-0.18\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Switching charge	Q_{sw}	-	-0.21	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-0.18\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate charge total	Q_g	-	-0.59	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-0.18\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	-3.5	-	V	$V_{DD}=-30\text{ V}$, $I_D=-0.18\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Output charge	Q_{oss}	-	-0.20	-	nC	$V_{DD}=-30\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-0.18	A	$T_A=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-0.72	A	$T_A=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-0.9	-1.2	V	$V_{GS}=0\text{ V}$, $I_F=-0.18\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	10	-	ns	$V_R=-30\text{ V}$, $I_F=-0.18\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	-5	-	nC	$V_R=-30\text{ V}$, $I_F=-0.18\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$

¹⁾ See diagram ,Gate charge waveforms, for gate charge parameter definition

4 Electrical characteristics diagrams

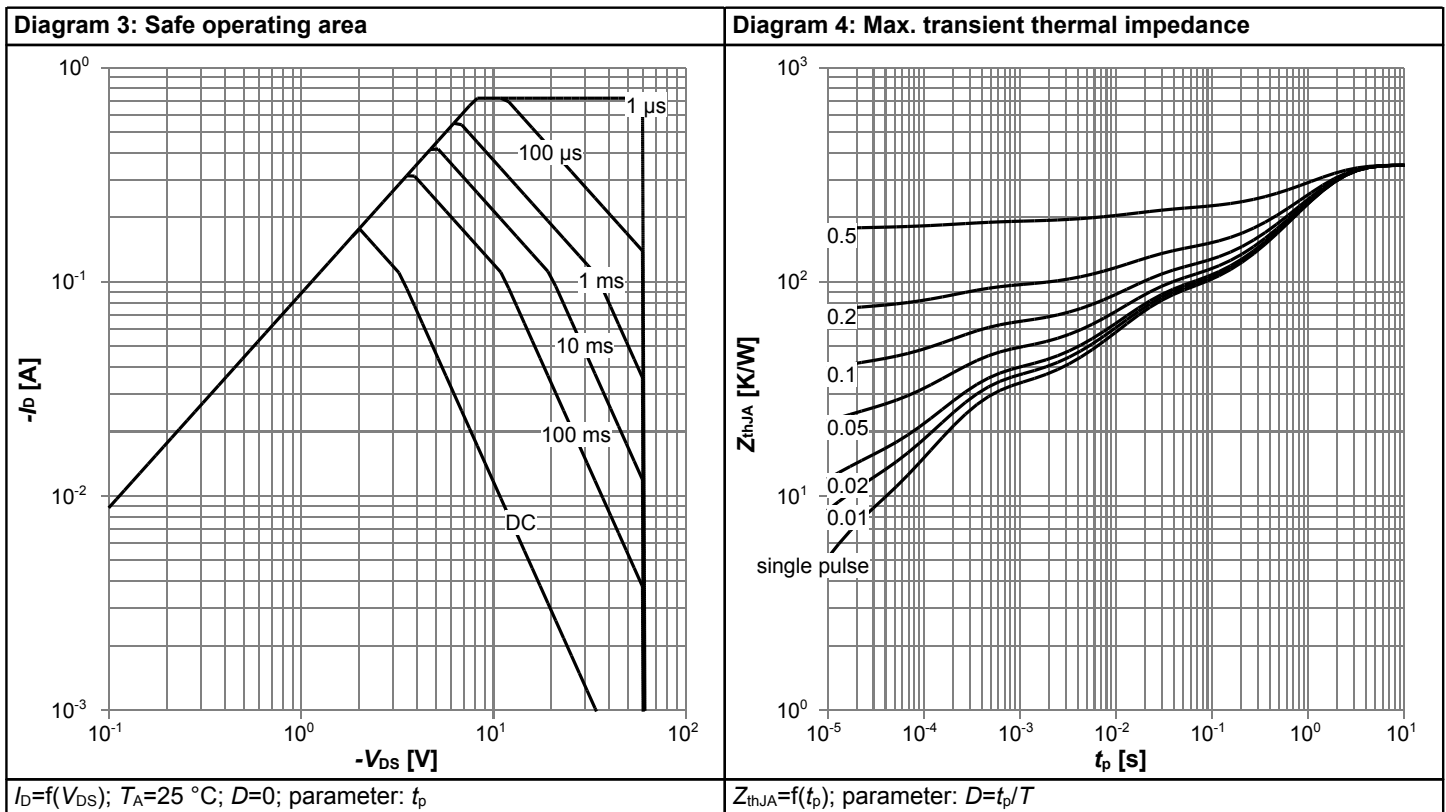
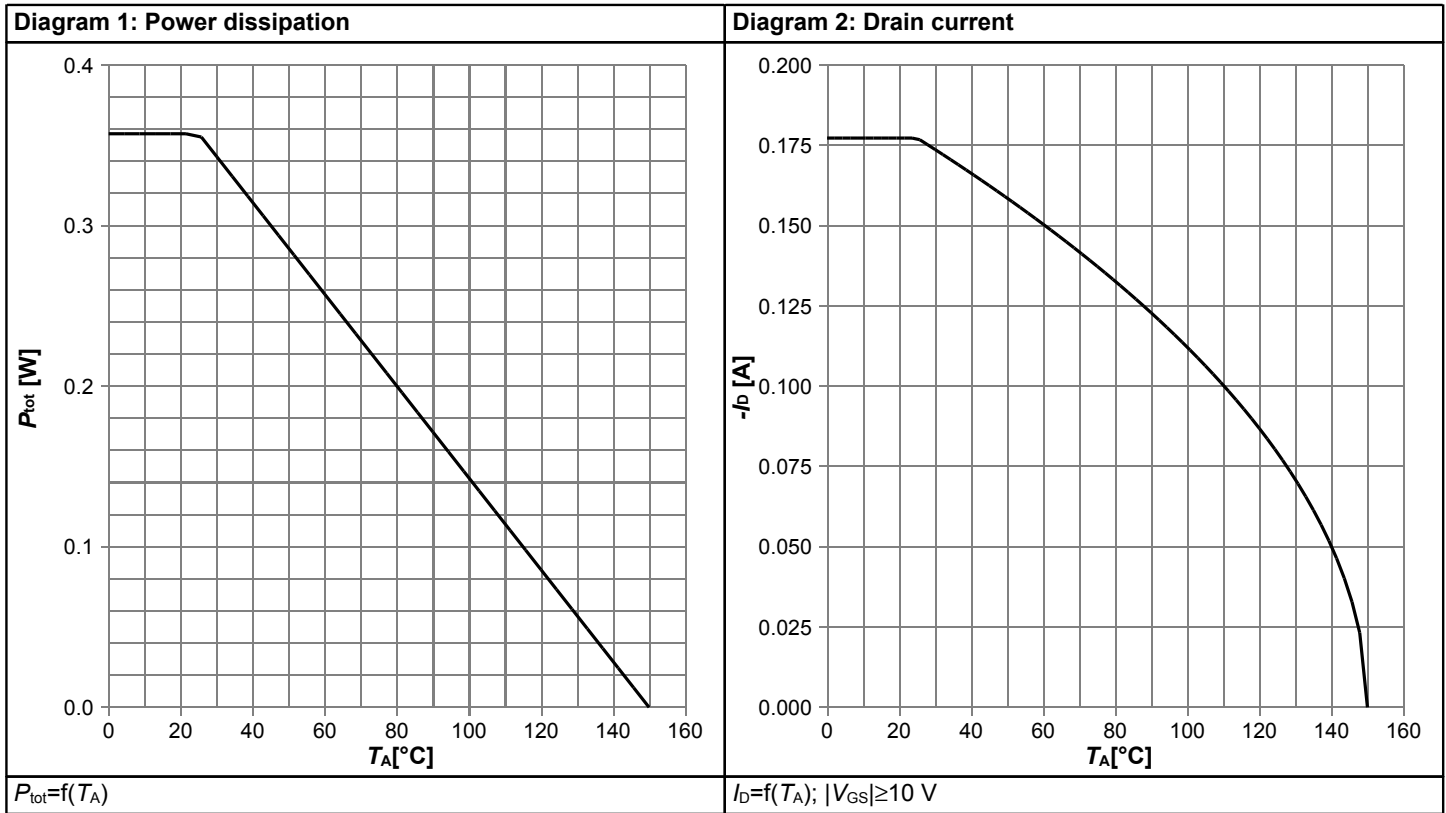
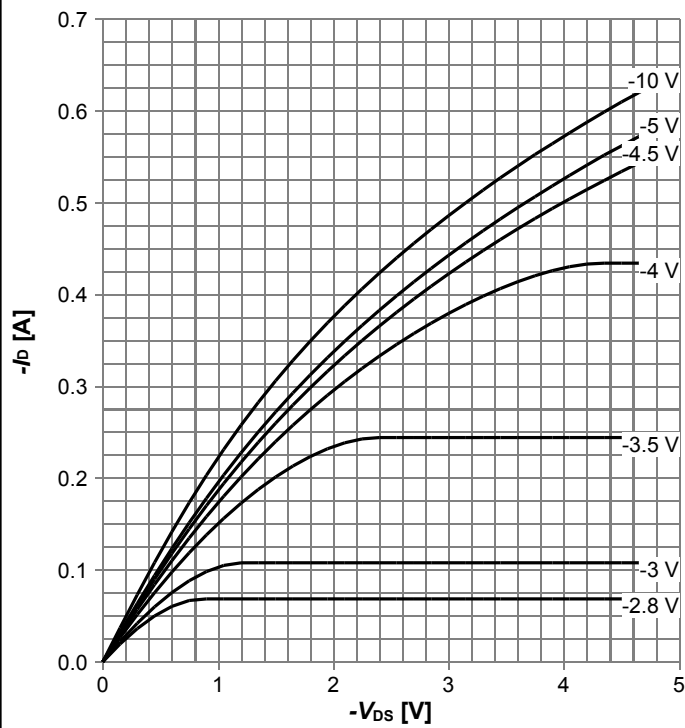
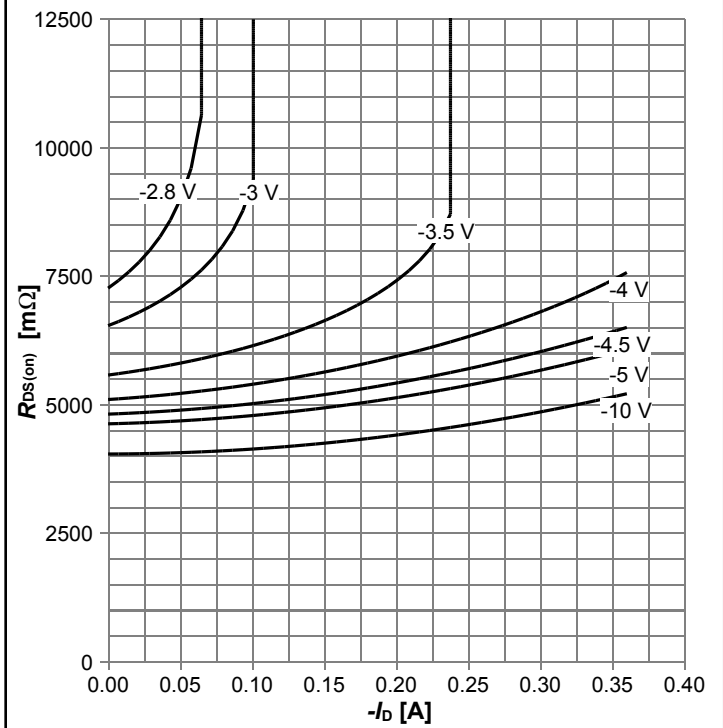


Diagram 5: Typ. output characteristics



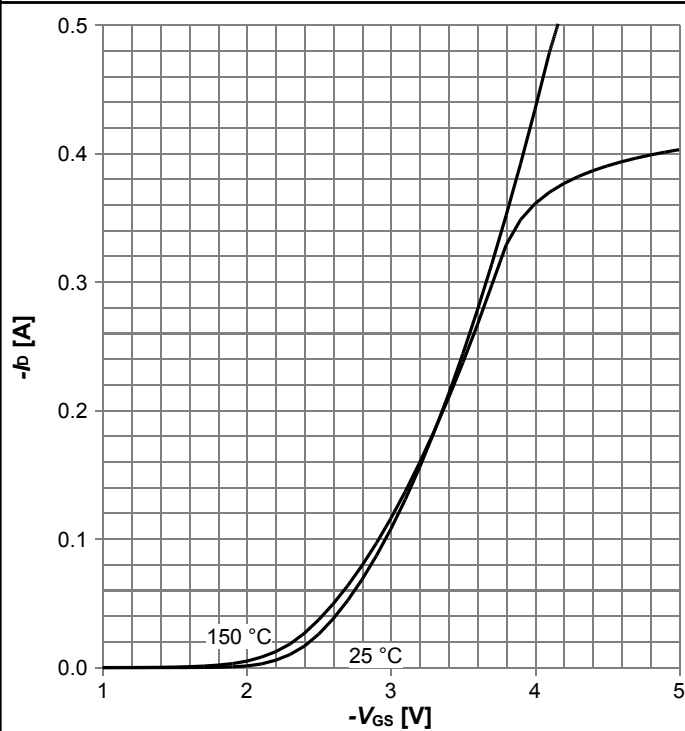
$I_D=f(V_{DS})$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



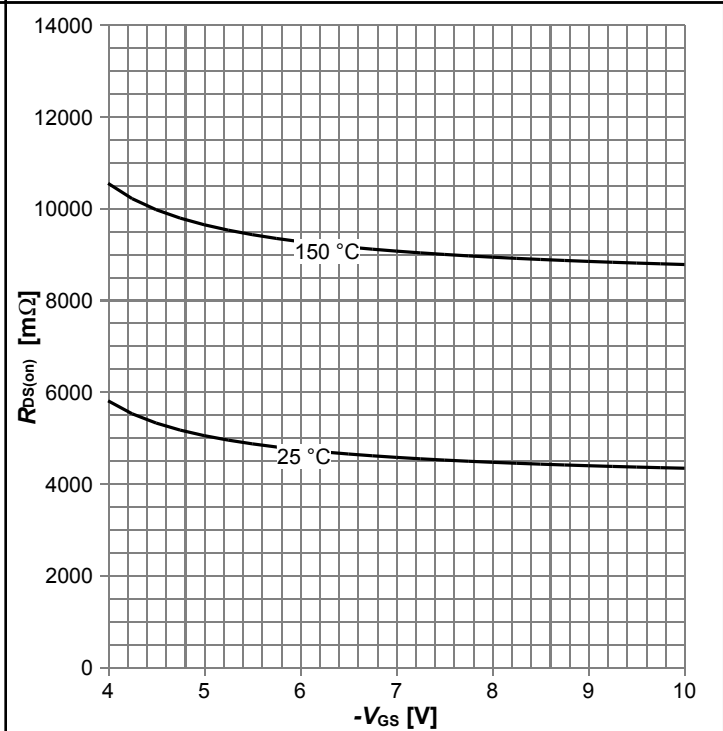
$R_{DS(on)}=f(I_D)$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



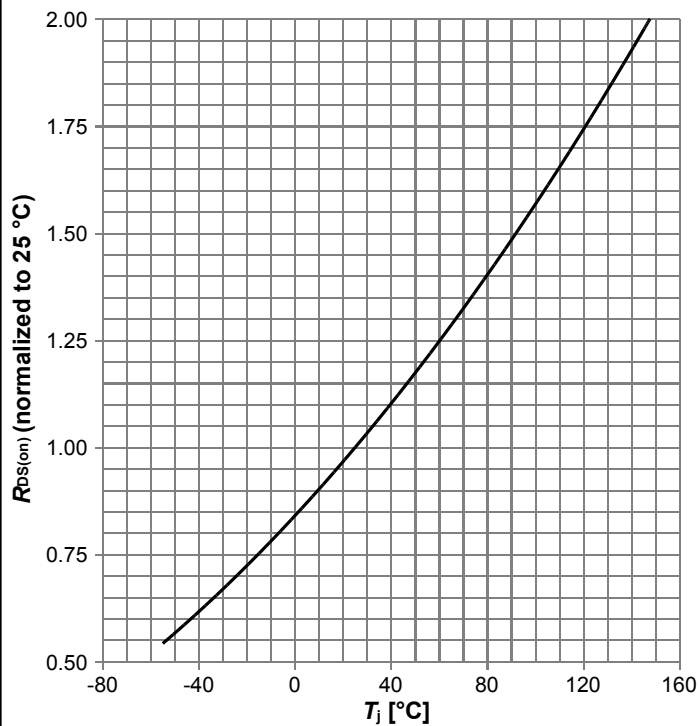
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



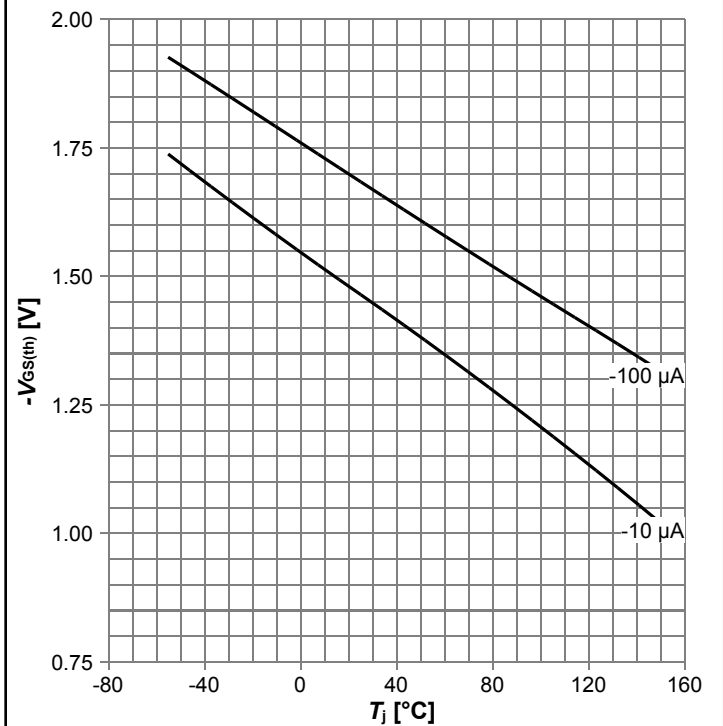
$R_{DS(on)}=f(V_{GS})$, $I_D=-0.18\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



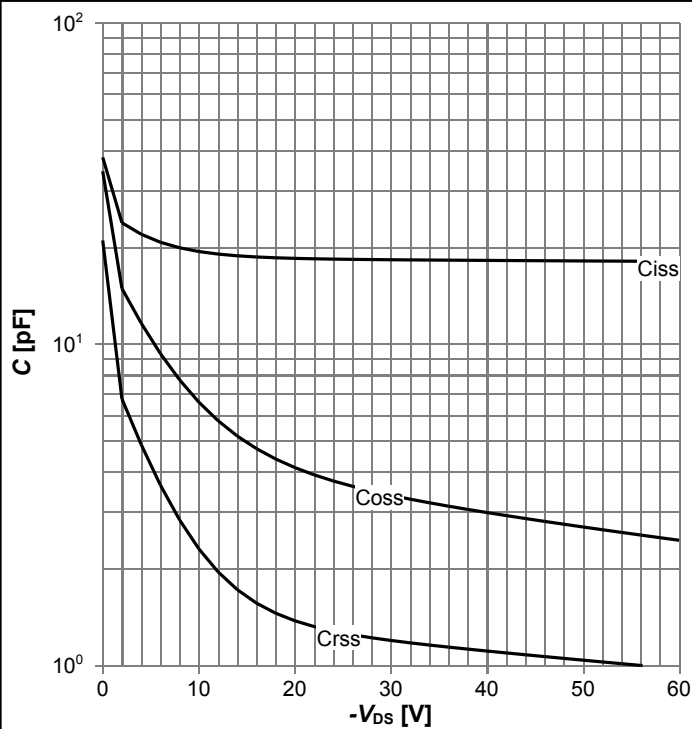
$R_{DS(on)}=f(T_j)$, $I_D=-0.18$ A, $V_{GS}=-10$ V

Diagram 10: Typ. gate threshold voltage



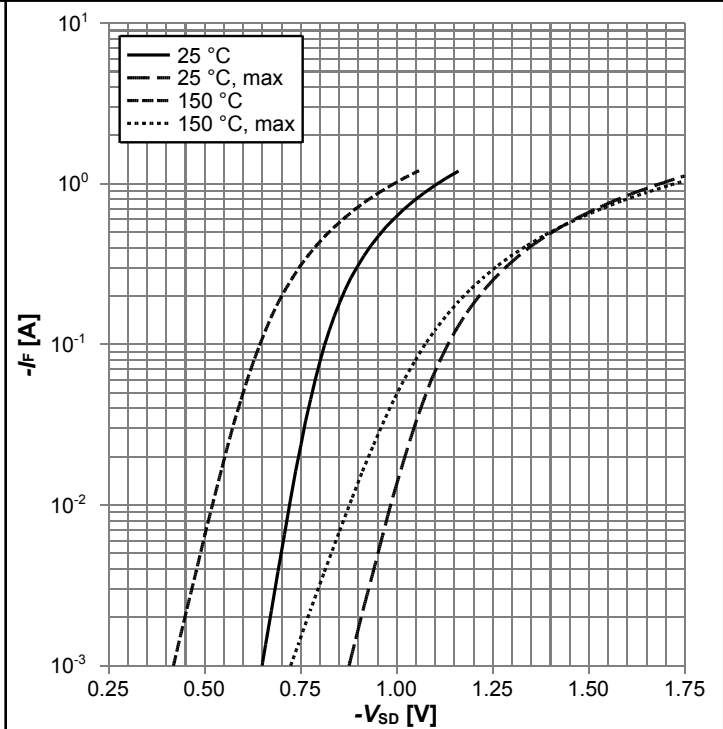
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



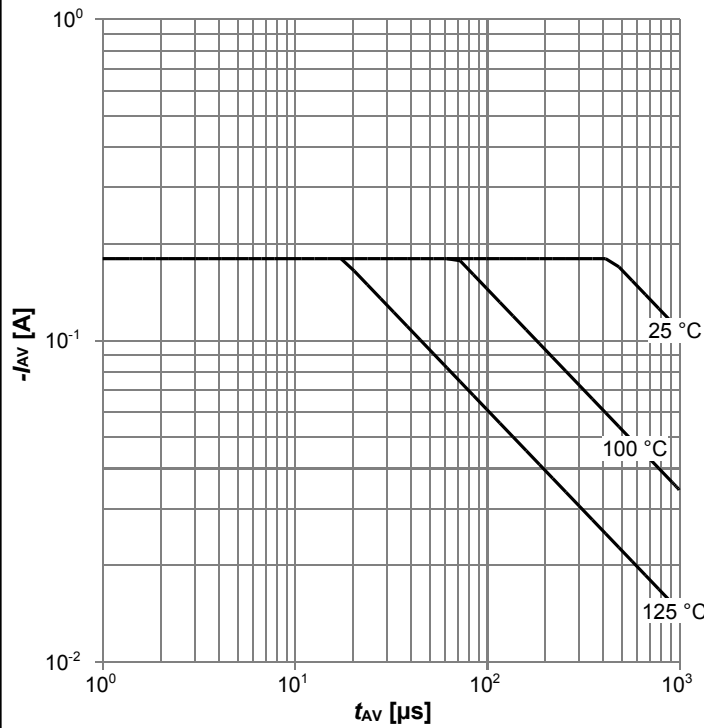
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



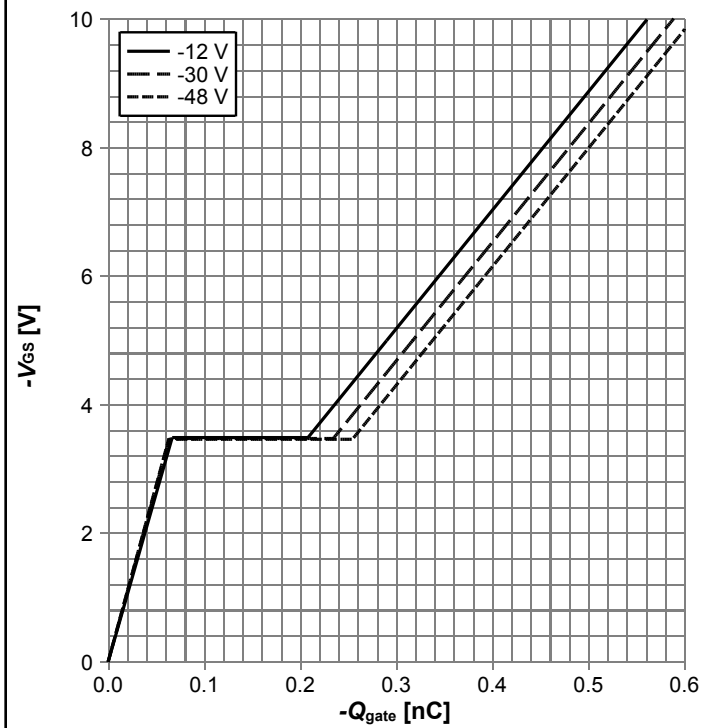
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



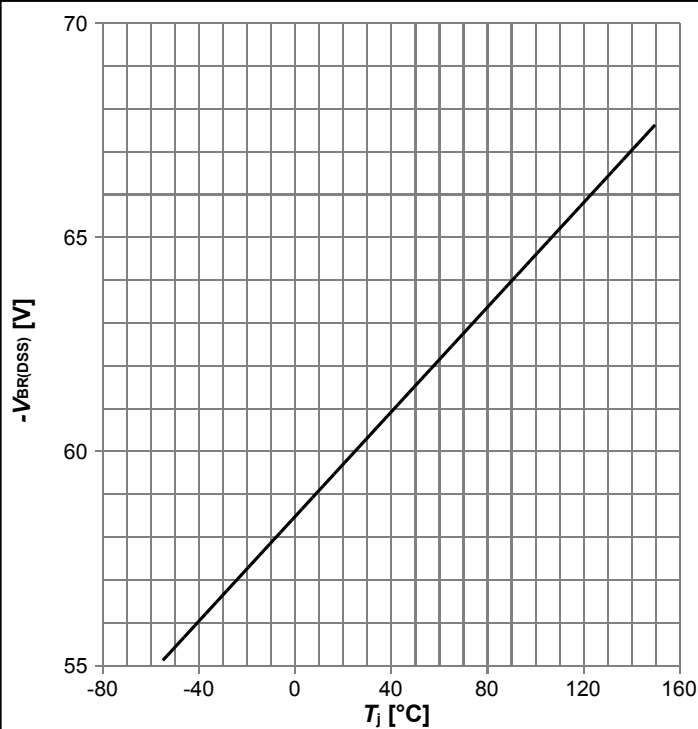
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



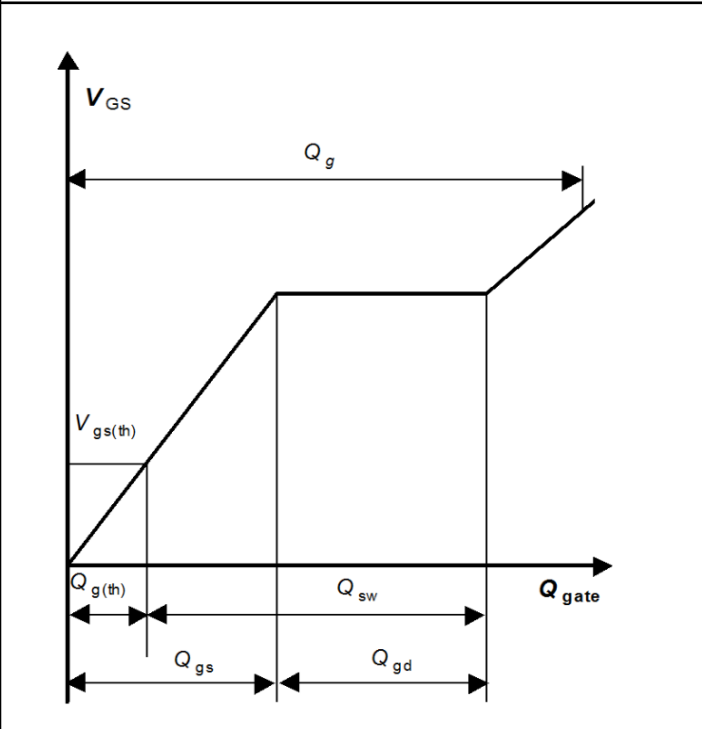
$V_{GS}=f(Q_{gate}), I_D=-0.18 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



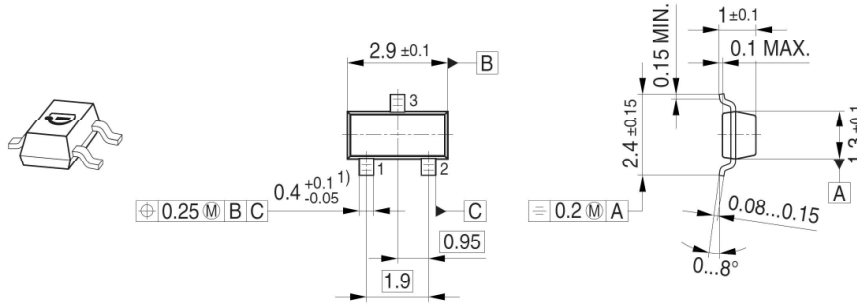
$V_{BR(DSS)}=f(T_j); I_D=-250 \mu\text{A}$

Diagram Gate charge waveforms



5 Package Outlines

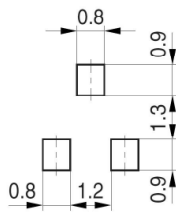
Package Outline



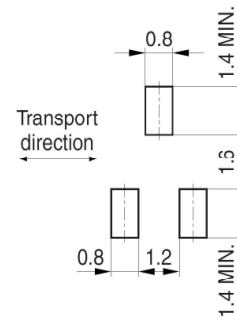
1) Lead width can be 0.6 max. in dambar area

Foot Print

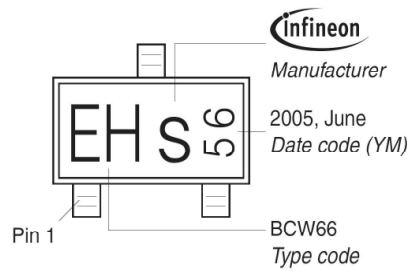
Soldering Type: Reflow Soldering



Soldering Type: Wave Soldering



Marking Layout (Example)



Tape and Reel

Reel ϕ 180 mm: 3.000 Pieces/Reel
 Reels/Box: 1 x 3.000 = 3.000
 Reels/Box: 10 x 3.000 = 30.000

Reel ϕ 330 mm: 10.000 Pieces/Reel
 Reels/Box: 1 x 10.000 = 10.000

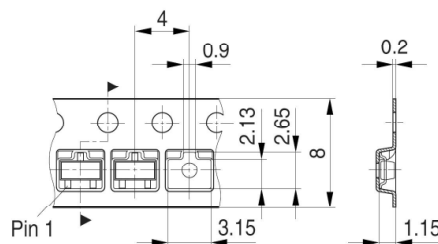


Figure 1 Outline PG-SOT23, dimensions in mm

Revision History

ISS55EP06LM

Revision: 2019-04-03, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-04-03	Release of final version

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[DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)