

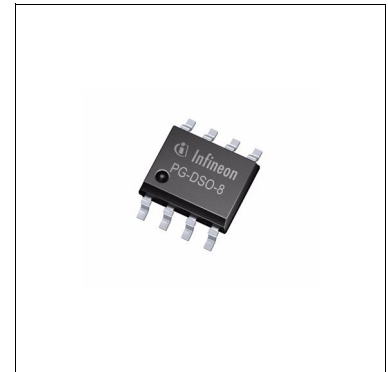
Smart high-side NMOS-power switch

ITS4200S-SJ-D



Features

- CMOS compatible input
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized electromagnetic compatibility (EMC)
- Open drain diagnostic output for overtemperature and short circuit
- Open load detection in OFF-state with external resistor
- Overload protection
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of Vbb protection
- Electrostatic discharge protection (ESD)
- Green Product (RoHS compliant)



Potential applications

- All types of resistive, inductive and capacitive loads
- Power switch for 12V, 24V and 45V DC applications with CMOS compatible control interface
- Open drain diagnosis feedback for overtemperature and short circuit
- Driver for electromagnetic relays
- Power management for high-side-switching with low current consumption in OFF-mode

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC.

Description

The ITS4200S-SJ-D is a protected 200m Ω single channel Smart High-Side NMOS-Power Switch in a PG-DSO-8 package with charge pump, CMOS compatible input and diagnostic feedback.

Table 1 Product summary

| Parameter | Symbol | Values |
|-----------------------------|--------------|---------------------|
| Overvoltage protection | V_{SAZmin} | 62 V |
| Operating voltage range | V_S | $6V < V_S < 52V$ |
| On-state resistance | R_{DSON} | typ. 150 m Ω |
| Nominal load current | $I_{L(nom)}$ | 1.2 A |
| Operating temperature range | T_j | -40°C to 125°C |

| Type | Package | Marking |
|---------------|----------|---------|
| ITS4200S-SJ-D | PG-DSO-8 | I200SD |

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Block diagram and terms

1 Block diagram and terms

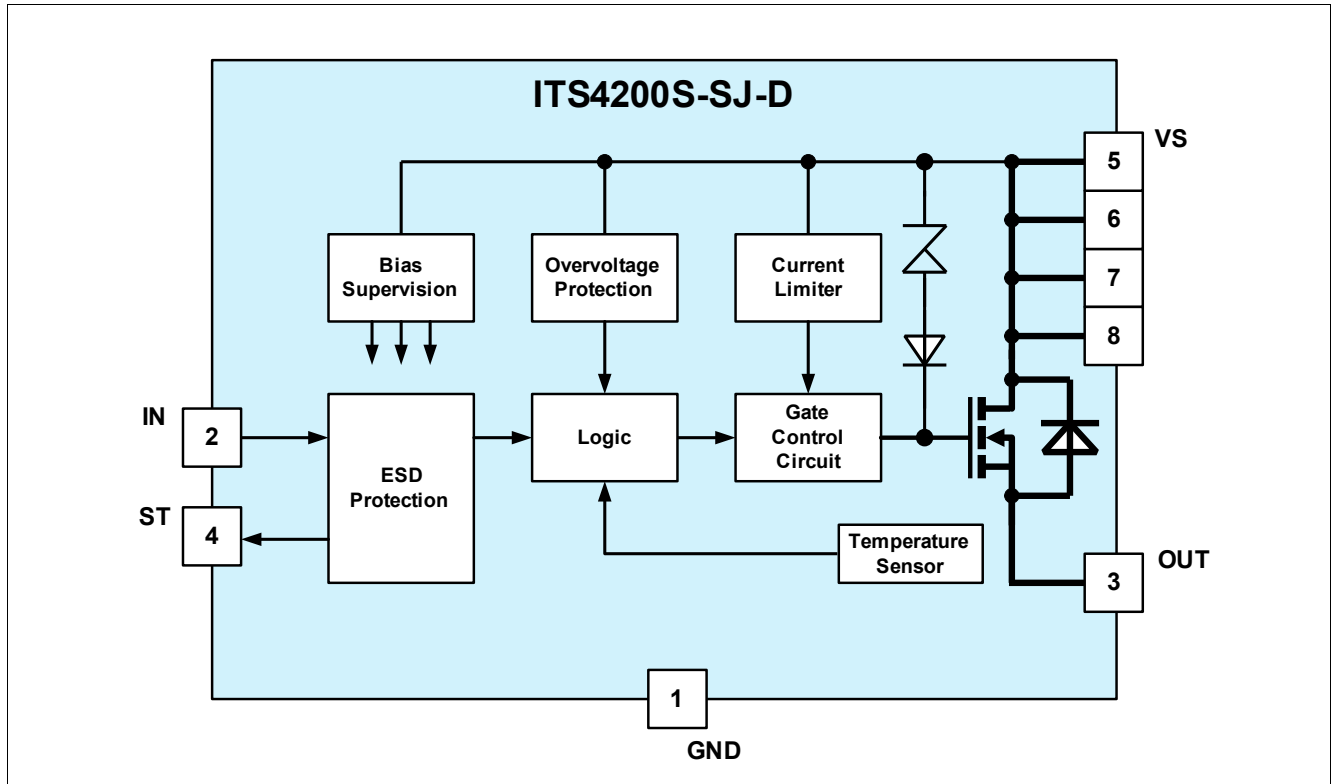


Figure 1 Block diagram

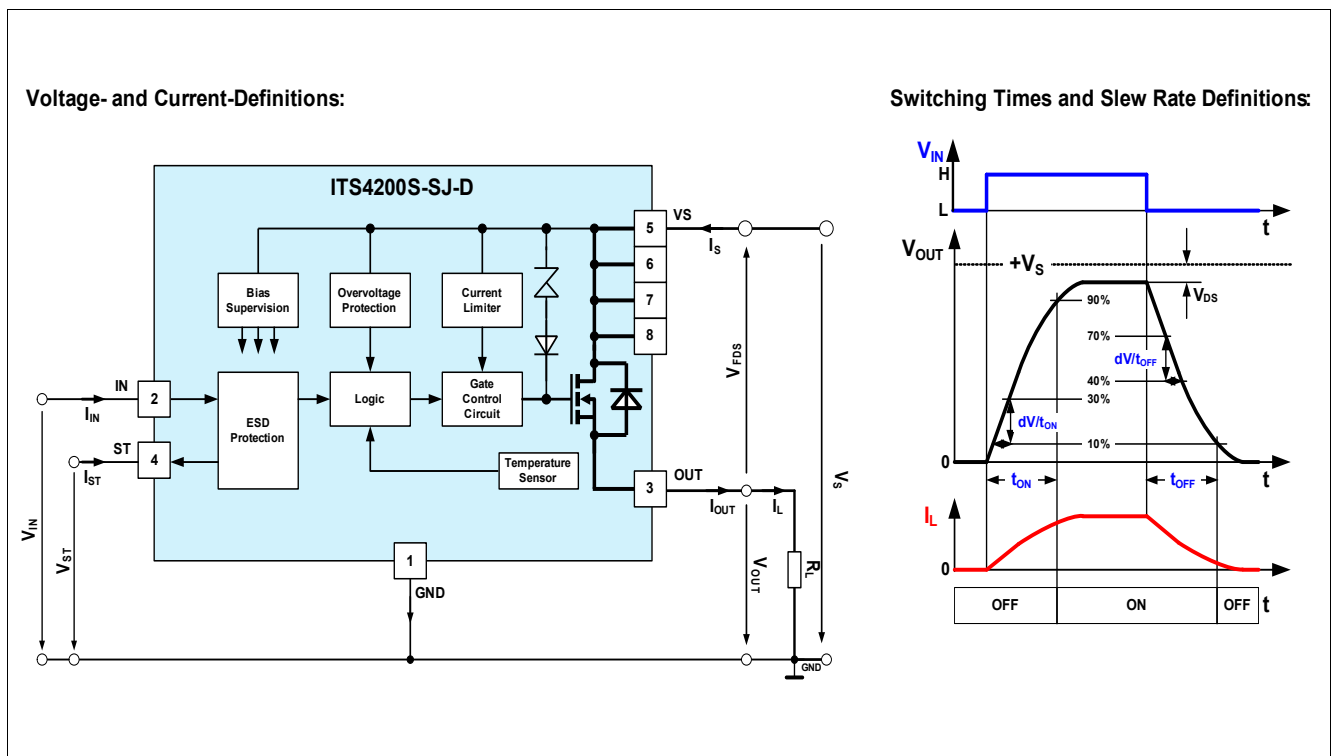


Figure 2 Terms - parameter definition

Pin configuration

2 Pin configuration

2.1 Pin assignment

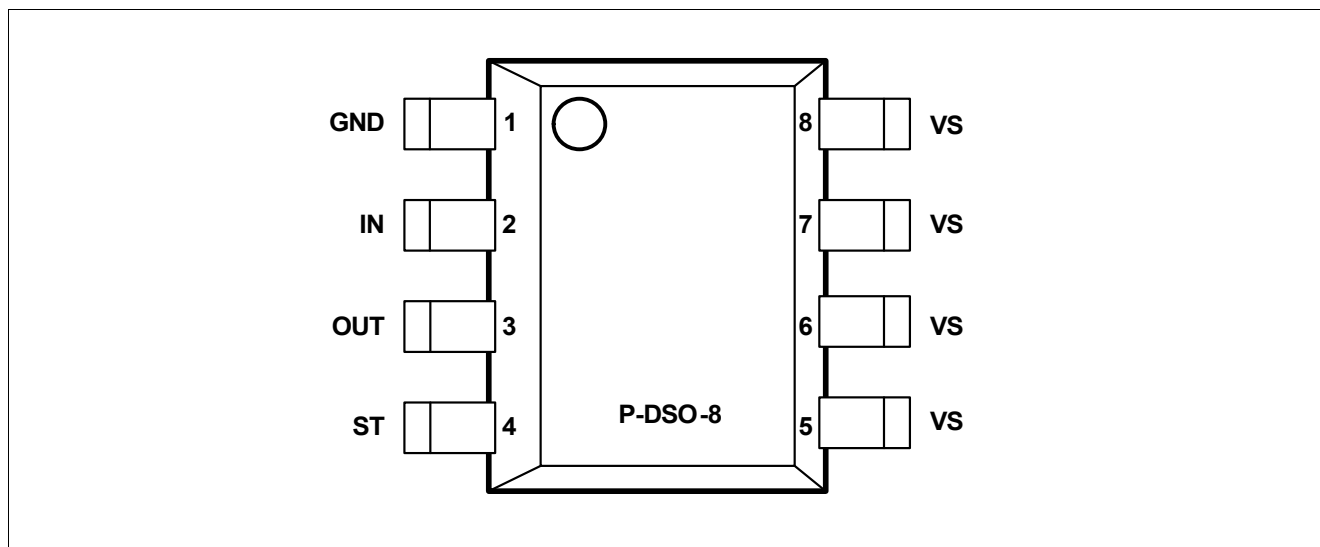


Figure 3 Pin configuration top view, PG-DSO-8

2.2 Pin definitions and functions

| Pin | Symbol | Function |
|------------|--------|--|
| 1 | GND | Logic ground |
| 2 | IN | Input, controls the power switch; the powerswitch is ON when high |
| 3 | OUT | Output to the load |
| 4 | ST | Status flag; diagnosis feedback; NMOS open drain |
| 5, 6, 7, 8 | VS | Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance) |

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings¹⁾ at $T_j = 25^\circ\text{C}$ unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter “Block Diagram and Terms”

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------|--------|------|--------------|------------------|------------------------|--------|
| | | Min. | Typ. | Max. | | | |
| Supply voltage VS | | | | | | | |
| Voltage | V_S | – | – | 52 | V | – | 4.1.1 |
| Voltage for short circuit protection | V_{SSC} | – | – | 36 | V | – | 4.1.2 |
| Output stage OUT | | | | | | | |
| Output current; (short circuit current see electrical characteristics) | I_{OUT} | – | – | self limited | A | – | 4.1.3 |
| Input IN | | | | | | | |
| Current | I_{IN} | -5 | – | 5 | mA | – | 4.1.4 |
| Status ST | | | | | | | |
| Current | I_{ST} | -5 | – | 5 | mA | – | 4.1.5 |
| Temperatures | | | | | | | |
| Junction temperature | T_j | -40 | – | 125 | $^\circ\text{C}$ | – | 4.1.6 |
| Storage temperature | T_{stg} | -55 | – | 125 | $^\circ\text{C}$ | – | 4.1.7 |
| Power dissipation | | | | | | | |
| $T_a = 25^\circ\text{C}^{2)}$ | P_{tot} | – | – | 1.4 | W | – | 4.1.8 |
| Inductive load switch-off energy dissipation | | | | | | | |
| $T_j = 125^\circ\text{C}; I_L = 1\text{A}^{3)}$ | E_{AS} | – | – | 125 | mJ | single pulse | 4.1.9 |
| ESD susceptibility | | | | | | | |
| ESD susceptibility (input pin IN) | V_{ESD} | -1 | – | 1 | kV | HBM ⁴⁾ | 4.1.10 |
| ESD susceptibility (output pin OUT) | V_{ESD} | -6 | – | 6 | kV | HBM ⁴⁾ | 4.1.12 |
| ESD susceptibility (all other pins) | V_{ESD} | -4 | – | 4 | kV | HBM ⁴⁾ | 4.1.11 |

1) Not subject to production test, specified by design.

2) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70mm thick) copper area for Vbb connection. PCB is vertical without blown air.

3) Not subject to production test, specified by design.

4) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS001 (1.5 k Ω , 100 pF)

Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

General product characteristics

3.2 Functional range

Table 3 Functional range

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------------|--------|--------|------|------|------|------------------------|--------|
| | | Min. | Typ. | Max. | | | |
| Nominal operating voltage | V_S | 6 | – | 52 | V | V_S increasing | 4.2.1 |

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 4 Thermal resistance¹⁾

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---------------------------|--------|-------|------|------|------------------------|--------|
| | | Min. | Typ. | Max. | | | |
| Thermal resistance - junction to pin5 | $R_{thj-pin5}$ | – | 23.3 | – | K/W | – | 4.3.1 |
| Thermal resistance - junction to ambient - 1s0p, minimal footprint | R_{thJA_1s0p} | – | 128.7 | – | K/W | ²⁾ | 4.3.2 |
| Thermal resistance - junction to ambient - 1s0p, 300mm ² | $R_{thJA_1s0p_300mm^2}$ | – | 70.1 | – | K/W | ³⁾ | 4.3.3 |
| Thermal resistance - junction to ambient - 1s0p, 600mm ² | $R_{thJA_1s0p_600mm^2}$ | – | 65.6 | – | K/W | ⁴⁾ | 4.3.4 |
| Thermal resistance - junction to ambient - 2s2p | R_{thJA_2s2p} | – | 55.4 | – | K/W | ⁵⁾ | 4.3.5 |
| Thermal resistance - junction to ambient with thermal vias - 2s2p | R_{thJA_2s2p} | – | 53.5 | – | K/W | ⁶⁾ | 4.3.6 |

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm²; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

4) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm²; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

6) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). The diameter of the two vias are equal 0.3mm and have a plating of 25µm with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.

Electrical characteristics

4 Electrical characteristics

Table 5 $V_S = 12\text{ V to }42\text{ V}$; $T_j = -40^\circ\text{C to }+125^\circ\text{C}$; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter “Block Diagram and Terms”); typical values at $V_S = 13.5\text{V}$, $T_j = 25^\circ\text{C}$

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------|--------|------|------|-------------------|---|--------|
| | | Min. | Typ. | Max. | | | |
| Powerstage | | | | | | | |
| NMOS ON resistance | R_{DSON} | – | 150 | 200 | m Ω | $I_{\text{OUT}} = 1\text{A}; T_j = 25^\circ\text{C};$ $9\text{V} < V_S < 52\text{V}; V_{\text{IN}} = 5\text{V}$ | 5.0.1 |
| NMOS ON resistance | R_{DSON} | – | 250 | 350 | m Ω | $I_{\text{OUT}} = 1\text{A}; T_j = 125^\circ\text{C};$ $9\text{V} < V_S < 52\text{V}; V_{\text{IN}} = 5\text{V}$ | 5.0.2 |
| Nominal load current; device on PCB ¹⁾ | I_{LNOM} | 1.2 | – | – | A | $T_{\text{pin5}} = 85^\circ\text{C}$ | 5.0.3 |
| Timings of power stages²⁾ | | | | | | | |
| Turn ON time (to 90% of V_{out}); L to H transition of V_{IN} | t_{ON} | – | 80 | 180 | μs | $V_S = 13.5\text{V}; R_L = 47\Omega$ | 5.0.4 |
| Turn OFF time (to 10% of V_{out}); H to L transition of V_{IN} | t_{OFF} | – | 80 | 200 | μs | $V_S = 13.5\text{V}; R_L = 47\Omega$ | 5.0.5 |
| ON-slew rate; $\Delta V_{\text{OUT}} / \Delta t$; (10 to 30% of V_{out}); L to H transition of V_{IN} | SR_{ON} | – | 0.7 | 2.0 | V / μs | $V_S = 13.5\text{V}; R_L = 47\Omega$ | 5.0.6 |
| OFF-slew rate; $\Delta V_{\text{OUT}} / \Delta t$; (70 to 40% of V_{out}); H to L transition of V_{IN} | SR_{OFF} | – | 0.9 | 2.0 | V / μs | $V_S = 13.5\text{V}; R_L = 47\Omega$ | 5.0.7 |
| Under voltage lockout (charge pump start-stop-restart) | | | | | | | |
| Supply undervoltage; charge pump stop voltage | V_{SUV} | – | – | 4 | V | V_S decreasing $-40^\circ\text{C} < T_j < 85^\circ\text{C}$ | 5.0.8 |
| Supply undervoltage; Charge pump stop voltage | V_{SUV} | – | – | 5.5 | V | V_S decreasing; $T_j = 125^\circ\text{C}$ | 5.0.9 |
| Supply startup voltage; Charge pump restart voltage | V_{SSU} | – | 4 | 5.5 | V | V_S increasing | 5.0.10 |
| Current consumption | | | | | | | |
| Operating current | I_{GND} | – | 0.8 | 2 | mA | $V_{\text{IN}} = 5\text{V}$ | 5.0.11 |
| Standby current | I_{SSTB} | – | – | 15 | μA | $V_{\text{IN}} = 0\text{V}; V_{\text{OUT}} = 0\text{V}$ $-40^\circ\text{C} < T_j < 85^\circ\text{C}$ | 5.0.12 |
| Standby current | I_{SSTB} | – | – | 18 | μA | $V_{\text{IN}} = 0\text{V}; T_j = 125^\circ\text{C}$ | 5.0.13 |
| Output leakage current | I_{OUTLK} | – | – | 5 | μA | $V_{\text{IN}} = 0\text{V}; V_{\text{OUT}} = 0\text{V}$ | 5.0.14 |
| Protection functions³⁾ | | | | | | | |
| Initial peak short circuit current limit | I_{LSCP} | – | – | 9 | A | $T_j = -40^\circ\text{C}; V_S = 20\text{V};$ $V_{\text{IN}} = 5.0\text{V}; t_m = 150\mu\text{s}$ | 5.0.15 |
| Initial peak short circuit current limit | I_{LSCP} | – | 6.5 | – | A | $T_j = 25^\circ\text{C}; V_S = 20\text{V};$ $V_{\text{IN}} = 5.0\text{V}; t_m = 150\mu\text{s}$ | 5.0.16 |

Electrical characteristics

Table 5 $V_S = 12\text{ V to }42\text{ V}$; $T_j = -40^\circ\text{C to }+125^\circ\text{C}$; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter “Block Diagram and Terms”); typical values at $V_S = 13.5\text{V}$, $T_j = 25^\circ\text{C}$

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-------------|--------|------|------|------------------|---|--------|
| | | Min. | Typ. | Max. | | | |
| Initial peak short circuit current limit | I_{LSCP} | 4 | – | – | A | $T_j = 125^\circ\text{C}$; $V_S = 20\text{V}$; $V_{IN} = 5.0\text{V}$; $t_m = 150\mu\text{s}$ | 5.0.17 |
| Initial peak short circuit current limit ⁴⁾ | I_{LSCP} | – | 5 | – | A | $V_S > 40\text{V}$; $V_{IN} = 5.0\text{V}$; $t_m = 150\mu\text{s}$ | 5.0.18 |
| Repetitive short circuit current limit $T_j = T_{jTrip}$; see timing diagrams | I_{LSCR} | – | 6 | – | A | $V_{IN} = 5.0\text{V}$; $V_S < 40\text{V}$ | 5.0.19 |
| Repetitive short circuit current limit $T_j = T_{jTrip}$; see timing diagrams | I_{LSCR} | – | 4.5 | – | A | $V_{IN} = 5.0\text{V}$; $V_S > 40\text{V}$ | 5.0.20 |
| Output clamp at $V_{OUT} = V_S - V_{DSCL}$ (inductive load switch off) | V_{DSCL} | 59 | 63 | – | V | $I_S = 4\text{mA}$ | 5.0.22 |
| Overshoot protection $V_{OUT} = V_S - V_{ONCL}$ | V_{SAZ} | 62 | – | – | V | $I_S = 4\text{mA}$ | 5.0.23 |
| Thermal overload trip temperature | T_{jTrip} | 150 | – | – | $^\circ\text{C}$ | – | 5.0.24 |
| Thermal hysteresis | T_{HYS} | – | 10 | – | K | – | 5.0.25 |
| Reverse battery⁵⁾ | | | | | | | |
| Continuous reverse battery voltage | V_{SREV} | – | – | 52 | V | – | 5.0.26 |
| Forward voltage of the drain-source reverse diode | V_{FDS} | – | 600 | – | mV | $I_{FDS} = 200\text{mA}$; $V_{IN} = 0\text{V}$; $T_j = 125^\circ\text{C}$ | 5.0.27 |
| Input interface; pin IN | | | | | | | |
| Input turn-ON voltage (logic input high-level) | V_{INON} | 2.2 | – | – | V | – | 5.0.28 |
| Input turn-OFF voltage (logic input low-level) | V_{INOFF} | – | – | 0.8 | V | – | 5.0.29 |
| Input threshold hysteresis | V_{INHYS} | – | 0.4 | – | V | – | 5.0.30 |
| Off state input current | I_{INOFF} | 1 | – | 25 | μA | $V_{IN} = 0.7\text{V}$ | 5.0.31 |
| On state input current | I_{INON} | 3 | – | 25 | μA | $V_{IN} = 5.0\text{V}$ | 5.0.32 |
| Input resistance | R_{IN} | 2.0 | 3.5 | 5.0 | k Ω | – | 5.0.33 |
| Status output (NMOS open drain); pin ST | | | | | | | |
| Status output zener voltage | V_{STZ} | 5.4 | 6.1 | 6.8 | V | $I_{ST} = 1.6\text{mA}$ | 5.0.34 |
| Status output low voltage | V_{STLO} | – | – | 0.4 | V | $I_{ST} = 1.6\text{mA}$; $T_j < 25^\circ\text{C}$ | 5.0.35 |
| Status output low voltage | V_{STLO} | – | – | 0.6 | V | $I_{ST} = 1.6\text{mA}$; $T_j < 125^\circ\text{C}$ | 5.0.36 |
| Status leakage current | I_{STLK} | – | – | 2 | μA | $V_{ST} = 5\text{V}$; $T_j < 105^\circ\text{C}$ | 5.0.37 |
| Status invalid time after positive input slope ⁶⁾⁷⁾ | t_{dP} | – | 120 | 160 | μs | $V_S = 13.5\text{V}$ | 5.0.38 |
| Status invalid time after negative input slope ⁸⁾⁹⁾ | t_{dN} | – | 250 | 400 | μs | $V_S = 13.5\text{V}$ | 5.0.39 |

Electrical characteristics

Table 5 $V_s = 12\text{ V to }42\text{ V}$; $T_j = -40^\circ\text{C to }+125^\circ\text{C}$; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter “Block Diagram and Terms”); typical values at $V_s = 13.5\text{V}$, $T_j = 25^\circ\text{C}$

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------|--------|--------|------|------|------|------------------------|--------|
| | | Min. | Typ. | Max. | | | |

Diagnostic characteristics

| | | | | | | | |
|--|-------------|---|-----|---|------------|-----------------------|--------|
| Short circuit detection voltage | V_{OUTSC} | – | 2.8 | – | V | – | 5.0.40 |
| Open load detection voltage ¹⁰⁾ | V_{OUTOL} | – | 3 | 4 | V | – | 5.0.41 |
| Internal pull down resistor ¹¹⁾ | R_{OUTPD} | – | 200 | – | k Ω | $V_{OUT} = 4\text{V}$ | 5.0.42 |

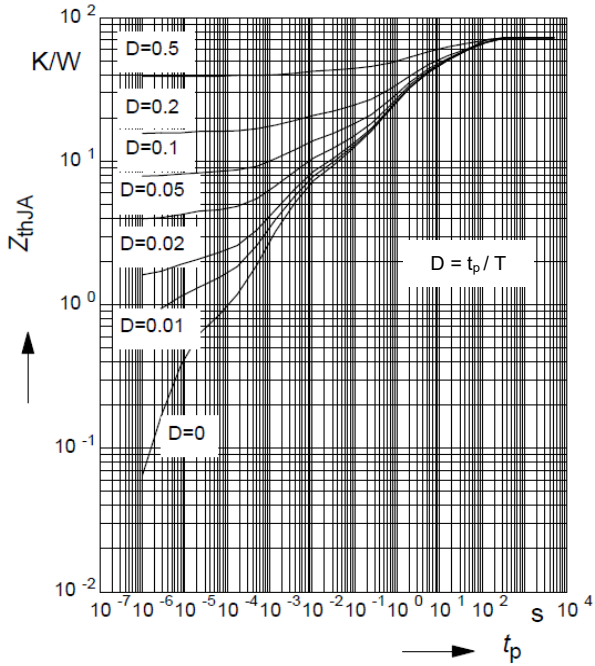
- 1) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm² (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position without blown air.
- 2) Timing values only with high slewrate input signal; otherwise slower.
- 3) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.
- 4) No subject to production test; specified by design.
- 5) Requires a 150 Ω resistor in GND connection. The reverse load current trough the intrinsic drain-source diode of the power-MOS has to be limited by the connected load. Power dissipation is higher compared to normal operation due to the voltage drop across the drain-source diode. The temperature protection is not functional during reverse current operation! Input current has to be limited (see max ratings).
- 6) No delay time after overtemperature switch off and short circuit in on-state.
- 7) No subject to production test; specified by design.
- 8) No delay time after overtemperature switch off and short circuit in on-state.
- 9) No subject to production test; specified by design.
- 10) External pull up resistor required for open load detection in off state.
- 11) No subject to production test; specified by design.

Typical performance graphs

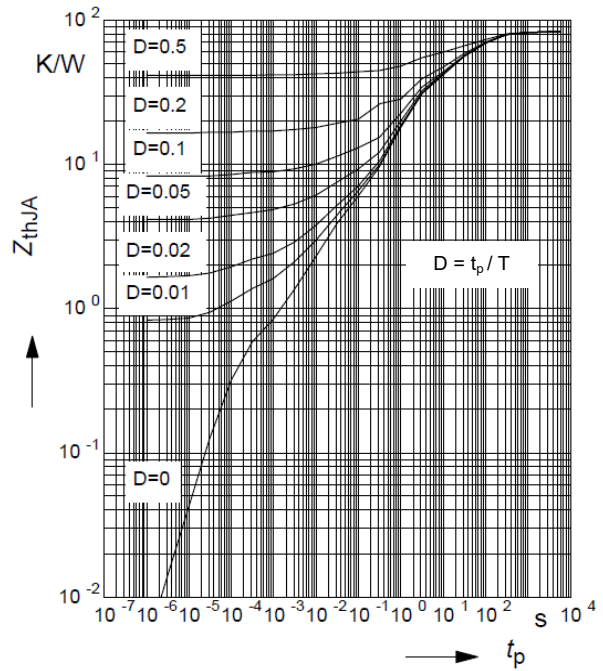
5 Typical performance graphs

Typical characteristics

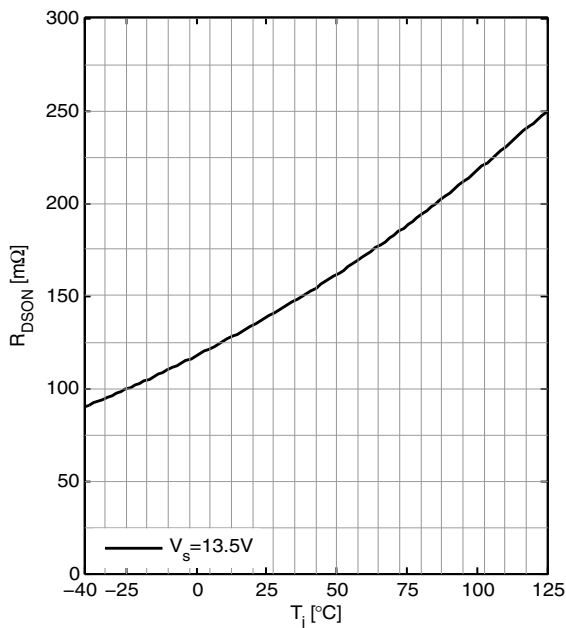
Transient thermal impedance Z_{thJA} versus pulse time t_p @ 6cm² heatsink area



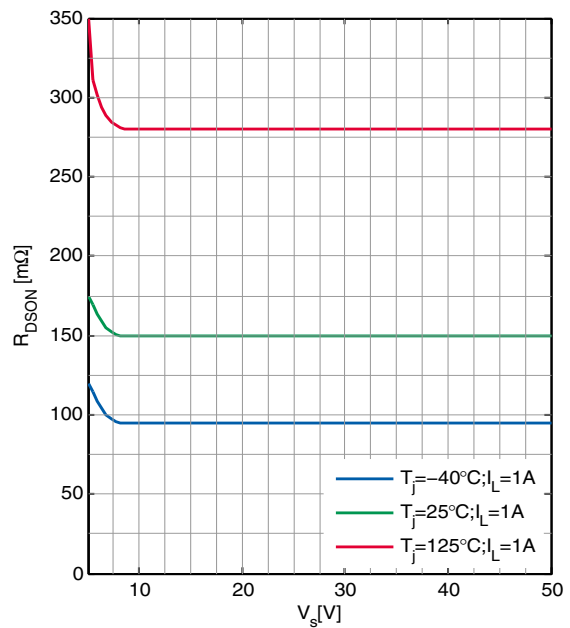
Transient thermal impedance Z_{thJA} versus pulse time t_p @ min. footprint



On-resistance R_{DSON} versus junction temperature T_j



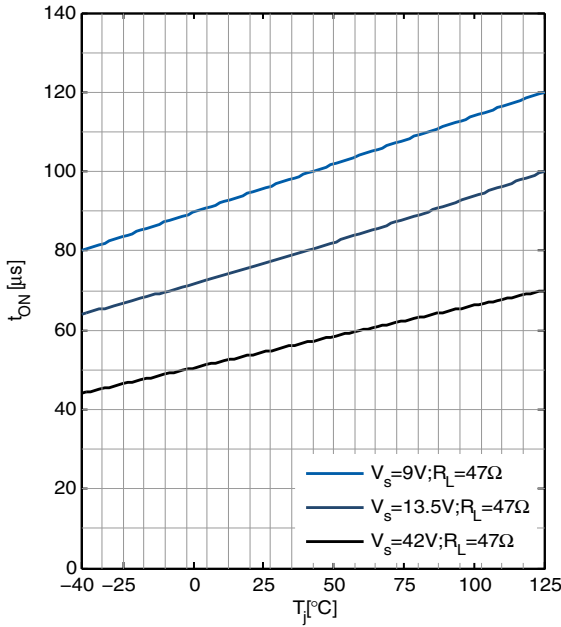
On-resistance R_{DSON} versus supply voltage V_s



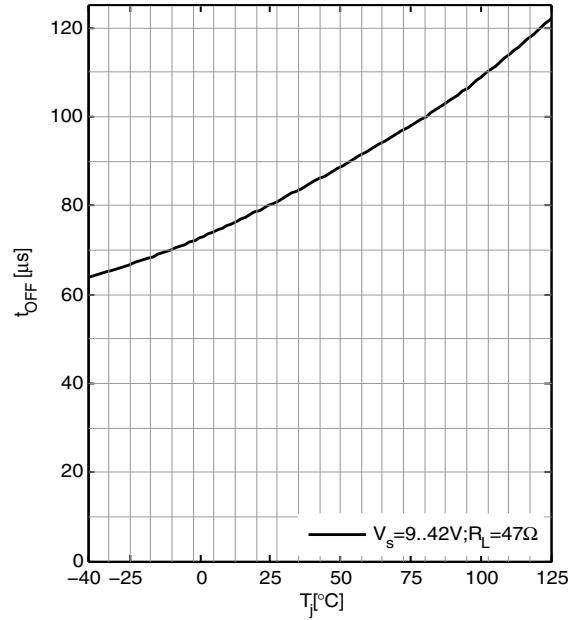
Typical performance graphs

Typical characteristics

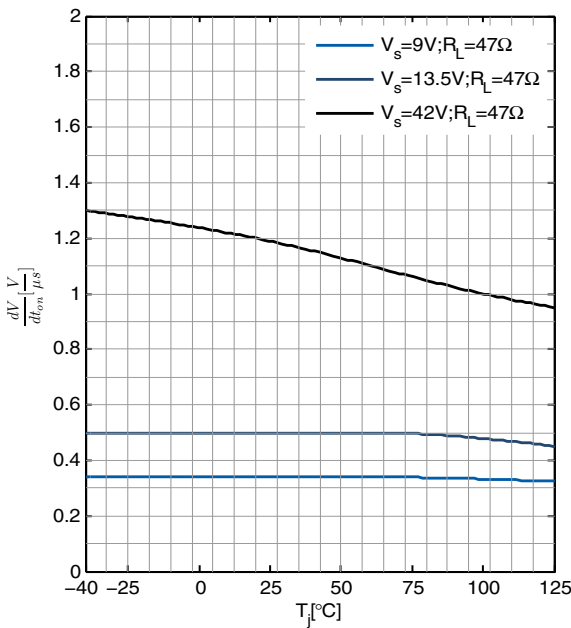
Switch ON time t_{ON} versus junction temperature T_j



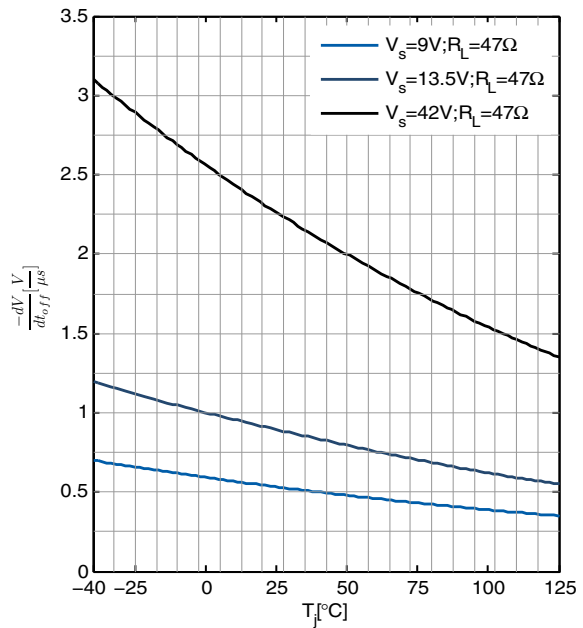
Switch OFF time t_{OFF} versus junction temperature T_j



ON slewrate SR_{ON} versus junction temperature T_j



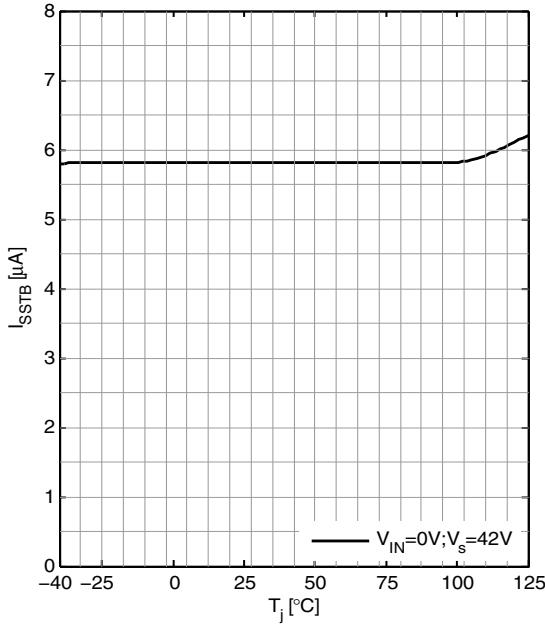
OFF slewrate SR_{OFF} versus junction temperature T_j



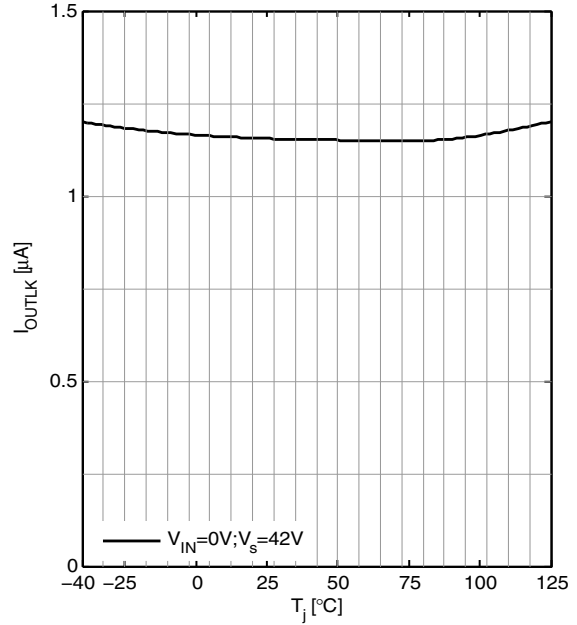
Typical performance graphs

Typical characteristics

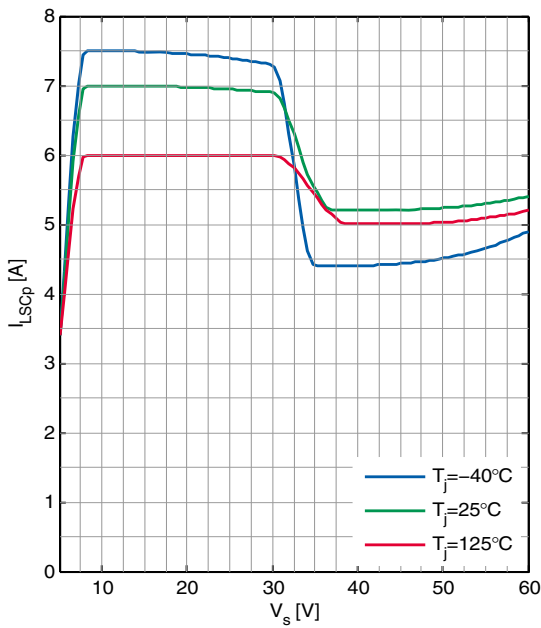
Standby current I_{SSTB} versus junction temperature T_j



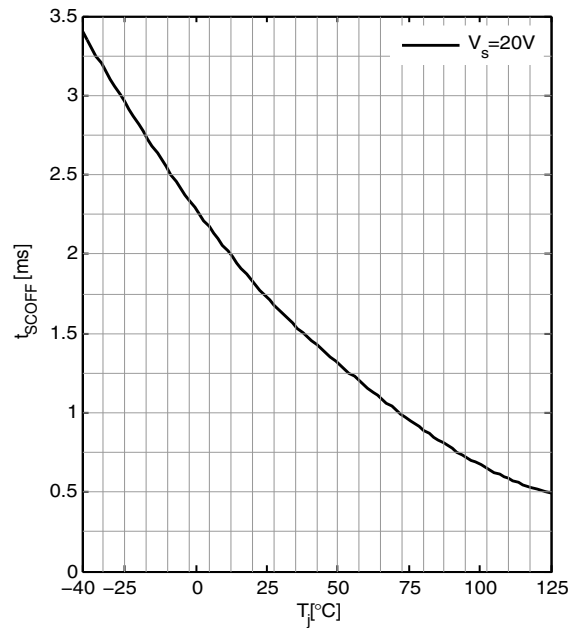
Output leakage current I_{OUTLK} versus junction temperature T_j



Initial peak short circuit current limit I_{LSCP} versus junction temperature T_j



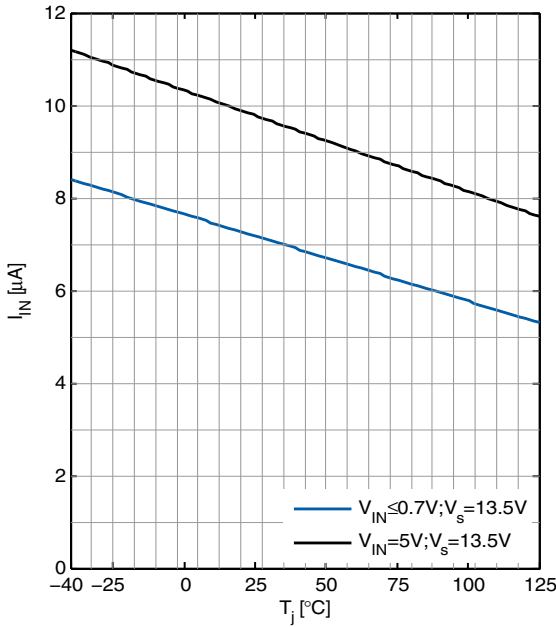
Initial short circuit shutdown time t_{SCOFF} versus junction temperature T_j



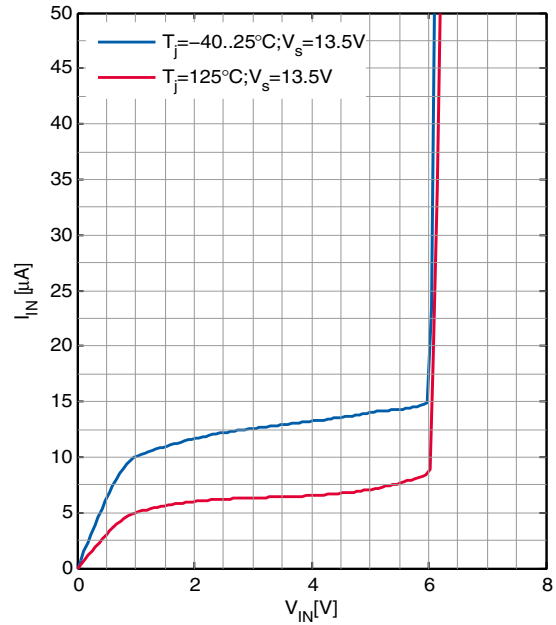
Typical performance graphs

Typical characteristics

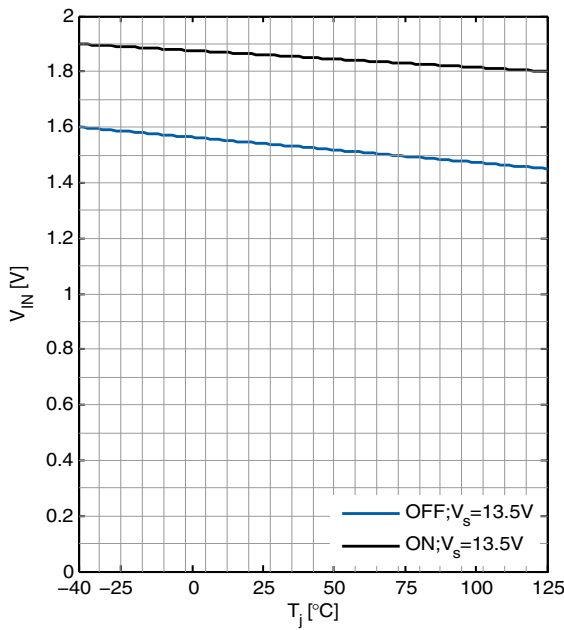
Input current consumption I_{IN} versus junction temperature T_j



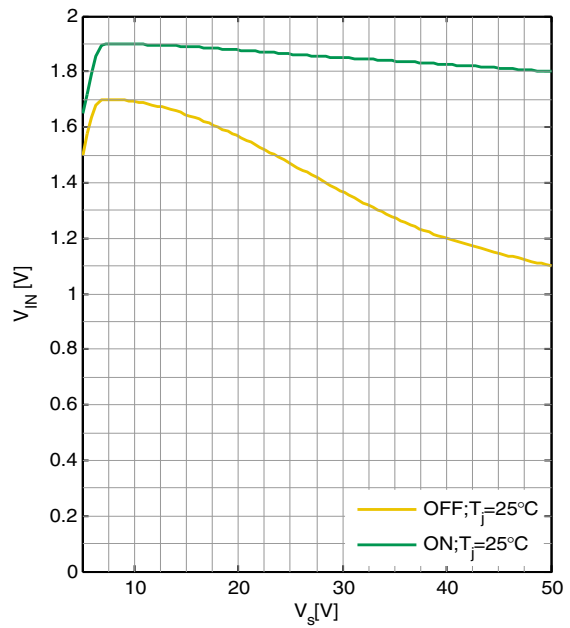
Input current consumption I_{IN} versus input voltage V_{IN}



Input threshold voltage $V_{INH,L}$ versus junction temperature T_j



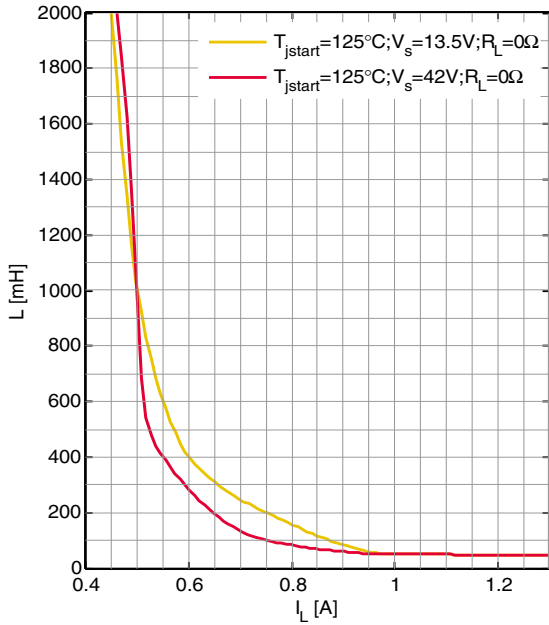
Input threshold voltage $V_{INH,L}$ versus supply voltage V_S



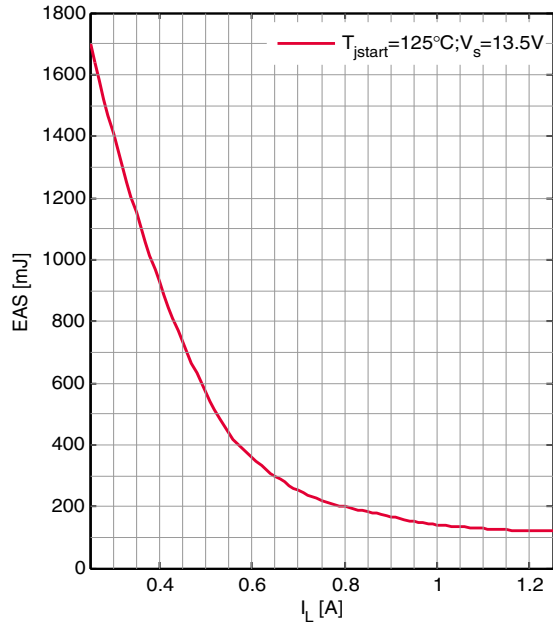
Typical performance graphs

Typical characteristics

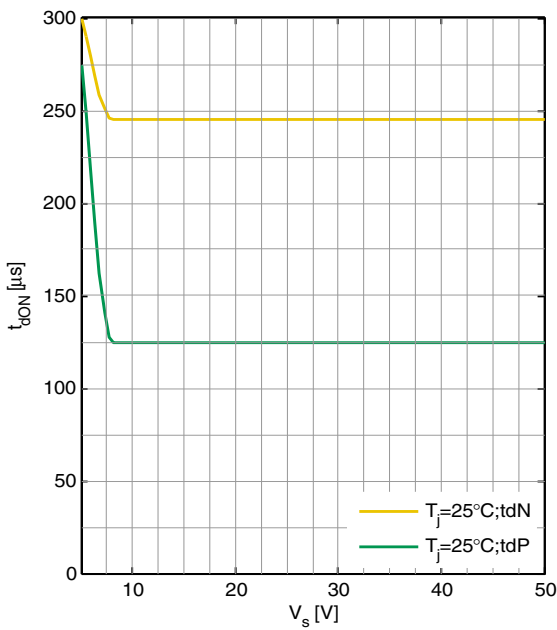
Max. allowable load inductance L versus load current I_L



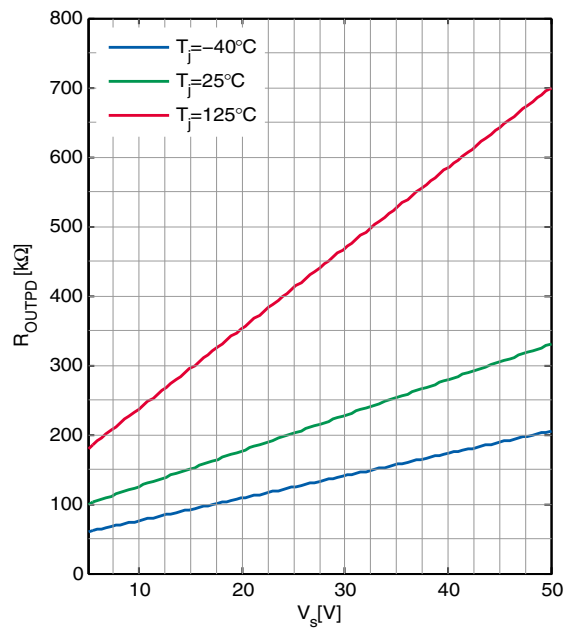
Max. allowable Inductive single pulse Switch-off energy E_{AS} versus load current I_L



Status delay time $t_{N,P}$ versus supply voltage V_S



Internal output pull down resistor R_{OUTPPD} versus supply voltage V_S



6 Application information

6.1 Application diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.

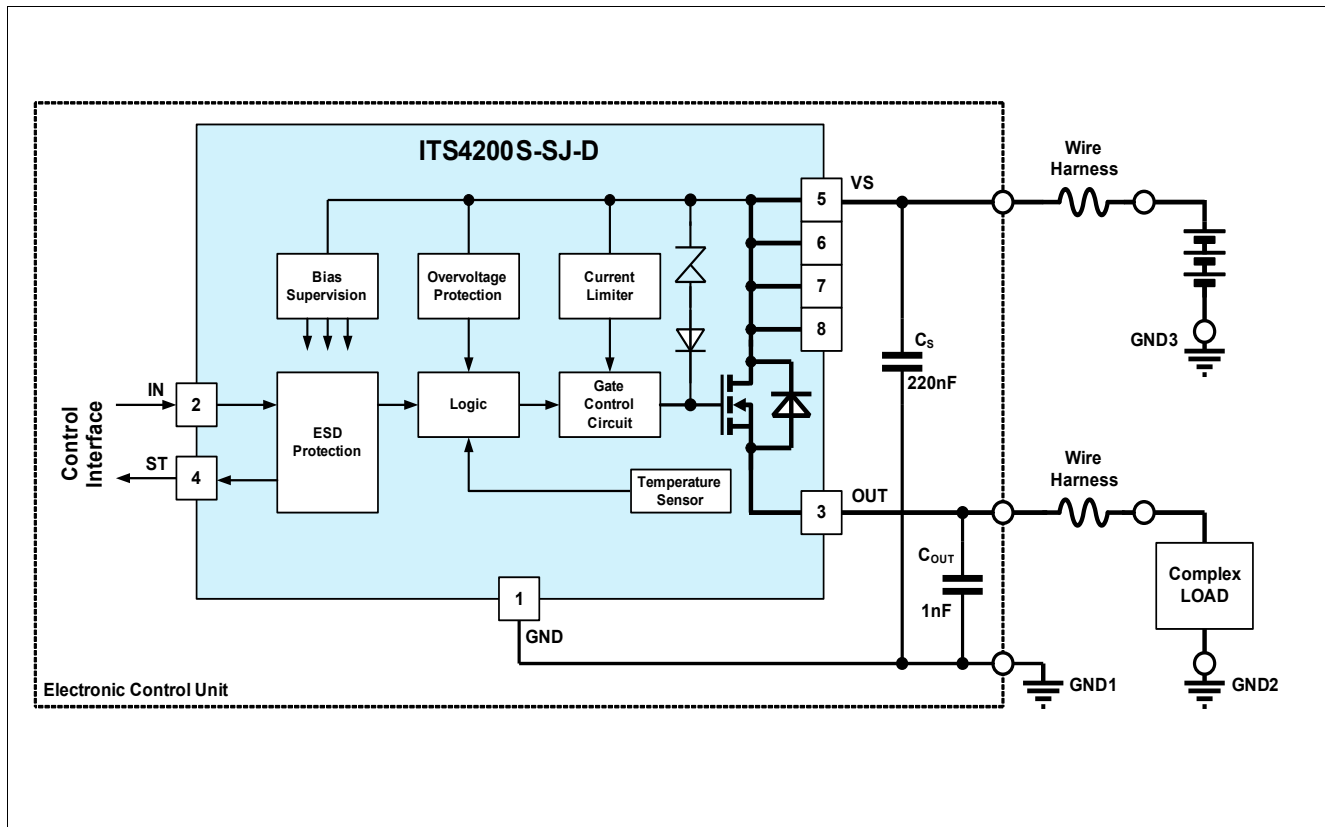


Figure 4 Application diagram

The ITS4200S-SJ-D can be connected directly to the battery of a supply network. It is recommended to place a ceramic capacitor (e.g. $C_S = 220\text{nF}$) between supply and GND of the ECU to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS4200S-SJ-D can be switched on and off with standard logic ground related logic signal at pin IN.

In standby mode (IN=L) the ITS4200S-SJ-D is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transition to minimize emissions. Only a small ceramic capacitor $C_{OUT}=1\text{nF}$ is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behavior of the ITS4200S-SJ-D is shown. For further details please refer to application notes on the Infineon homepage.

Application information

6.2 Diagnosis description

For diagnostic purpose the device provides a digital output pin ST in order to indicate fault conditions.

The status output (ST) of the ITS4200S-SJ-D is a high voltage open drain output.

In “normal” operation mode the NMOS open drain transistor is switched OFF.

The following truth table defines the status output.

Table 6 Truth table of diagnosis feature

| Device operation | IN | OUT | ST | Comment |
|---------------------------------------|-----------|------------|-----------|---|
| Normal operation | L | L | H | |
| Normal operation | H | H | H | |
| Short circuit to GND | L | L | H | |
| Short circuit to GND | H | L | L | OUT=L: $V_{OUT} < V_{OUTSC}$; Short circuit detection voltage; typ 2.8V |
| Short circuit to V_S (in OFF state) | L | H | L | |
| Short circuit to V_S (in OFF state) | H | H | H | |
| Overload | L | L | H | |
| Overload | H | H | H | OUT=H: $V_{OUT} > V_{OUTSC}$; Short circuit detection voltage; typ 2.8V |
| Overtemperature | L | L | H | |
| Overtemperature | H | L | L | |
| Open load in OFF state | L | Z | H | OUT=Z: high impedance; potential depends on external circuit |
| Open load in OFF state | L | H | L | with external resistor between V_S and OUT |

Application information

6.3 Special feature description

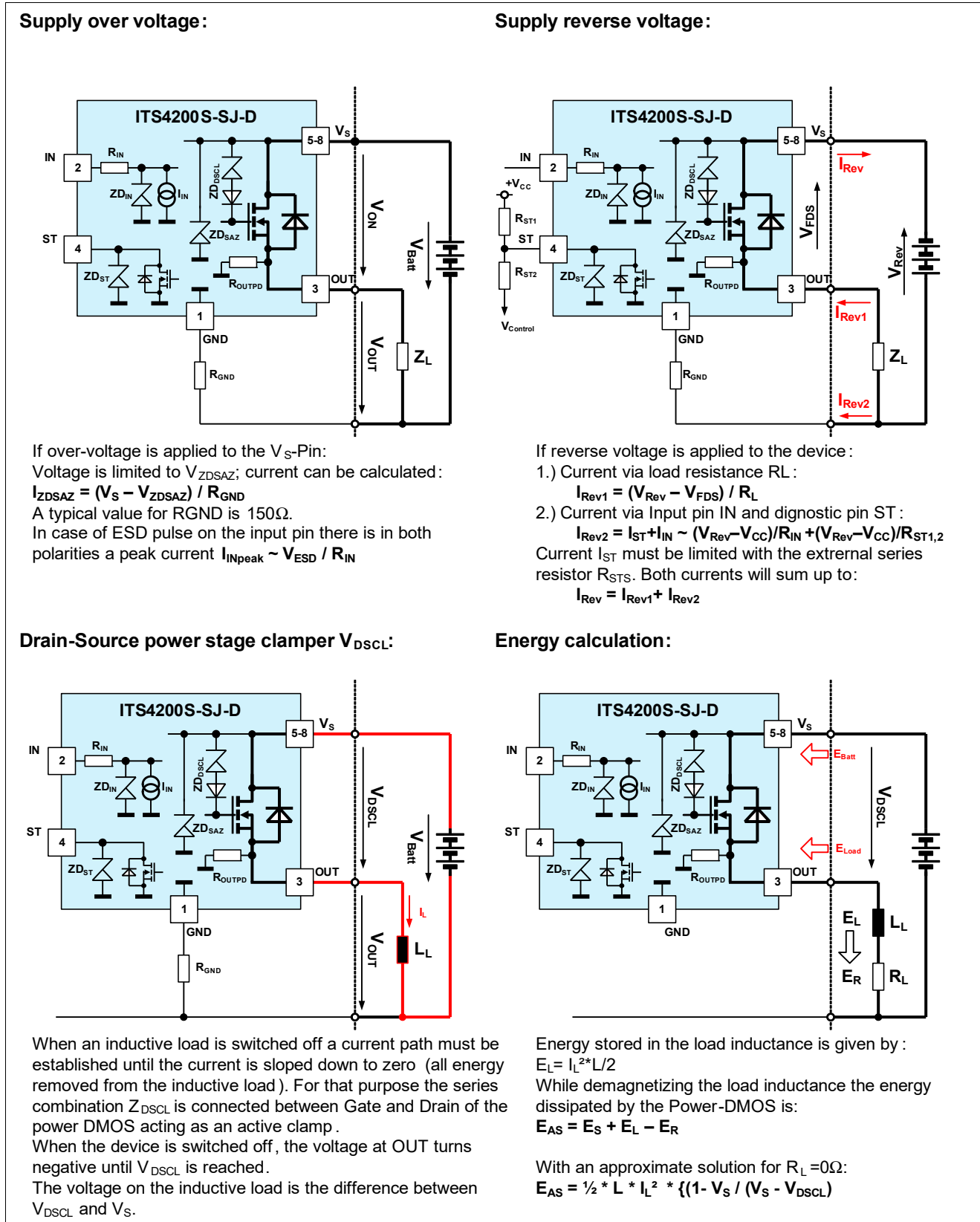


Figure 5 Special feature description

6.4 Typical application waveforms

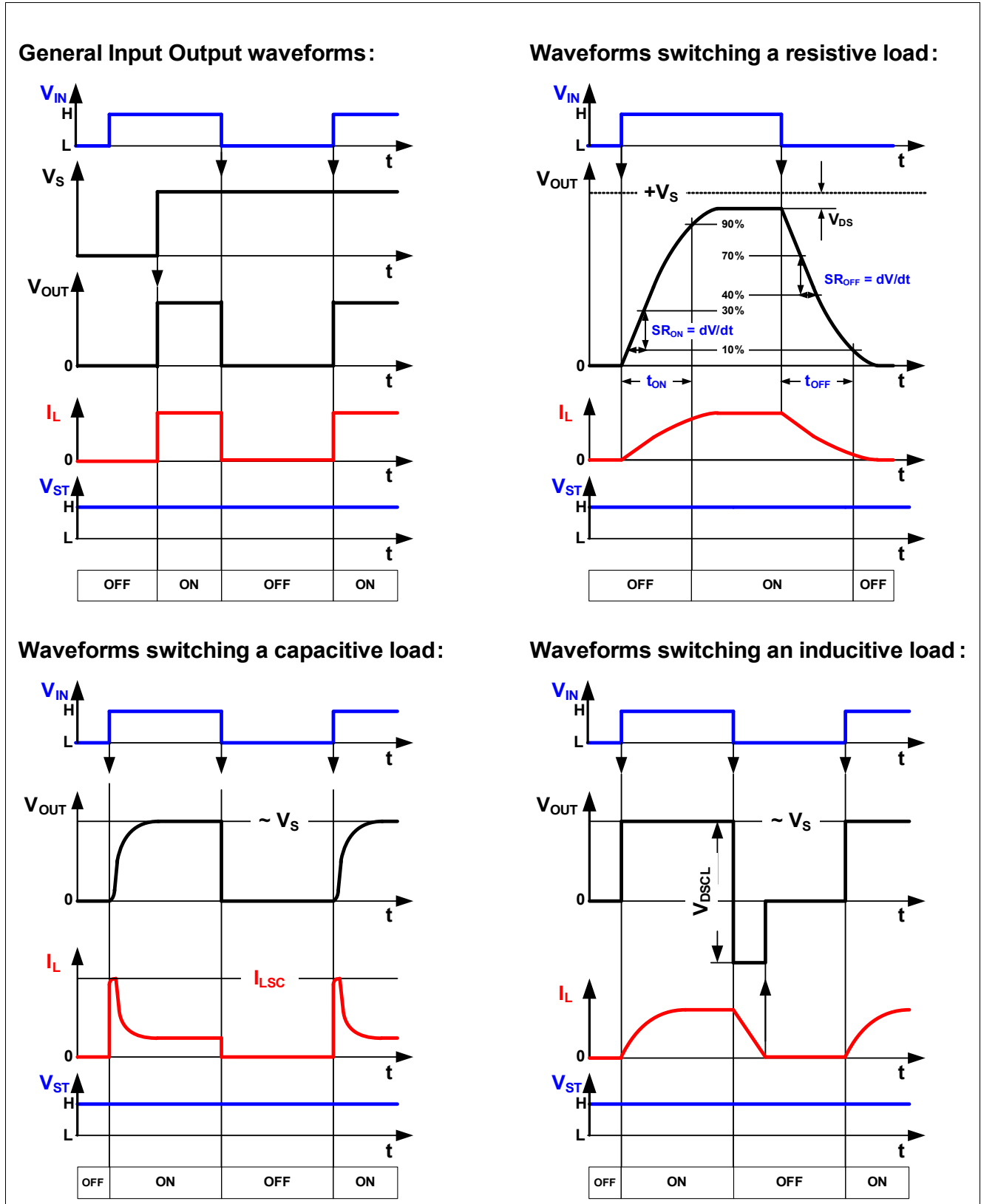


Figure 6 Typical application waveforms of the ITS4200S-SJ-D

6.5 Protection behavior

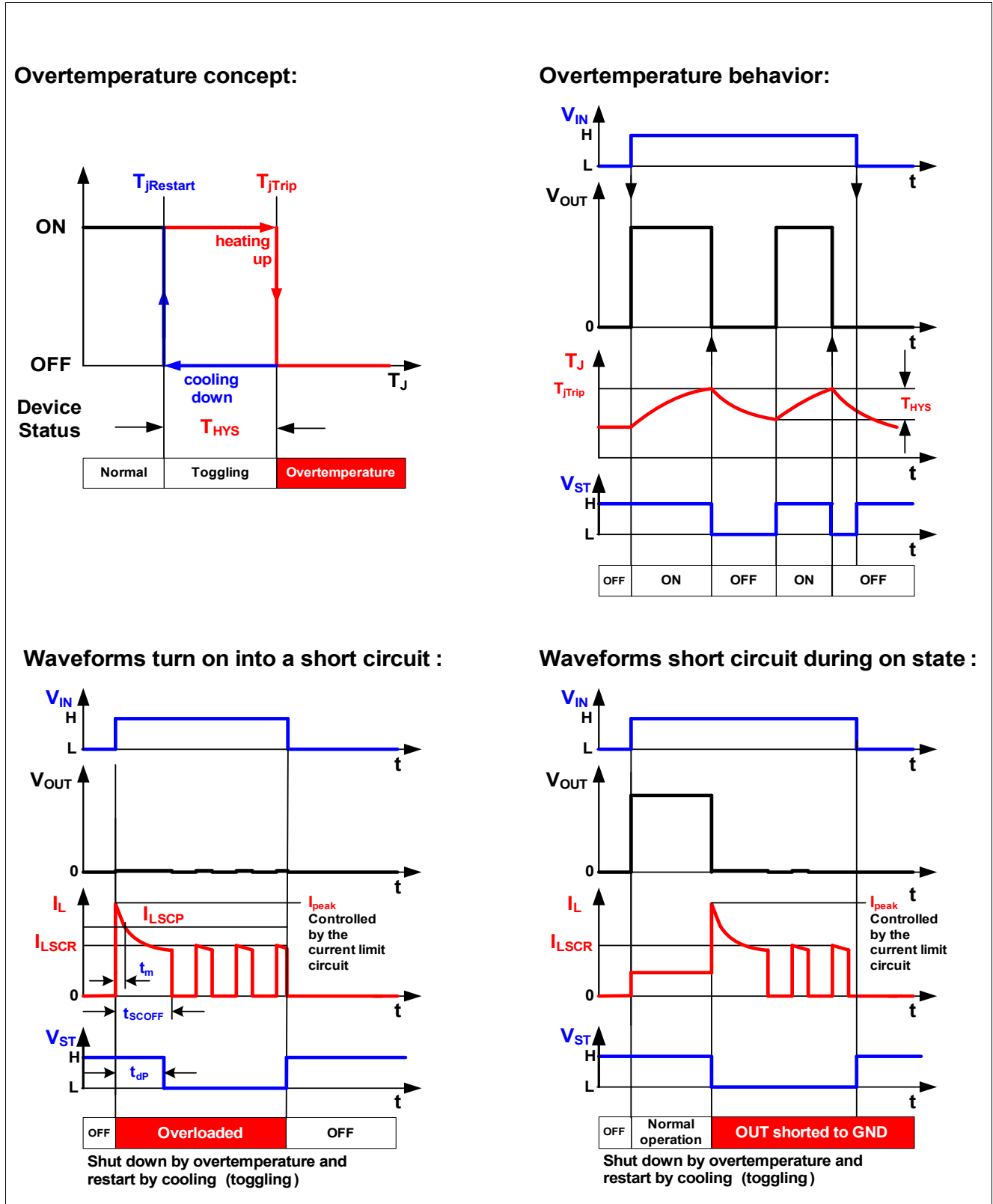


Figure 7 Protective behavior of the ITS4200S-SJ-D

Package information

7 Package information

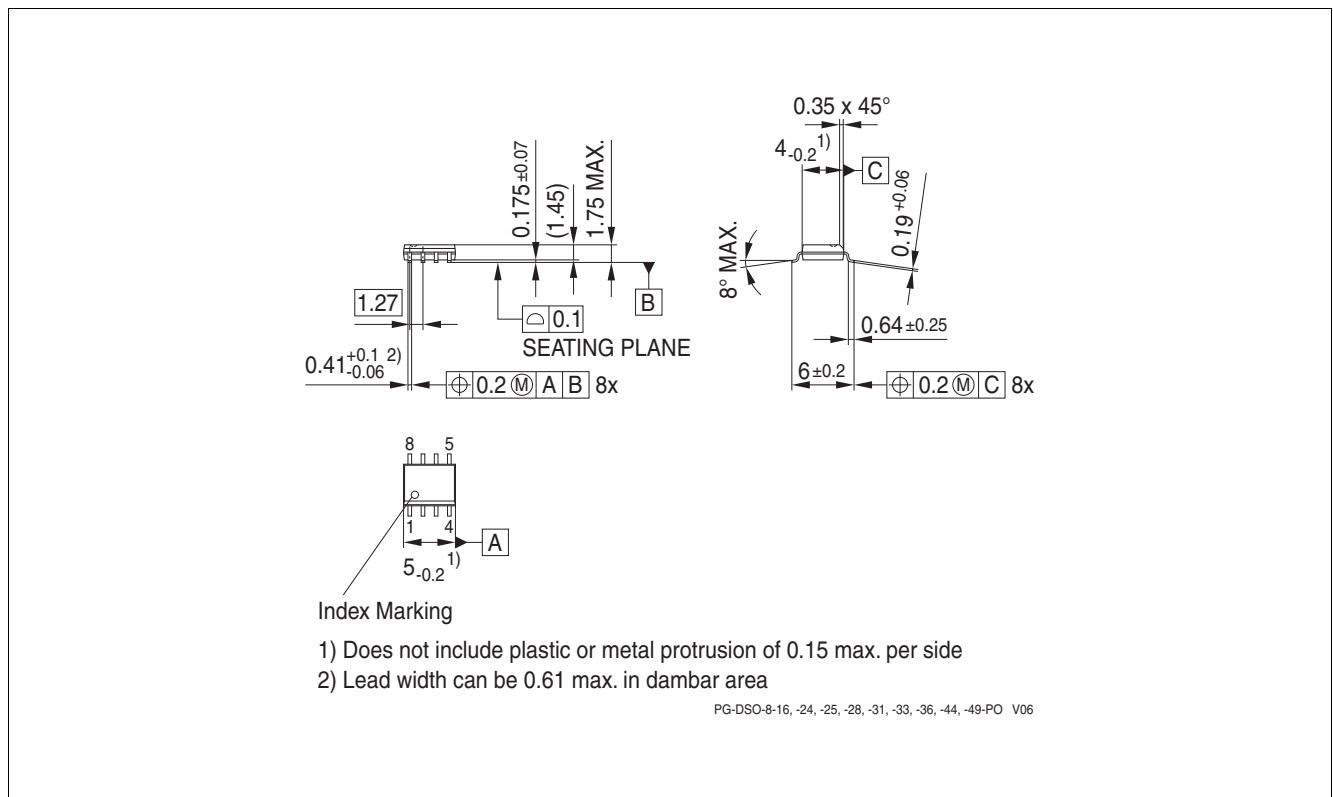


Figure 8 PG-DSO-8¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

Revision history

8 Revision history

| Revision | Date | Changes |
|----------|------------|---|
| 1.10 | 2019-07-25 | Datasheet updated: - ESD ratings for HBM updated according ANSI/ESDA/JEDEC JS-001 - Editorial changes |
| 1.0 | 2012-09-01 | Datasheet release |

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