Filterless and High-Efficiency +4V to +18V Audio Amplifier with I²S Digital Input

Description

The MA12040P is a super-efficient audio power amplifier based on proprietary multi-level switching technology. It supports a 4-18V supply voltage range, allowing it to be used in many different applications.

Multi-level switching enables very low power loss during operation. In addition, it allows the amplifier to be used in filterless configurations at full rated power in a wide range of audio products.

The MA12040P features an embedded digital power management scheme. The power management algorithm dynamically adjusts switching frequency and modulation to optimize power loss and EMI across the output power range.

An integrated digital-to-analog converter enables digital I2S audio stream input. It supports sample rates from 44.1 kHz to 192 kHz.

Highly flexible output stage configurations are offered, ranging from four single-ended outputs to a single parallel-BTL output.

The MA12040P features protection against DC, short-circuits, over-temperature and under-voltage situations.

Flexible “Power Mode Profiles” allow the user to utilize the multi-level switching technique for very low power loss or very high audio performance.

Device communication and programming is controlled through an I2C interface as well as dedicated control pins.

Applications

- Battery Operated Speakers
- Wireless and Docking Speakers
- Soundbars
- Multiroom Systems
- Home Theater Systems

Features

- Proprietary Multi-level Switching Technology
  - 3-level and 5-level modulation
    - Low EMI emission
    - Filterless amplification
  - Digital Power Management Algorithm
- High Power Efficiency (PMP4)
  - <110mW Idle power dissipation (18V PVDD, all channels switching)
  - >77% Efficiency at 1W power (1kHz sine, 8Ω)
  - >92% Efficiency at Full Power (1kHz sine, 8Ω)
- Audio Performance (PMP2)
  - >98dB DNR (A-w, rel. to 1% THD+N power level)
  - 135µV output integrated noise (A-w)
  - 0.006% THD+N at high output levels
- 4th Order Feedback Error Control
  - High suppression of supply disturbance
  - HD audio quality
- Supply Voltages: +4V to +18V (PVDD) and +5V (A/DVDD)
- Volume Control and Limiter
- 2×40W peak output power (18V PVDD, R_L = 4Ω, 10% THD+N level)
- 2×20W continuous output power (RL = 8Ω at 18V, PMP4, 10% THD+N level, without heatsink)
- 2.0, 2.1, 4.0, 1.0 Output Stage Configurations
- Protection
  - Under-voltage-lockout
  - Over-temperature warning/error
  - Short-circuit/overload protection
  - Power stage pin-to-pin short-circuit
  - Error-reporting through serial interface (I2C)
  - DC protection
- I2C control (four selectable addresses)
- Heatsink free operation with EPAD-down package

Package

- 64-pin QFN Package with exposed thermal pad (EPAD)
- Lead-free Soldering

1 Ordering Information

Table 1-1

Part Number	Package	Moisture Sensitivity Level	Description
MA12040PQFN	QFN-64	Level 3	Quad Flat No-leads package, EPAD-down (exposed thermal pad on bottom side)

2 Known Issues and Limitations

Please refer to the “MA12040 / MA12040P Known Issues and Limitations” document for descriptions of issues and limitations relating to device operation and performance.

3 Typical Application Block Diagram

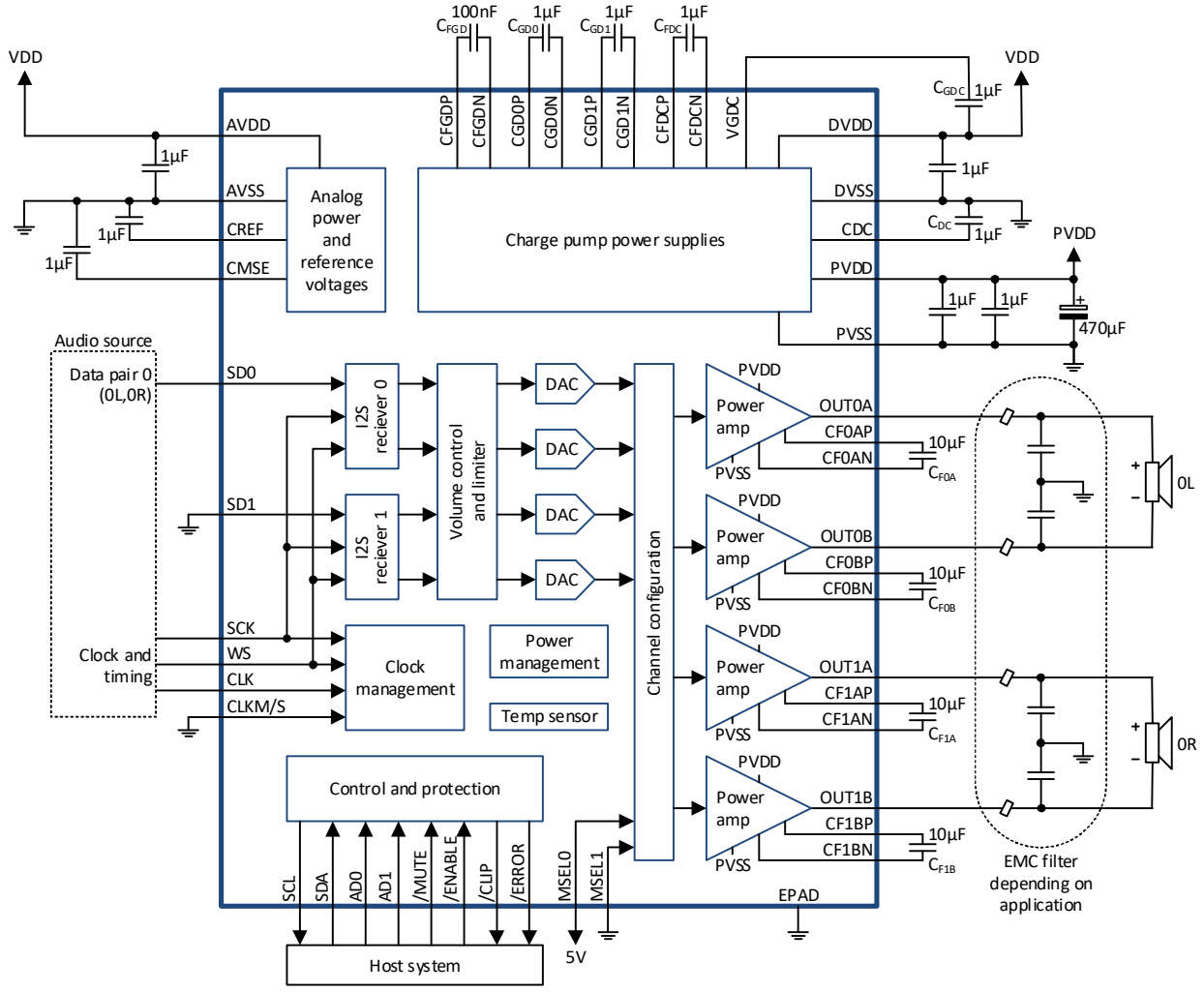


Figure 3-1 Typical application block diagram

4 Pin Description

4.1 Pinout MA12040PQFN

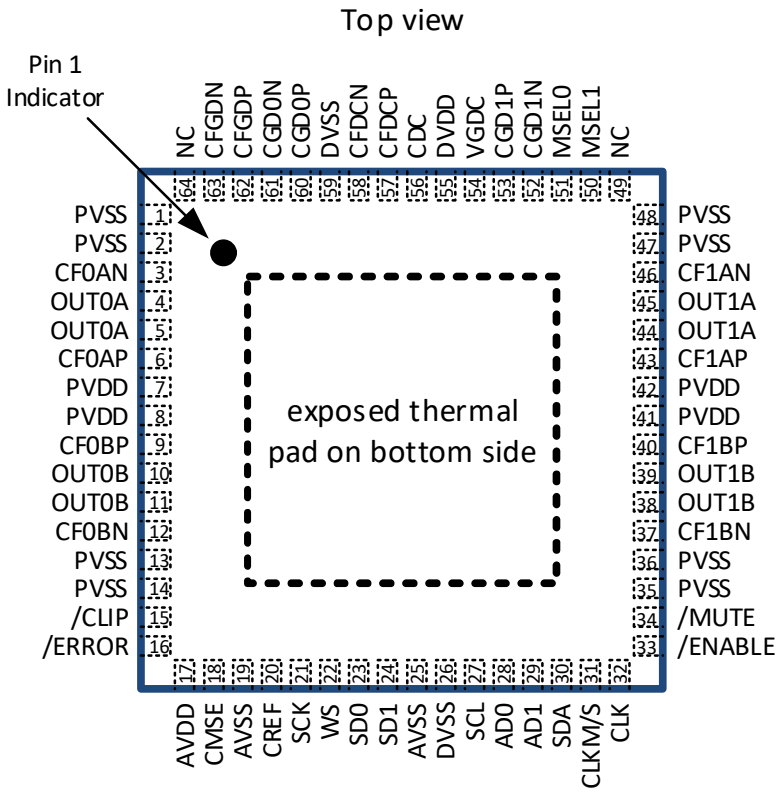


Figure 4-1 Pinout MA12040PQFN

4.2 Pin Function

Table 4-1

Pin No.	Name	Type[1]	Description
1	PVSS	P	Power ground for internal power amplifiers
2	PVSS	P	Power ground for internal power amplifiers
3	CF0AN	P	Connect to external flying capacitor negative terminal for amplifier channel 0A
4	OUT0A	O	Audio power output 0A
5	OUT0A	O	Audio power output 0A
6	CF0AP	P	Connect to external flying capacitor positive terminal for amplifier channel 0A
7	PVDD	P	Power supply for internal power amplifiers
8	PVDD	P	Power supply for internal power amplifiers
9	CF0BP	P	Connect to external flying capacitor positive terminal for amplifier channel 0B
10	OUT0B	O	Audio power output 0B
11	OUT0B	O	Audio power output 0B
12	CF0BN	P	Connect to external flying capacitor negative terminal for amplifier channel 0B
13	PVSS	P	Power ground for internal power amplifiers
14	PVSS	P	Power ground for internal power amplifiers
15	/CLIP	O	Audio clipping indicator (open drain output), pulled low when clipping occurs
16	/ERROR	O	Error indicator (open drain output), pulled low when an error occurs
17	AVDD	P	Power supply for internal analog circuitry
18	CMSE	O	Decoupling pin for internally generated common-mode voltage in SE configuration. Should be externally decoupled to AVSS.
19	AVSS	P	Ground for internal analog circuitry
20	CREF	O	Decoupling pin for internally generated analog reference voltage. Should be externally decoupled to AVSS.
21	SCK	I	I2S, digital audio serial clock. Must be synchronized to CLK
22	WS	I	I2S, digital audio word select. Must be synchronized to CLK
23	SD0	I	I2S, digital audio serial data pair 0
24	SD1	I	I2S, digital audio serial data pair 1
25	AVSS	P	Ground for internal analog circuitry
26	DVSS	P	Ground for internal digital circuitry
27	SCL	IO	I2C bus serial clock
28	AD0	I	I2C device address select 0 (see “MCU/Serial control interface” section)
29	AD1	I	I2C device address select 1 (see “MCU/Serial control interface” section)
30	SDA	IO	I2C bus serial data
31	CLKM/S	I	Reserved - must be pulled low
32	CLK	I	Clock input. Must be present before enabling the amplifier.
33	/ENABLE	I	When pulled high, the device is reset and kept in an inactive state with minimum power consumption.
34	/MUTE	I	Mute audio output when pulled low
35	PVSS	P	Power ground for internal power amplifiers
36	PVSS	P	Power ground for internal power amplifiers
37	CF1BN	P	Connect to external flying capacitor negative terminal for amplifier channel 1B
38	OUT1B	O	Audio power output 1B
39	OUT1B	O	Audio power output 1B
40	CF1BP	P	Connect to external flying capacitor positive terminal for amplifier channel 1B
41	PVDD	P	Power supply for power amplifiers

Pin No.	Name	Type[1]	Description
42	PVDD	P	Power supply for power amplifiers
43	CF1AP	P	Connect to external flying capacitor positive terminal for amplifier channel 1A
44	OUT1A	O	Audio power output 1A
45	OUT1A	O	Audio power output 1A
46	CF1AN	P	Connect to external flying capacitor negative terminal for amplifier channel 1A
47	PVSS	P	Power ground for internal power amplifiers
48	PVSS	P	Power ground for internal power amplifiers
49	NC	P	Internally connected to DVDD
50	MSEL1	I	SE/BTL/PBTL configuration select 1
51	MSEL0	I	SE/BTL/PBTL configuration select 0
52	CGD1N	P	Connect to external decoupling capacitor negative terminal for internal gate driver power supply 1
53	CGD1P	P	Connect to external decoupling capacitor positive terminal for internal gate driver power supply 1
54	VGDC	P	Internally generated virtual ground voltage for digital core. Should be decoupled to DVDD.
55	DVDD	P	Power supply for internal digital circuitry and charge pumps
56	CDC	P	Connect to external decoupling capacitor for digital core internal power supply
57	CFDCP	P	Connect to external flying capacitor positive terminal for internal digital core power supply
58	CFDCN	P	Connect to external flying capacitor negative terminal for internal digital core power supply
59	DVSS	P	Power ground for internal digital circuitry
60	CGD0P	P	Connect to external decoupling capacitor positive terminal for internal gate driver power supply 0
61	CGD0N	P	Connect to external decoupling capacitor negative terminal for internal gate driver power supply 0
62	CFGDP	P	Connect to external flying capacitor positive terminal for internal gate driver power supplies
63	CFGDN	P	Connect to external flying capacitor negative terminal for internal gate driver power supplies
64	NC	P	Internally connected to DVDD

Type[1]: P = Power; I = Input; O = Output; IO = Input or Output

5 Absolute Maximum Ratings

Table 5-1

Parameter		Value	Unit
Power Supplies			
	Power stage supply voltage, PVDD	-0.5 to +20	V
	System supply voltage, DVDD, AVDD	-0.5 to +6.0	V
Input / Output			
	Digital: SCK, WS, SD0, SD1	-0.5 to +6.0	V
	Logic: /ENABLE, /MUTE, /ERROR, /CLIP, MSEL0, MSEL1	-0.5 to +6.0	V
	Clock: CLK, CLKM/S	-0.5 to +6.0	V
	Interface: SCL, SDA, AD0, AD1	-0.5 to +6.0	V
	Output current, Logic and Interface	25	mA
Thermal Conditions			
	Ambient temperature range, T_A	-40 to +85	°C
	Junction temperature range, T_J	-40 to +150	°C
	Storage temperature range	-65 to +150	°C
	Thermal resistance, Junction-to-Ambient	23	°C/W
	Thermal resistance, Junction-to-EPAD	2.3	°C/W
	Lead soldering temperature, 10s	300	°C
Electrostatic Discharge (ESD)			
	Human body model (HBM)	± 2000	V
	Charged device model (CDM)	± 1000	V

PLEASE NOTE:

Device usage beyond the above stated ratings may cause permanent damage to the device. Permanent usage at the above stated ratings may limit device lifetime and result in reduced reliability. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

See “Recommended Operation Conditions” for continuous functional ratings.

6 Recommended Operating Conditions

Table 6-1

Symbol	Parameter	Min	Typ	Max	Unit
PVDD	Power Stage Power Supply	4		18	V
DVDD	Digital Power Supply	4.75	5	5.25	V
AVDD	Analog Power Supply	4.75	5	5.25	V
V_{IH}	High Level for Logic, Clock, Interface	2			V
V_{IL}	Low Level for Logic, Clock, Interface			0.8	V
V_{IN_dc}	DC Offset Level for Analog Inputs	1.2	2.5	3.8	V
V_{IN_ac}	Audio Signal Level for Analog Inputs		1.8		Vpp
R_L (BTL)	Minimum Load in Bridge-Tied Load Mode	3.2	4		Ω
R_L (PBTL)	Minimum Load in Parallel Bridge-Tied Load Mode	1.6	2		Ω
R_L (SE)	Minimum Load in Single Ended Mode	2.4	3		Ω
L_{Leq}	Minimum required equivalent load inductance per output pin for short circuit protection	0.5			µH
T_A	Ambient temperature range	0	+25	+85	°C

Note: Minimum Load resistance was measured in Filterless output condition.

7 Electrical and Audio Characteristics

Table 7-1

Power Mode Profile = 0; VDD (Analog & Digital) = +5V; PVDD = +18V; T_A = 0°C to +85°C. Typical values are at T_A = +25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{OUT} (BTL)	Output Power per channel (peak) Without Heatsink, see Note 1	THD+N = 10%, RL = 8Ω, f = 1kHz		20		W
		THD+N = 10%, RL = 4Ω, f = 1kHz		40		W
		THD+N = 1%, RL = 8Ω, f = 1kHz		15		W
		THD+N = 1%, RL = 4Ω, f = 1kHz		30		W
	Output Power per channel (continuous) Without Heatsink, see Note 2	RL = 8Ω, f = 1kHz, PVDD = +18V		20		W
		RL = 4Ω, f = 1kHz, PVDD = +13V		20		W
P_{OUT} (PBTL)	Output Power (peak), see Note 1	THD+N = 10%, RL = 2Ω, f = 1kHz		80		W
		THD+N = 1%, RL = 2Ω, f= 1kHz		60		W
P_{OUT} (SE)	Output Power per channel (peak), see Note 1	THD+N = 10%, RL = 4Ω, f = 1kHz		10		W
		THD+N = 10%, RL = 3Ω, f = 1kHz		14		W
		THD+N = 1%, RL = 4Ω, f = 1kHz		8		W
		THD+N = 1%, RL = 3Ω, f = 1kHz		11		W
T_{ENABLE}	Shutdown/Full Operation Timing	NENABLE = 1 → 0	1			ms
T_{MUTE}	Mute/Unmute Timing	NMUTE = 1 → 0 and 0 → 1	0.3			ms
V_{OS}	Output Offset Voltage				±200	mV
PSRR	Power Supply Rejection Ratio	± 100mVpp ripple voltage		70		dB
R_{on}	Resistance, switch on		0.10	0.15	0.20	Ω
f_{SW}	Power MOSFET Switching Frequency, see Note 3	Power Mode A	618	672	726	kHz
		Power Mode B & C	316	336	356	kHz
		Power Mode D	158	168	178	kHz
f_{CLK_IO}	Clock Output Frequency		2.7151	2.8224	2.9296	MHz
I_{OUT}	Maximum Output Current		6			A
X_{Talk}	Crosstalk	BTL, POUT = 1W, f=1kHz, Ch1 & 2		-108		dB

Note 1: The thermal design of the target application will significantly impact the ability to achieve the peak output power levels for extended time. See “Thermal Characteristics and Test Signals” section for thermal optimization recommendations.

Note 2: Continuous power measurements were performed on the MA12040/MA12040P proprietary Amplifier EVK without heatsinking at 25°C ambient temperature in Power Mode Profile 4.

Note 3: Power MOSFET switching frequency depends on which properties are assigned to the individual power modes of the device. Detailed information on this can be found in “Power Mode Management” section.

Table 7-2

VDD (Analog & Digital) = +5V; PVDD = +18V; Typical values are at T_A = +25°C; Output Configuration: BTL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
η	Efficiency	POUT = 2×20W, 8Ω , PMP = 0		91		%
		POUT = 2×20W, 8Ω , PMP = 1		91		%
		POUT = 2×20W, 8Ω , PMP = 2		90		%
		POUT = 2×20W, 8Ω , PMP = 4		92		%
		POUT = 2×40W, 4Ω , PMP = 0		88		%
		POUT = 2×40W, 4Ω , PMP = 1		88		%
		POUT = 2×40W, 4Ω , PMP = 2		87		%
		POUT = 2×40W, 4Ω , PMP = 4		89		%

Table 7-3

Power Mode Profile = 0; VDD (Analog & Digital) = +5V; PVDD = +18V; T_A = 0°C to +85°C. Typical values are at T_A = +25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{shutdown}$	Current Consumption, PVDD	Shutdown	10	35	180	µA
$I_{idle,mute}$	Current Consumption, PVDD	Idle, mute	4	6	9	mA
$I_{idle,unmute}$	Current Consumption, PVDD	Idle, unmute, inputs grounded	4	7	12	mA
$I_{AVDD+DVDD}$	Current Consumption, AVDD+DVDD	Idle, unmute, inputs grounded	30	35	42	mA
THD+N	Total Harmonic Distortion + Noise	1kHz, POUT = 1W, RL = 4Ω		0.012		%
		1kHz, POUT = 20W, RL = 4Ω		0.015		%
DNR	Dynamic Range[1]	20-20kHz, A-weighted		97		dB
V_{noise}	Output integrated noise level	20-20kHz, A-weighted	105	150	190	µVrms

Table 7-4

Power Mode Profile = 2; VDD (Analog & Digital) = +5V; PVDD = +18V; T_A = 0°C to +85°C. Typical values are at T_A = +25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{shutdown}$	Current Consumption, PVDD	Shutdown	10	35	180	µA
$I_{idle,mute}$	Current Consumption, PVDD	Idle, mute	4	6	9	mA
$I_{idle,unmute}$	Current Consumption, PVDD	Idle, unmute, inputs grounded	4	8	14	mA
$I_{AVDD+DVDD}$	Current Consumption, AVDD+DVDD	Idle, unmute, inputs grounded	33	38	45	mA
THD+N	Total Harmonic Distortion + Noise	1kHz, POUT = 1W, RL = 4Ω		0.010		%
		1kHz, POUT = 20W, RL = 4Ω		0.012		%
DNR	Dynamic Range[1]	20-20kHz, A-weighted		98		dB
V_{noise}	Output integrated noise level	20-20kHz, A-weighted	110	135	170	µVrms

[1] Output power at THD+N < 1% reference to noise floor at -60dBFS signal.

NOTE: MA12040P gives users the freedom to choose Power Mode Profiles (PMP) independently. As noted in the specifications table, the choice in power mode profiles gives a trade-off between power efficiency and audio performance as an individual set of performance characteristics. See "Power Mode Profiles" section for more details.

8 Functional description

Multi-level modulation

The power stage of the MA12040P is a true multi-level switching topology. Each half-bridge is capable of delivering a PWM output with three voltage levels, rather than the conventional two. The three-level half-bridges are each driven with a two-phase PWM signal, so that the switching frequency seen at the PWM output is twice that of the individual power MOSFET switching frequency.

For very low EMI in BTL configuration, the two half-bridges are operated in a complementary fashion (i.e. with 180^o phase shift), which removes common-mode PWM output content. This configuration is ideal for driving long speaker cables without an output filter. Differentially, this modulation method drives the filter/load assembly with three PWM levels.

For reduced power loss in the BTL configuration, the half-bridges can also be driven in a quadrature phase shifted fashion (i.e. with 90^o phase shift). This provides a total of five PWM levels at the load, along with a quadrupling of MOSFET switching frequency with respect to the differential PWM switching frequency. With this modulation scheme, the MOSFET switching frequency can therefore be lowered, in order to decrease switching losses. The five-level modulation scheme produces a common-mode voltage on the load wires, but with less high-frequency content compared to conventional two-level BD modulation.

The multi-level switching topology of the MA12040P makes filterless operation viable, since the modulation schemes ensure little or no idle losses in the speaker magnetic system.

For applications with stringent EMC requirements or long speaker cables, the MA12040P can operate with a very small and inexpensive EMI/EMC output filter. This is enabled by the multiple PWM output levels and the frequency multiplication seen on the PWM switching nodes. Notably, with the multi-level modulation of the MA12040P, there is no tradeoff between idle power loss and inductor cost/size, which is due to the absence of inductor ripple current under idle conditions in all configurations. Due to the high filter cutoff frequency, non-linearities of LC components have less impact on audio performance than with a conventional amplifier. Therefore, the MA12040P can operate with inexpensive iron-powder cored inductors and ceramic (X7R) filter capacitors with no significant audio performance penalty.

Very low power consumption

The MA12040P achieves very low power loss under idle and near-idle operating conditions. This is due to the zero idle ripple property of the multi-level PWM scheme, in combination with the programmable automatic reduction of switching frequency at low modulation index levels; resulting in a state-of-the-art power efficiency at low and medium output power levels.

For high output power levels, power efficiency is determined primarily by the on-resistance (Rds_{on}) of the output power MOSFETs. With music and music-like (e.g. pink noise) output signals with high crest factor, the reduced near-idle losses of the MA12040P contribute to reducing power losses compared to a conventional amplifier with the same Rds_{on}. In most applications, this allows the MA12040P to run at high power levels without a heatsink.

Power Mode Management

The MA12040P is equipped with an intelligent power management algorithm which applies automatic power mode selection during audio playback. In this state, the amplifier will seamlessly transition between three different power modes depending on the audio level in order to achieve optimal performance in terms of power loss, audio performance and EMI. Figure 8-1 shows an illustration of the basic power mode management. Alternatively, it is possible to manually select the desired power mode for the MA12040P via the serial interface.

In both manual and automatic power mode selection, the power mode can be configured and set on-the-fly during audio playback, with no audible artifacts. This makes it possible to optimize the target application to achieve the best possible operating performance at all audio power levels.

During automatic power mode selection, the MA12040P can transition between power modes at programmable audio level thresholds. The thresholds can be set via the serial control interface, by addressing the associated registers.

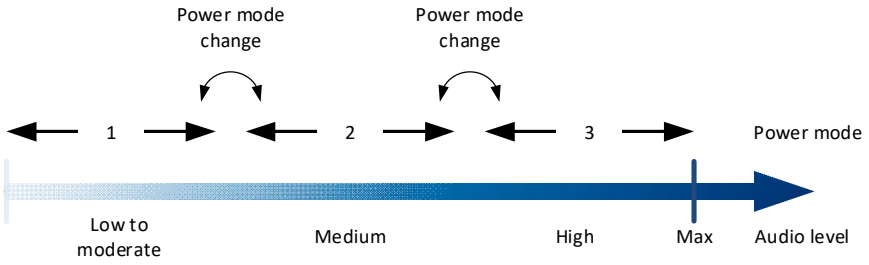


Figure 8-1 Illustration of automatic power mode selection ranges.

To allow easy use of the power mode management, “Power Mode Profiles” have been defined. The “Power Mode Profiles” address the appropriate power modes for a variety of applications.

Power Modes Profiles

The MA12040P provides 5 different power mode profiles for operating the internal power amplifiers. The power mode profiles give the user freedom to choose optimal settings of the amplifier for the intended application.

The available power modes profiles are referred to as 0, 1, 2, 3 and 4 and can be set by programming the according register (see Register Map). The power mode profile selection affects various parameters such as switching frequency, modulation scheme and loop-gain, thus providing flexibility in design tradeoffs such as audio performance, power loss and EMI. Table 8-1 shows the characteristics of the power mode profiles.

Table 8-1 Power Mode Profile characteristics

Property	Profile 0	Profile 1	Profile 2	Profile 3	Profile 4
PM switch seq.	D↔D↔C	B↔B↔B	B↔B↔A	D↔B↔A	D↔D↔D
Idle loss	Very low	Low	Low	Very low	Very low
Full scale efficiency	Good	Good	Good	Normal	Best
THD+N	Good	Best	Best	Good/Best	Good
Common-mode content, idle	Only DC	Only DC	Only DC	Only DC	Only DC
Common-mode content, full-scale audio	Only DC	DC + Sidebands around 660kHz, 1.98MHz, 3.3MHz	Only DC	Only DC	DC + sidebands around 330kHz, 990kHz, 1.65MHz
Differential content low-to-mid-power	Audio + sidebands around multiples of 1.2MHz	Audio + sidebands around multiples of 1.2MHz	Audio + sidebands around multiples of 1.32MHz	Audio + sidebands around multiples of 660kHz	Audio + sidebands around multiples of 660kHz
Differential content mid-to-high power	Audio + sidebands around multiples of 600kHz	Audio + sidebands around multiples of 1.2MHz	Audio + sidebands around multiples of 1.32MHz	Audio + sidebands around multiples of 1.32MHz	Audio + sidebands around multiples of 660kHz
Application	Filterfree: optimized efficiency, default applications	Filterfree: optimized audio performance, active speaker applications	Filterfree: optimized audio performance, default applications	LC filter: high efficiency, high audio perform-ance, good EMI, low ripple loss	Filterfree: optimized efficiency, active speaker applications

Note: There is a programmable “Profile 5” which allows the user to set up a custom profile.

The first row of Table 8-1 shows that each Power Mode Profile follows a certain Power Mode transition sequence. This means that each Power Mode within every Power Mode Profile will have its specific set of properties (A, B, C or D). The exact details of each assigned set of properties is reflected in Table 8-2.

Table 8-2 Set of properties assigned to Power Modes in the selectable Power Mode Profiles

Property	A	B	C	D
FET switching frequency, f_{FET}	660kHz	330kHz	330kHz	165kHz
Modulation scheme	3-level	5-level	3-level	5-level
Switching frequency seen at load, f_{SW}	1.32MHz (2 x f_{FET})	1.32MHz (4 x f_{FET})	660kHz (2 x f_{FET})	660kHz (4 x f_{FET})
Idle loss	Reduced	Low	Low	Very low
Full scale efficiency	Normal	Good	Good	Best
Open-loop gain	High	High	Low	Low
THD+N	Best	Best	Good	Good
Common-mode content, idle	Only DC	Only DC	Only DC	Only DC
Common-mode content, full-scale audio	Only DC	DC + sidebands around 660kHz, 1.98MHz, 3.3MHz	Only DC	DC + sidebands around 330kHz, 990kHz, 1.65MHz
Differential content	Audio + sidebands around multiples of 1.32MHz	Audio + sidebands around multiples of 1.32MHz	Audio + sidebands around multiples of 660kHz	Audio + sidebands around multiples of 660kHz

Next to the pre-defined Power Mode Profiles it is also possible to define a custom profile which will be available under Power Mode Profile 5. This profile can be configured using the “custom power mode profile” register (address 30). See “Register Map” section for more details.

The MA12040P employs feedback of the output PWM signals in order to compensate for noise and other non-idealities in the power processing path. A fourth-order analog feedback loop is used, which typically provides a loop gain of 60dB to suppress errors in the audio band. For the typical high efficiency application this results in low THD (Total Harmonic Distortion) at all audio frequencies, as well as excellent immunity (in excess of 75dB) to power supply borne interferences.

Maximum achievable loop-gain is typically set by the PWM frequency stability criteria. Inherent frequency multiplication of the multilevel topology therefore allows for a much more aggressive loop-filter (and therefore better THD and noise properties) because of a higher effective PWM switching frequency seen at the output. See “Profile 0 and Profile 2” in Table 8-1 for high-fidelity Power Mode Profiles.

For the lowest switching frequencies, the proprietary loop filter architecture seamlessly reduces feedback bandwidth to ensure loop stability. In most applications (e.g. filterless applications), no further special attention is required to ensure loop stability. In applications with very stringent EMI requirements, an LC filter can be used. In these cases attention to loop stability is required since an un-damped LC filter effectively represents a short-circuit to ground at the resonance frequency. In extreme cases, this can cause instability of the analog feedback loops. In order to avoid this, an LC filter should use an inductor with more than 10mΩ DC resistance, and a series R-C circuit should be used to limit the Q of the LC circuit to around 5.

Power supplies

The MA12040P generates internal supply voltages and uses external capacitors for this purpose and for decoupling.

Gate driver supplies

The MA12040P utilizes a floating supply voltage for the gate driver circuitry generated internally by a charge pump. The gate driver power supply voltage is approximately 6V to 9V higher than PVDD. Table 8-3 shows the required external charge pump and decoupling capacitors.

Table 8-3 Gate driver supply capacitors

Name	Purpose	Connection	Type	Value
C_{GD0}	Decoupling of gate driver supply voltage 0	CGD0P, CGD0N	16V, high capacity, low precision	1uF
C_{GD1}	Decoupling of gate driver supply voltage 1	CGD1P, CGD1N	16V, high capacity, low precision	1uF
C_{FGD}	Charge pump flying capacitor	CFGDP, CFGDN	50V, high capacity, low precision	100nF

Digital core supply

The digital control unit in the MA12040P uses a supply voltage generated internally by a charge pump and a voltage regulator for highest efficiency. Table 8-4 lists the external capacitors required and describes their function and connection.

Table 8-4 Digital supply capacitors

Name	Purpose	Connection	Type	Value
C_{DC}	Charge pump output voltage decoupling to GND	CDC, GND	>=6.3V, high capacity, low precision	1uF
C_{FDC}	Charge pump flying capacitor	CFDCP, CFDCN	>=6.3V, high capacity, low precision	1uF
C_{GDC}	Decoupling of digital core virtual ground voltage on the VGDC pin. The voltage on the VGDC pin is approximately 1.8V below DVDD, i.e. about 3.2V	VGDC, DVDD	>=6.3V, high capacity, low precision	1uF

Flying capacitors

The MA12040P power stage uses flying capacitors to generate a ½PVDD supply voltage to enable multi-level operation. Each output switch node OUTXX has a corresponding flying capacitor, with a positive and a negative terminal, CFXXP and CFXXN.

The two flying capacitor terminals are to be considered high power switching nodes carrying voltages and currents similar to that on the OUTXX nodes. Care must be taken in the PCB design to reduce both the inductance and the resistance of these nodes. Table 8-5 lists the flying capacitors, incl. connection, type and value.

Table 8-5 Flying capacitors

Name	Purpose	Connection	Type	Value
C_{F0A}	Half-bridge 0A flying capacitor	CF0AP, CF0AN	>=25V, high capacity, low precision	10uF
C_{F0B}	Half-bridge 0B flying capacitor	CF0BP, CF0BN	>=25V, high capacity, low precision	10uF
C_{F1A}	Half-bridge 1A flying capacitor	CF1AP, CF1AN	>=25V, high capacity, low precision	10uF
C_{F1B}	Half-bridge 1B flying capacitor	CF1BP, CF1BN	>=25V, high capacity, low precision	10uF

Care must be taken when choosing flying capacitors in applications where maximum output power is needed. The effective capacitance of poor ceramic capacitors can be greatly reduced when a DC bias voltage is applied. A recommended part is the GRM21BZ71E106KE15L capacitor from Murata. Other parts may also be used as long as the effective capacitance is minimum 3.0 µF at 0.5*PVDD voltage.

Protection

The MA12040P integrates a range of protection features to protect the device and attached speakers from damage. Protection features include:

- Current protection on OUTXX nodes during operation.
- On-chip temperature sensor for protection against device over-heating.
- Undervoltage supply monitors on AVDD, DVDD, VGDC and PVDD.
- DC protection, preventing DC to be present on the amplifier outputs.

Over-current protection on OUTXX nodes

During switching operation the output stage monitors the forward current flow in all output switches that are turned on. This is done to limit the maximum power dissipated in the switches and prevent damage to the device and the speaker load. The current in the output stage can exceed unwanted levels if:

- The speaker load impedance drops to a low value while the device is powered from a high PVDD supply.
- A failure occurs on the speaker terminals causing a low impedance short.
- The speaker is damaged and thereby exhibiting a low impedance.

Over-current protection and short-circuit protection use a latching mechanism. If an over current or a short-circuit condition occurs, it will shut down the power stage and report the error on the /ERROR pin. By default the device will restart. Current limiting will not occur for currents below the OCE_{THR} level, see Table 7-1.

Current protection against speaker terminal shorts requires an equivalent load inductance L_{Leq} on each of the output OUTXX pins (see Table 6-1). Load inductance from loudspeaker cables and, if used, ferrite beads (EMC filter) will typically be sufficient.

Temperature protection

An on-chip temperature sensor effectively safeguards the device against a thermally induced failure due to overloading and/or insufficient cooling.

A high junction temperature initially causes a temperature warning, TW. This can be detected by reading the error register (address 124, bit 4) via I2C. If the temperature continues to rise the device will reach the temperature error (TE) level and set the TE bit in the error register (address 124, bit 5). This will cause the device to stop all switching activity. The device will restart after sufficient cooling down of the system. Both TW and TE will report the error on the /ERROR pin.

Table 8-6 High-Temperature Warning and Error Signaling Levels

Symbol	Parameter	Test Conditions	Typical Value	Unit
$TE_{THR,SET}$	High-Temperature Error (TE) Set Threshold	Temperature rising	150	°C
$TE_{THR,CLR}$	High-Temperature Error (TE) Clear Threshold	Temperature falling	135	°C
$TW_{THR,SET}$	High-Temperature Warning (TW) Set Threshold	Temperature rising	125	°C
$TW_{THR,CLR}$	High-Temperature Warning (TW) Clear Threshold	Temperature falling	105	°C

Power supply monitors

The MA12040P features integrated PVDD, DVDD and AVDD under-voltage lockout. Table 8-7 shows typical limits for the supply monitors.

Table 8-7 Under-voltage lockout levels

Symbol	Parameter	Test Conditions	Typical Value	Unit
UVP_{DVDD}	DVDD under-voltage error threshold	DVDD Rising	4.2	V
		DVDD Falling	4.0	V
UVP_{AVDD}	AVDD under-voltage error threshold	AVDD Rising	4.2	V
		AVDD Falling	4.0	V
UVP_{PVDD}	PVDD under-voltage error threshold	PVDD Rising	4.3	V
		PVDD Falling	4.1	V

DC protection

The MA12040P incorporates a circuit, detecting whether a DC is present on the amplifier output terminals driving the loudspeaker. In case of an unexpected DC being present on any of the amplifier outputs, the power stage will be shut down to protect the loudspeaker from harmful DC content. Furthermore, a failure is reported on the /ERROR pin and in the error register readable by the device serial interface. The power stage can be restarted by resetting the device by cycling the /ENABLE pin or toggle the clear bit (bit 2, address 45) to clear the error register. DC protection is default on. It can be disabled by clearing bit 2 of Eh_dcShdn (address 0x26).

For the DC protection circuit to trigger, the DC value of an output pin must be staying above 0.63*PVDD or below 0.37*PVDD for more than 700ms.

Digital serial audio input

The MA12040P provides a digital serial audio interface for providing up to four input PCM audio signals to the amplifier. The digital serial audio input port on the MA12040P consist of the pins SCK (serial clock), WS (word select), SD0 (serial data 0 – input channels 0L and 0R), and SD1 (serial data 1 – input channels 1L and 1R). All pins are inputs, i.e. the serial input port is slave. The format of the digital serial audio inputs can be configured using the serial control interface. The timing diagram for left justified mode (default) are illustrated in Figure 8-2 and I2S mode in Figure 8-3. In the following the various settings for the digital serial audio input interface are described.

Table 8-8 Parameters for the digital serial audio input interface

Address(bits)	Register name	Description
0x35(2-0)	i2s_format	PCM word format: 000: i2s 001: left justified (default) 100: right justified 16bits 101: right justified 18bits 110: right justified 20bits 111: right justified 24bits
0x36(0)	i2s_sck_pol	Clocking edge of the serial clock signal (SCK): 0: Serial data (SDX) and word select (WS) are changing at rising edge of the serial clock signal (SCK). The MA12040P will capture data at the falling edge of the serial clock signal SCK. 1: Serial data (SDX) and word select (WS) are changing at falling edge of the serial clock signal (SCK). The MA12040P will capture data at the rising edge of the serial clock signal SCK. (default)
0x36(4-3)	i2s_framesize	Number of data bits per frame: 00: 64 serial clock (SCK) cycles are present in each period of the word select signal (WS). (default) 01: 48 serial clock (SCK) cycles are present in each period of the word select signal (WS). 10: 32 serial clock (SCK) cycles are present in each period of the word select signal (WS). 11: reserved
0x36 (1)	i2s_ws_pol	Temporal pairing of the two PCM data words in the serial data signals: 0: First word of a simultaneously sampled PCM data pair is transmitted while word select (WS) is low. (default) 1: First word of a simultaneously sampled PCM data pair is transmitted while word select (WS) is high.
0x36(2)	i2s_order	Bit order for PCM data words:

		0: Most significant bit of the PCM data word is transmitted first. (default) 1: Least significant bit of the PCM data word is transmitted first.
0x36(5)	i2s_rightfirst	Left/right order of the two temporally paired PCM words: 0: Left PCM data word (of a simultaneously sampled PCM data pair) is send first. (default) 1: Right PCM data word (of a simultaneously sampled PCM data pair) is send first.

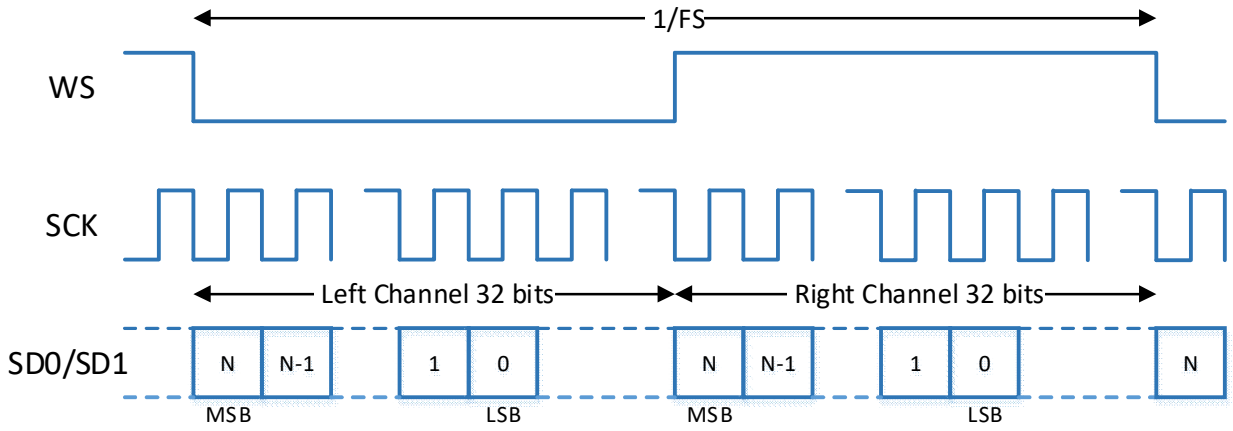


Figure 8-2 Timing diagram of left justified mode (default).

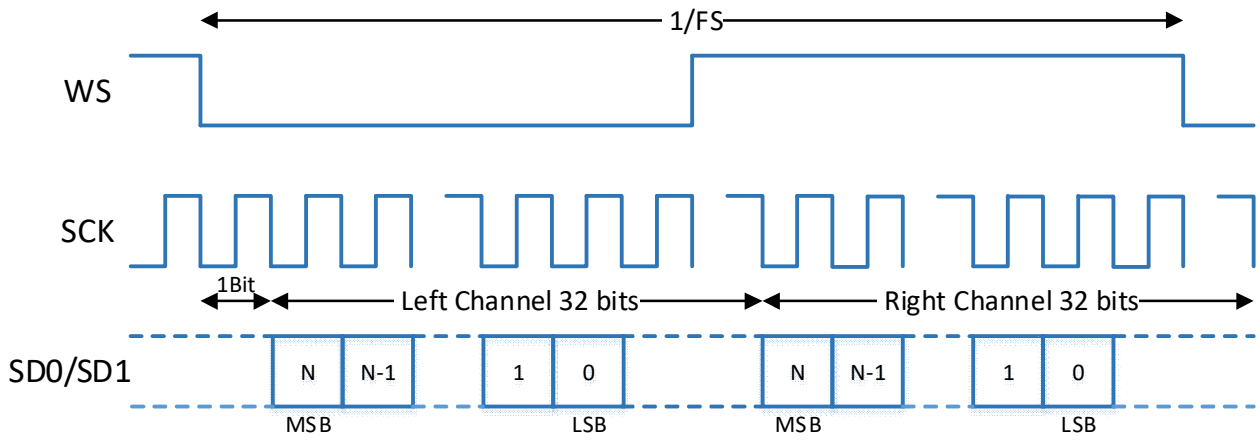


Figure 8-3 Timing diagram of I2S mode with 2x32 bit.

Volume and limiter processor (VLP)

The MA12040P incorporates a volume and limiter processor (VLP). The VLP is a dedicated digital signal processor capable of processing up to four audio channels. Customized signal processing is used to ensure preservation of the audio quality in all stages of the VLP.

Figure 8-4 shows a functional block diagram of the VLP. The VLP is capable of applying a high precision volume control on the incoming audio signals. After volume scaling, the signals can be passed through high precision limiters to protect the loudspeakers from overload or to avoid undesired clipping occurring due to bad signal or gain scaling (volume overdrive). The VLP can also be programmed to reduce the signal level in case of a temperature warning event to prevent a system shutdown caused by overheating.

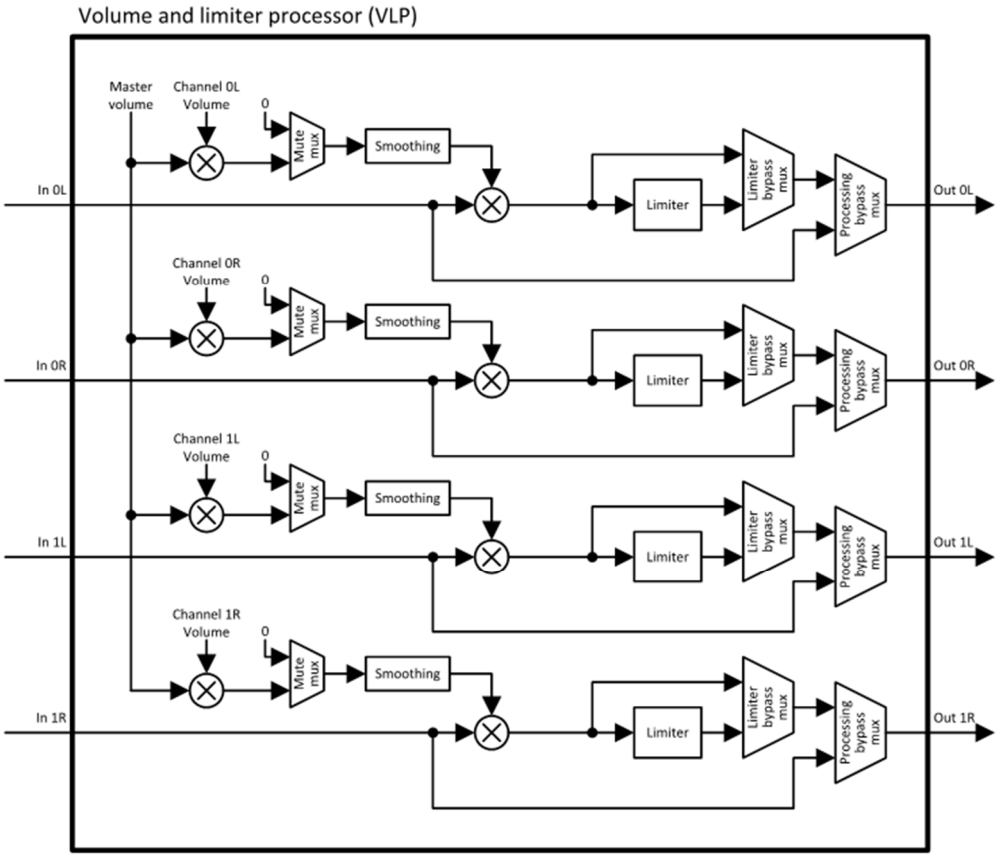


Figure 8-4. Functional block diagram of the volume and limiter processor (VLP)

Volume control

The volume controls in the VLP are organized as a master volume, which applies gain on all channels and four channel volumes, applying gain on each of the individual channels. The resulting gain for a channel will consequently be a product of the master volume and the channel gain. To avoid undesired audible artifacts when changing the volume settings, smoothing is performed on the resulting gain before applying it to the audio signal.

The master volume and the channel volume settings can be controlled via the serial control interface. Each volume setting is represented by 10 bits. The 10 bits are organized as an 8-bit number giving the integer part of the gain in dB (the digits before the decimal point) - and a 2-bit number giving the fractional part of the gain in dB (the digits after the decimal point). The granularity of volume settings is 0.25dB. The mapping from the serial control interface register to the gain is shown in Table 8-9.

Table 8-9 VLP Mapping from register values to gain and level

Integer dB register setting		Fractional dB register setting		VLP Gain/Level dB
dec	Hex	dec	hex	
0	(0x00)	0	(0x0)	24.00
0	(0x00)	1	(0x1)	23.75
…	…	…	…	…
22	(0x16)	3	(0x3)	1.25
23	(0x17)	0	(0x0)	1.00
23	(0x17)	1	(0x1)	0.75
23	(0x17)	2	(0x2)	0.50
23	(0x17)	3	(0x3)	0.25
24	(0x18)	0	(0x0)	0.00
24	(0x18)	1	(0x1)	-0.25
24	(0x18)	2	(0x2)	-0.50
24	(0x18)	3	(0x3)	-0.75
25	(0x19)	0	(0x0)	-1.00
…	…	…	…	…
167	(0xA7)	3	(0x3)	-143.75
168	(0xA8)	0	(0x0)	-144.00
…	…	…	…	…
255	(0xFF)	2	(0x2)	-144.00
255	(0xFF)	3	(0x3)	-144.00

Limiter

The limiter block in the VLP is capable of ensuring that the audio output level from the MA12040P is kept below a programmable threshold level, regardless of the volume gain settings and signal level. This way, the limiter can protect the loudspeakers against harmful signal levels and prevent severe degradation of audio quality, due to clipping caused by volume over-drive of the audio system.

The input to output level characteristic for the limiter is illustrated on Figure 8-5. At input audio levels below the threshold, the gain through the limiter is unity and consequently the limiter passes the signal unaffected. This is seen as a 1:1 slope on the input to output level characteristic plot. If the input signal level increases above the threshold level, the limiter reduces the gain correspondingly in order to reduce the output signal level to the threshold level. This way the output signal level will generally not exceed the threshold.

The slew-rate of the limiter is finite and the output signal can therefore occasionally exceed the set threshold. When the limiter reduces the gain (caused by the input signal level exceeding the threshold) the speed of gain reduction is limited by an attack-time constant. Similarly, when the limiter restores the gain to unity after being active the speed of gain increase is limited by a release-time constant. The attack-time constant and the release-time constant can be controlled in three steps (“slow”, ”normal” and “fast”) via the serial control interface. An example of the attack and release behavior for the limiter is shown in Figure 8-6.

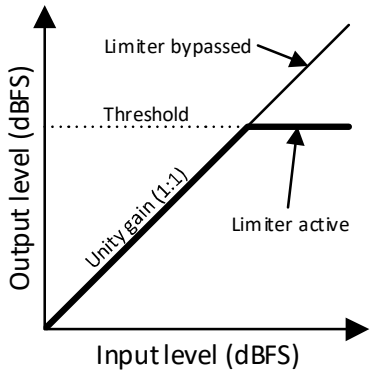


Figure 8-5 Input to Output level characteristic for the Limiter

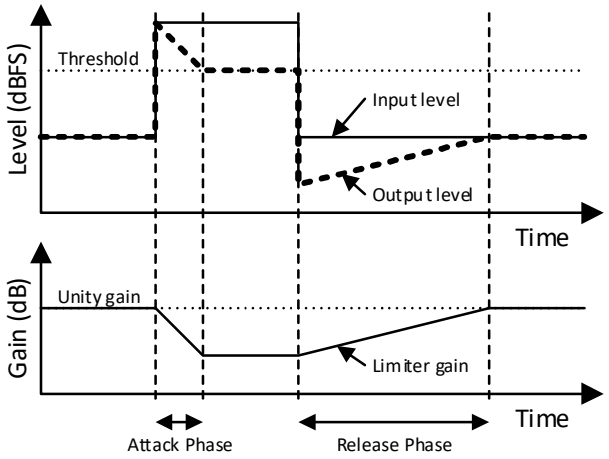


Figure 8-6 Example of limiter attack - and release behavior

VLP parameter interface

The parameters for the volume controls and limiters are accessible via the serial control interface. In Table 8-10 is shown a list of parameters in the VLP.

Table 8-10 Parameters and status signals for the VLP accessible via the serial control interface.

Address (bits)	Register name	Description
0x35 (5-4)	audio_proc_release	Controls the limiter release time. 00: slow, 01: normal, 10: fast
0x35 (7-6)	audio_proc_attack	Controls the limiter attack time. 00: slow, 01: normal, 10: fast
0x35 (3)	audio_proc_enable	Controls the processing bypass mux When high use the VLP When low: bypass the VLP
0x36 (6)	audio_proc_ limiterEnable	Controls the Limiter bypass mux When high: use the limiter When low: bypass the limiter
0x36 (7)	audio_proc_mute	Controls the mute mux

		When high: mute the audio When low: play as normal
0x40	vol_db_master	Controls the integer dB gain for the master volume[1]
0x41 (1-0)	vol_lsb_master	Controls the fractional dB gain for the master volume (quarter dB's) [1]
0x42	vol_db_ch0	Controls the integer dB gain for channel 0L[1]
0x43	vol_db_ch1	Controls the integer dB gain for channel 0R[1]
0x44	vol_db_ch2	Controls the integer dB gain for channel 1L[1]
0x45	vol_db_ch3	Controls the integer dB gain for channel 1R[1]
0x46 (1-0)	vol_lsb_ch0	Controls the fractional dB gain for channel 0R (quarter dBs) [1]
0x46 (3-2)	vol_lsb_ch1	Controls the fractional dB gain for channel 0L (quarter dBs) [1]
0x46 (5-4)	vol_lsb_ch2	Controls the fractional dB gain for channel 1R (quarter dBs) [1]
0x46 (7-6)	vol_lsb_ch3	Controls the fractional dB gain for channel 1L (quarter dBs) [1]
0x47	thr_db_ch0	Controls the integer dBFS limiter threshold level for channel 0L[1]
0x48	thr_db_ch1	Controls the integer dBFS limiter threshold level for channel 0R[1]
0x49	thr_db_ch2	Controls the integer dBFS limiter threshold level for channel 1L[1]
0x4A	thr_db_ch3	Controls the integer dBFS limiter threshold level for channel 1R[1]
0x4B (1-0)	thr_lsb_ch0	Controls the fractional dBFS limiter threshold level for channel 0L(quarter dBFS)[1]
0x4B (3-2)	thr_lsb_ch1	Controls the fractional dBFS limiter threshold level for channel 0R(quarter dBFS)[1]
0x4B (5-4)	thr_lsb_ch2	Controls the fractional dBFS limiter threshold level for channel 1L(quarter dBFS)[1]
0x4B (7-6)	thr_lsb_ch3	Controls the fractional dBFS limiter threshold level for channel 1R(quarter dBFS)[1]
0x7E (7-4)	audio_proc_limiter_mon	Indicates if limiters are active Bit 4 high: limiter is active on channel 0L Bit 5 high: limiter is active on channel 0R Bit 6 high: limiter is active on channel 1L Bit 7 high: limiter is active on channel 1R
0x7E (3-0)	audio_proc_clip_mon	Indicates if clipping occurs on the VLP output signals Bit 0 high: clipping present on channel 0L Bit 1 high: clipping present on channel 0R Bit 2 high: clipping present on channel 1L Bit 3 high: clipping present on channel 1R

[1] See Table 8-9 for mapping.

Clock system

The MA12040P incorporates a clock system consisting of an input clock divider, a PLL, a low-jitter low-TC oscillator (2.8224 MHz), and control logic. At the CLK input pin the MA12040P requires a clock signal that is in phase-lock with the incoming digital serial audio samples. This CLK input signal provides the reference for the internal PLL through the input clock divider circuit. The CLK frequency is auto-detected by the MA12040P, and when a valid frequency is detected, the corresponding input divider ratio is selected to internally generate the correct reference clock to the PLL. The PLL divider ratio is also selected as a function of the CLK base frequency (2.8224 or 3.072 MHz).

The clock for the internal DAC's can be sourced from the PLL (use_int_dac_clk_reg = 1), or at some CLK rates, a divided version of the CLK input (use_int_dac_clk_reg = 0). Valid combinations of audio sample rate (fs) and CLK frequency are listed in

Table 8-11 together with the possible use_int_dac_clk_reg setting, and the maximum number of supported VLP channels.

Table 8-11 Valid combinations of audio sample rate and CLK frequency

Maximum number of supported VLP channels are shown

Audio sample rate (fs)	CLK frequency	use_int_dac_clk_reg	No. VLP channels
44.1kHz	64 x fs = **2822.4kHz**	1	4
	128 x fs = **5644.8kHz**	1	4
	256 x fs = **11289.6kHz**	0/1	4
	512 x fs = **22579.2kHz**	0/1	4
48kHz	64 x fs = **3072kHz**	1	4
	128 x fs = **6144kHz**	1	4
	256 x fs = **12288kHz**	0/1	4
	512 x fs = **24576kHz**	0/1	4
88.2kHz	32 x fs = **2822.4kHz**	1	2
	64 x fs = **5644.8kHz**	1	2
	128 x fs = **11289.6kHz**	0/1	2
	256 x fs = **22579.2kHz**	0/1	2
96kHz	32 x fs = **3072kHz**	1	2
	64 x fs = **6144kHz**	1	2
	128 x fs = **12288kHz**	0/1	2
	256 x fs = **24576kHz**	0/1	2
176.4kHz	16 x fs = **2822.4kHz**	1	None
	32 x fs = **5644.8kHz**	1	None
	64 x fs = **11289.6kHz**	0/1	None
	128 x fs = **22579.2kHz**	0/1	None
192kHz	16 x fs = **3072kHz**	1	None
	32 x fs = **6144kHz**	1	None
	64 x fs = **12288kHz**	0/1	None
	128 x fs = **24576kHz**	0/1	None

MCU/Serial control interface

The I2C serial control interface of the MA12040P allows an I2C master to read and/or modify a wide range of device parameters.

The I2C interface consists of four physical pins, SDA, SCL, AD0 and AD1. I2C decoder logic handles transaction protocol and read/write access to the device register bank. SDA and SCL are standard bidirectional I2C slave pins for data and clock, respectively. Both SDA and SCL must be pulled-up to a digital I/O (3.3V - 5V) with a 5k resistor on each pin and

operated in standard I2C mode up to 100 kbps transmission rate. Pins AD0 and AD1 are used to configure the 7-bit I2C address of the device. The I2C address is decoded according to Table 8-12.

Table 8-12 I2C address decoding

I2C device address	AD1 pin	AD0 pin	7-bit I2C address
0x20	0	0	0b0100000
0x21	0	1	0b0100001
0x22	1	0	0b0100010
0x23	1	1	0b0100011

The I2C interface enables read/write operations to the device register bank. The register bank is organized as a 128 entry, byte wide memory, holding device configuration and status registers. The address space from 0 to 80 holds read/write registers and the address space from 96 to 127 are read only. The complete address map and description of each register is presented in “Register Map” section. Figure 8-7 shows the block schematic of the I2C interface between: I2C bus and MA12040P (serial interface controller and the register bank).

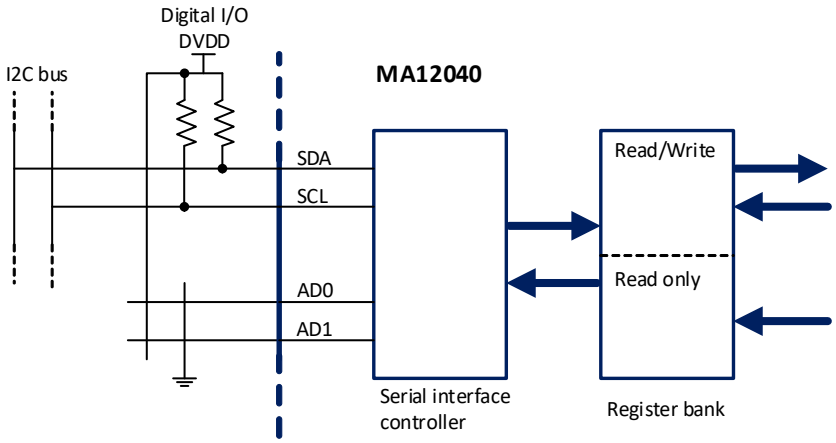


Figure 8-7. I2C bus interface and register bank

I2C write operation

Each I2C transaction is initiated from a master by sending an I2C start condition followed by the 7-bit I2C device address and cleared read/write bit. The device address and read/write bit is signaled on the SDA bus by pulling the bus to ground indicating a ‘0’ or releasing the bus to indicate a ‘1’. The I2C SDA input is sampled by the device on the rising edge of the SCL bus.

If the transmitted I2C address matches the configured address of the device, the device will acknowledge the request by pulling the SDA bus to ground. The master samples the acknowledged bit from the device on the next rising edge of SCL. The I2C initialization as described is shown in the waveform in Figure 8-8.

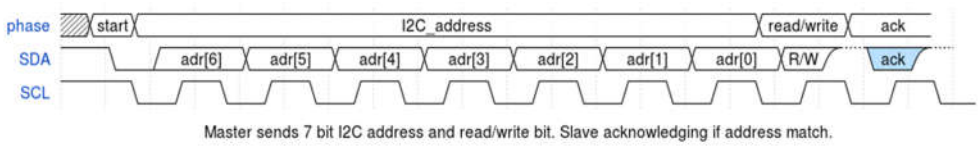


Figure 8-8. I2C init addressing sequence.

To complete the device register write operation, the master must continue transmitting the address and at least one data byte. The device continues to acknowledge each byte received on the 9th SCL rising edge. Each additional data written to the device is written to the next address in the register bank.

The write transaction is terminated when the master sends a stop signal to the device. The stop signal consists of a rising edge on SDA during SCL kept high. Figure 8-9 shows a single write operation.

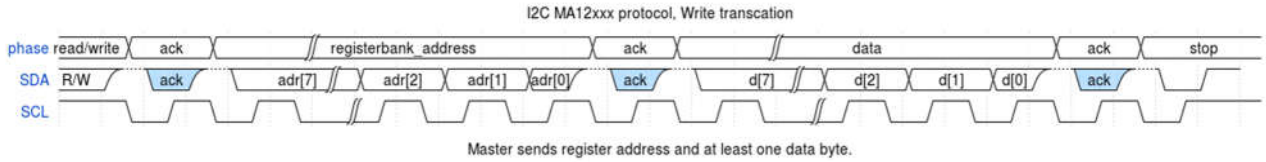


Figure 8-9 I2C write operation.

I2C read operation

To read data from the device register bank, the read transaction is started by sending a write command to the I2C address with the R/W bit cleared, followed by the device address to read from. See Figure 8-10.

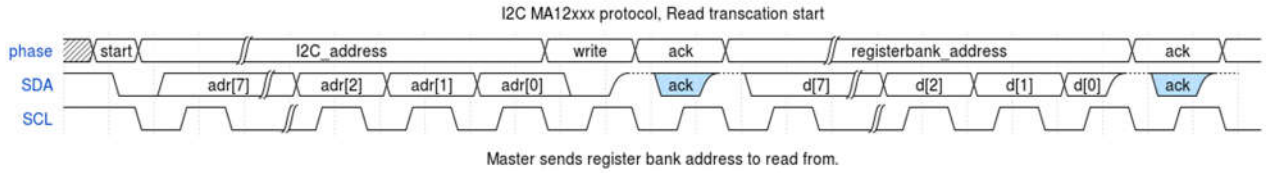


Figure 8-10 I2C read transaction, register bank to be read from is written to the device.

The device will acknowledge the two bytes. Then data can be fetched from the device by sending a repeated start, followed by an I2C read command consisting of a byte with the device I2C address and the R/W bit set.

The device will acknowledge the read request and start to drive the SDA bus with the bits from the requested register bank address. See Figure 8-11.

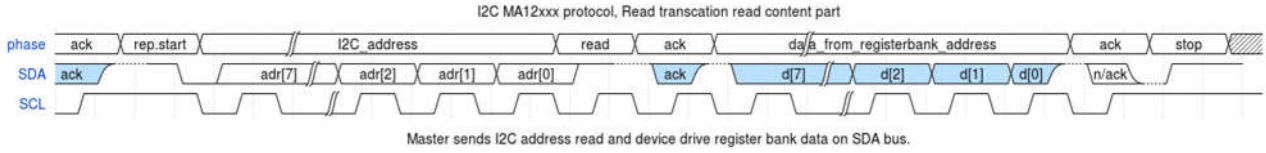


Figure 8-11 I2C read transaction last part.

The read transaction continues until the master does not acknowledge the 9th bit of the data read byte transaction and sends a stop signal. The stop condition is defined as a rising edge of SDA while SCL is high.

Table 8-13 I2C timing requirements

Parameter	Min	Typ	Max	Unit
Clock frequency	0	100	400	kHz

SDA and SCL rise time		1	µs
SDA and SCL fall time		1	µs
SCL clock high	1		µs
SCL clock low	1		µs
Data, setup	300		ns
Data, hold	10		ns
Min stop to start condition	1		µs

NOTE[1]: Pull up resistance is equal to 2.2kΩ for 400kHz.

/CLIP pin and soft-clipping

The /CLIP pin changes from a HIGH state to LOW state when audio output is close to clipping. A system microcontroller can at this instance decrease volume level or, if possible, increase power stage voltage in order to avoid clipping. The associated modulation index for both channel 0 and channel 1 can be read out by reading address 98 and address 102 respectively. Note that /CLIP pin is an open-drain output which means that it should be pulled-up through a pull-up resistor to the digital I/O DVDD of the system.

To minimize possible audible artifacts from sticky clipping or ringing around the clipping region, it is possible to enable a soft-clipping scheme. This clipping scheme prevents the amplifier to sticky clip and minimizes ringing which subsequently minimizes possible audible artifacts apart from normal clipping audibility. The soft-clipping scheme can be enabled by setting bit 7 of address 10.

/ERROR pin and error handling

The /ERROR pin changes from a HIGH state to a LOW state when one of the associated error sources is triggered. A system microcontroller can at this instance read out the error registers (address 45 and 109). According to the type of error or warning the right measures can be taken. The errors will be shown in the error register (address 124) which shows the live status of the error sources. Another register error_acc (address 109) will contain all the errors accumulated over time. The error_acc register can be cleared by toggling the eh_clear bit (bit 2, address 45).

Table 8-14 shows the content of the error vector which is mapped to both the error register and the accumulated error register. A more detailed explanation can be found in “Register Map” section.

Table 8-14 Error vector

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
dc_prot	pps	ote	otw	uvp	pll	ocp	fcov

Note that the /ERROR pin has an open-drain output and should be pulled up to the interface I/O rail.

9 Application Information

Input/Output Configurations

The MA12040P is highly flexible regarding configuration of the four power amplifier channels. MA12040P can be set to four different output configurations. By setting the configuration pins MSEL0 and MSEL1 according to Table 9-1, the device is configured to one of the four different configurations. Each configuration is individually described in the following sections.

Table 9-1 Signal configuration

MSEL0 pin	MSEL1 pin	Configuration
0	0	1 channel parallel bridge tied load (PBTL)
0	1	2 channels single ended load (SE) and 1 channel bridge tied load (BTL)
1	0	2 channels bridge tied load (BTL)
1	1	4 channels single ended load (SE)

Bridge Tied Load (BTL) Configuration

In BTL configuration, two input- and output terminals are used per channel as shown in Figure 9-1. This way two power stage half-bridges are used to form one differential output configuration. This configuration will enable the full potential of multi-level technology where the speaker load will experience up to 5 levels. This enables low near-idle power consumption and beneficial noise properties.

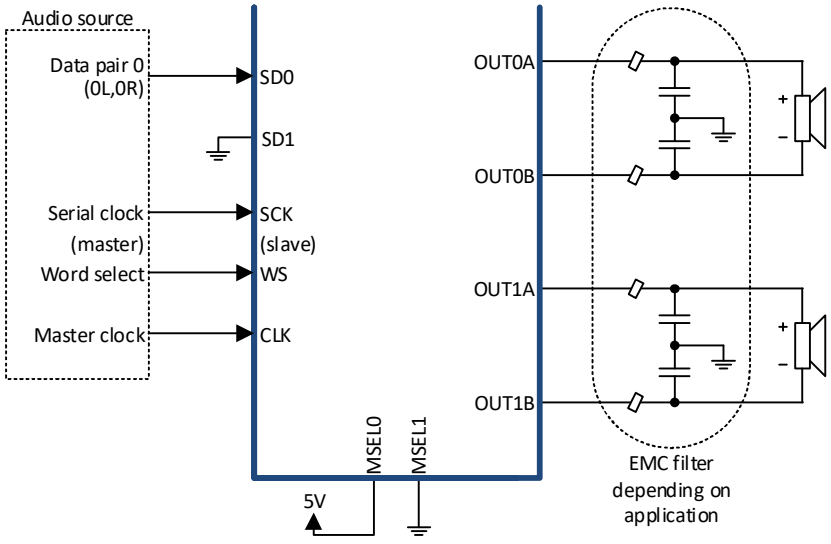


Figure 9-1 Bridge tied load (BTL) configuration, with symmetrical audio sources

Single Ended (SE) Configuration

In single ended (SE) configuration, the MA12040P is able to drive one loudspeaker per output power stage, i.e. up to four loudspeakers. The output is biased to half the power supply voltage, ½ PVDD. One of the solutions to drive a speaker in this configuration is to use AC-coupling capacitors (C_{out}) in series with the load, as shown in Figure 9-2. The value of the capacitors depends on the load resistance and the desired audio bandwidth.

Table 9-2 shows examples of AC-coupling capacitor values. The DC voltage across the capacitors at the output is approximately ½PVDD. However, significant AC-voltage swing might occur at low frequencies, which must be accounted for in the voltage rating of the capacitors.

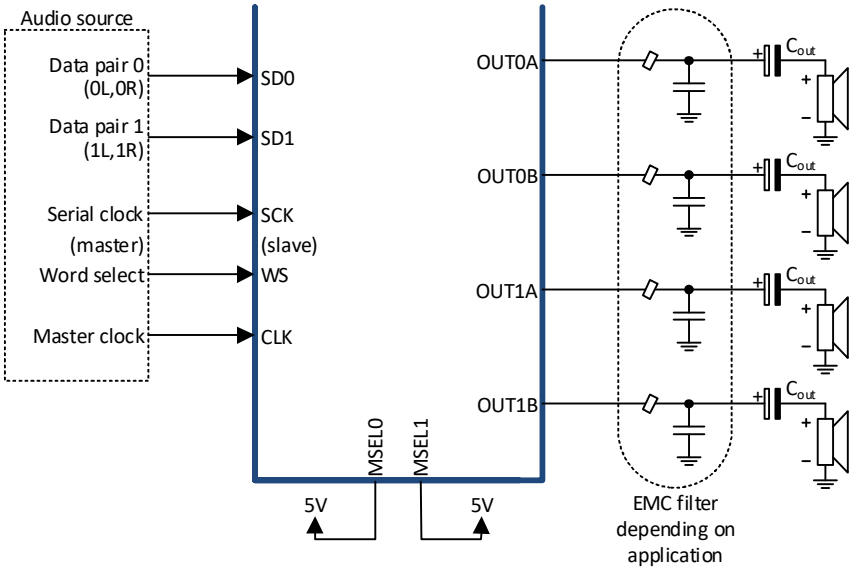


Figure 9-2 Four channel, single ended (SE) configuration

Table 9-2 Typical values for the output AC-coupling capacitor, C_{out}

Load Resistance	Output AC-coupling capacitor, C_{out}	-3dB frequency
8Ω	220µF	90Hz
8Ω	1000µF	20Hz
4Ω	2200µF	24Hz

Combined SE and BTL Configuration

A combination of SE and BTL configuration can be used as shown in Figure 9-3. In this configuration two half-bridges are combined to run in BTL configuration and the two remaining half-bridges are configured to run in SE configuration.

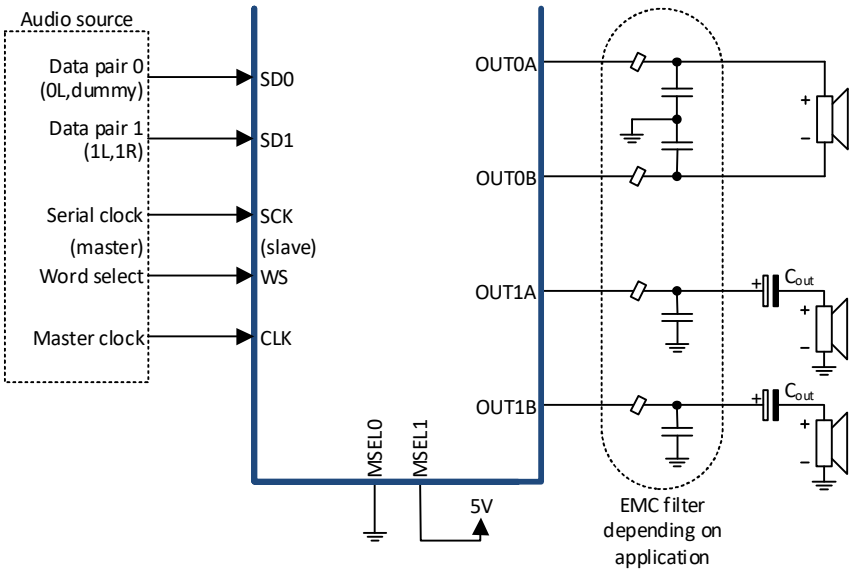


Figure 9-3 Combined Bridge tied load (BTL) and single ended (SE) configuration, with SE audio sources

Parallel Bridge Tied Load (PBTL)

For providing additional power the MA12040P can be configured for mono operation using a parallel BTL mode (PBTL), as shown in Figure 9-4. In this fashion the two BTL output stages are combined to be able to deliver twice the current. This makes high output power sub-woofer application possible.

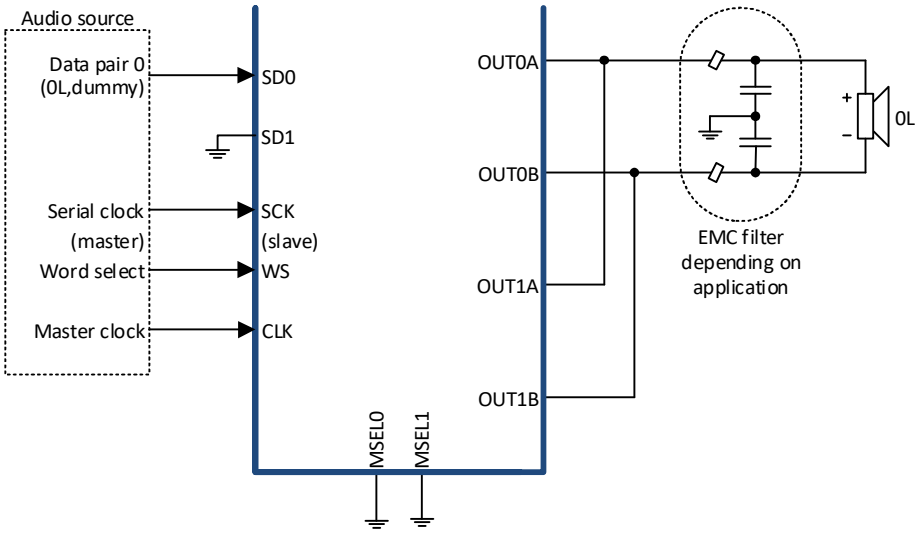


Figure 9-4 Parallel Bridge Tied Load (PBTL) configuration.

EMC output filter Considerations

The proprietary 5-level modulation significantly reduces EMC emissions, and the amplifiers can pass the Radiated Emission test with speaker cables lengths up to 80 cm with just a small ferrite filter. For cables longer than 80 cm it is recommended to use a LC-filter.

For more information regarding filter type, components and measurements, see the document “Applications note – EMC Output Filter Recommendations” at the Infineon homepage.

Audio Performance Measurements

In a typical audio application the outputs of the MA12040P will be connected directly to the speaker loads. However, for audio performance evaluation it can be beneficial to configure the circuit board with an LC filter. This is due to the fact that many audio analyzers do not handle PWM signals at their inputs well.

When using an audio analyzer configured with an external and/or internal measurement filter the use of an LC filter is not necessary. However, be sure to verify the audio analyzer's input limits before connecting it to a filterless amplifier output.

When using an LC filter, the design depends on the specific load. L and C values should therefore be optimized for this.

Thermal Characteristics and Test Signals

Performing audio measurements by use of an audio analyzer is typically very helpful during the evaluation of an amplifier. However, using an audio analyzer can be misleading when evaluating thermal performance.

Audio analyzers typically generate full tone, continuous sine wave signals as the input signal for the amplifier. While this is required to perform many audio measurements, it is also the worst-case thermal scenario for the device. Using full-scale continuous sine waves for thermal evaluation or testing will lead to an overly conservative and more costly thermal design which will be unnecessary in almost all real audio applications.

Actual audio content, such as music, has much lower RMS values compared to its maximum peak output power than a full-scale continuous sine wave. This results in significantly less heat dissipation from the device when amplifying actual audio. For thermal evaluation it is therefore recommended to use actual music signals during tests. Alternatively, a pink noise signal can be used to emulate a music signal.

It is not uncommon for an amplifier solution to have limited thermal performance, potentially resulting in thermal protection shutdown, when amplifying full-scale continuous sine wave signals.

Start-up procedure

It is recommended to follow the start-up procedure as described below:

1) Make sure the all hardware pins are configured correctly: e.g. BTL, Slave Clock mode.
2) Keep the device in disable and mute: /ENABLE = 1; /MUTE = 0.
3) Bring up 5V VDD supply and PVDD supply (it does not matter if VDD or PVDD comes up first, provided that the device is held in disable).
4) Wait for VDD and PVDD to be stable.
5) CLK must be present before enabling the amplifier.
6) Enable device: /ENABLE = 0.
7) Program applicable initialization to registers.
8) Unmute device: /MUTE = 1.
9) The device is now in normal operation state.

Shut-down / power-down procedure

It is recommended to follow the start-up procedure as described below:

1) The device is in normal operation state.
2) Mute device: /MUTE = 0.
3) Disable device: /ENABLE = 1.
4) The device is now power-down state.
5) Bring down 5V VDD supply and PVDD supply.
6) The device is now in shut-down state.

Recommended PCB Design for MA12040PQFN (EPAD-down package)

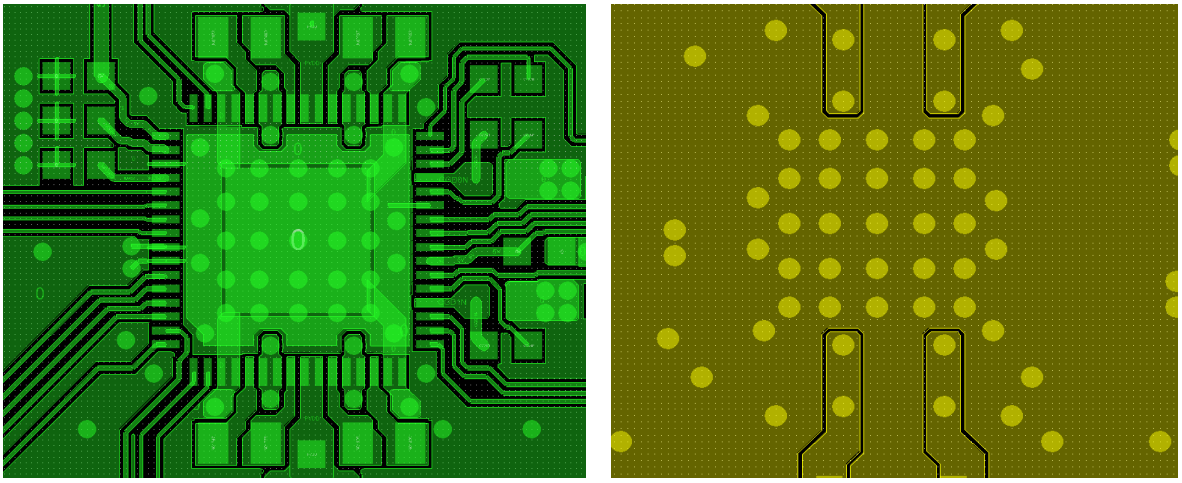
The QFN package with exposed thermal pad at the bottom side is thermally sufficient for most applications. However, in order to remove heat from the package care should be taken in designing the PCB.

The PCB footprint for the device should include a thermal relief pad underneath the device with a size of 6 x 6 mm. This thermal relief pad must be centered so the device can be soldered easily. It is recommended to use a PCB design with two or more layers of copper for good thermal performance. Using multiple layers enables a design with a large area of copper connected to the EPAD.

To achieve best thermal performance it is also important to design the surrounding connections in such a way that avoids cutting up the copper area into many sections.

Figure 9-5 shows a PCB design using 26 via connections directly underneath the chip between the top and bottom layers. These should be placed on a grid each with a 0.65 mm plated through hole. These connections ensure good thermal transfer from the top side EPAD to a large section of ground connected copper area on the bottom side of the PCB.

Figure 9-5 Example of 2-layer PCB layout, top and bottom layers



It is recommended to use a PCB made from glass/epoxy laminate (e.g. FR-4) material. This type of material works well with PCB designs that require thermal relief as it can endure high temperatures for a long duration of time.

PCB copper thickness is recommended to be a minimum of 35µ (1 oz) and the PCB must be made to the IPC 6012C, Class 2 standard.

10 Typical Characteristics (PVDD = +18V, Load = 4Ω + 22µH)

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

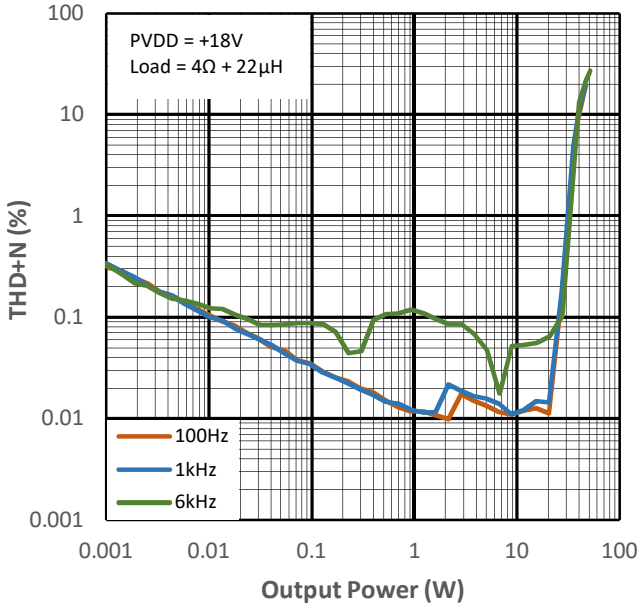


Figure 10-10-1 THD+N vs. Output Power for PMP0

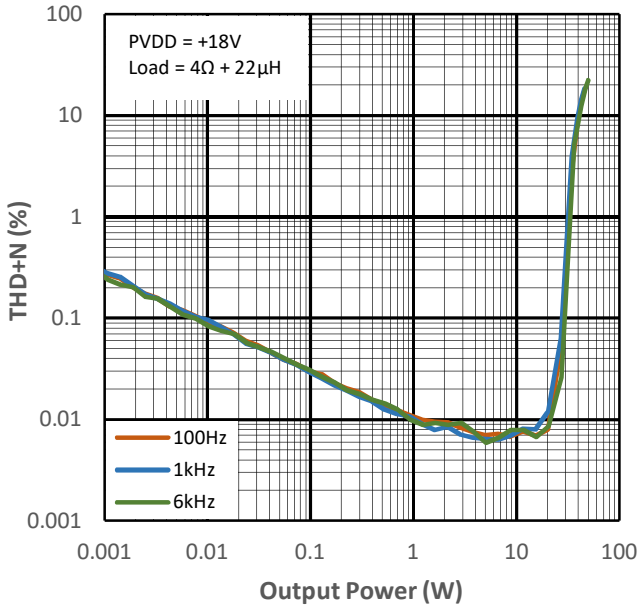


Figure 10-2 THD+N vs. Output Power for PMP1

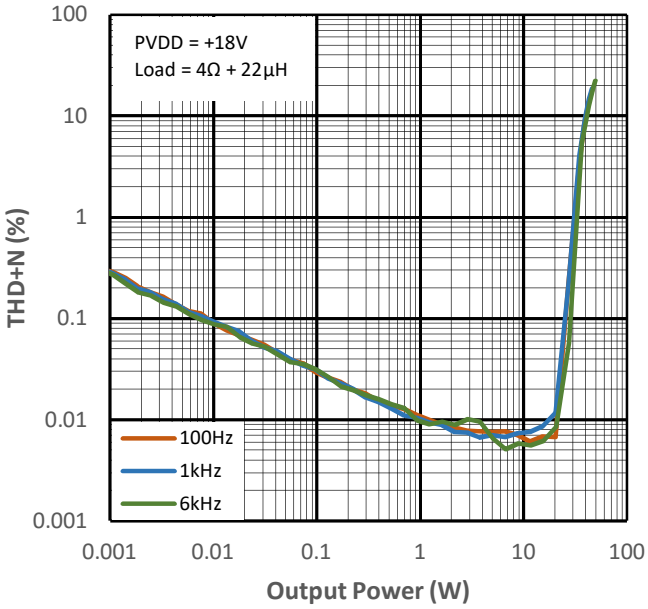


Figure 10-3 THD+N vs. Output Power for PMP2

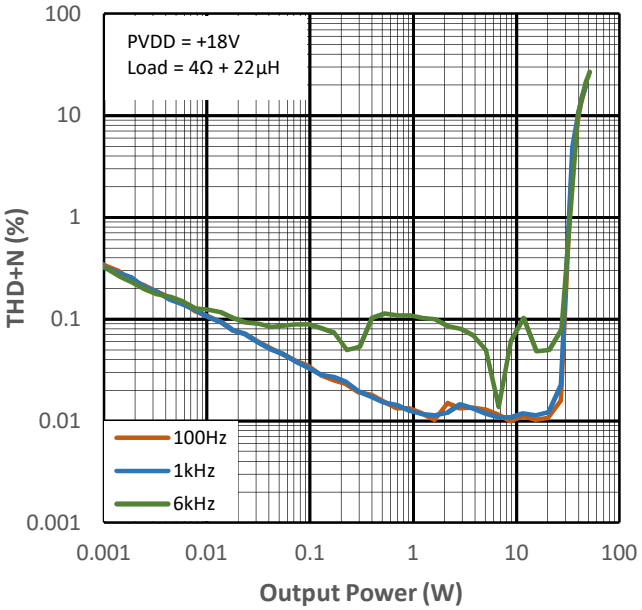


Figure 10-4 THD+N vs. Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

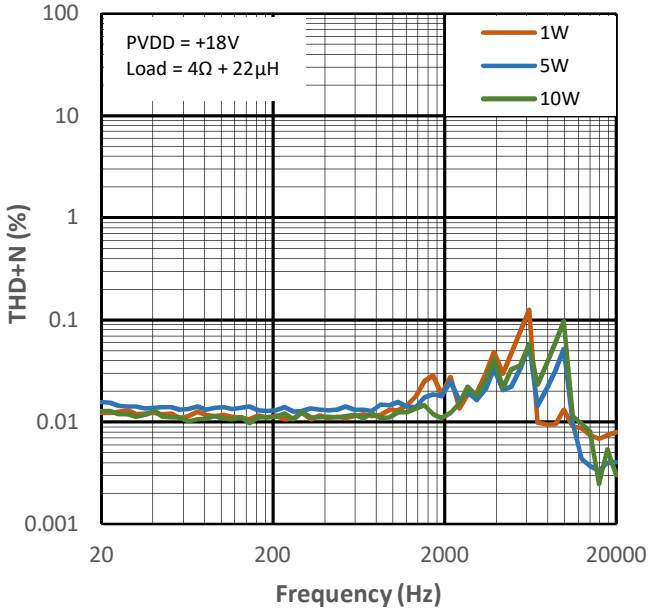


Figure 10-5 THD+N vs Frequency for PMP0

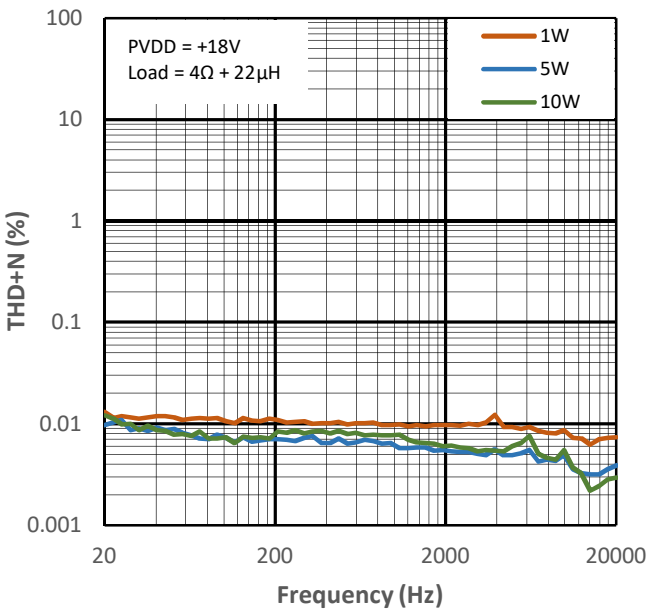


Figure 10-6 THD+N vs Frequency for PMP1

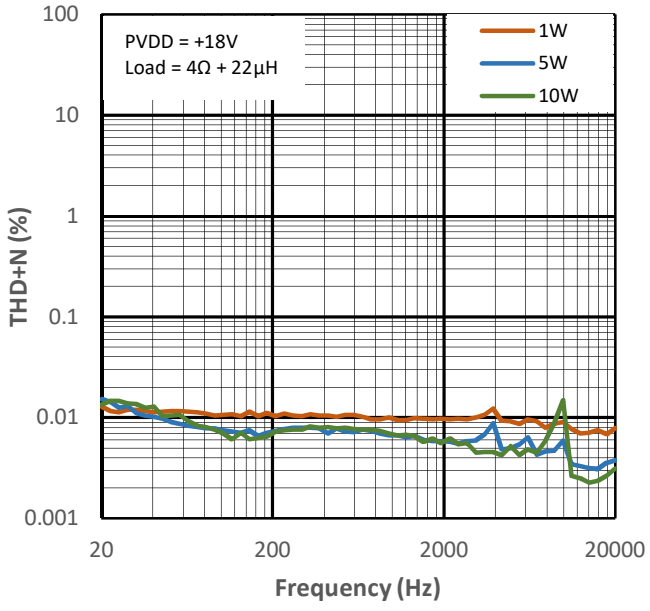


Figure 10-7 THD+N vs Frequency for PMP2

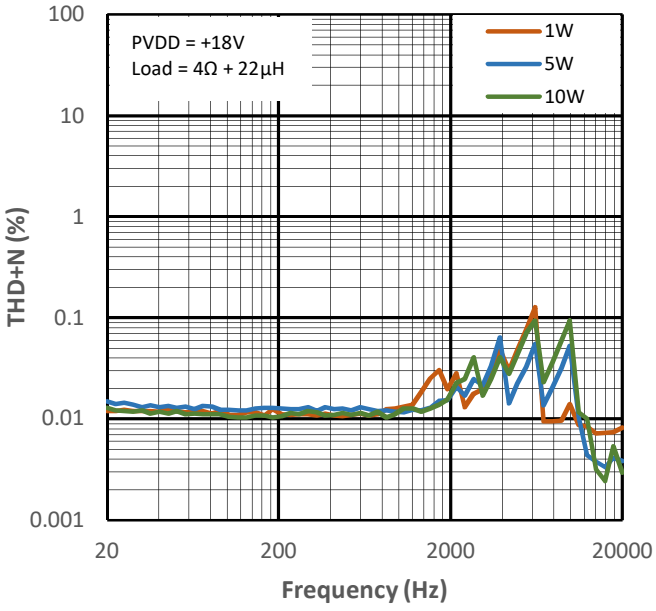


Figure 10-8 THD+N vs Frequency for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

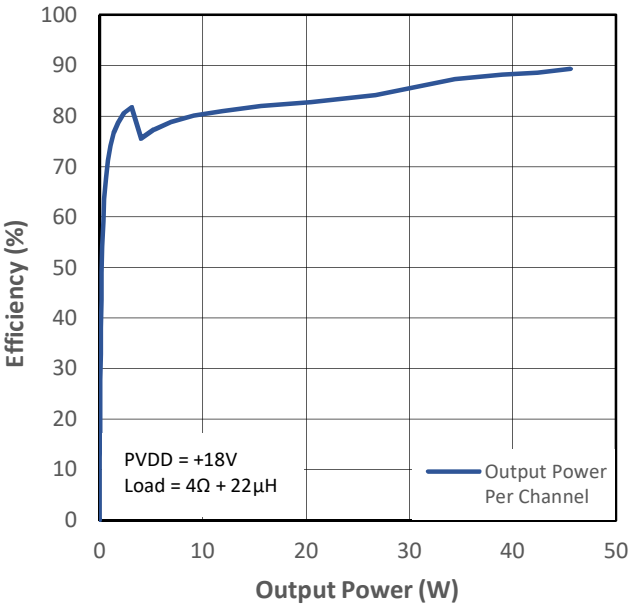


Figure 10-9 PMP0 Efficiency (VDD+PVDD) vs Output Power

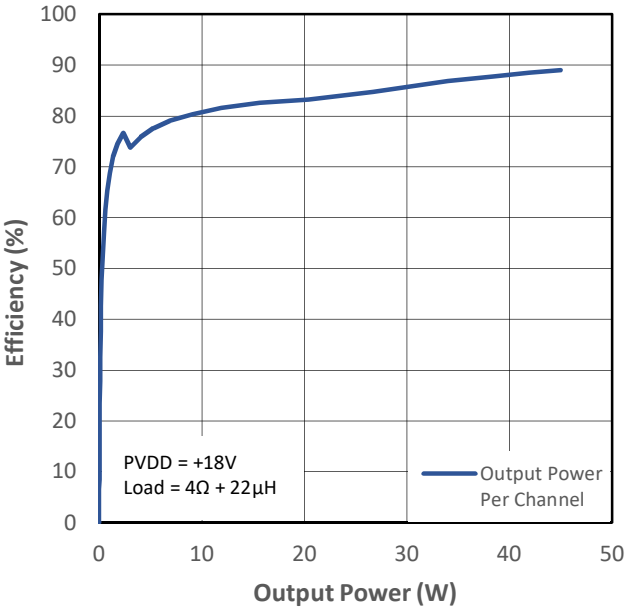


Figure 10-10 PMP1 Efficiency (VDD+PVDD) vs Output Power

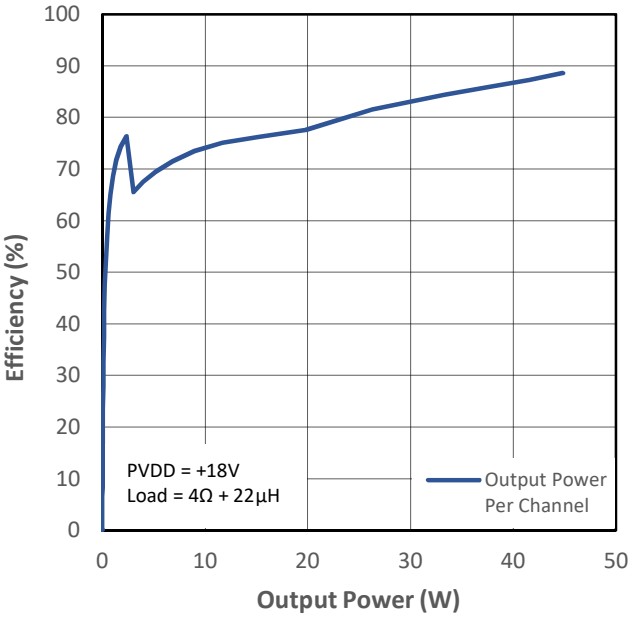


Figure 10-11 PMP2 Efficiency (VDD+PVDD) vs Output Power

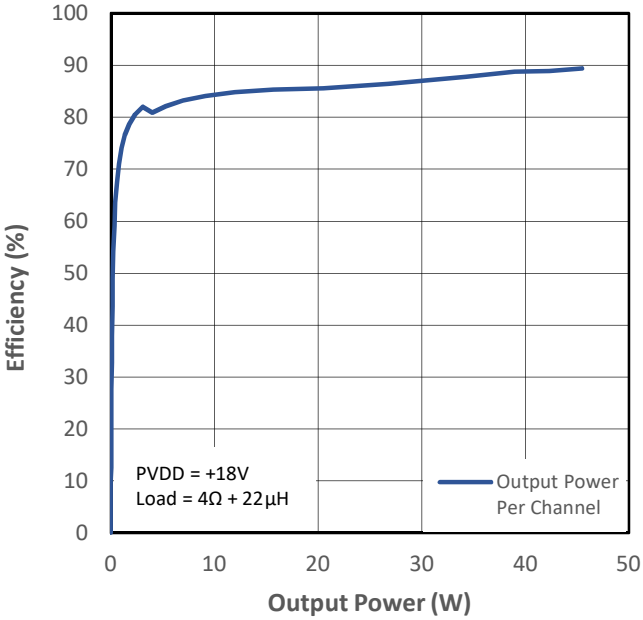


Figure 10-12 PMP4 Efficiency (VDD+PVDD) vs Output Power

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

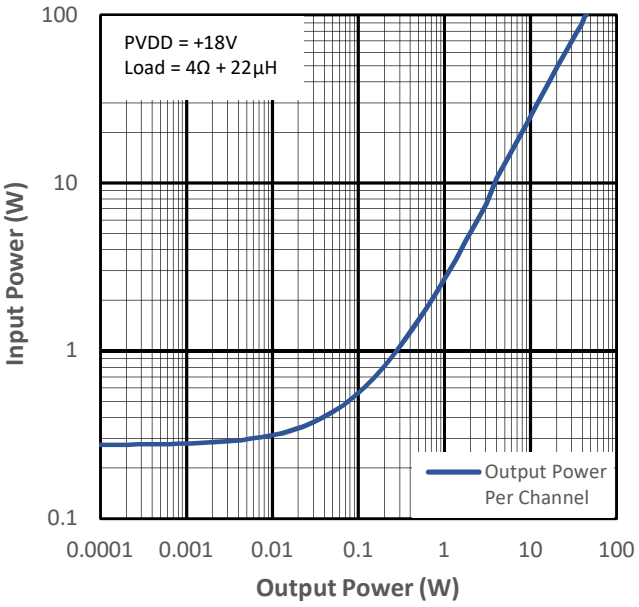


Figure 10-13 Input Power vs Output Power for PMP0

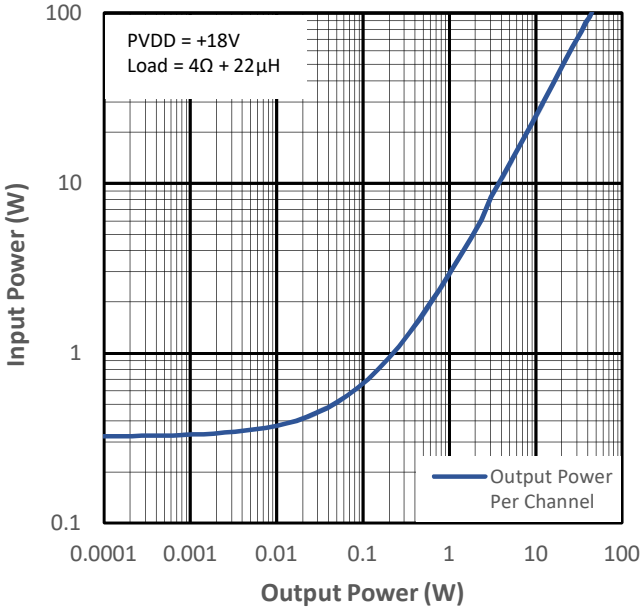


Figure 10-14 Input Power vs Output Power for PMP1

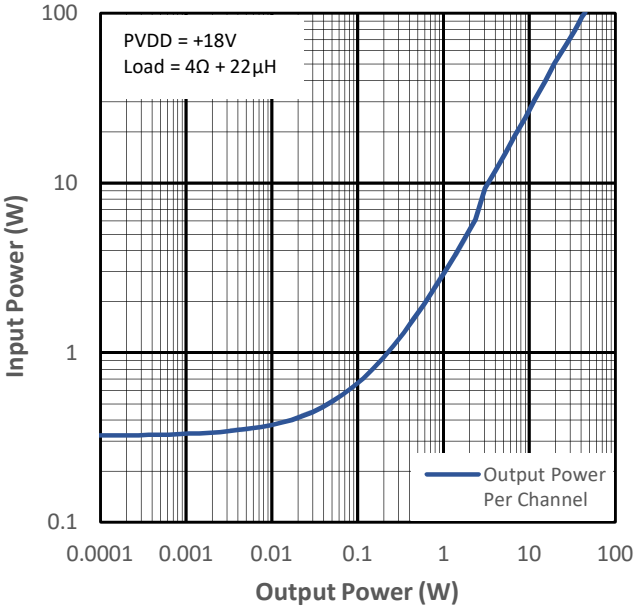


Figure 10-15 Input Power vs Output Power for PMP2

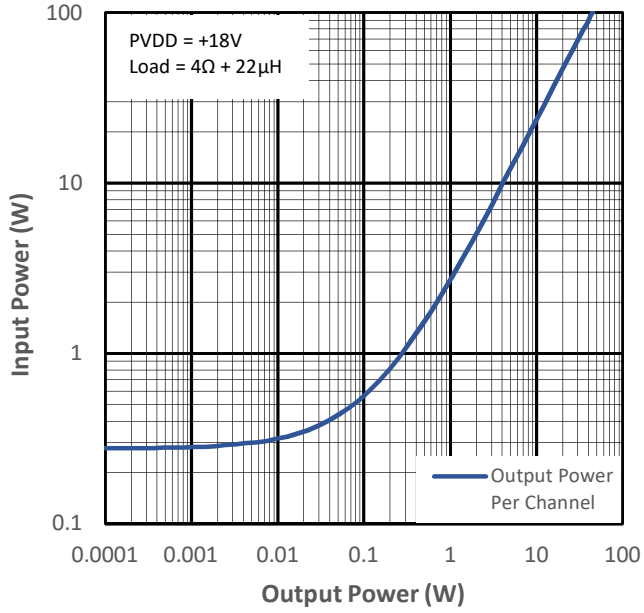


Figure 10-16 Input Power vs Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

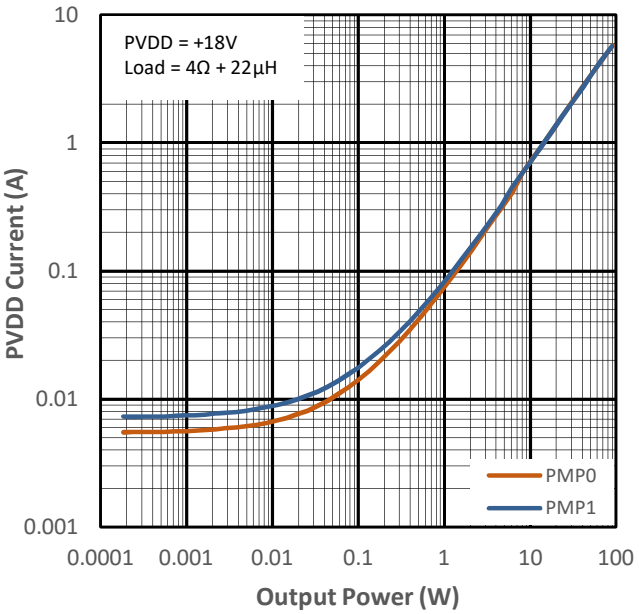


Figure 10-17 PVDD Current vs Output Power for PMP0 & PMP1

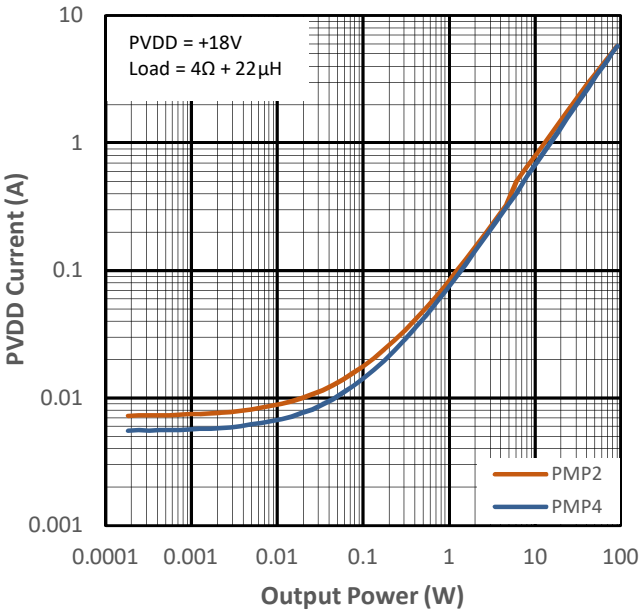


Figure 10-18 PVDD Current vs Output Power for PMP2 & PMP4

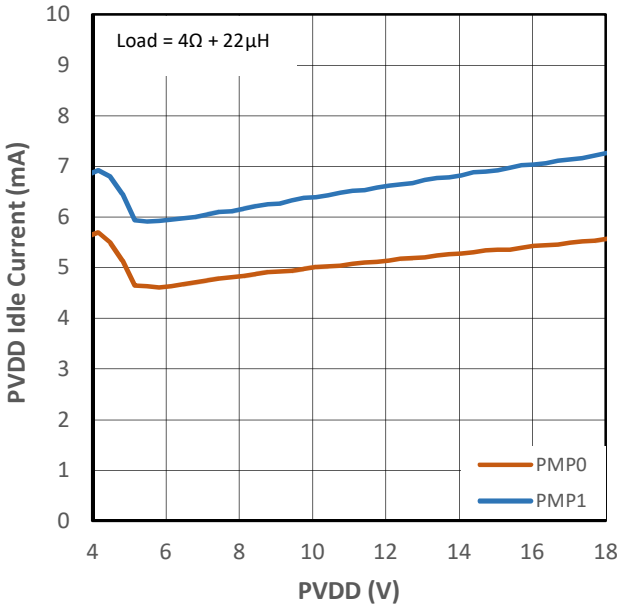


Figure 10-19 PVDD Current vs PVDD Voltage for PMP0 & PMP1

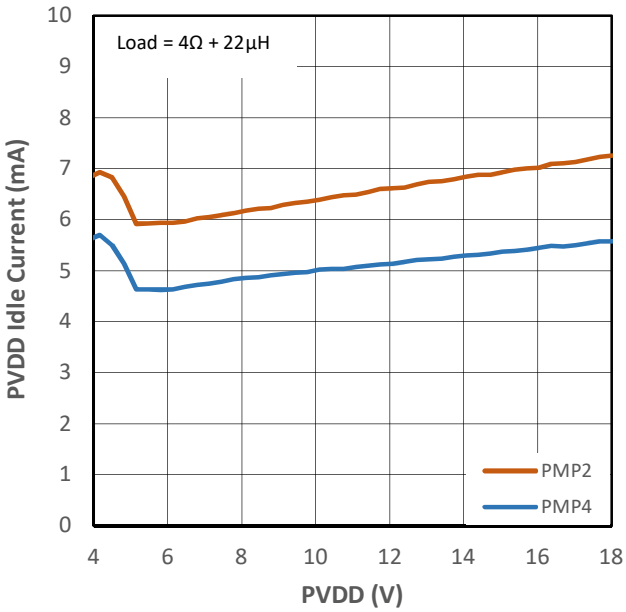


Figure 10-20 PVDD Current vs PVDD Voltage for PMP2 & PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

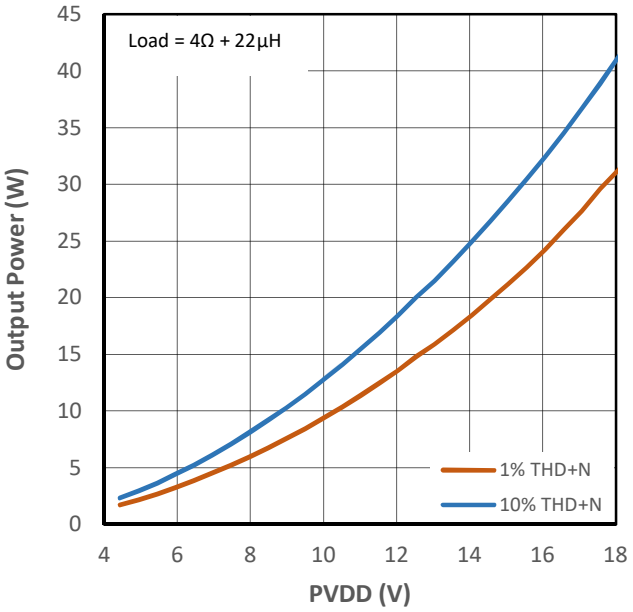


Figure 10-21 Output Power vs PVDD Voltage for PMP0

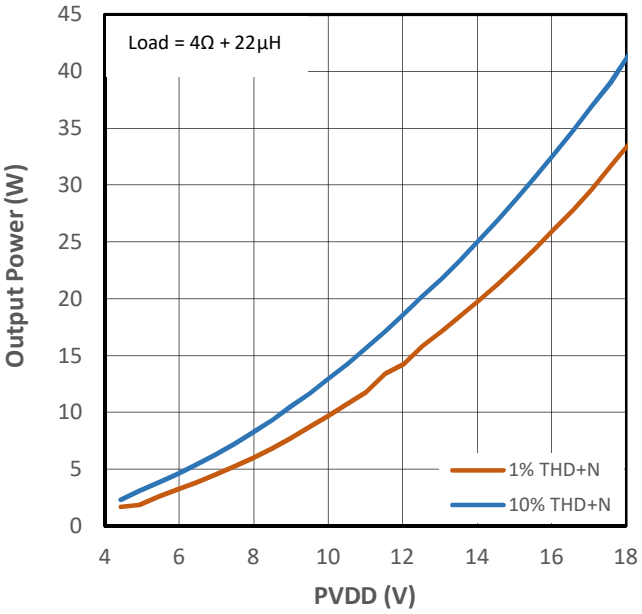


Figure 10-22 Output Power vs PVDD Voltage for PMP1

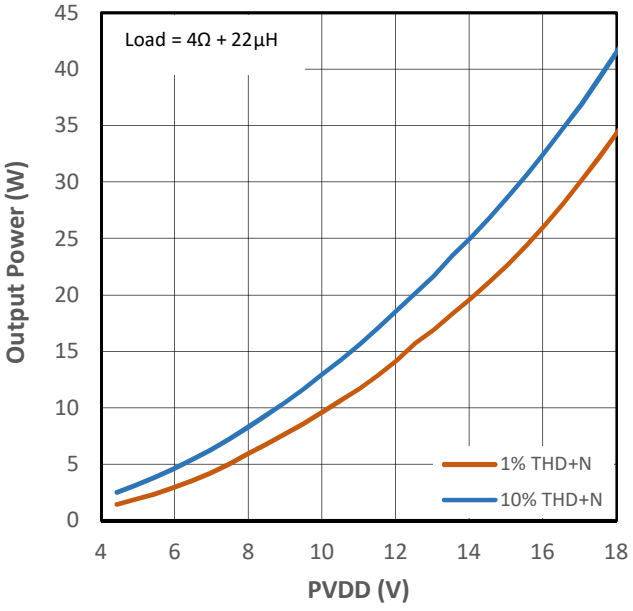


Figure 10-23 Output Power vs PVDD Voltage for PMP2

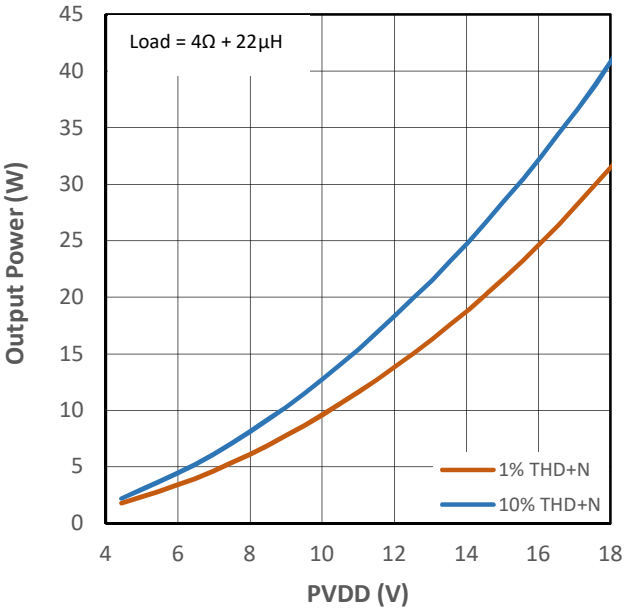


Figure 10-24 Output Power vs PVDD Voltage for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

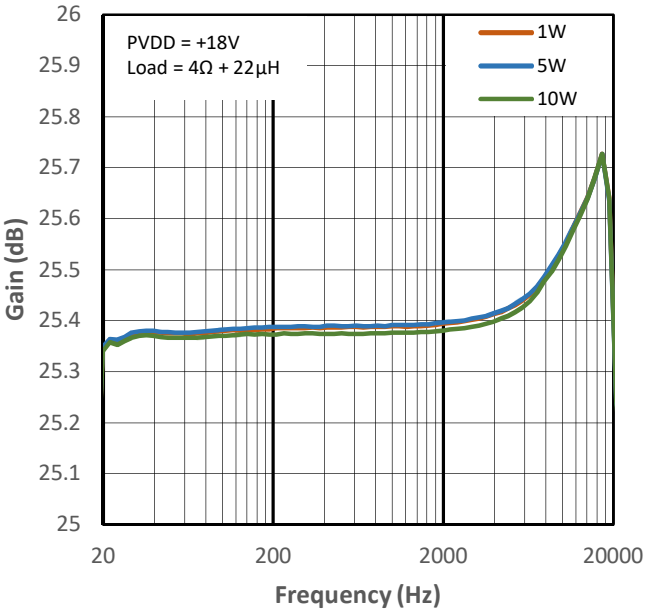


Figure 10-25 Gain vs Frequency for PMP0

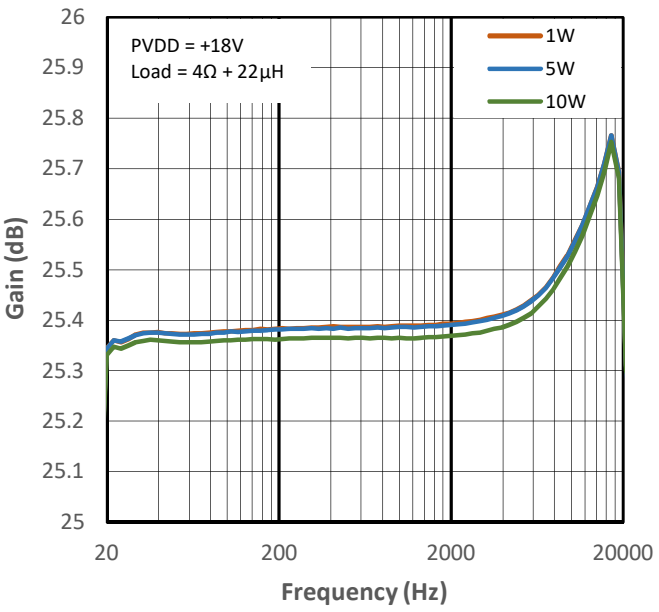


Figure 10-26 Gain vs Frequency for PMP1

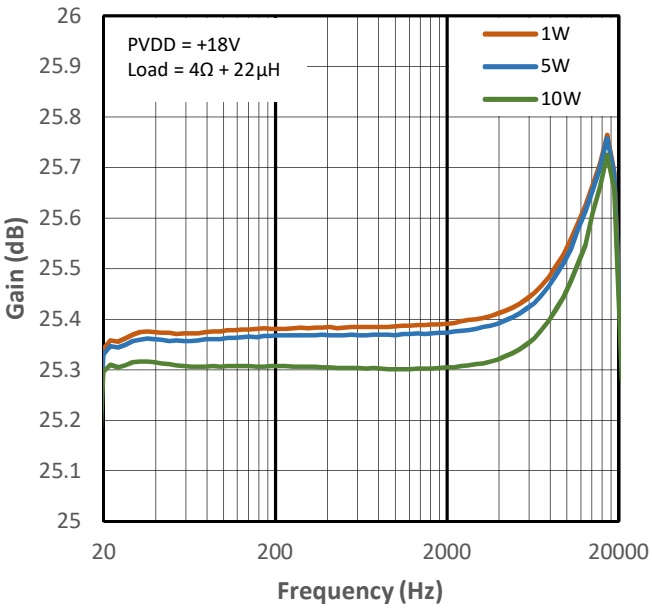


Figure 10-27 Gain vs Frequency for PMP2

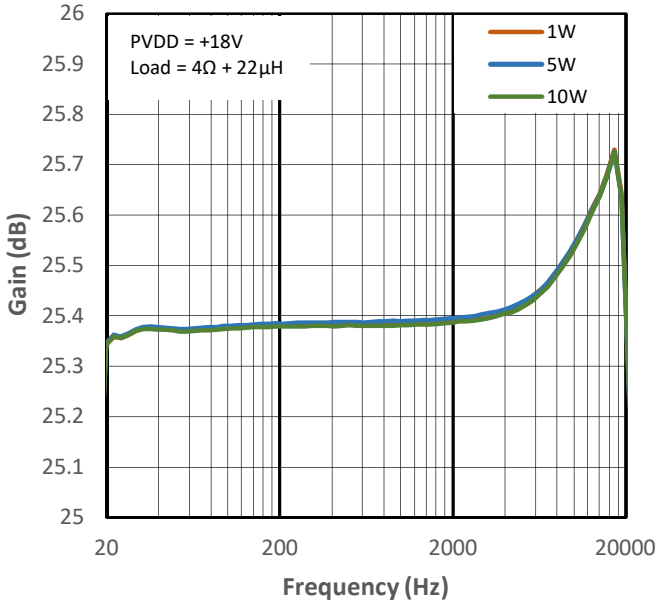


Figure 10-28 Gain vs Frequency for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

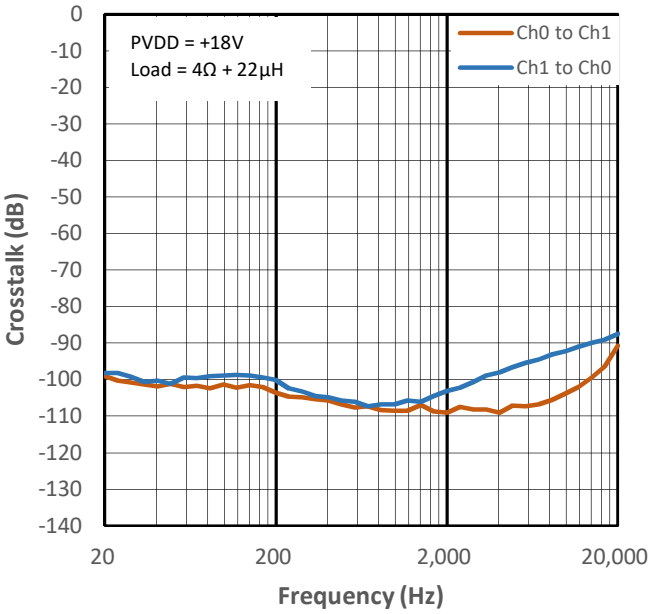


Figure 10-29 Crosstalk vs Frequency for PMP0

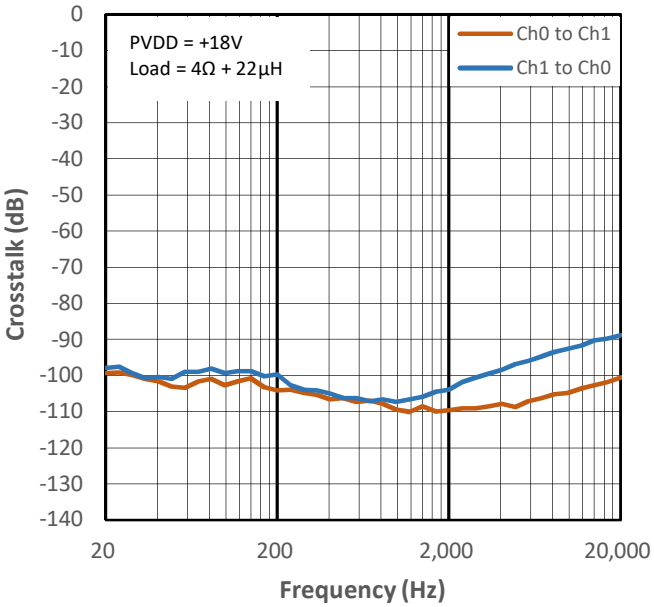


Figure 10-30 Crosstalk vs Frequency for PMP1

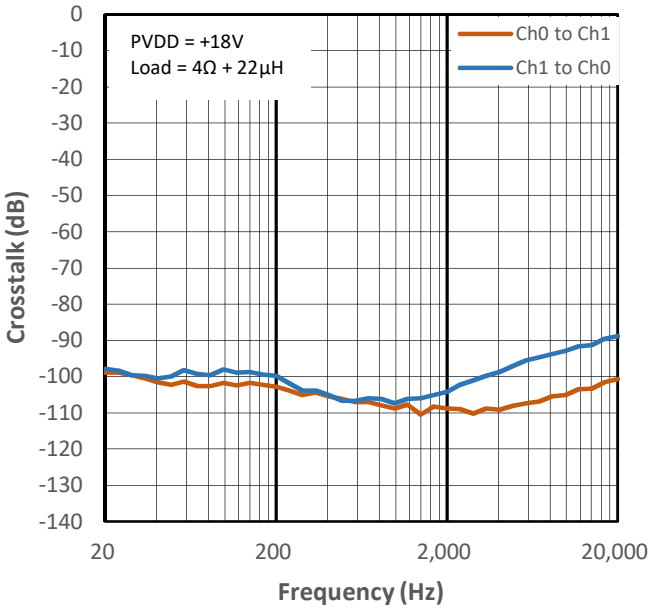


Figure 10-31 Crosstalk vs Frequency for PMP2

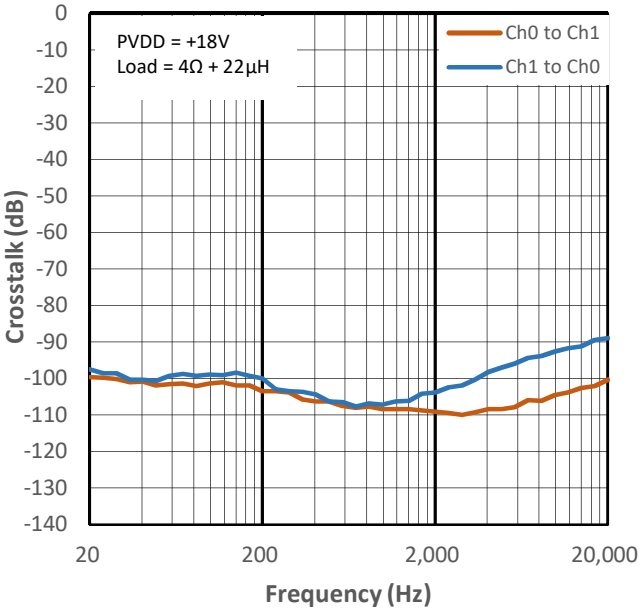


Figure 10-32 Crosstalk vs Frequency for PMP4

11 Typical Characteristics (PVDD = +18V, Load = 8Ω + 22µH)

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

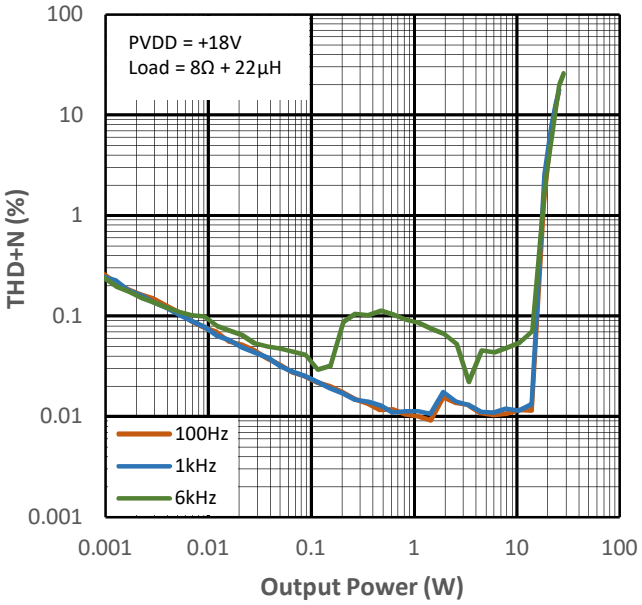


Figure 11-11-1 THD+N vs. Output Power for PMP0

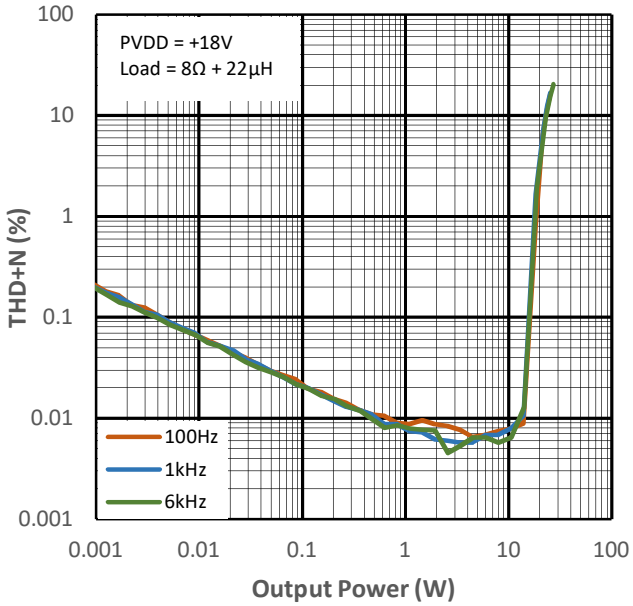


Figure 11-2 THD+N vs. Output Power for PMP1

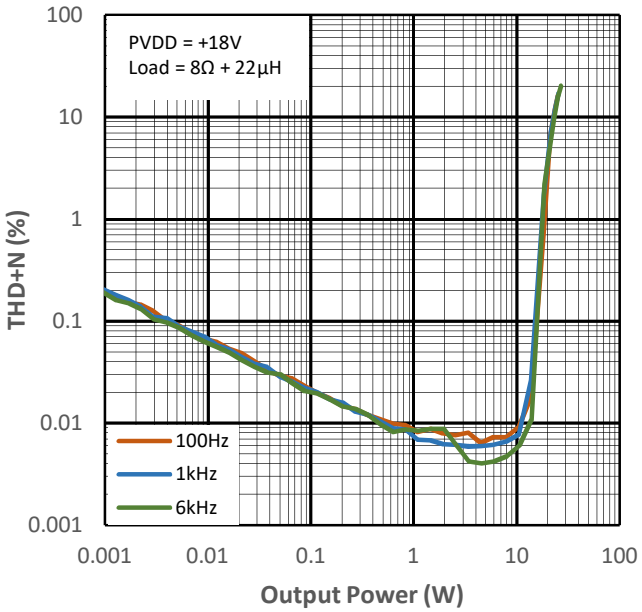


Figure 11-3 THD+N vs. Output Power for PMP2

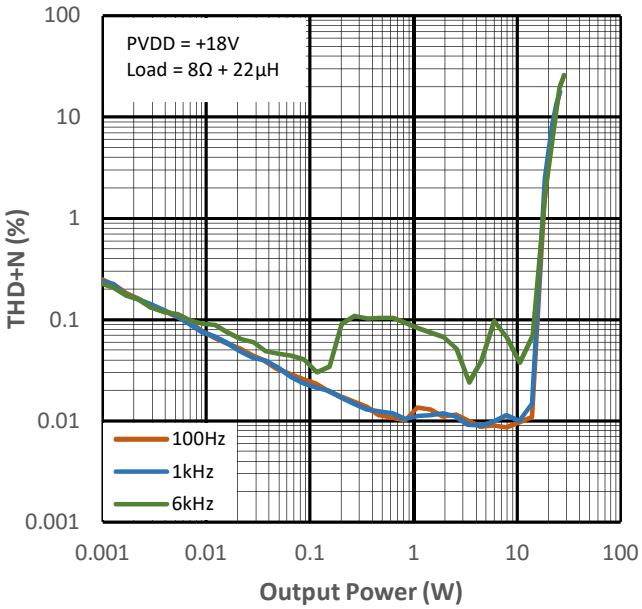


Figure 11-4 THD+N vs. Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

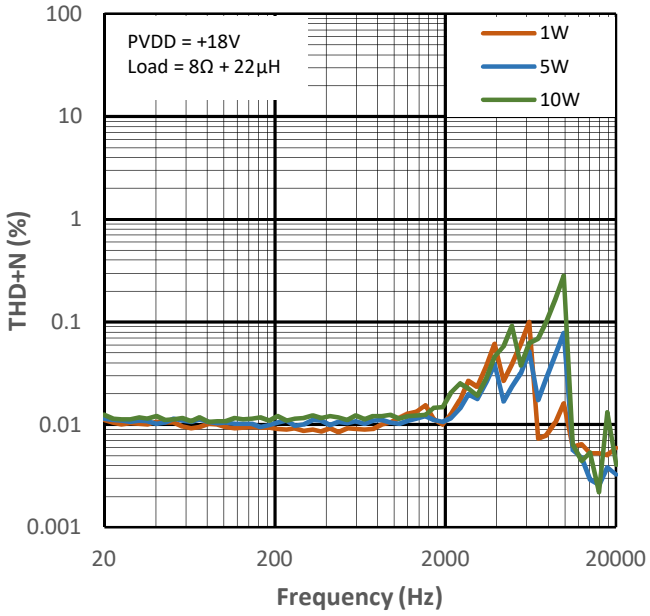


Figure 11-5 THD+N vs Frequency for PMP0

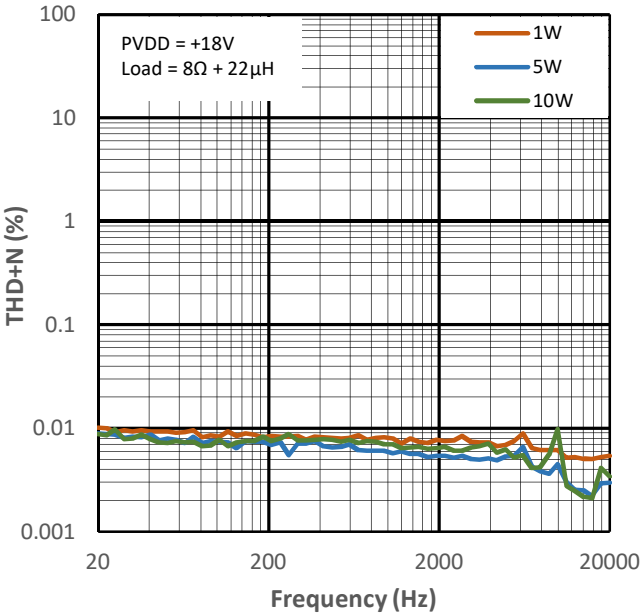


Figure 11-6 THD+N vs Frequency for PMP1

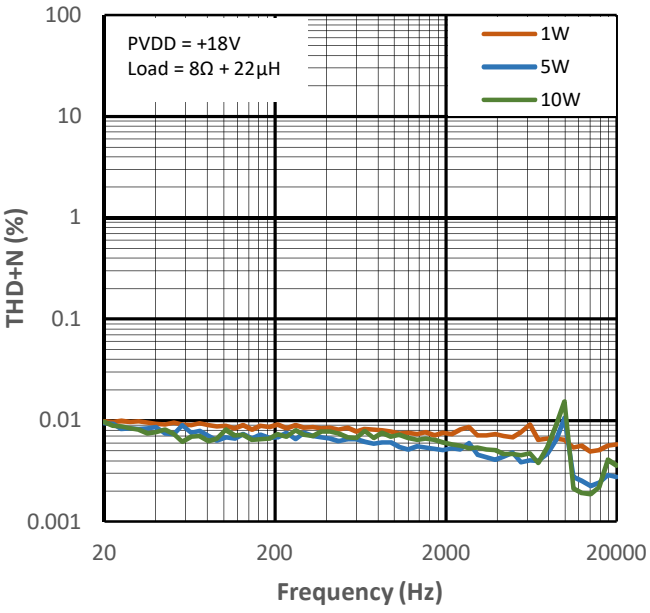


Figure 11-7 THD+N vs Frequency for PMP2

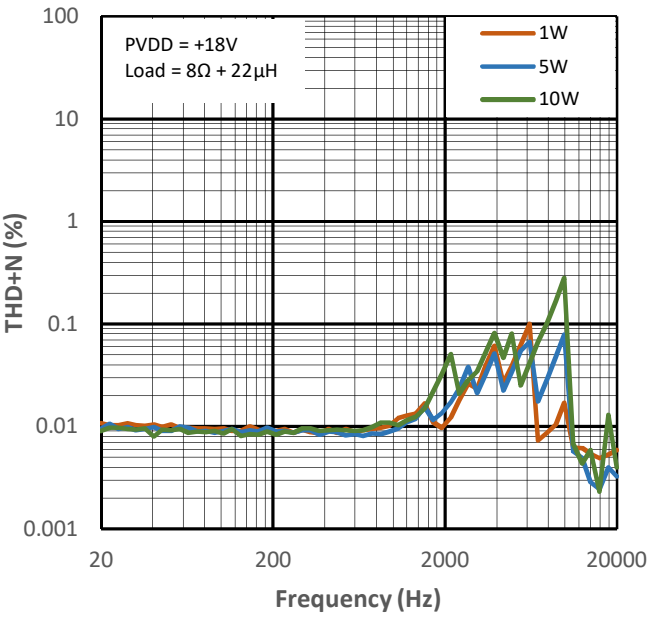


Figure 11-8 THD+N vs Frequency for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

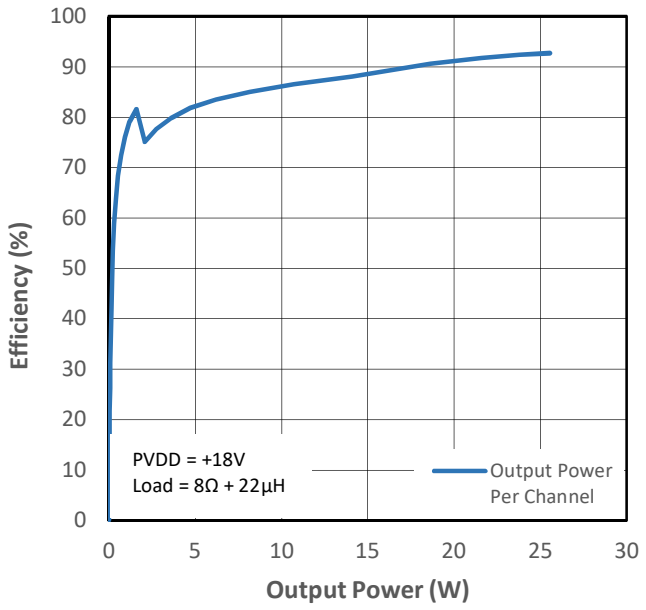


Figure 11-9 PMP0 Efficiency (VDD+PVDD) vs Output Power

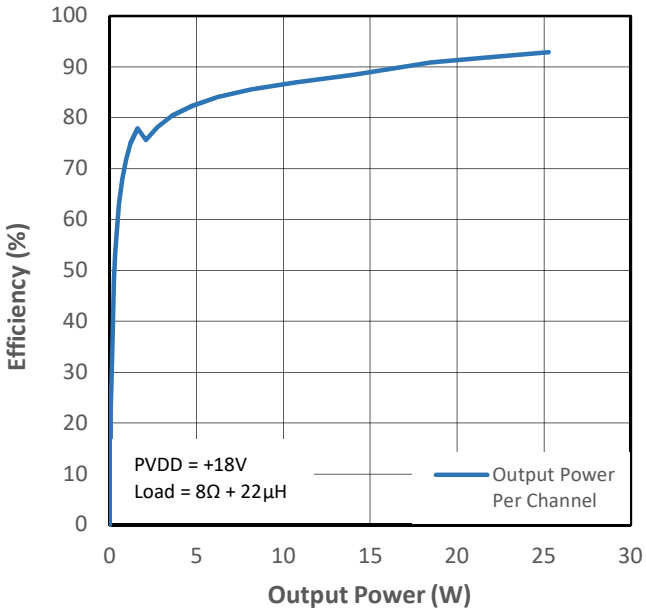


Figure 11-10 PMP1 Efficiency (VDD+PVDD) vs Output Power

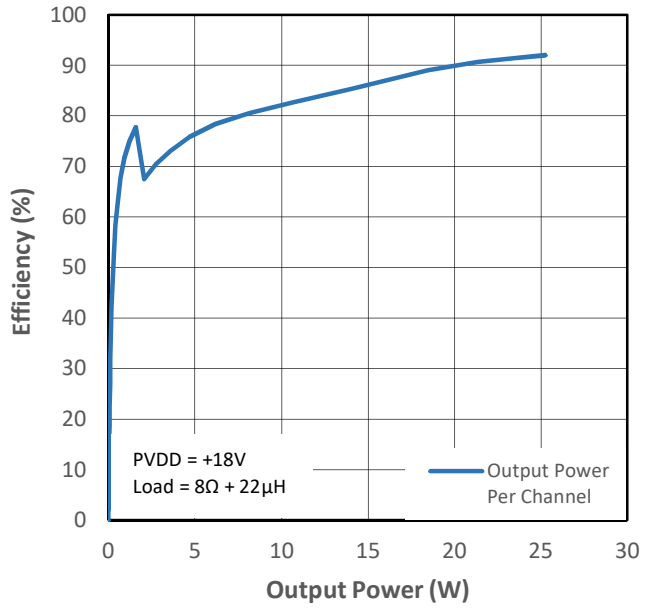


Figure 11-11 PMP2 Efficiency (VDD+PVDD) vs Output Power

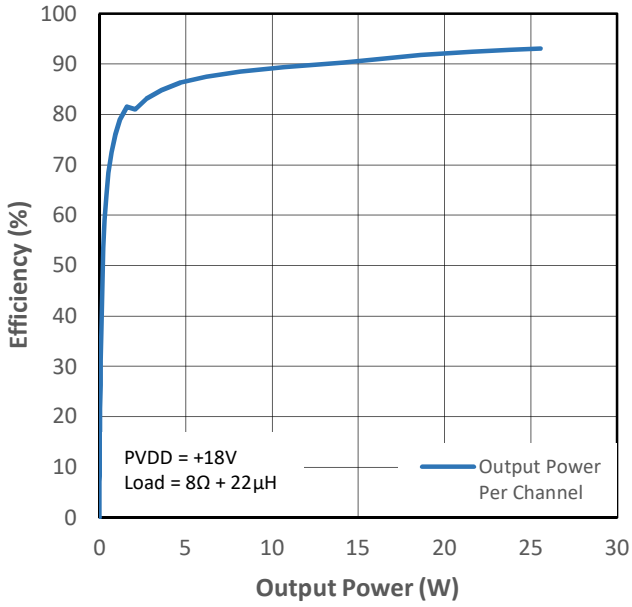


Figure 11-12 PMP4 Efficiency (VDD+PVDD) vs Output Power

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

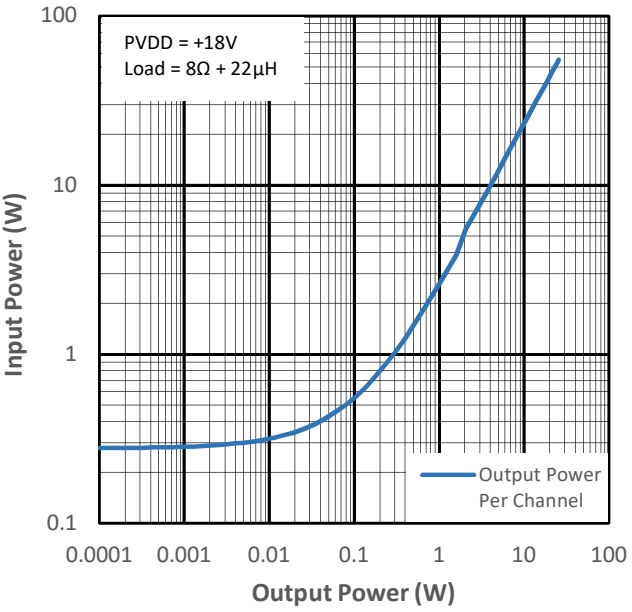


Figure 11-13 Input Power vs Output Power for PMP0

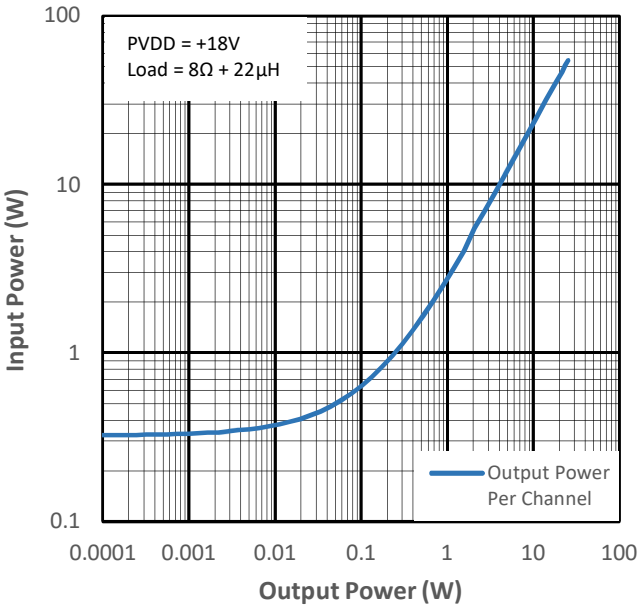


Figure 11-14 Input Power vs Output Power for PMP1

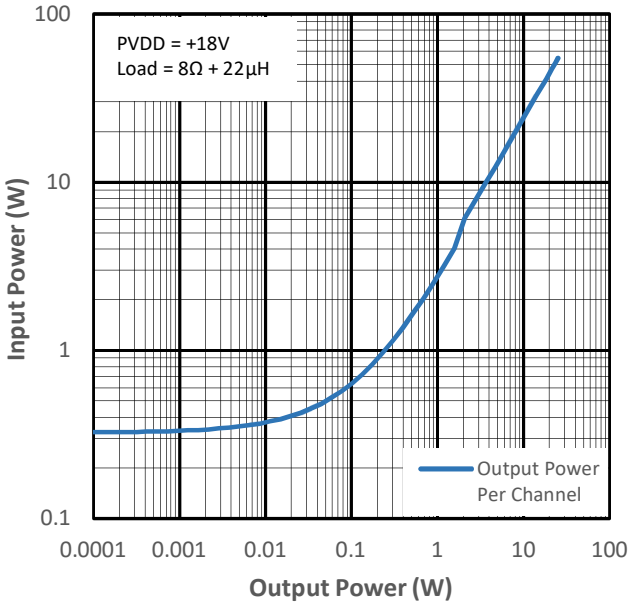


Figure 11-15 Input Power vs Output Power for PMP2

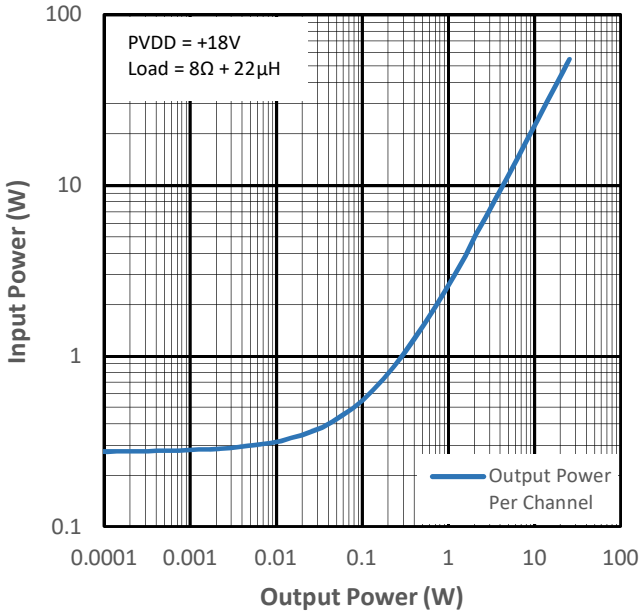


Figure 11-16 Input Power vs Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

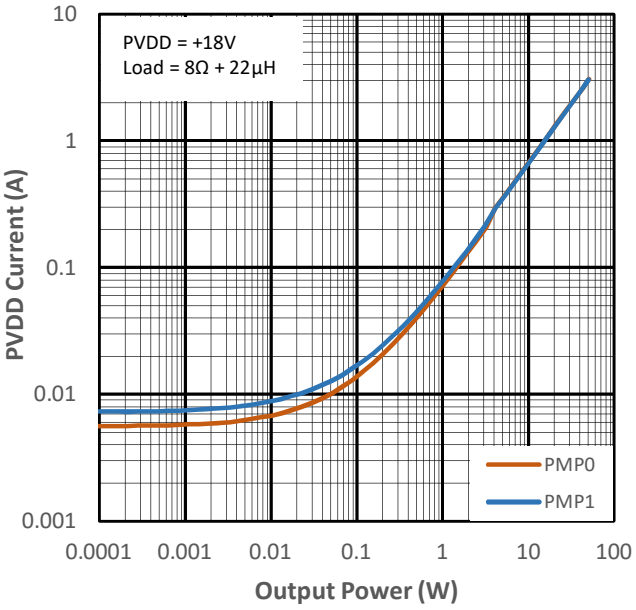


Figure 11-17 PVDD Current vs Output Power for PMP0 & PMP1

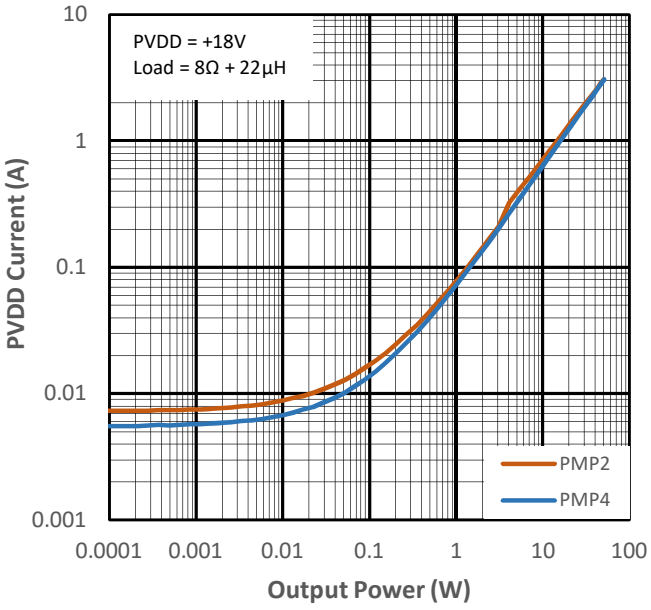


Figure 11-18 PVDD Current vs Output Power for PMP2 & PMP4

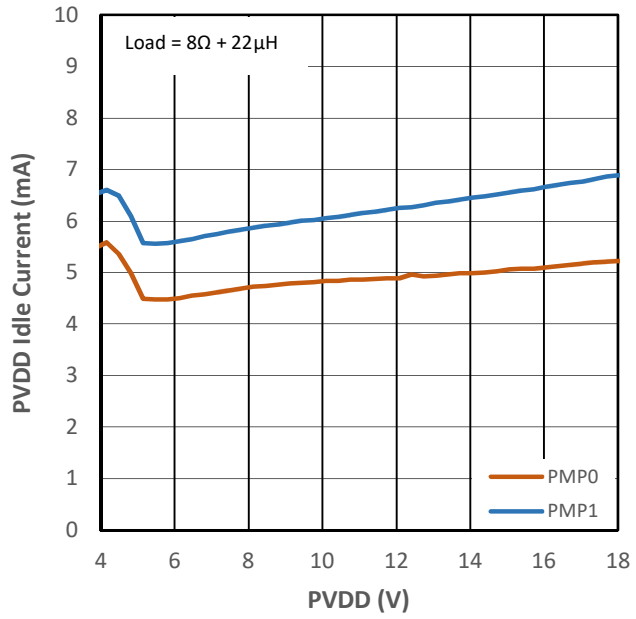


Figure 11-19 PVDD Current vs PVDD Voltage for PMP0 & PMP1

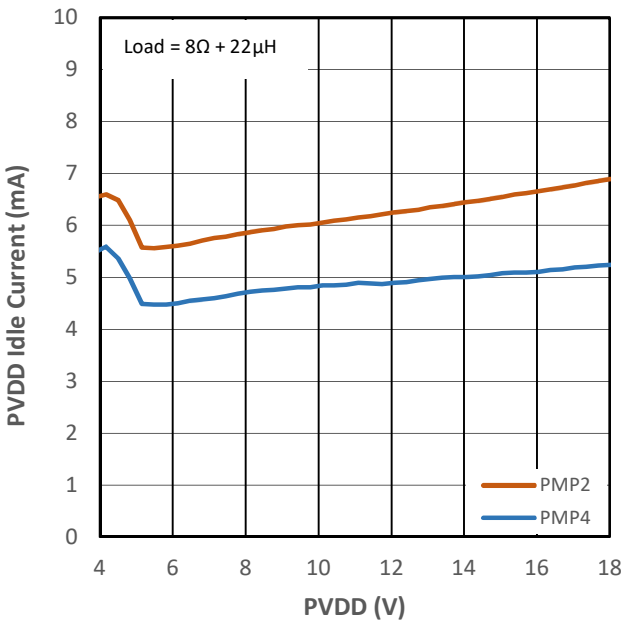


Figure 11-20 PVDD Current vs PVDD Voltage for PMP2 & PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

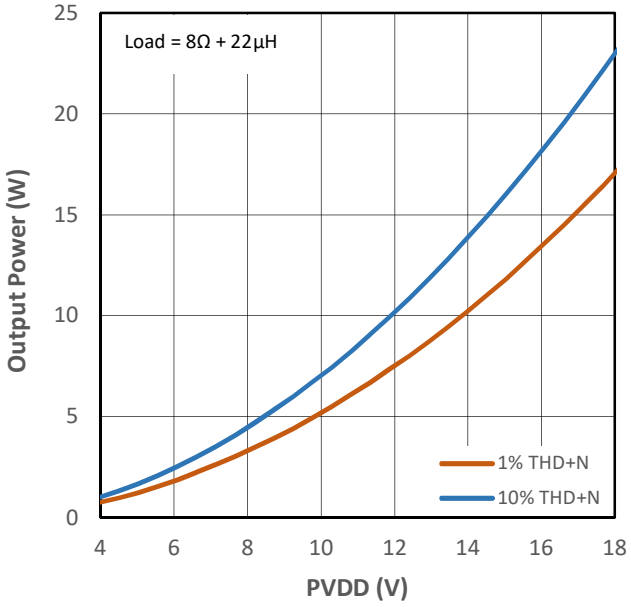


Figure 11-21 Output Power vs PVDD Voltage for PMP0

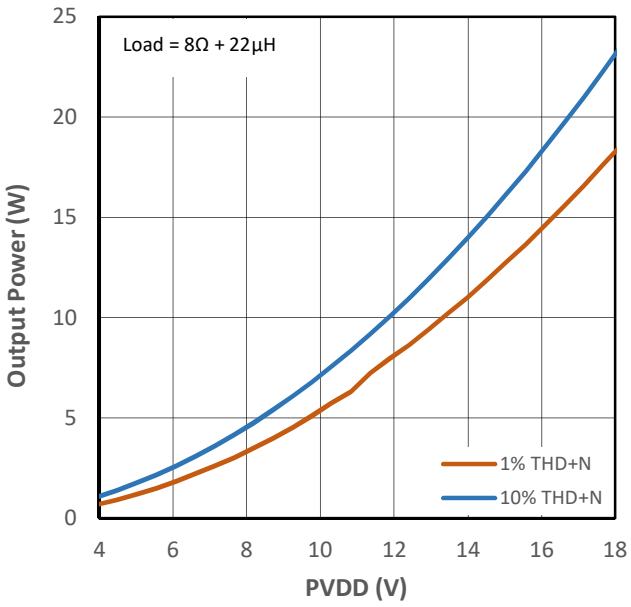


Figure 11-22 Output Power vs PVDD Voltage for PMP1

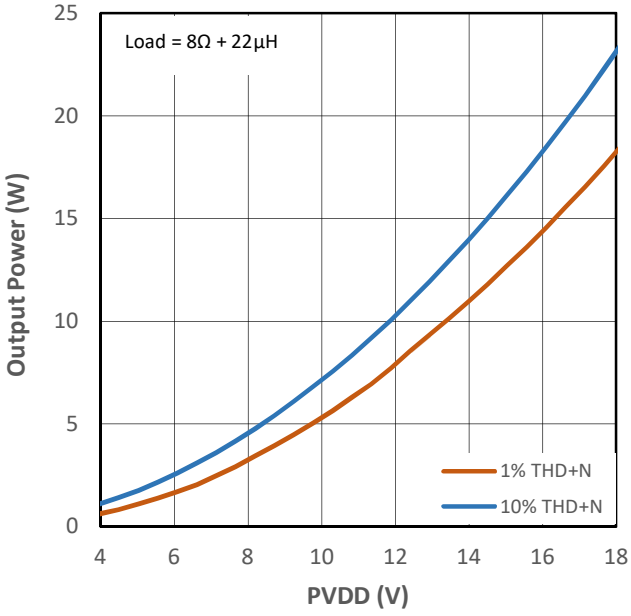


Figure 11-23 Output Power vs PVDD Voltage for PMP2

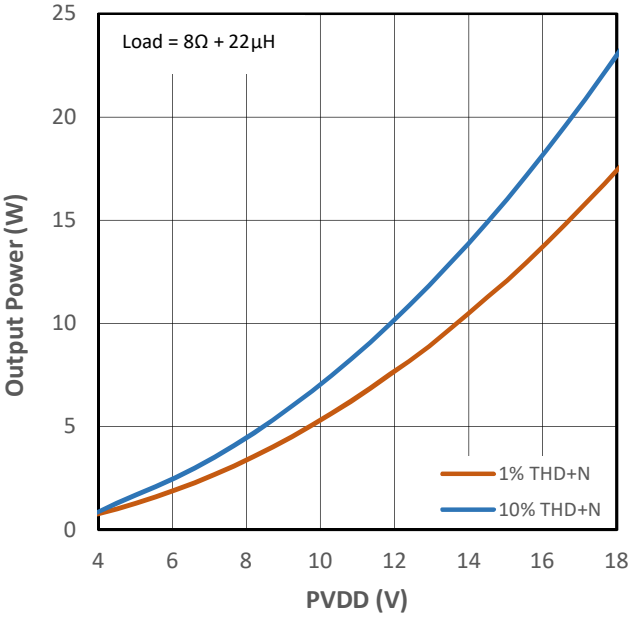


Figure 11-24 Output Power vs PVDD Voltage for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

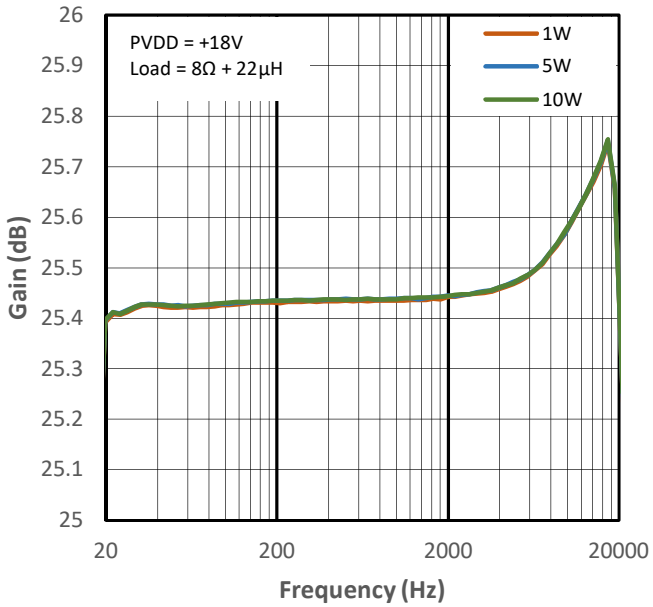


Figure 11-25 Gain vs Frequency for PMP0

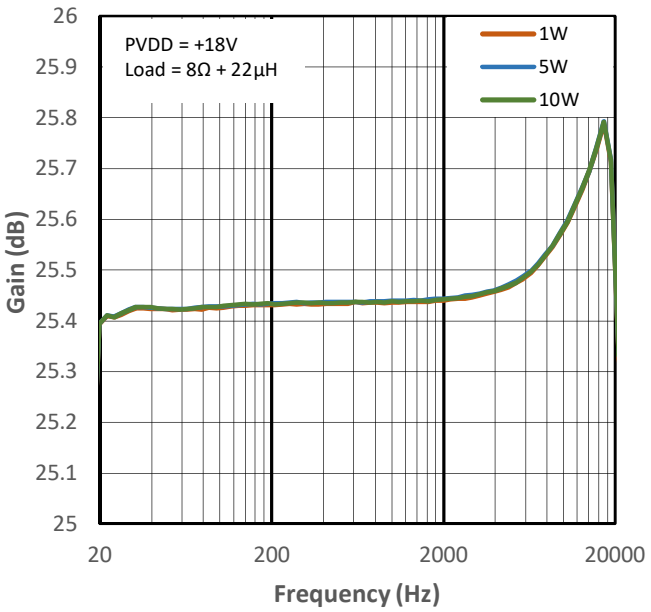


Figure 11-26 Gain vs Frequency for PMP1

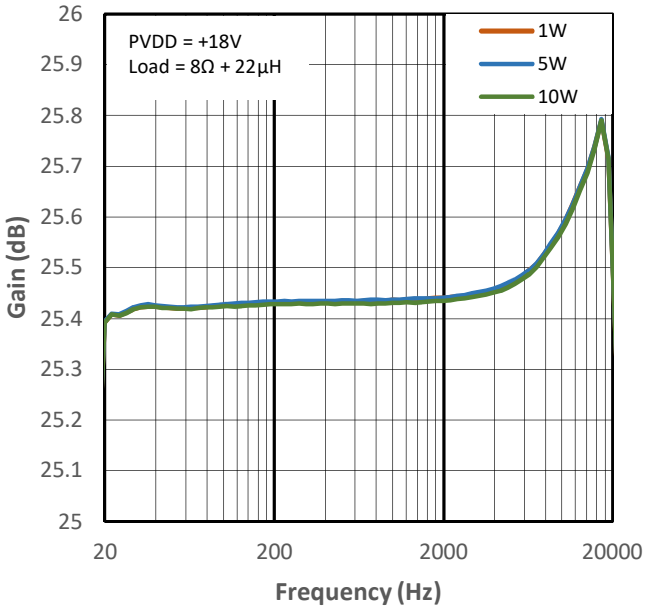


Figure 11-27 Gain vs Frequency for PMP2

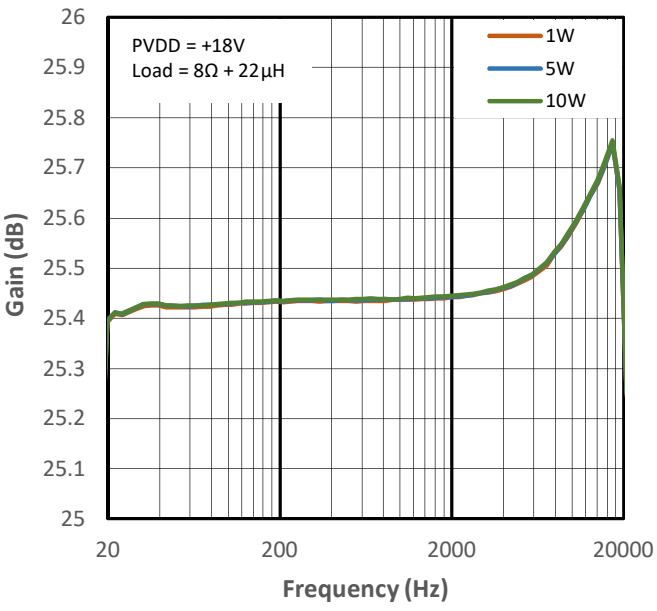


Figure 11-28 Gain vs Frequency for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

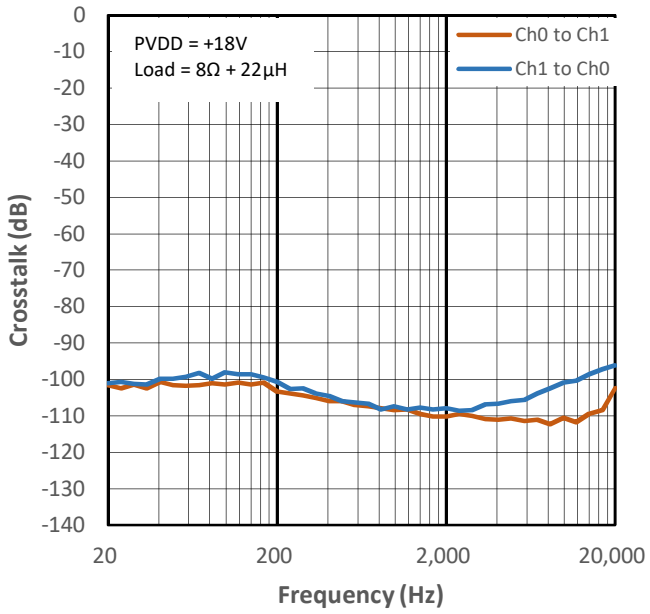


Figure 11-29 Crosstalk vs Frequency for PMP0

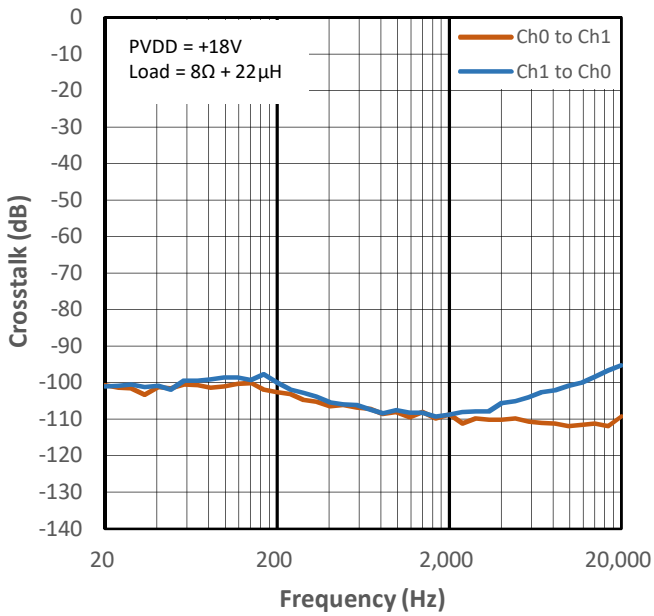


Figure 11-30 Crosstalk vs Frequency for PMP1

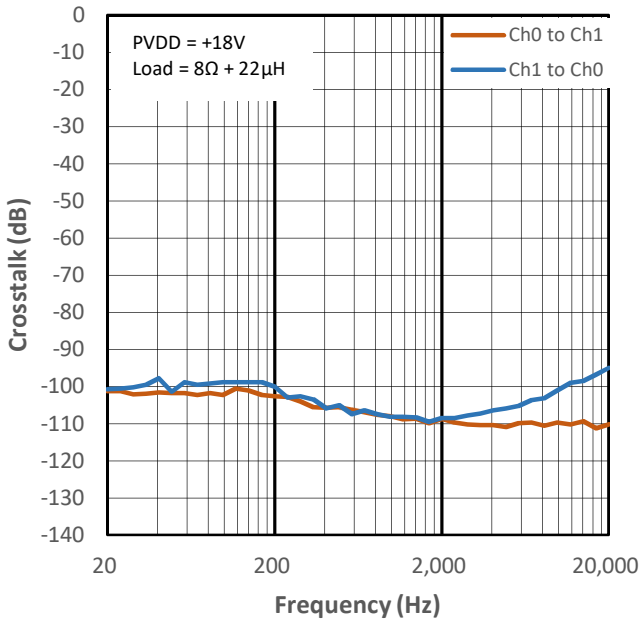


Figure 11-31 Crosstalk vs Frequency for PMP2

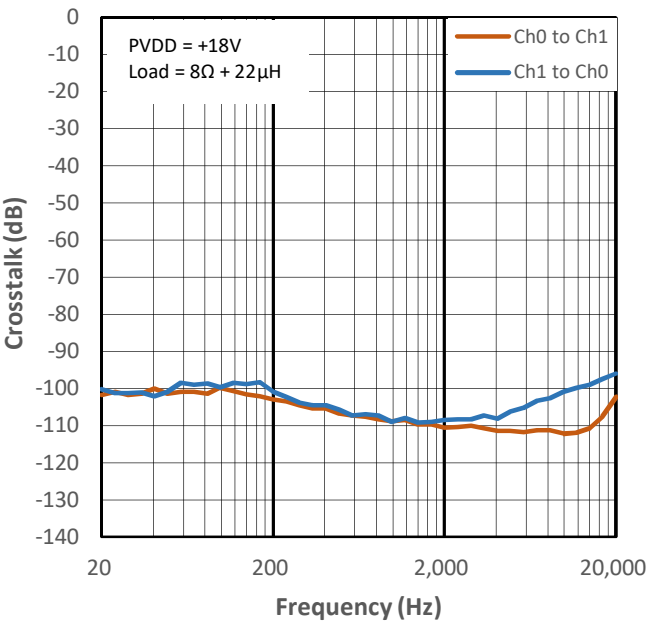


Figure 11-32 Crosstalk vs Frequency for PMP4

12 Typical Characteristics (PVDD = +15V, Load = 4Ω + 22µH)

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

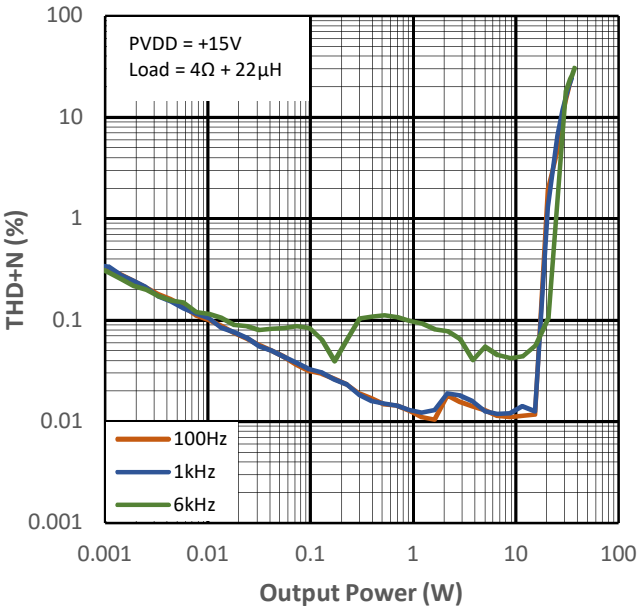


Figure 12-12-1 THD+N vs. Output Power for PMP0

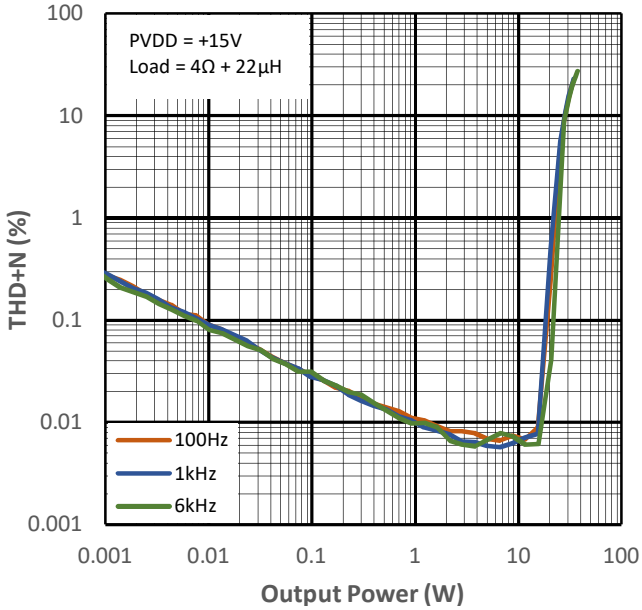


Figure 12-2 THD+N vs. Output Power for PMP1

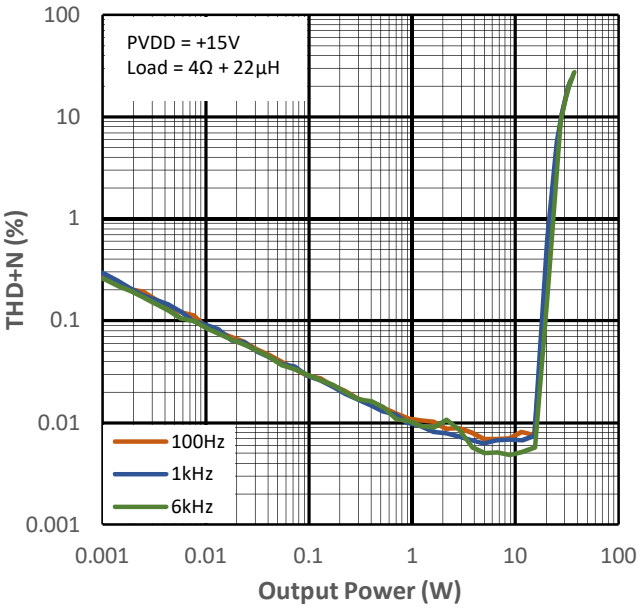


Figure 12-3 THD+N vs. Output Power for PMP2

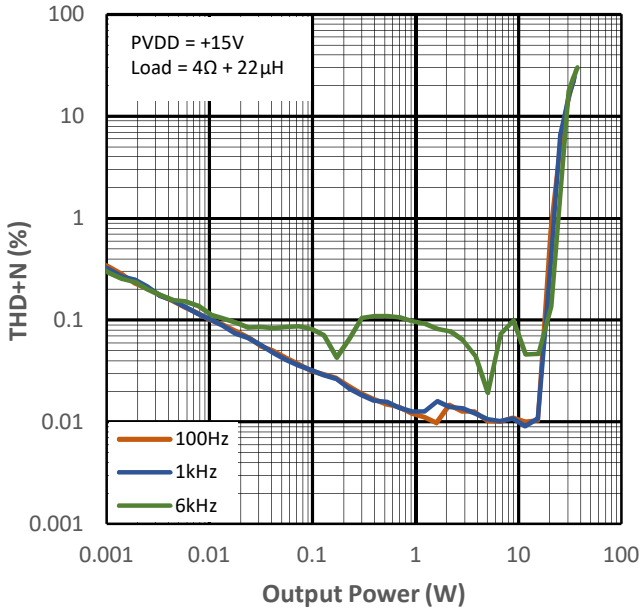


Figure 12-4 THD+N vs. Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

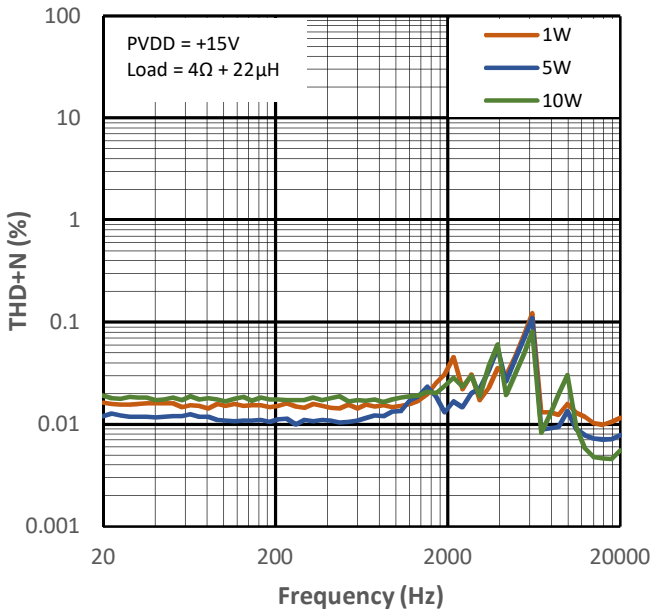


Figure 12-5 THD+N vs Frequency for PMP0

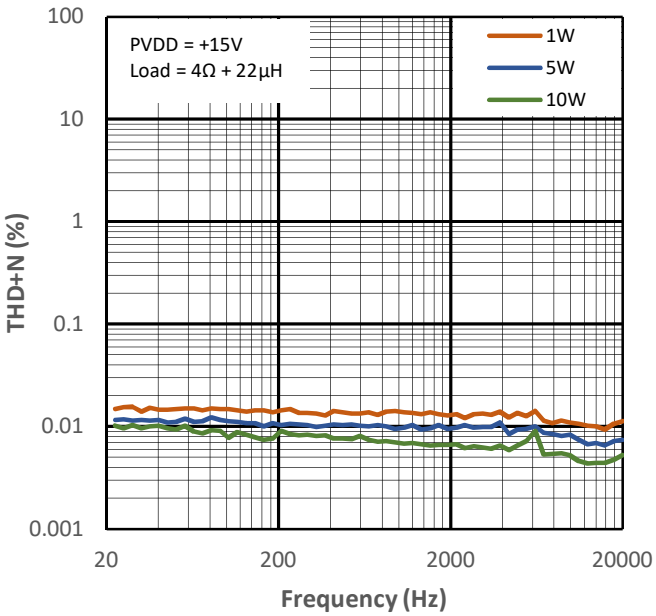


Figure 12-6 THD+N vs Frequency for PMP1

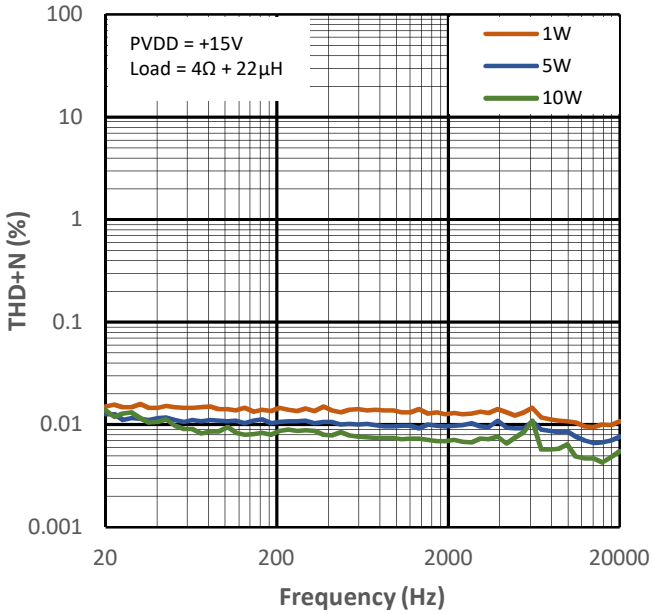


Figure 12-7 THD+N vs Frequency for PMP2

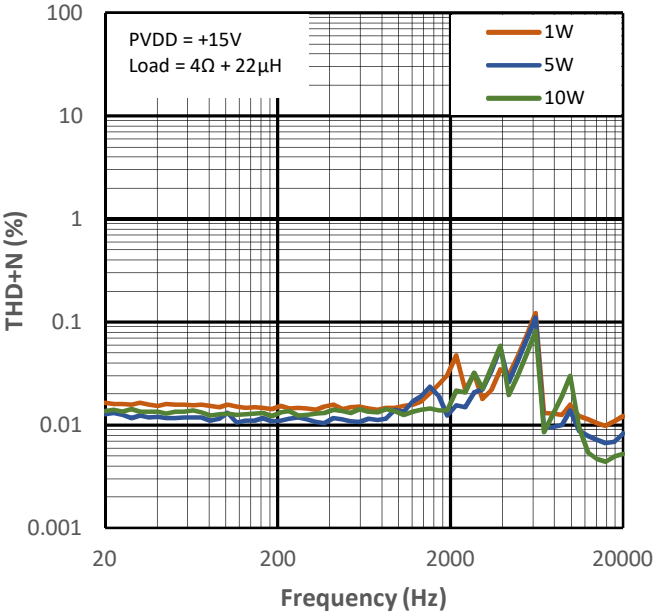


Figure 12-8 THD+N vs Frequency for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

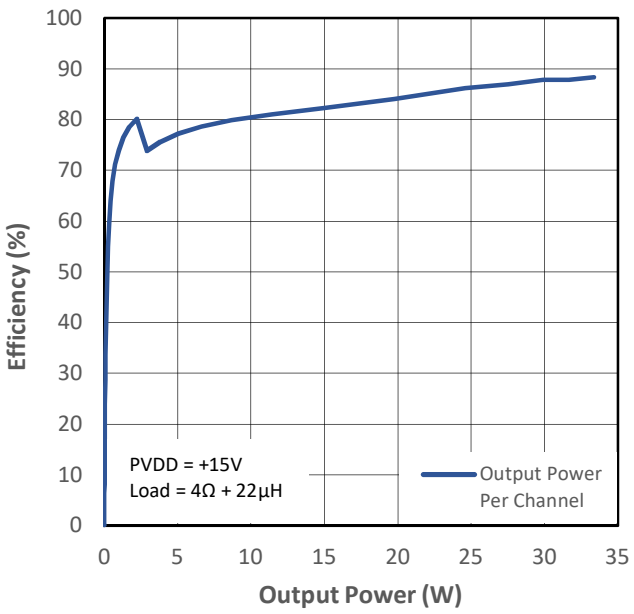


Figure 12-9 PMP0 Efficiency (VDD+PVDD) vs Output Power

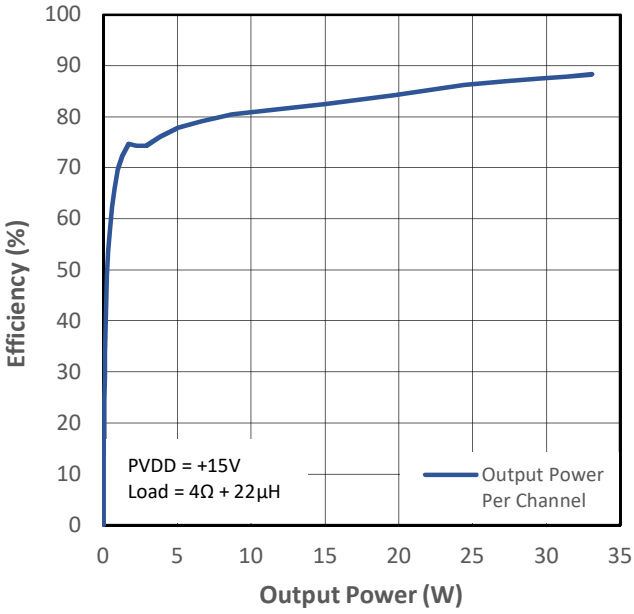


Figure 12-10 PMP1 Efficiency (VDD+PVDD) vs Output Power

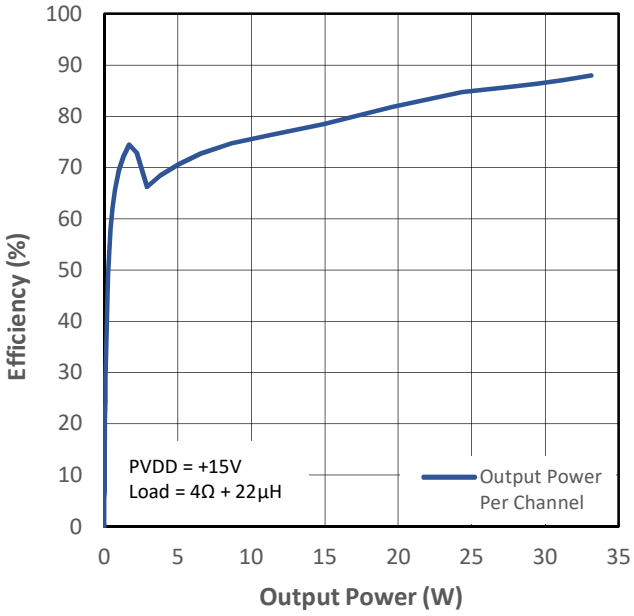


Figure 12-11 PMP2 Efficiency (VDD+PVDD) vs Output Power

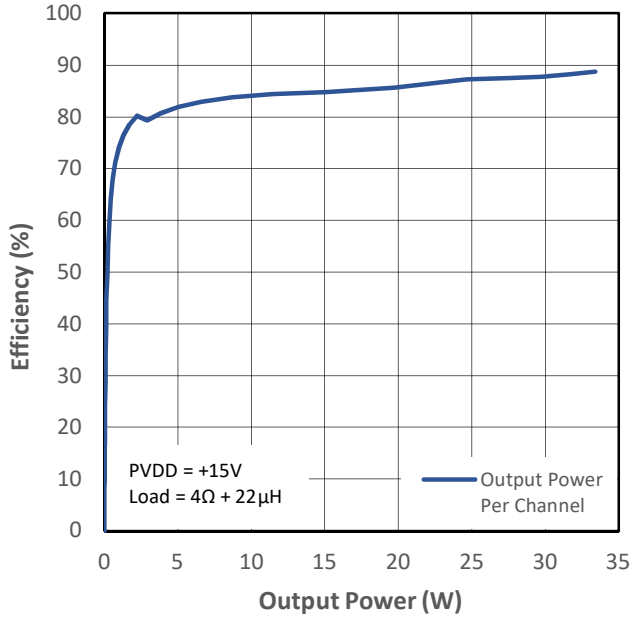


Figure 12-12 PMP4 Efficiency (VDD+PVDD) vs Output Power

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

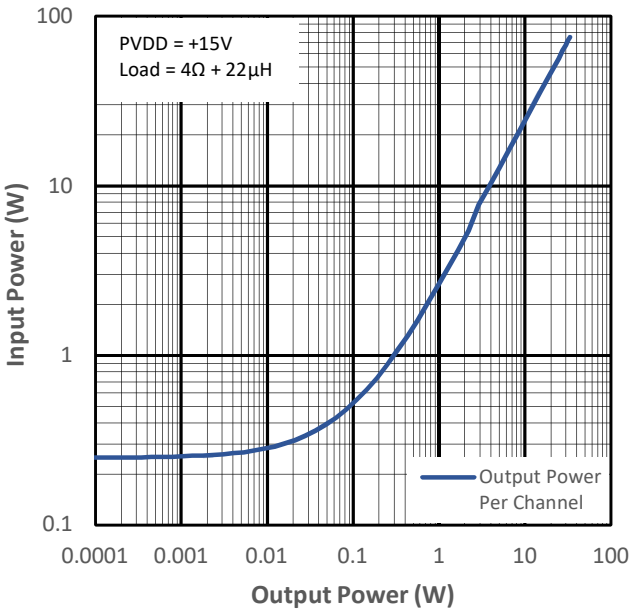


Figure 12-13 Input Power vs Output Power for PMP0

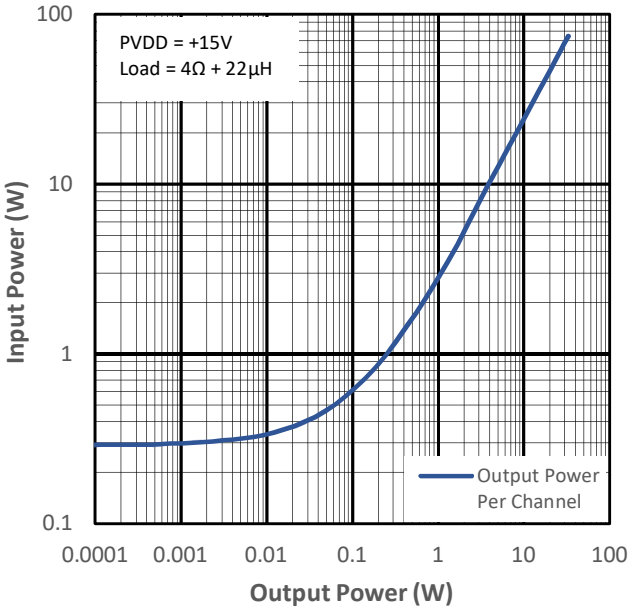


Figure 12-14 Input Power vs Output Power for PMP1

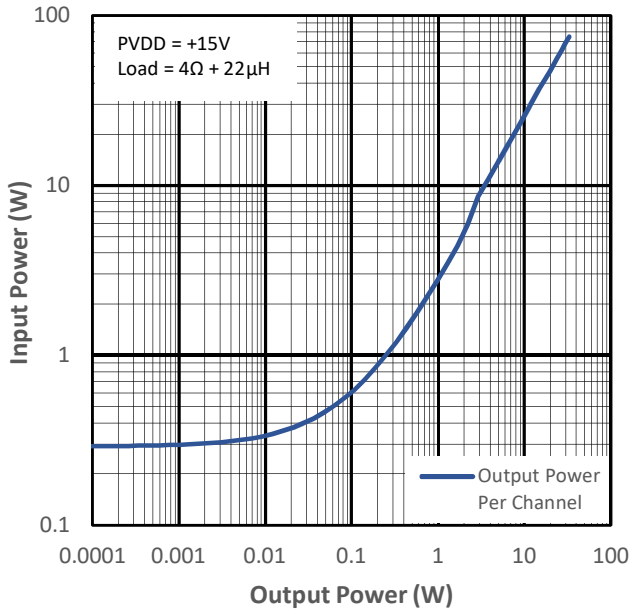


Figure 12-15 Input Power vs Output Power for PMP2

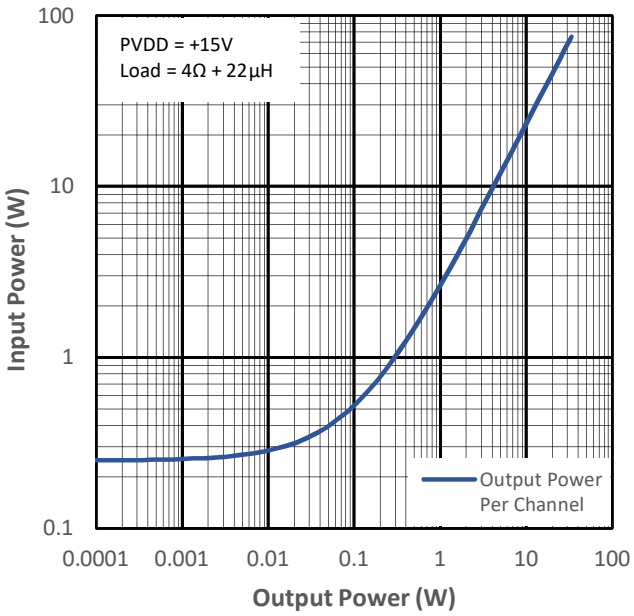


Figure 12-16 Input Power vs Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

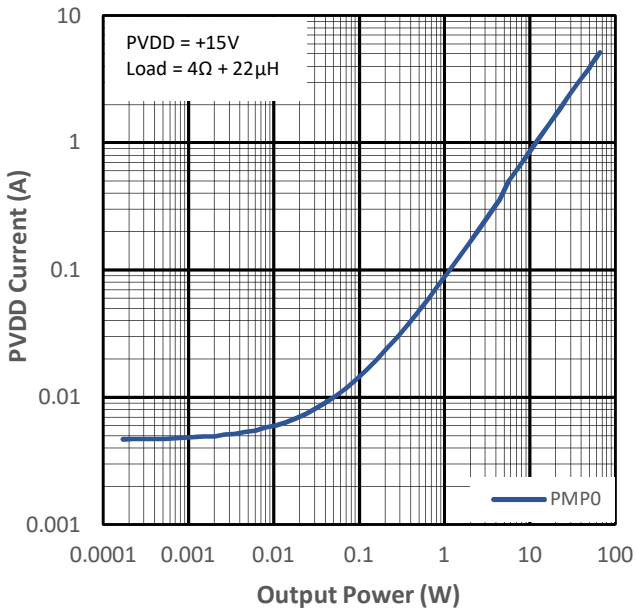


Figure 12-17 PVDD Current vs Output Power for PMP0

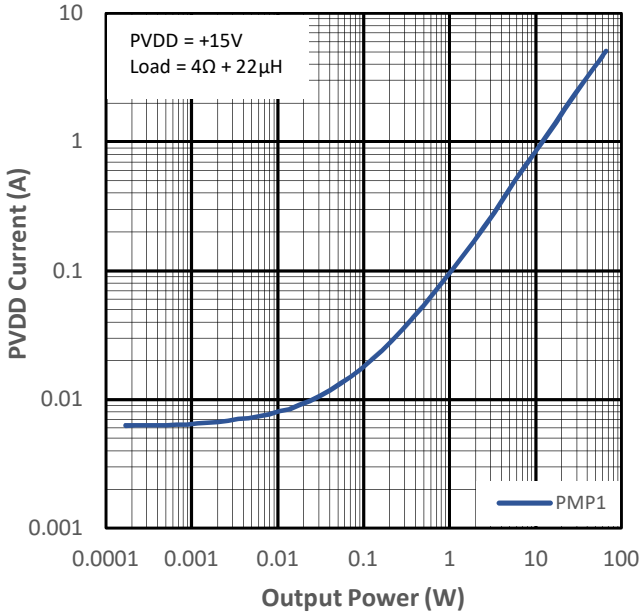


Figure 12-18 PVDD Current vs Output Power for PMP1

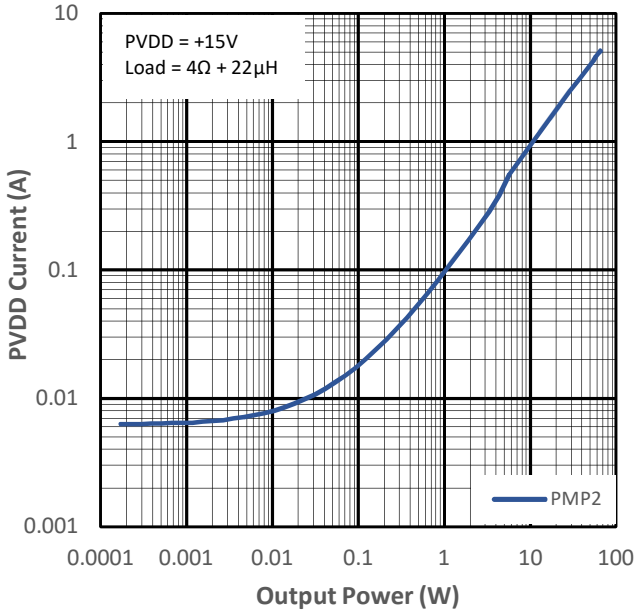


Figure 12-19 PVDD Current vs Output Power for PMP2

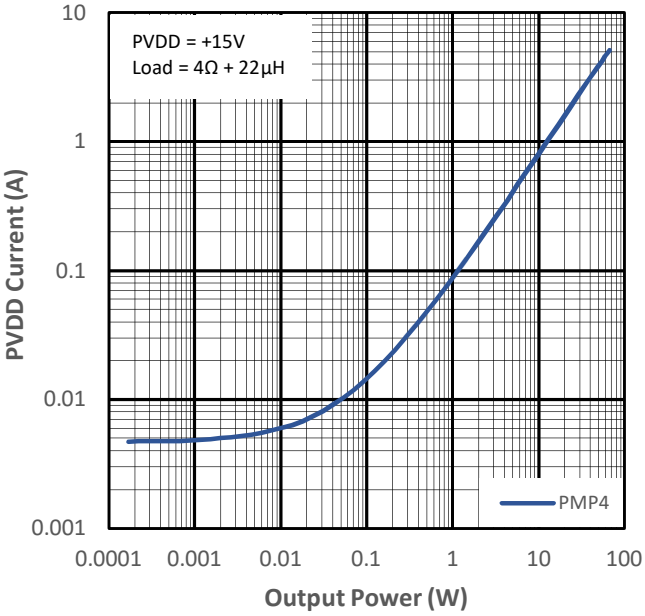


Figure 12-20 PVDD Current vs Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

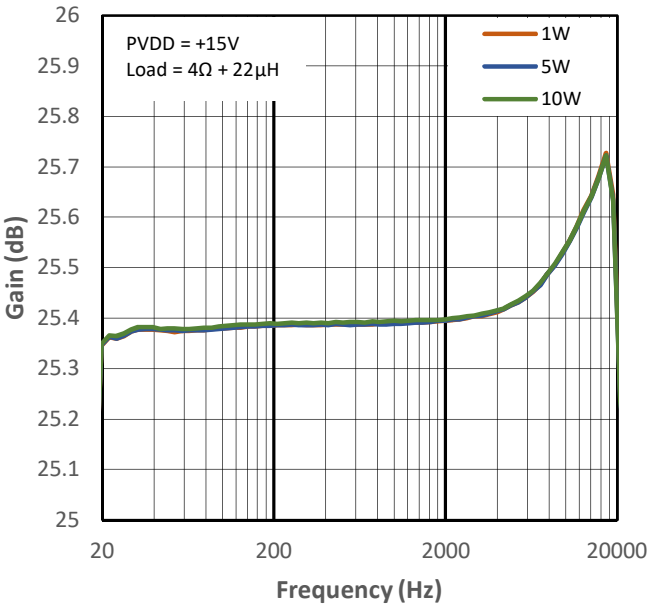


Figure 12-21 Gain vs Frequency for PMP0

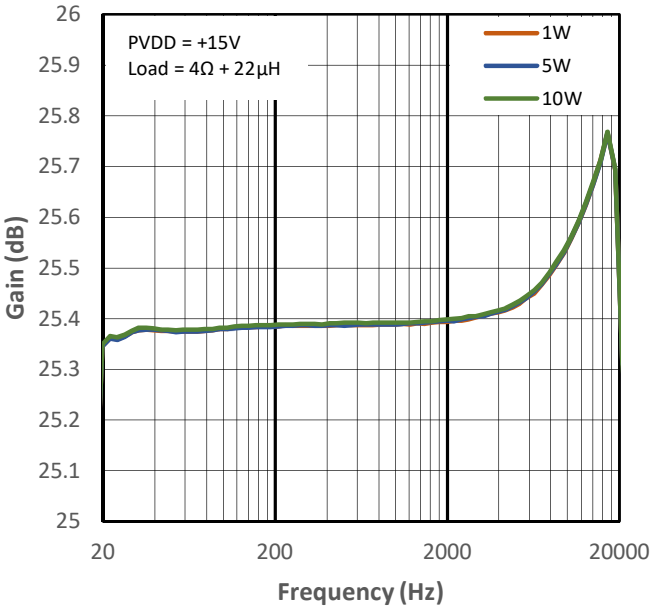


Figure 12-22 Gain vs Frequency for PMP1

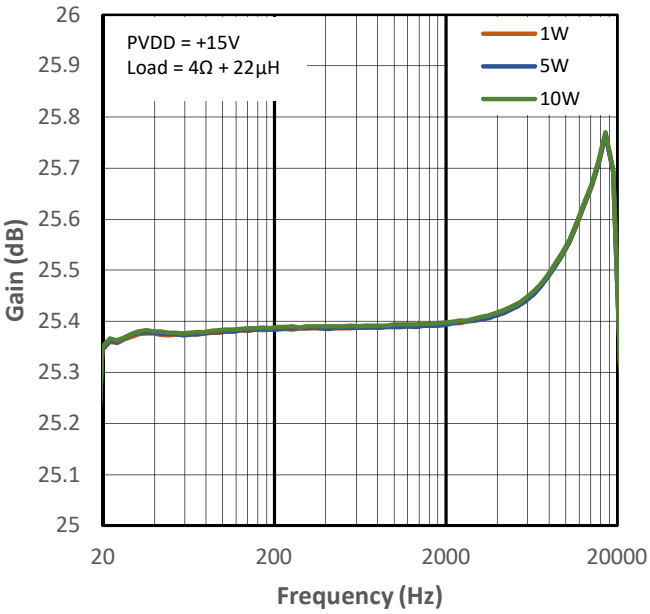


Figure 12-23 Gain vs Frequency for PMP2

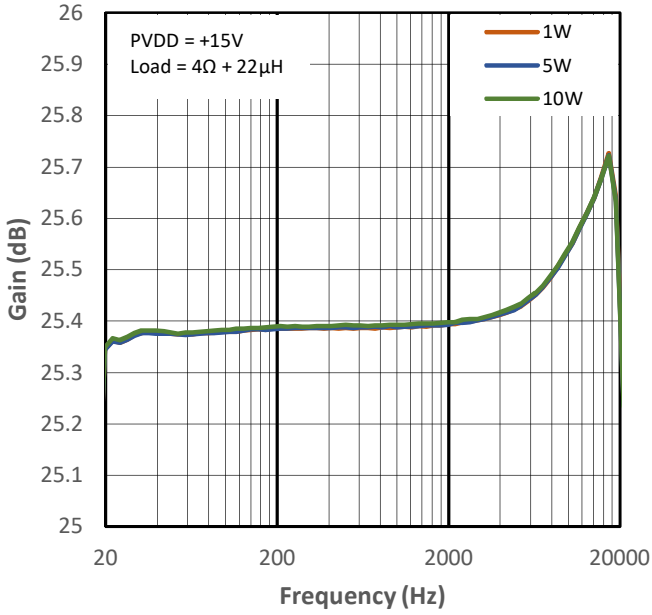


Figure 12-24 Gain vs Frequency for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

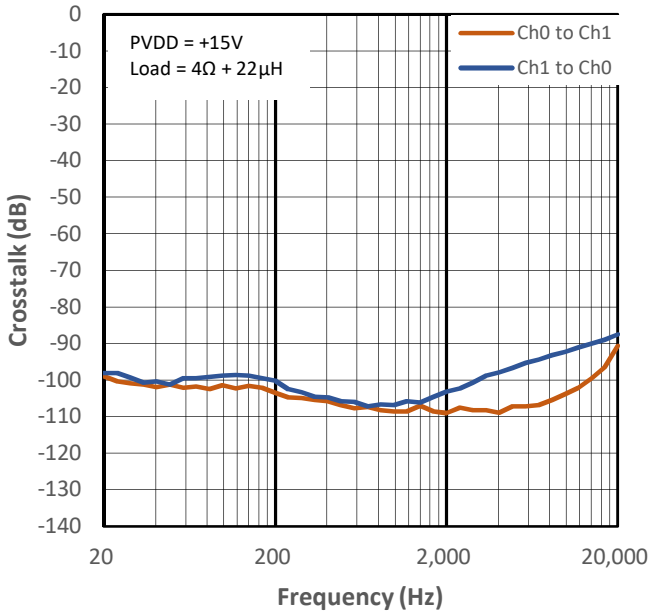


Figure 12-25 Crosstalk vs Frequency for PMP0

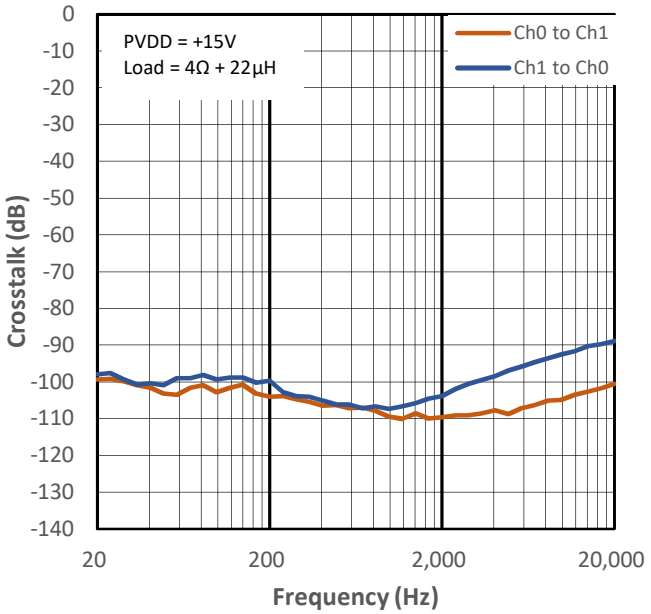


Figure 12-26 Crosstalk vs Frequency for PMP1

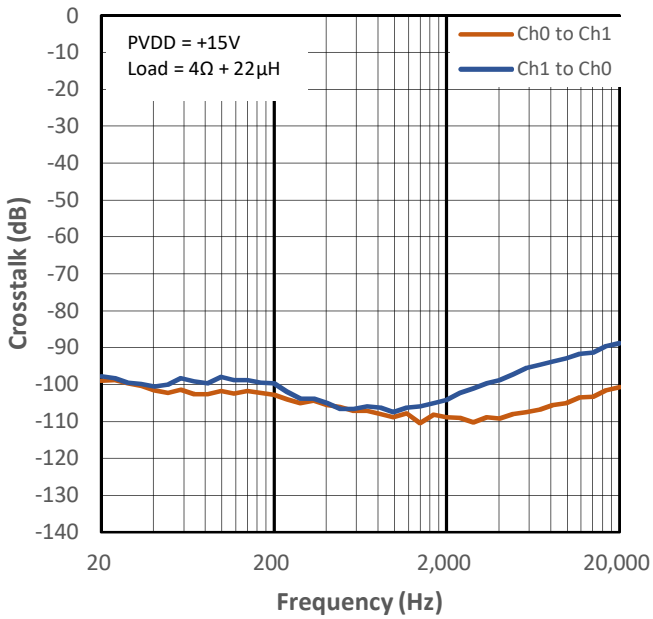


Figure 12-27 Crosstalk vs Frequency for PMP2

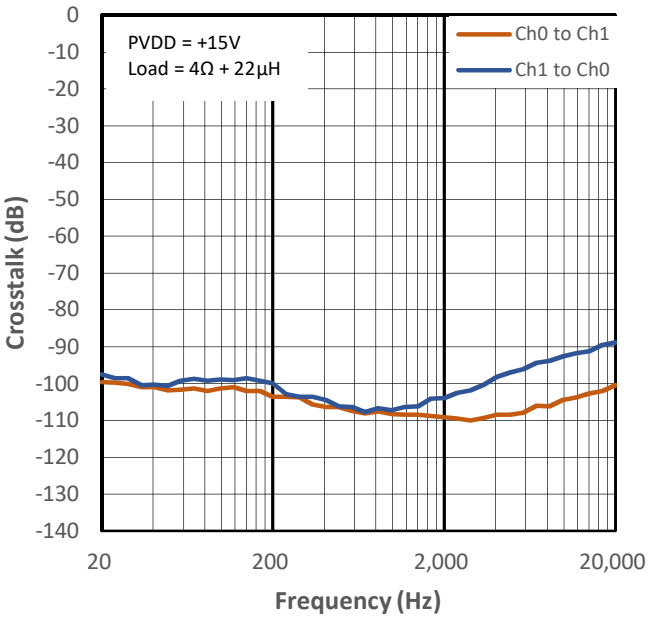


Figure 12-28 Crosstalk vs Frequency for PMP4

13 Typical Characteristics (PVDD = +15V, Load = 8Ω + 22µH)

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

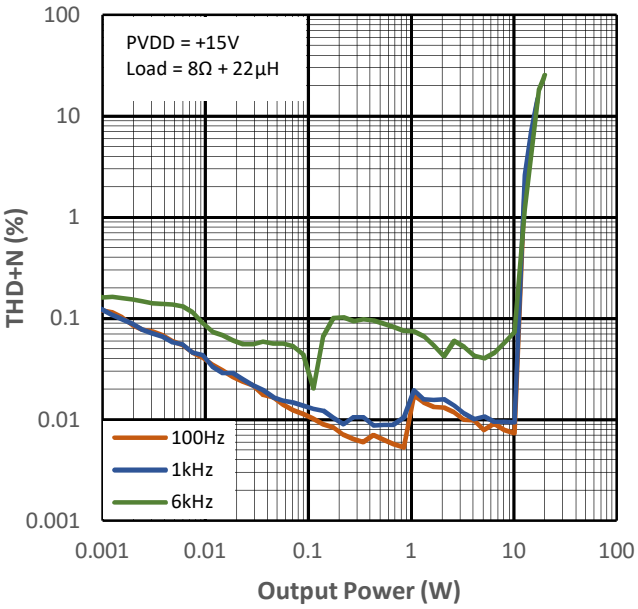


Figure 13-13-1 THD+N vs. Output Power for PMP0

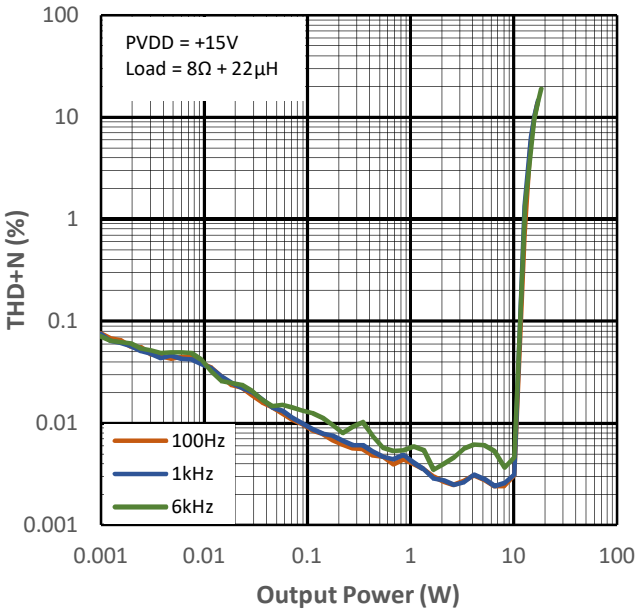


Figure 13-2 THD+N vs. Output Power for PMP1

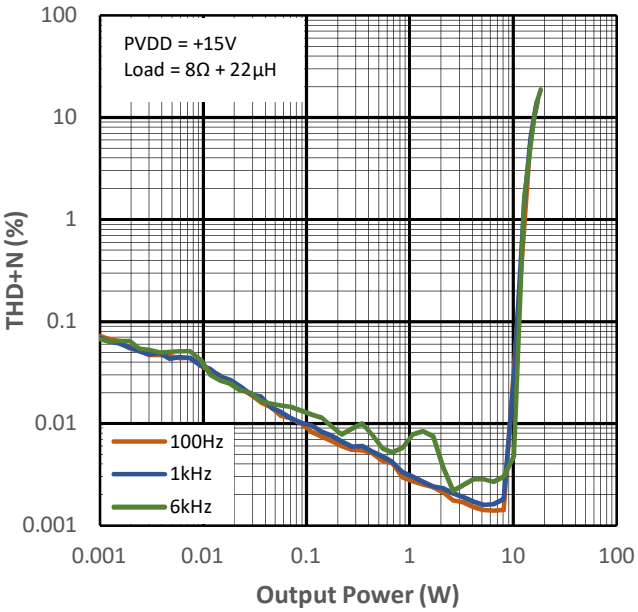


Figure 13-3 THD+N vs. Output Power for PMP2

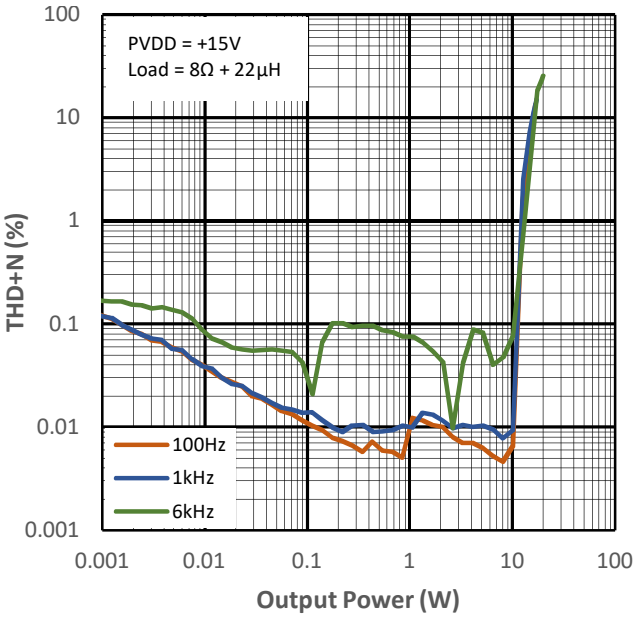


Figure 13-4 THD+N vs. Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

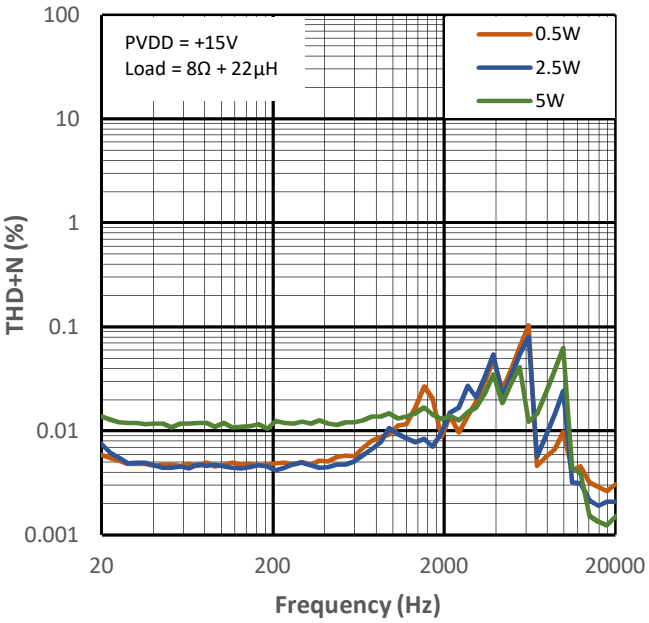


Figure 13-5 THD+N vs Frequency for PMP0

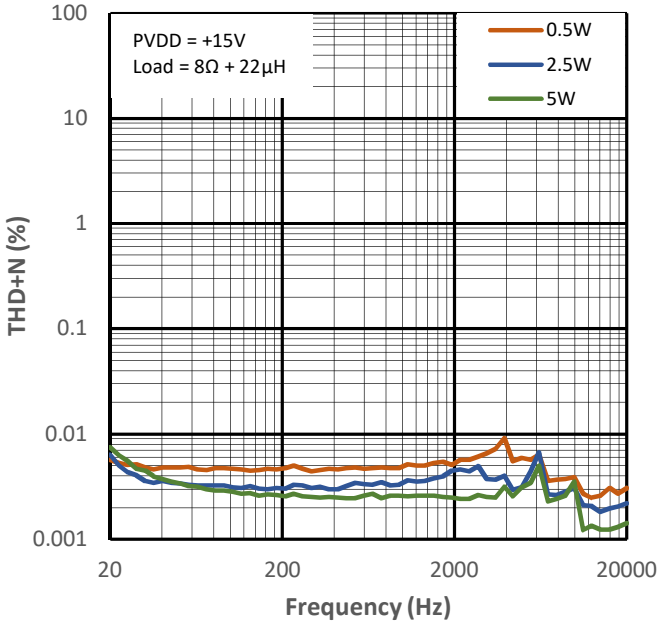


Figure 13-6 THD+N vs Frequency for PMP1

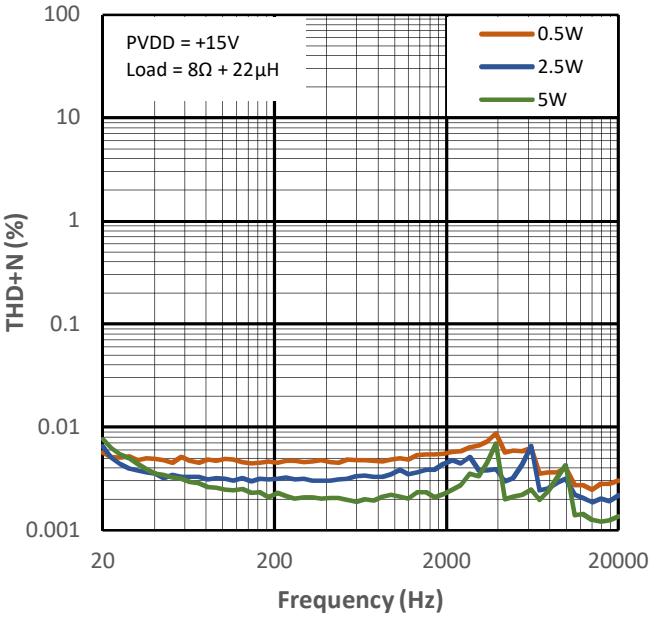


Figure 13-7 THD+N vs Frequency for PMP2

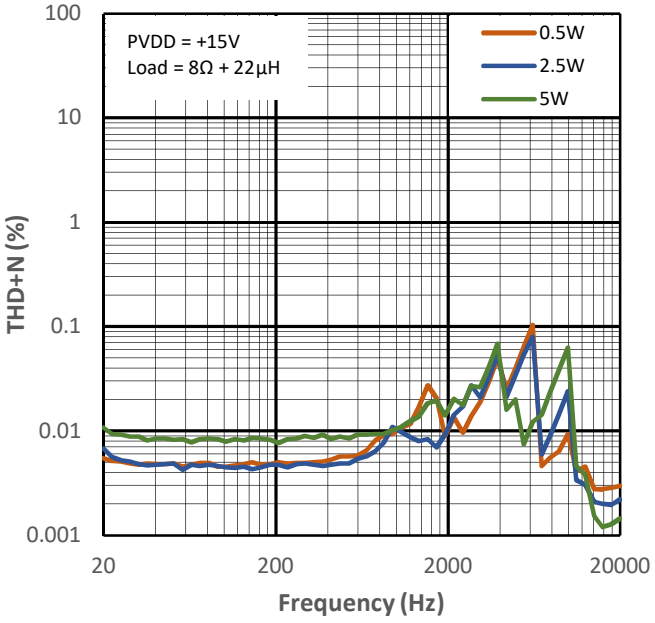


Figure 13-8 THD+N vs Frequency for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

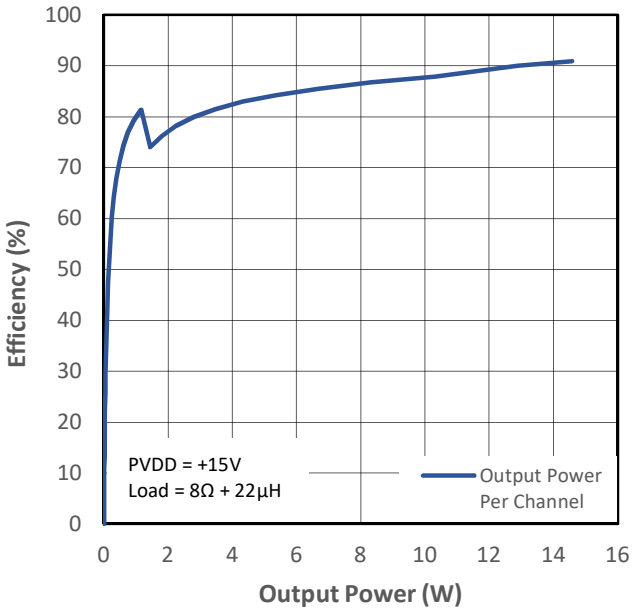


Figure 13-9 PMP0 Efficiency (VDD+PVDD) vs Output Power

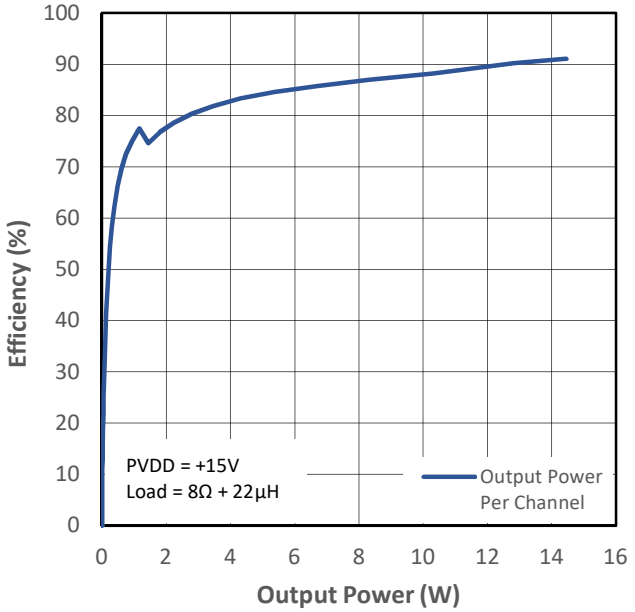


Figure 13-10 PMP1 Efficiency (VDD+PVDD) vs Output Power

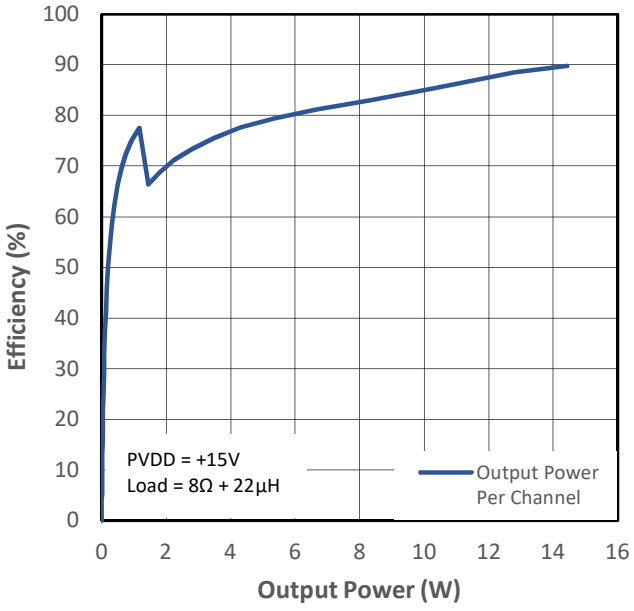


Figure 13-11 PMP2 Efficiency (VDD+PVDD) vs Output Power

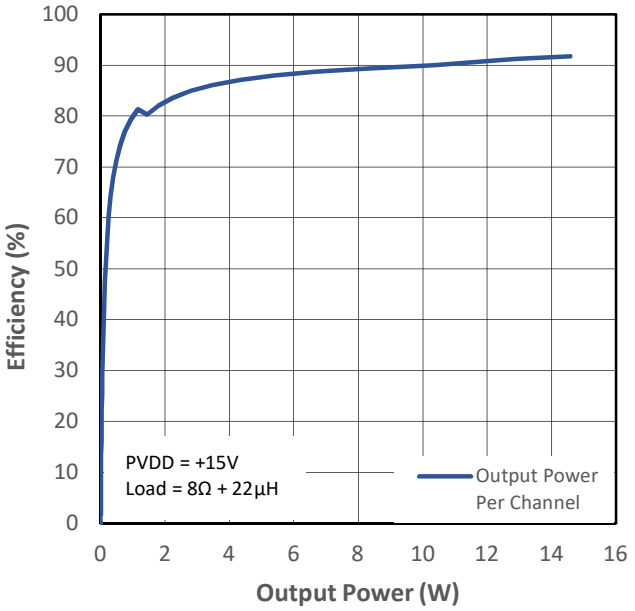


Figure 13-12 PMP4 Efficiency (VDD+PVDD) vs Output Power

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

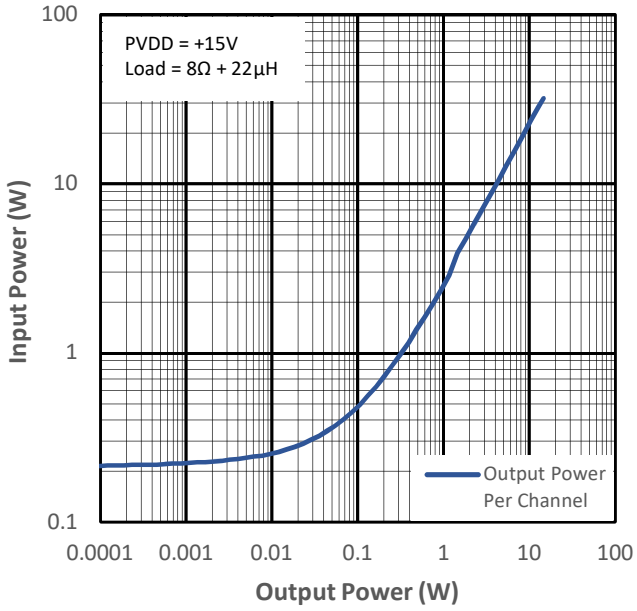


Figure 13-13 Input Power vs Output Power for PMP0

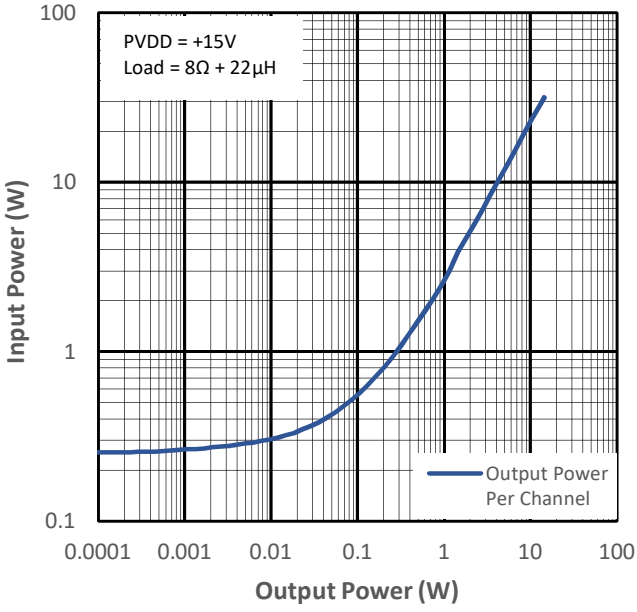


Figure 13-14 Input Power vs Output Power for PMP1

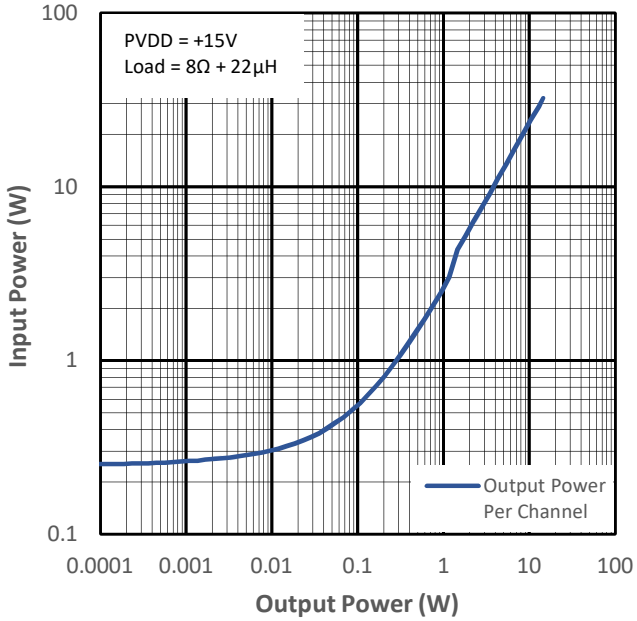


Figure 13-15 Input Power vs Output Power for PMP2

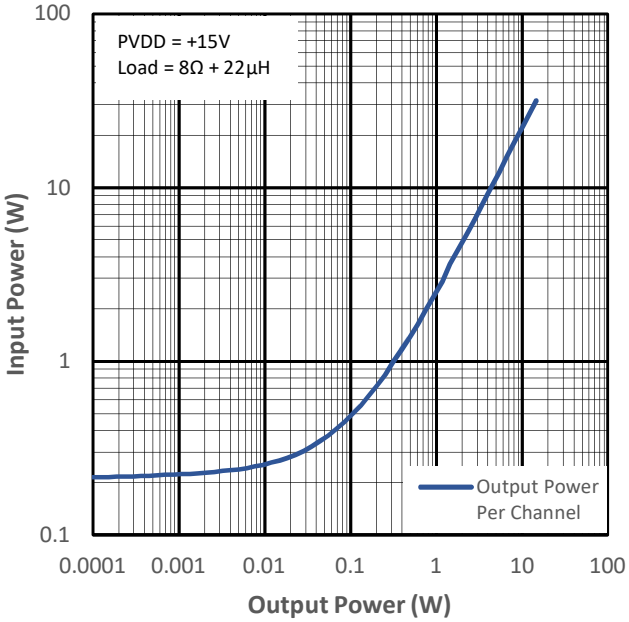


Figure 13-16 Input Power vs Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

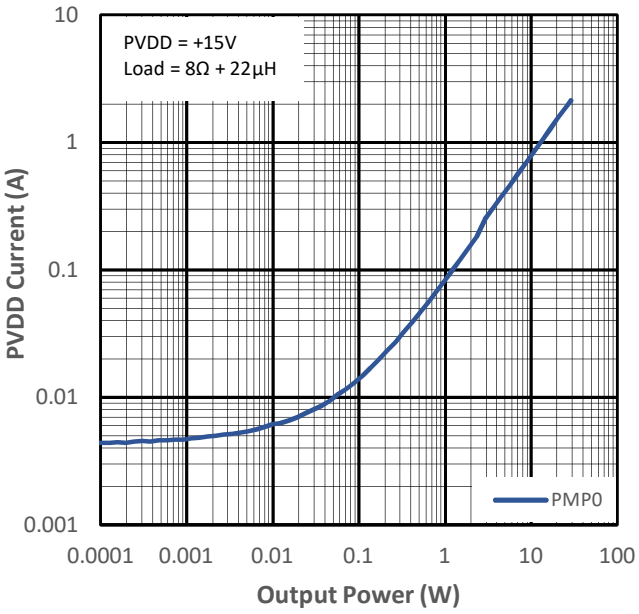


Figure 13-17 PVDD Current vs Output Power for PMP0

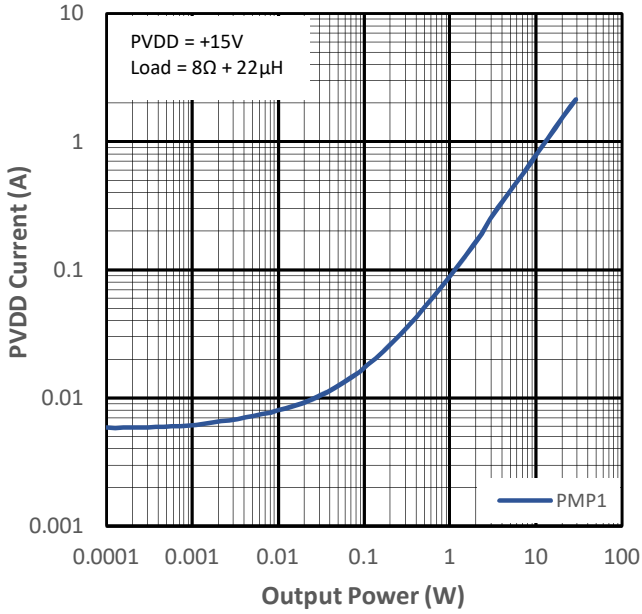


Figure 13-18 PVDD Current vs Output Power for PMP1

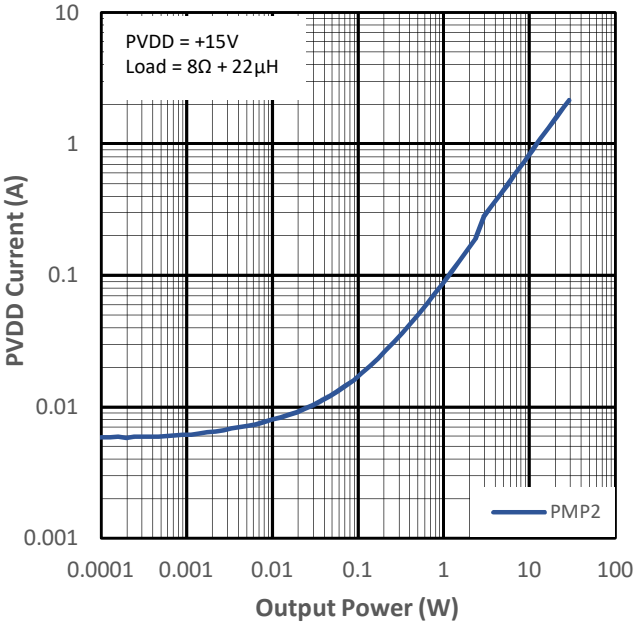


Figure 13-19 PVDD Current vs Output Power for PMP2

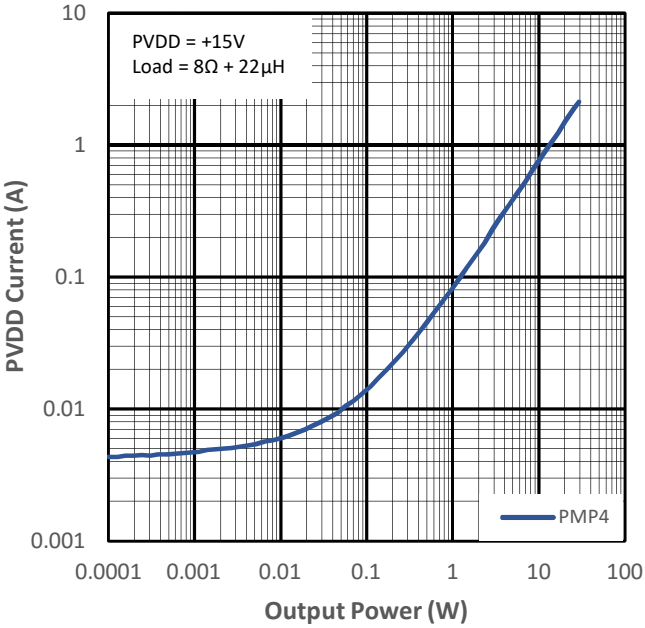


Figure 13-20 PVDD Current vs Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

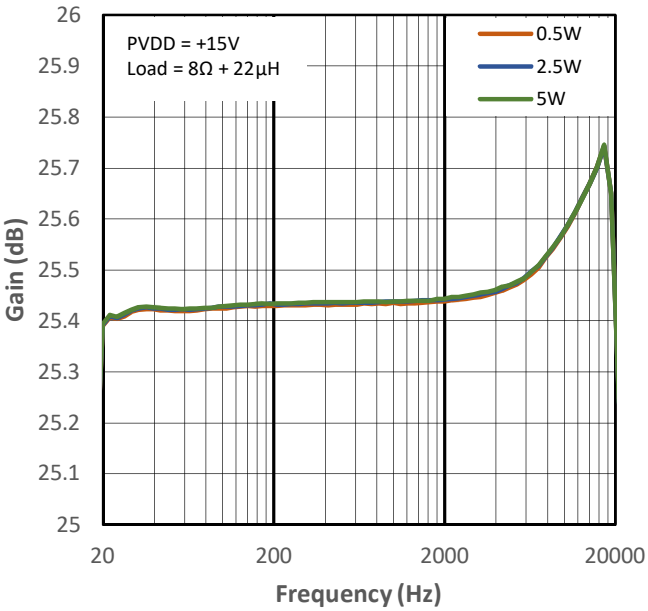


Figure 13-21 Gain vs Frequency for PMP0

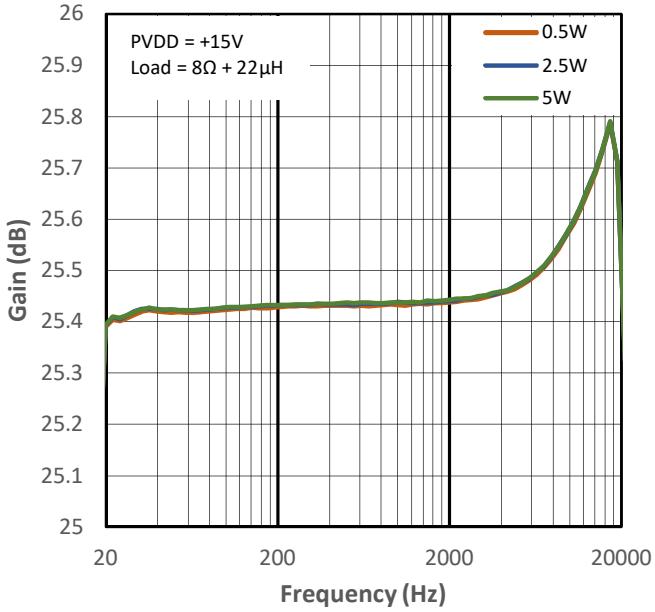


Figure 13-22 Gain vs Frequency for PMP1

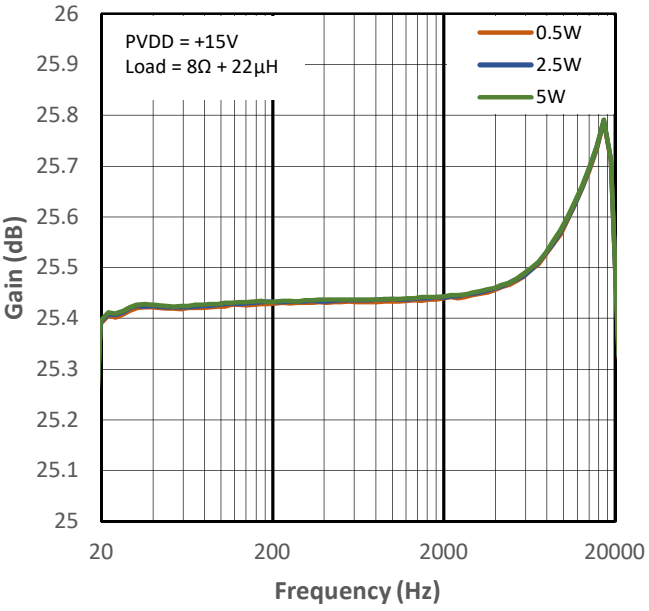


Figure 13-23 Gain vs Frequency for PMP2

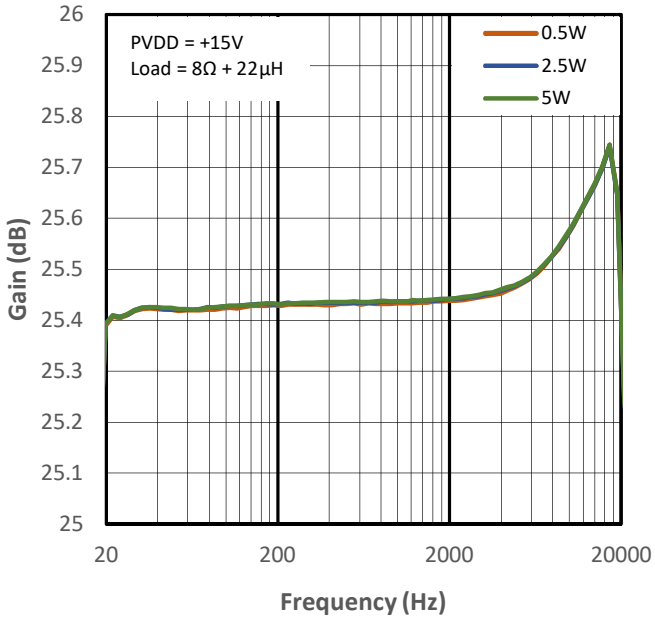


Figure 13-24 Gain vs Frequency for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

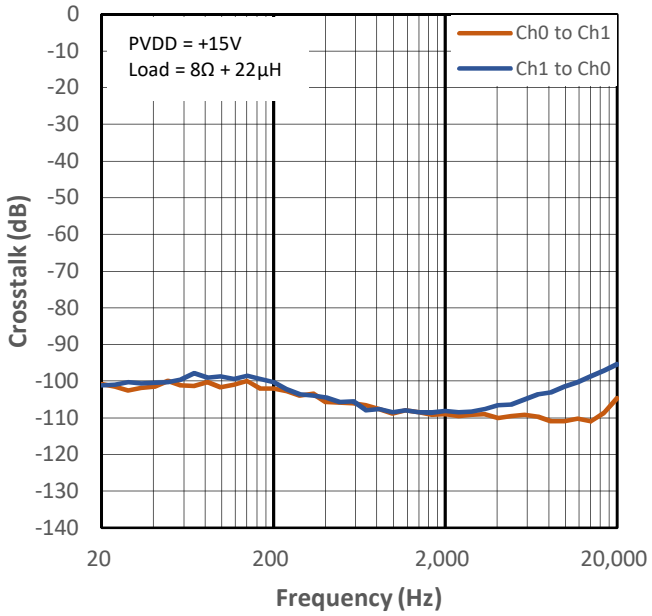


Figure 13-25 Crosstalk vs Frequency for PMP0

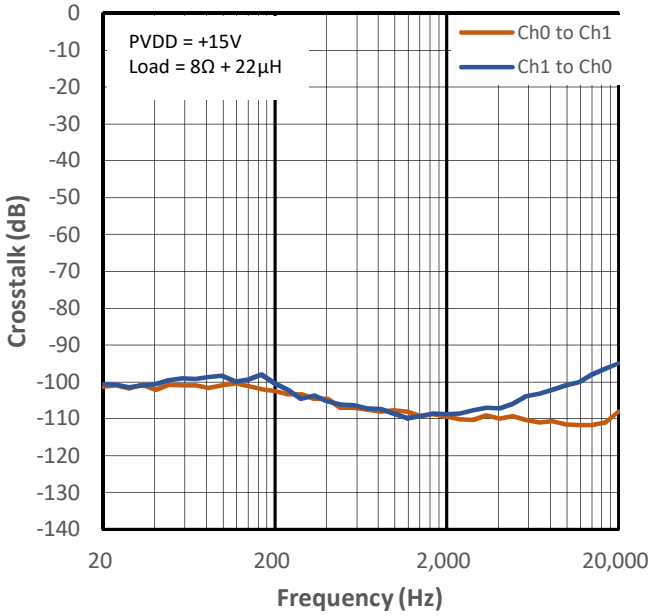


Figure 13-26 Crosstalk vs Frequency for PMP1

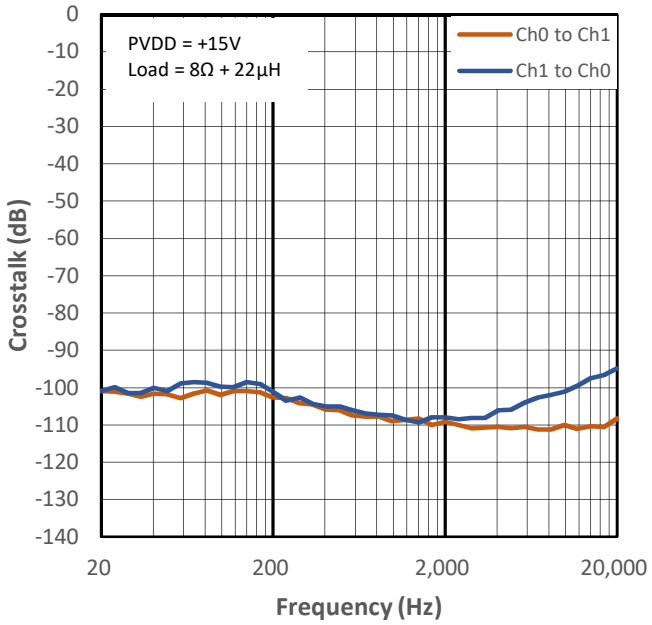


Figure 13-27 Crosstalk vs Frequency for PMP2

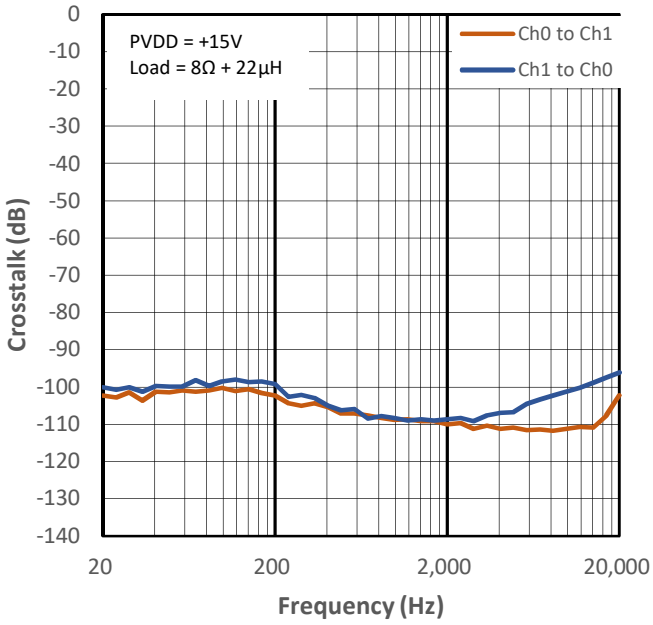


Figure 13-28 Crosstalk vs Frequency for PMP4

14 Typical Characteristics (PVDD = +12V, Load = 4Ω + 22µH)

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

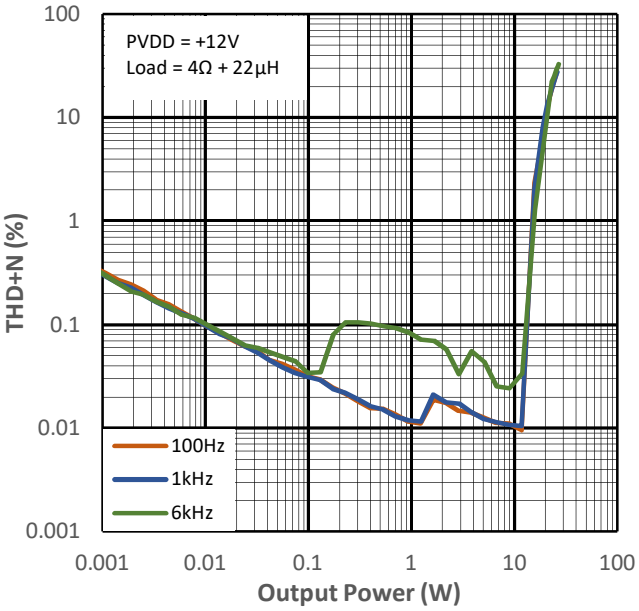


Figure 14-1 THD+N vs. Output Power for PMP0

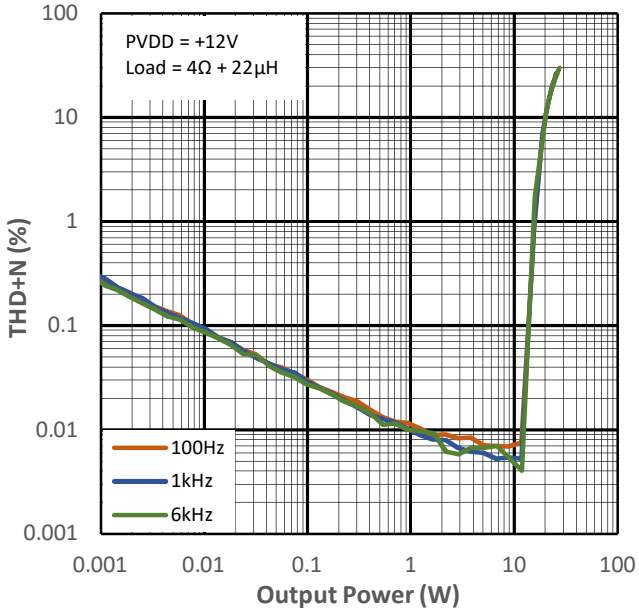


Figure 14-2 THD+N vs. Output Power for PMP1

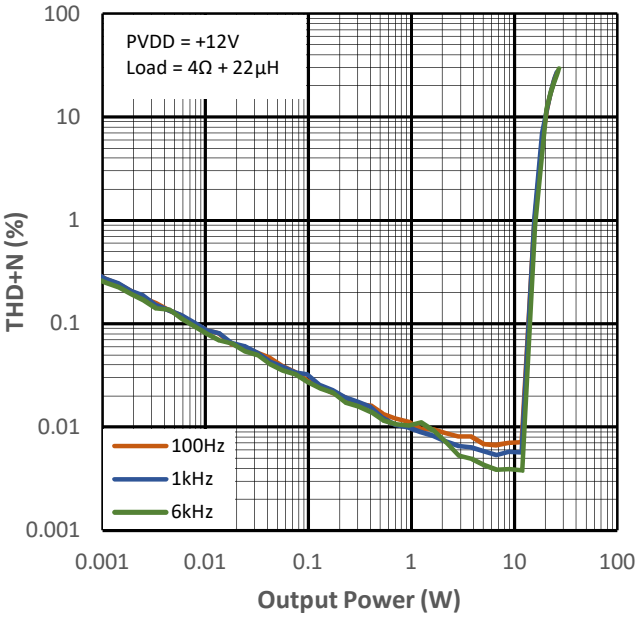


Figure 14-3 THD+N vs. Output Power for PMP2

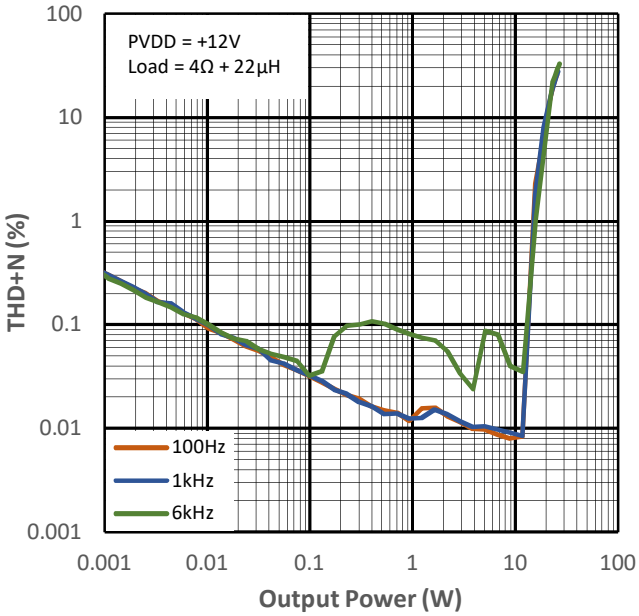


Figure 14-4 THD+N vs. Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

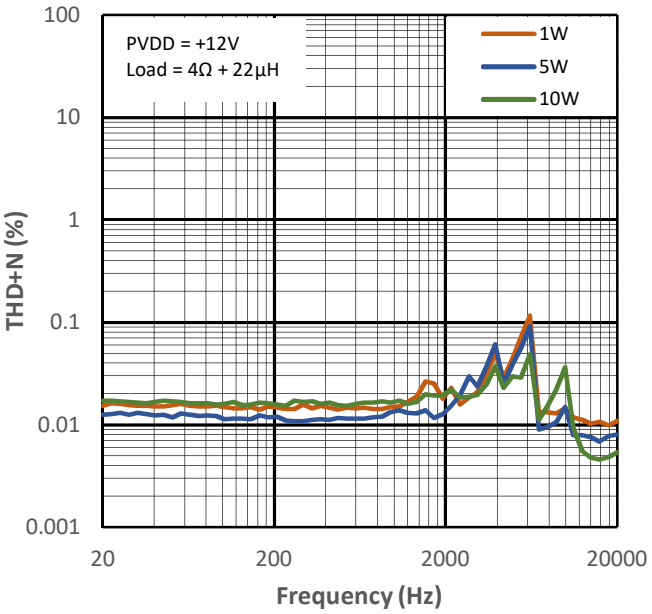


Figure 14-5 THD+N vs Frequency for PMP0

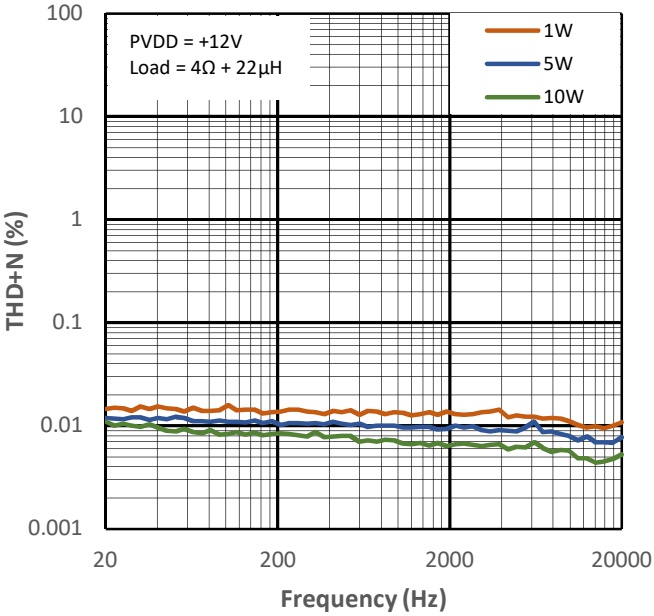


Figure 14-6 THD+N vs Frequency for PMP1

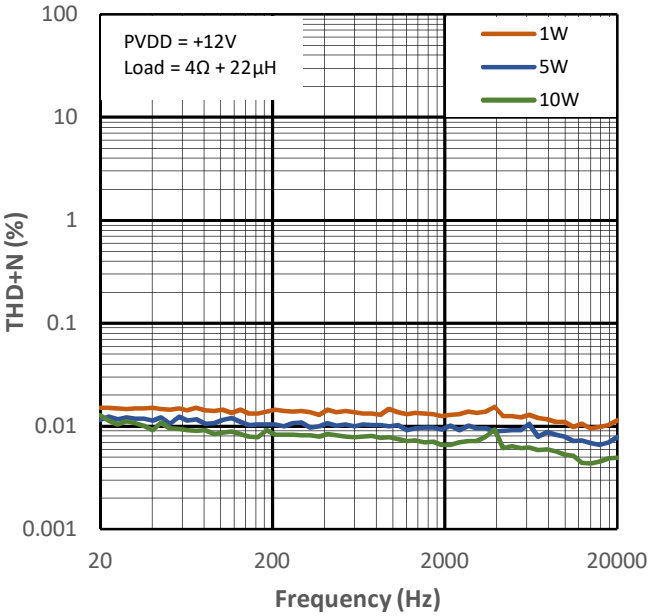


Figure 14-7 THD+N vs Frequency for PMP2

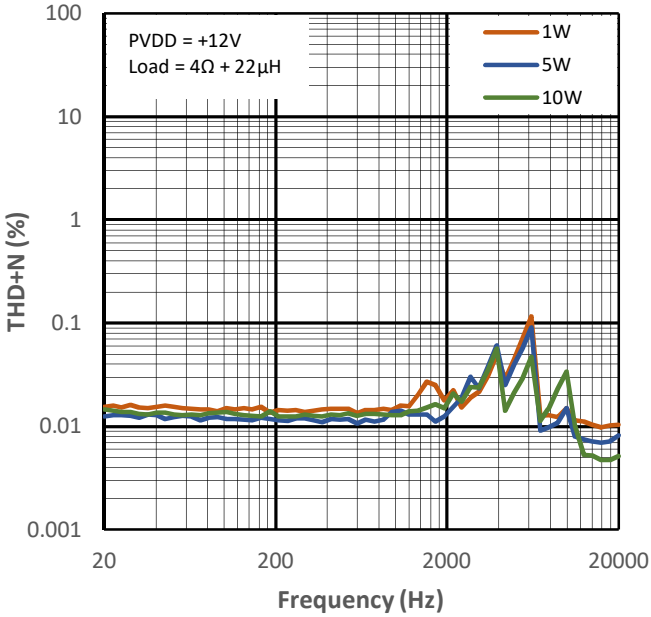


Figure 14-8 THD+N vs Frequency for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

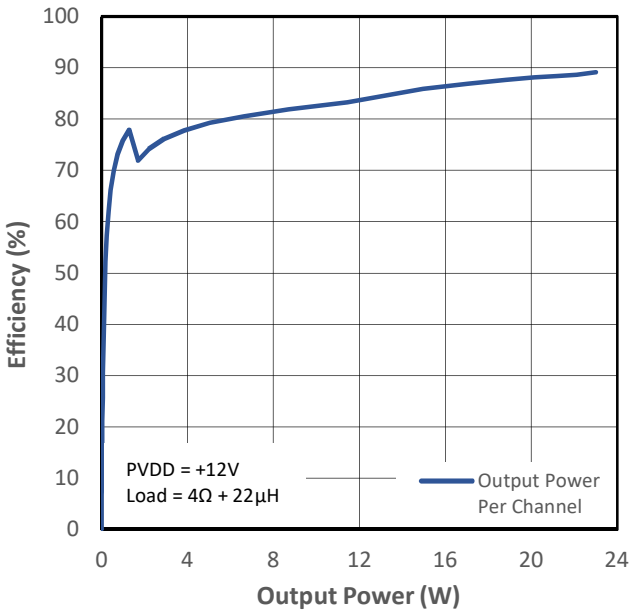


Figure 14-9 PMP0 Efficiency (VDD+PVDD) vs Output Power

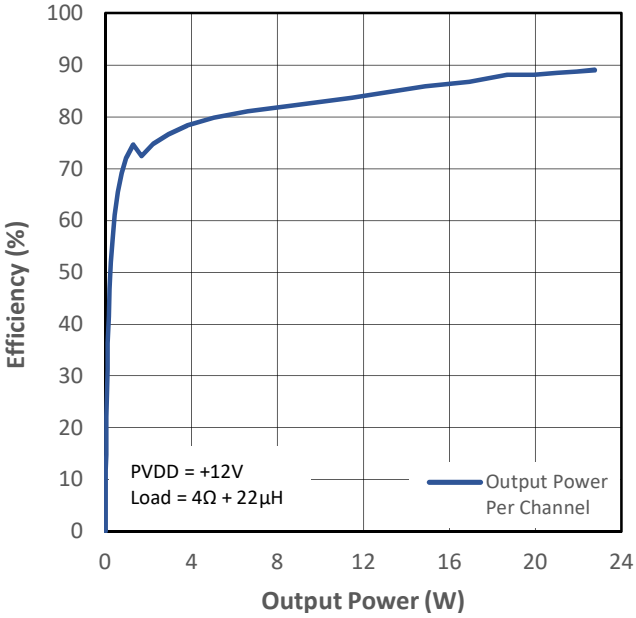


Figure 14-10 PMP1 Efficiency (VDD+PVDD) vs Output Power

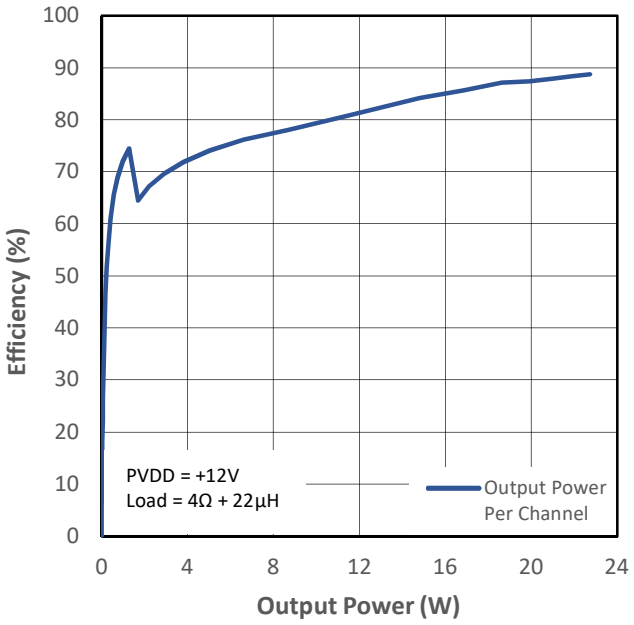


Figure 14-11 PMP2 Efficiency (VDD+PVDD) vs Output Power

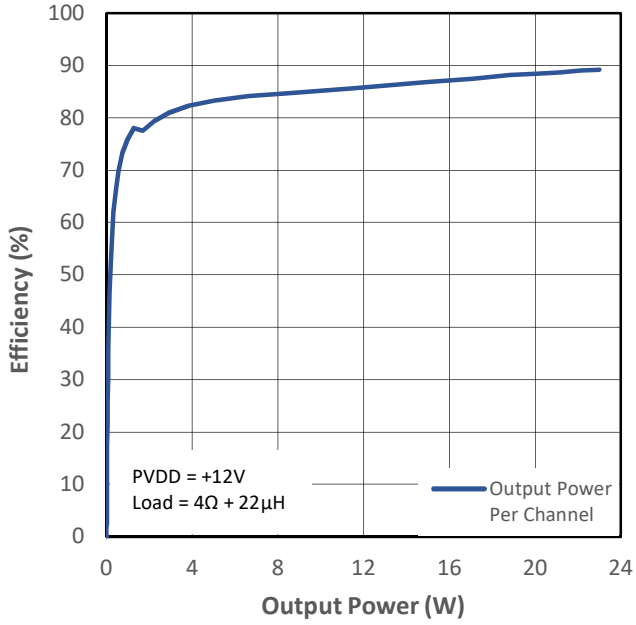


Figure 14-12 PMP4 Efficiency (VDD+PVDD) vs Output Power

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

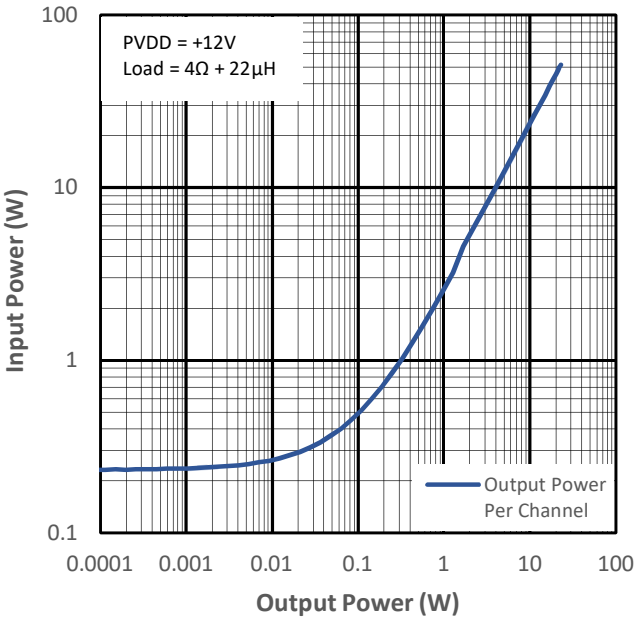


Figure 14-13 Input Power vs Output Power for PMP0

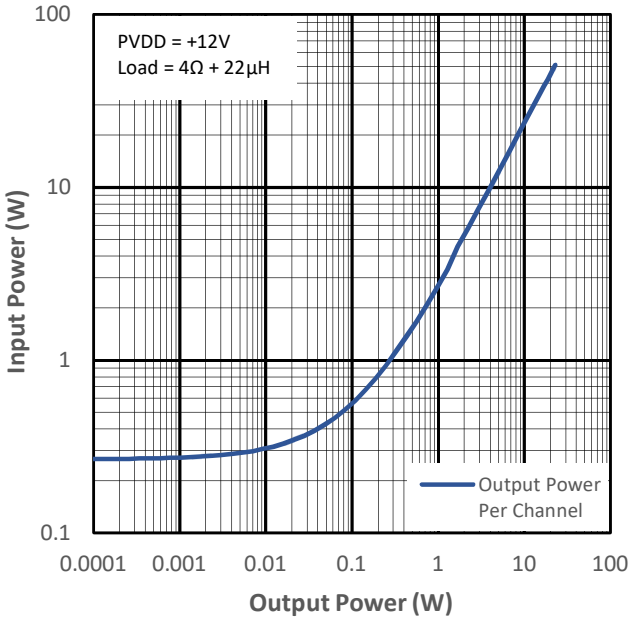


Figure 14-14 Input Power vs Output Power for PMP1

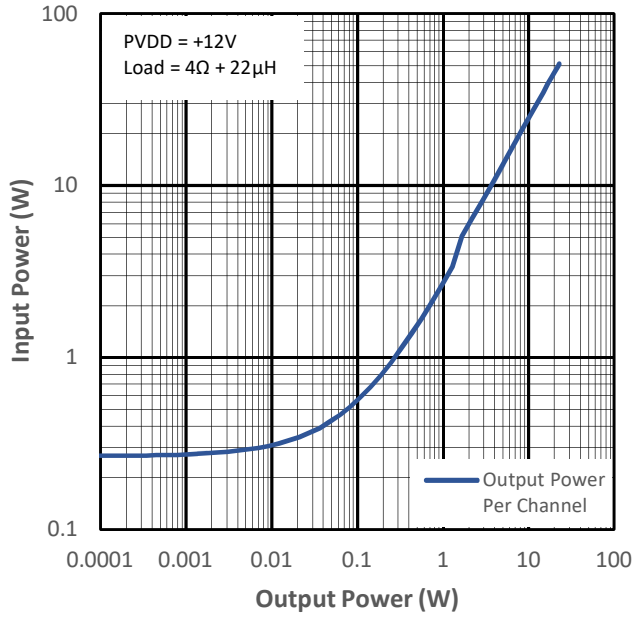


Figure 14-15 Input Power vs Output Power for PMP2

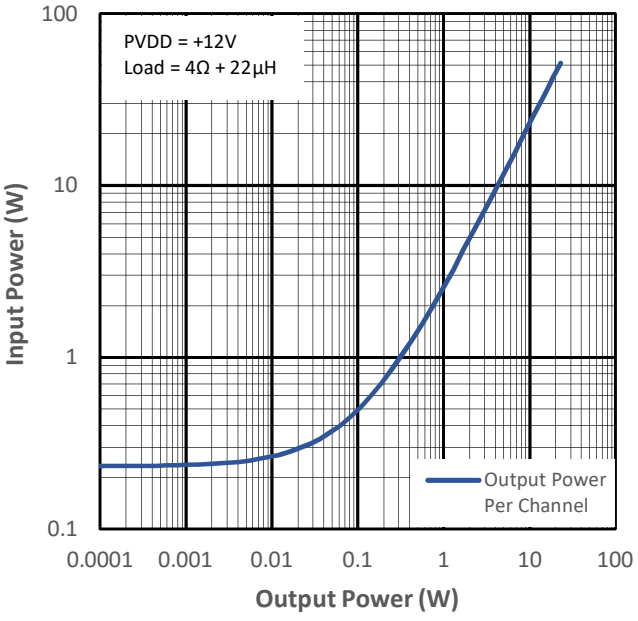


Figure 14-16 Input Power vs Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

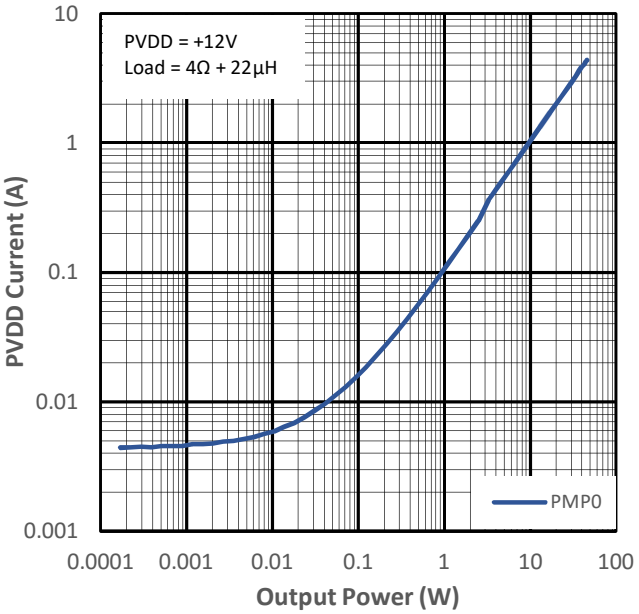


Figure 14-17 PVDD Current vs Output Power for PMP0

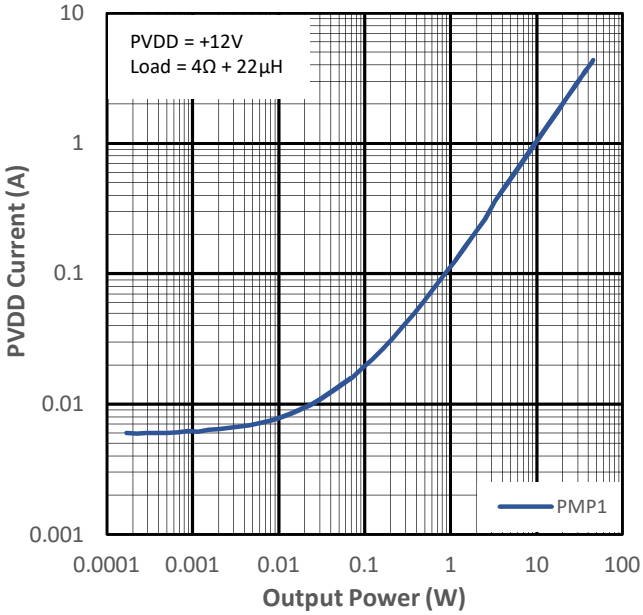


Figure 14-18 PVDD Current vs Output Power for PMP1

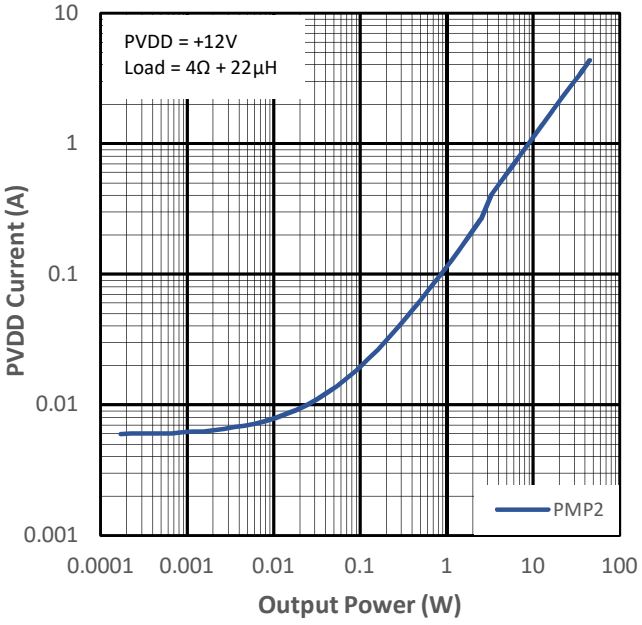


Figure 14-19 PVDD Current vs Output Power for PMP2

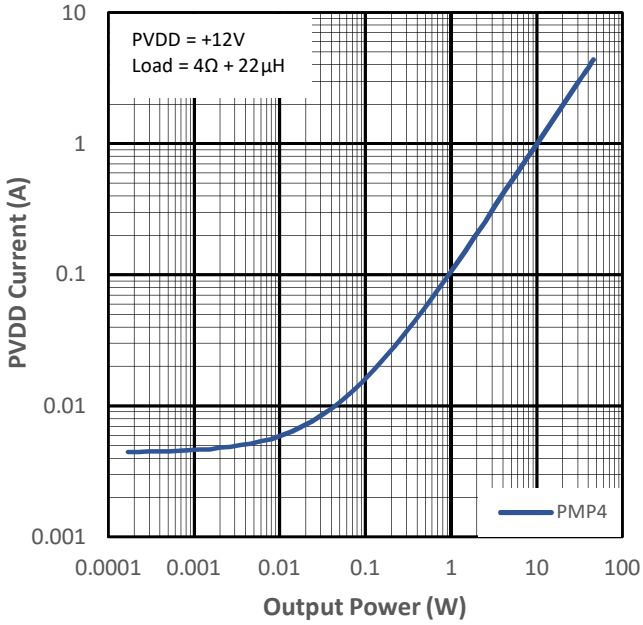


Figure 14-20 PVDD Current vs Output Power for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

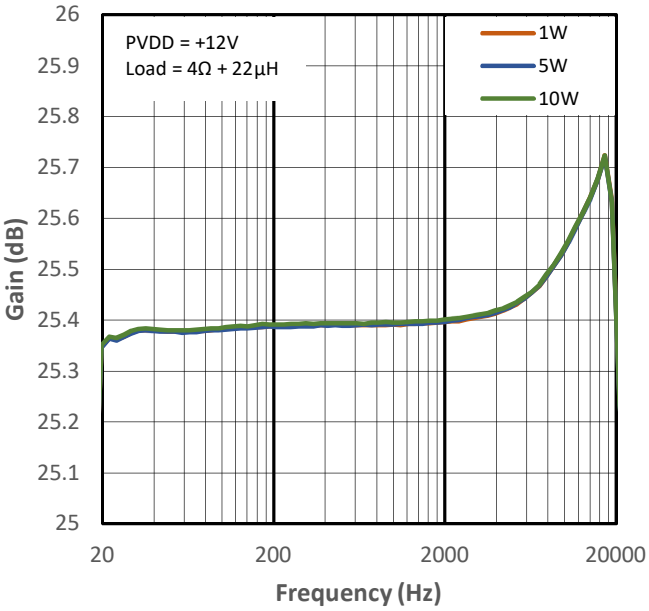


Figure 14-21 Gain vs Frequency for PMP0

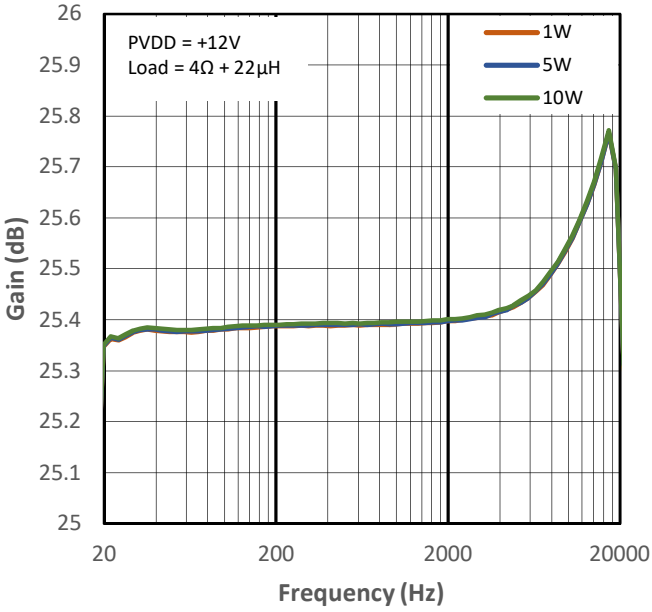


Figure 14-22 Gain vs Frequency for PMP1

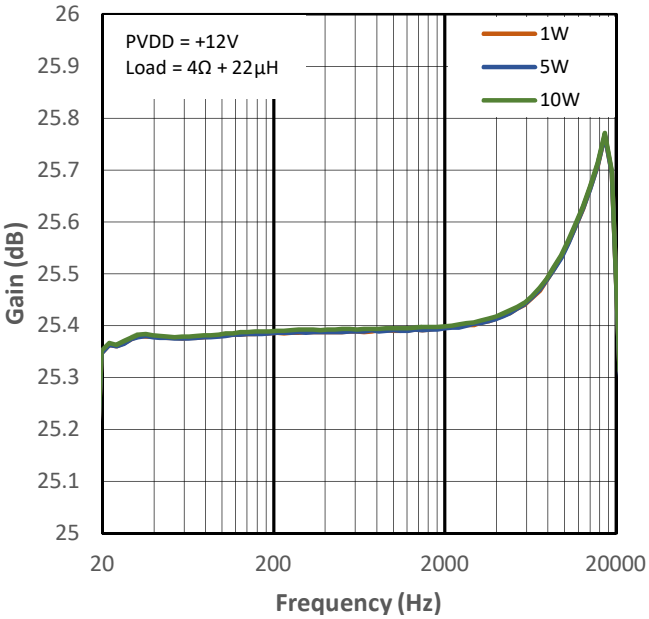


Figure 14-23 Gain vs Frequency for PMP2

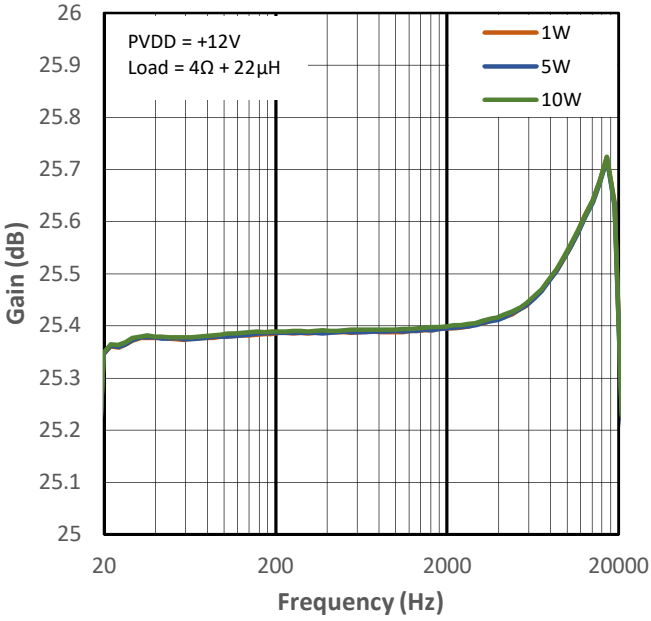


Figure 14-24 Gain vs Frequency for PMP4

BTL configuration; Load = 4Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

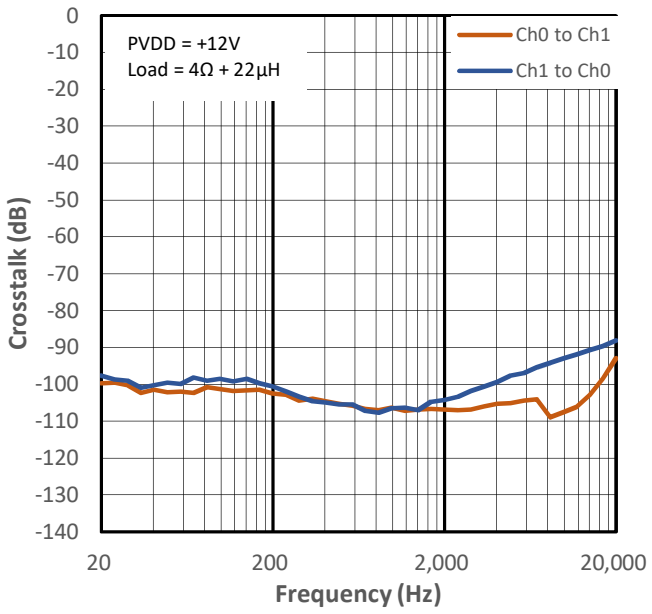


Figure 14-25 Crosstalk vs Frequency for PMP0

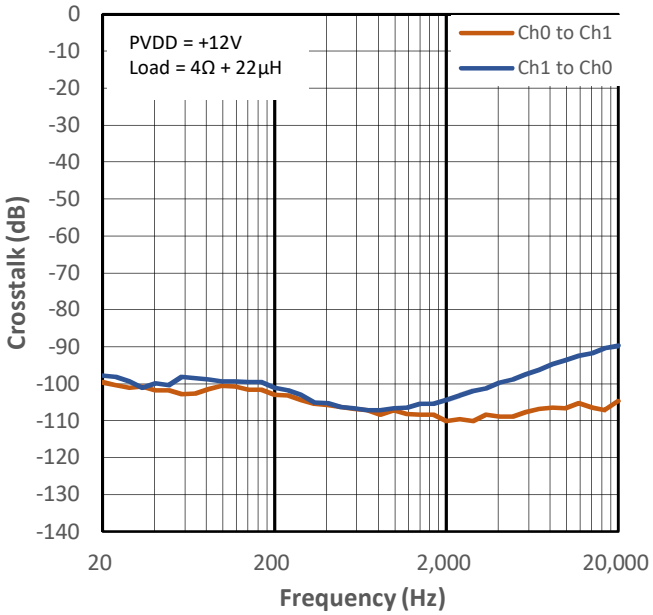


Figure 14-26 Crosstalk vs Frequency for PMP1

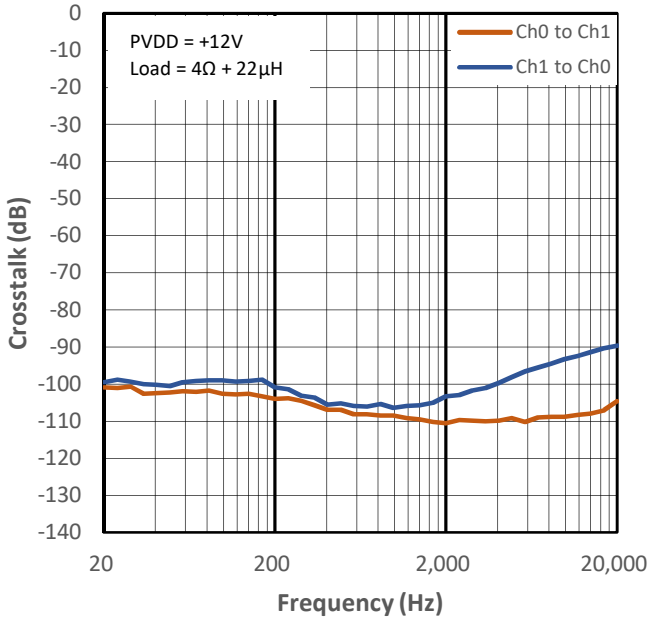


Figure 14-27 Crosstalk vs Frequency for PMP2

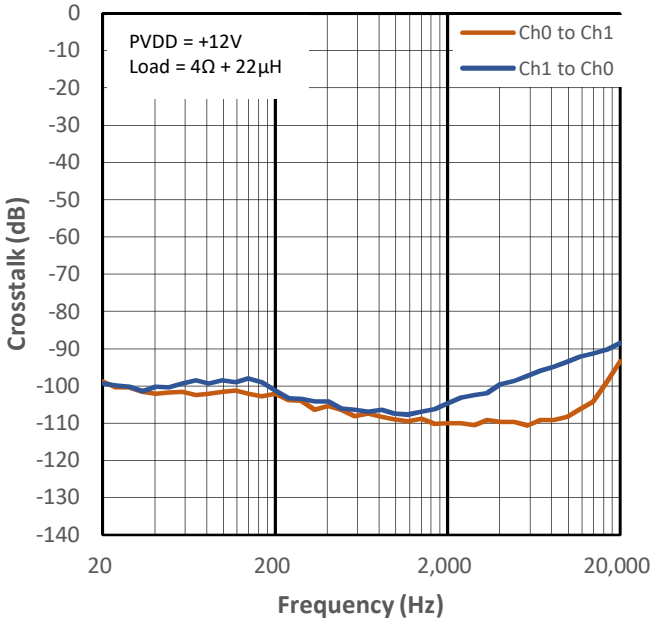


Figure 14-28 Crosstalk vs Frequency for PMP4

15 Typical Characteristics (PVDD = +12V, Load = 8Ω + 22µH)

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

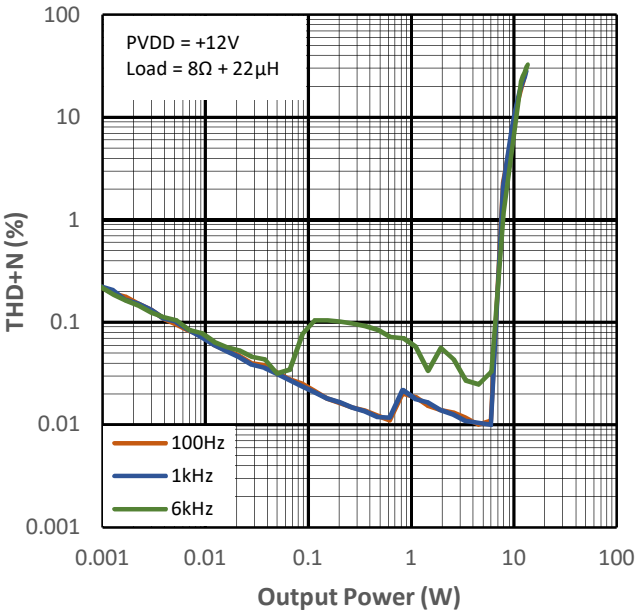


Figure 15-15-1 THD+N vs. Output Power for PMP0

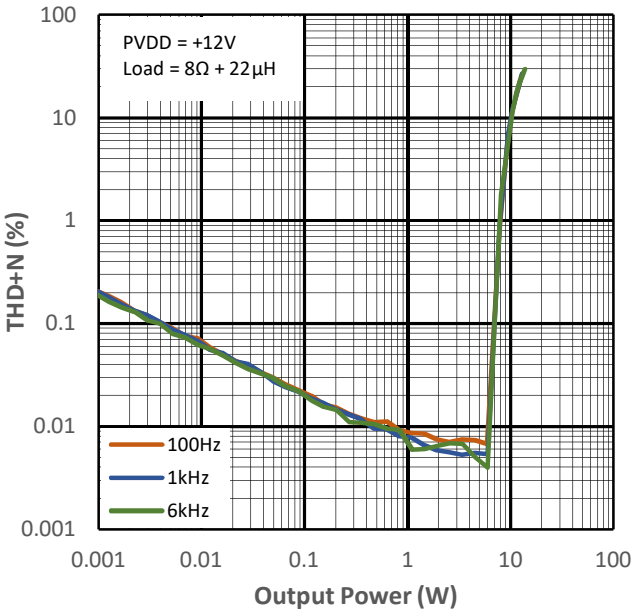


Figure 15-2 THD+N vs. Output Power for PMP1

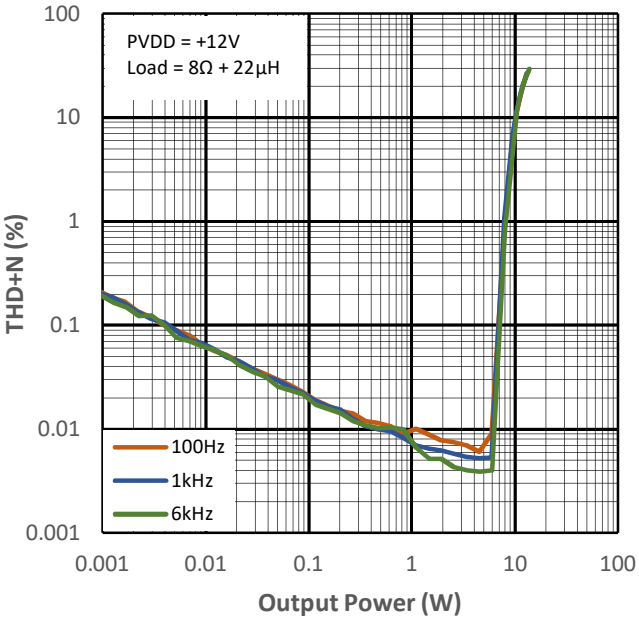


Figure 15-3 THD+N vs. Output Power for PMP2

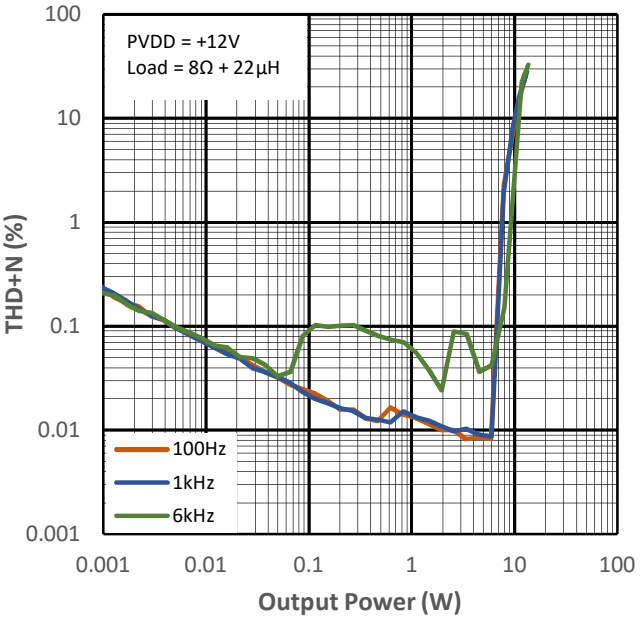


Figure 15-4 THD+N vs. Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

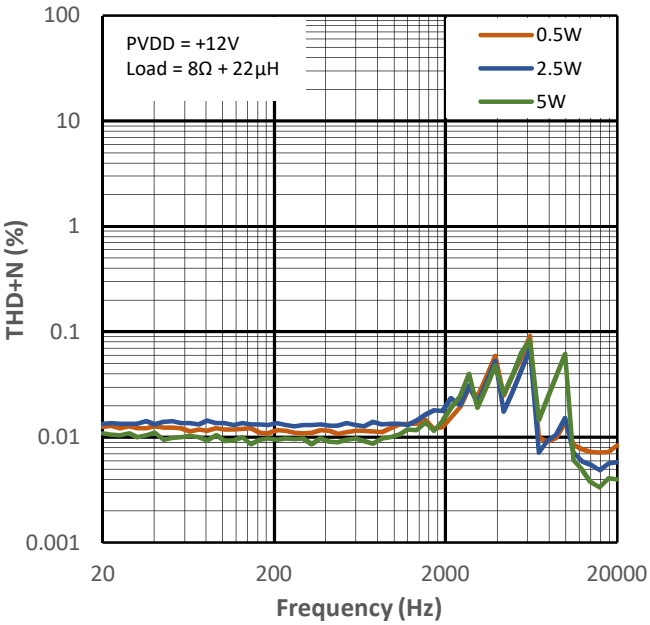


Figure 15-5 THD+N vs Frequency for PMP0

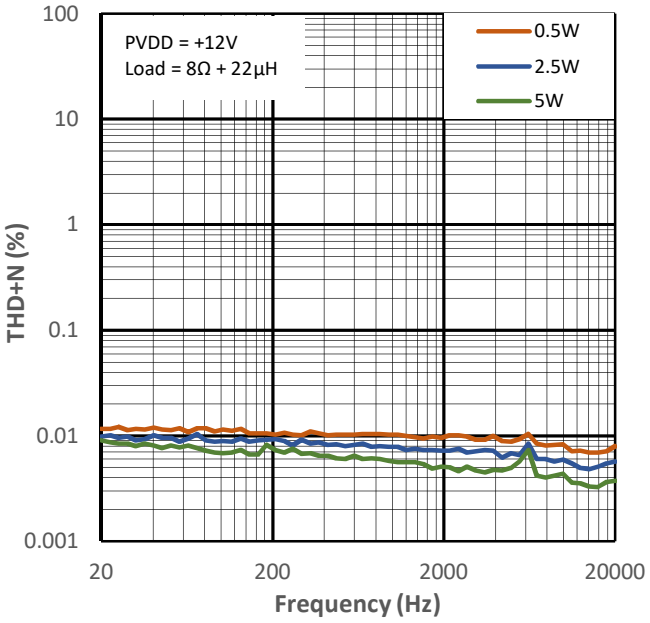


Figure 15-6 THD+N vs Frequency for PMP1

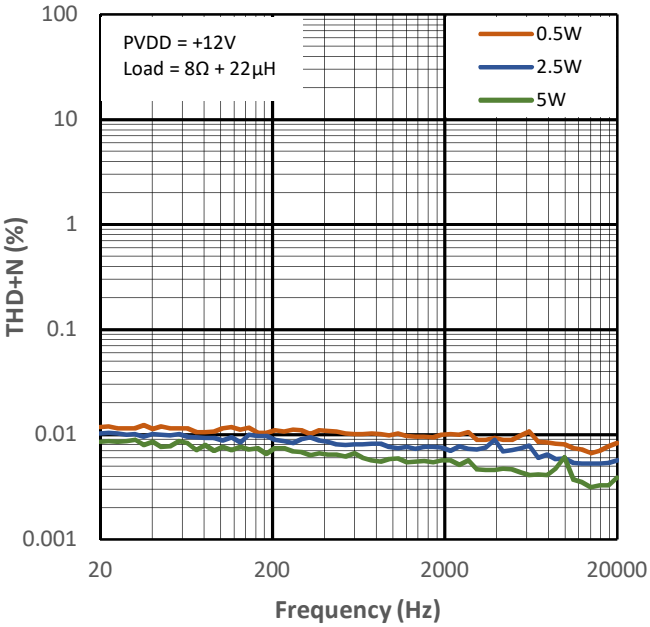


Figure 15-7 THD+N vs Frequency for PMP2

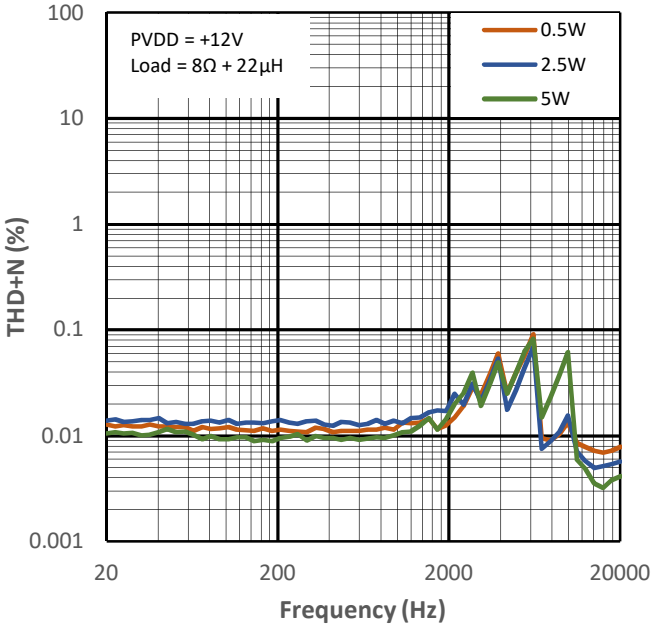


Figure 15-8 THD+N vs Frequency for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

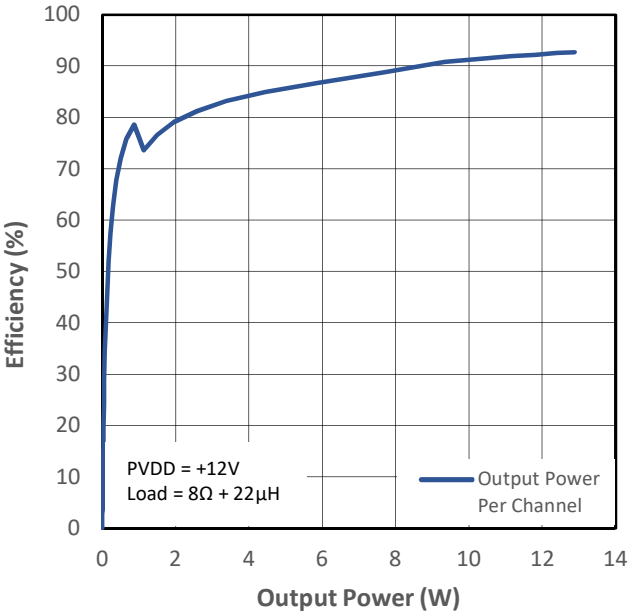


Figure 15-9 PMP0 Efficiency (VDD+PVDD) vs Output Power

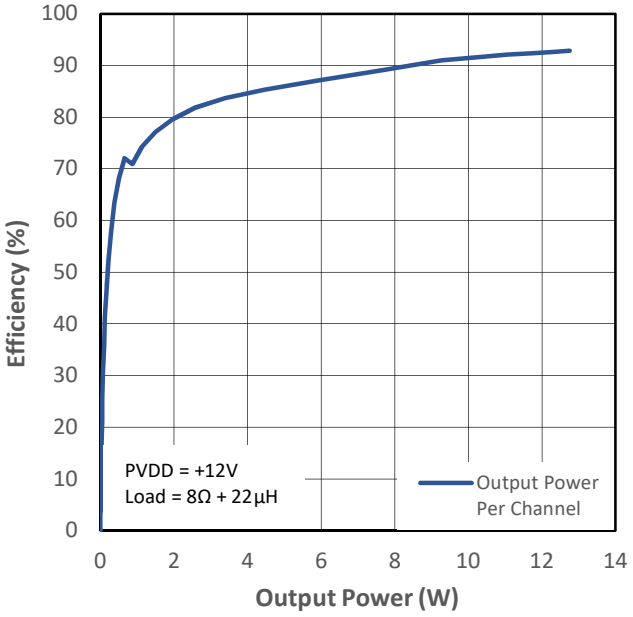


Figure 15-10 PMP1 Efficiency (VDD+PVDD) vs Output Power

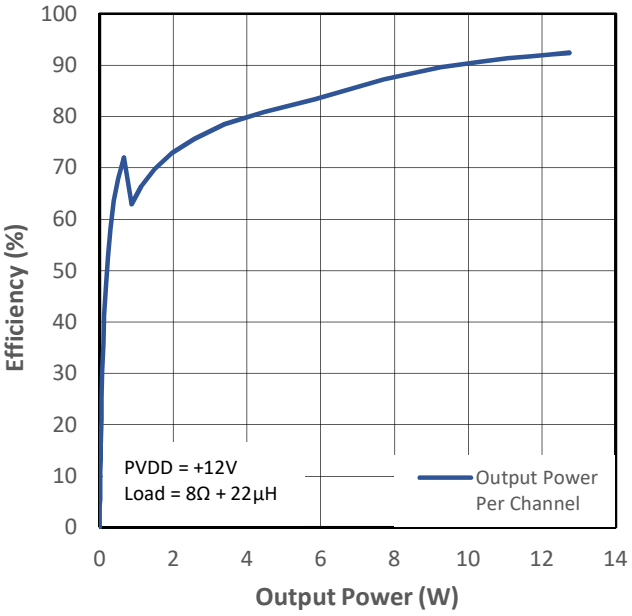


Figure 15-11 PMP2 Efficiency (VDD+PVDD) vs Output Power

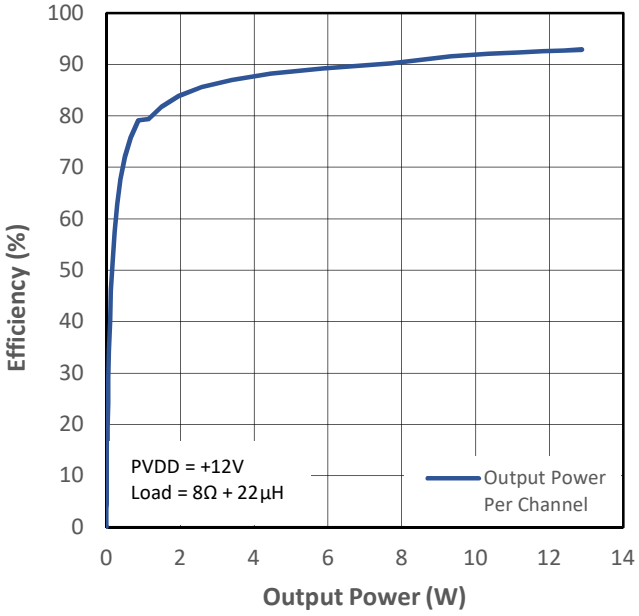


Figure 15-12 PMP4 Efficiency (VDD+PVDD) vs Output Power

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

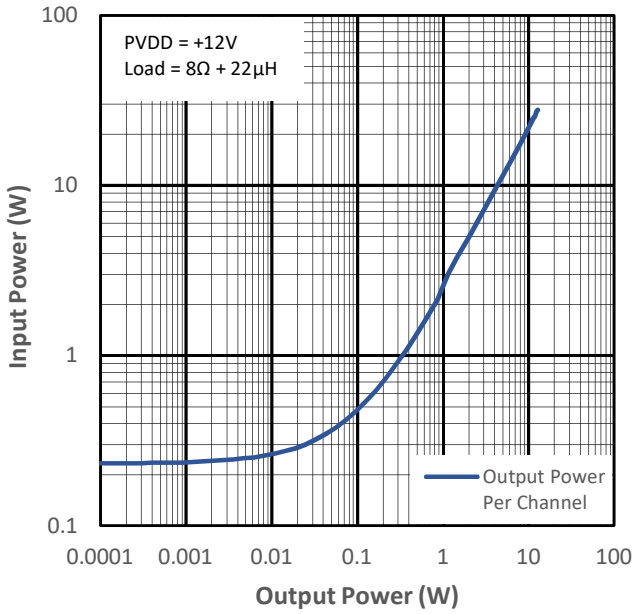


Figure 15-13 Input Power vs Output Power for PMP0

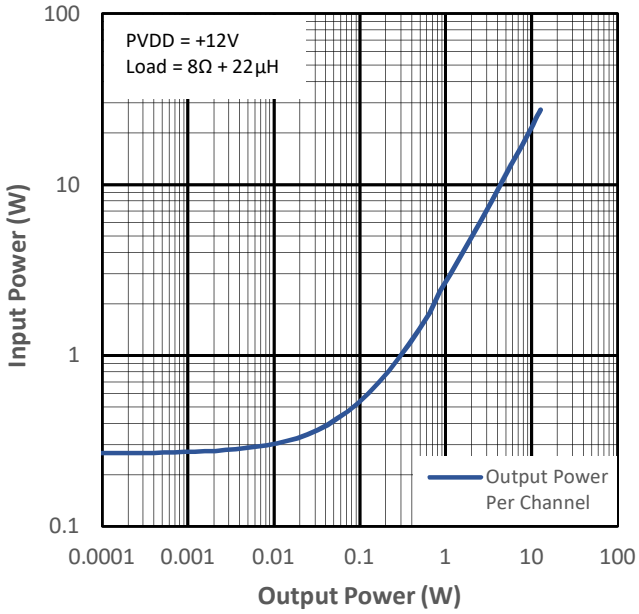


Figure 15-14 Input Power vs Output Power for PMP1

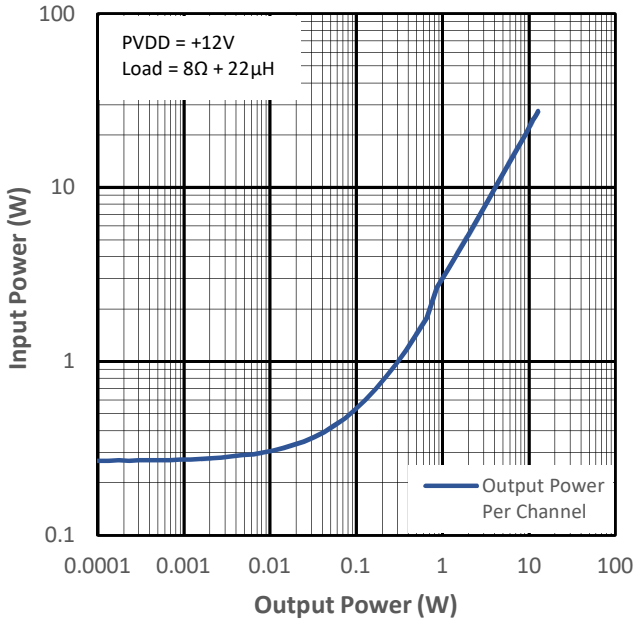


Figure 15-15 Input Power vs Output Power for PMP2

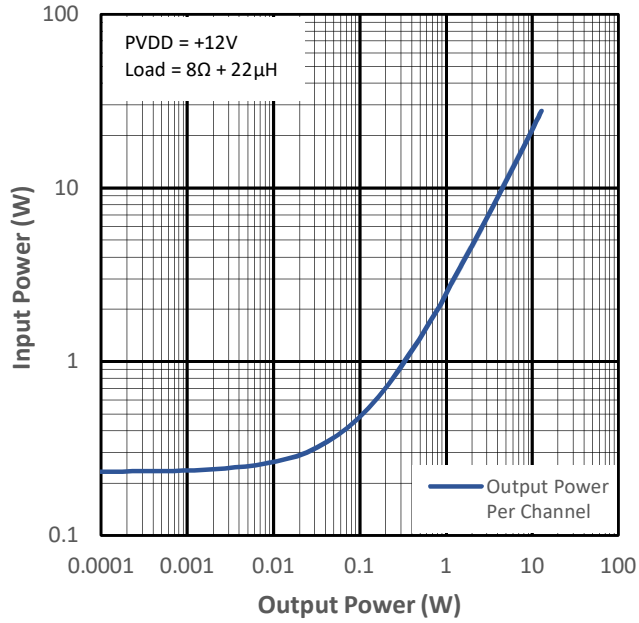


Figure 15-16 Input Power vs Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

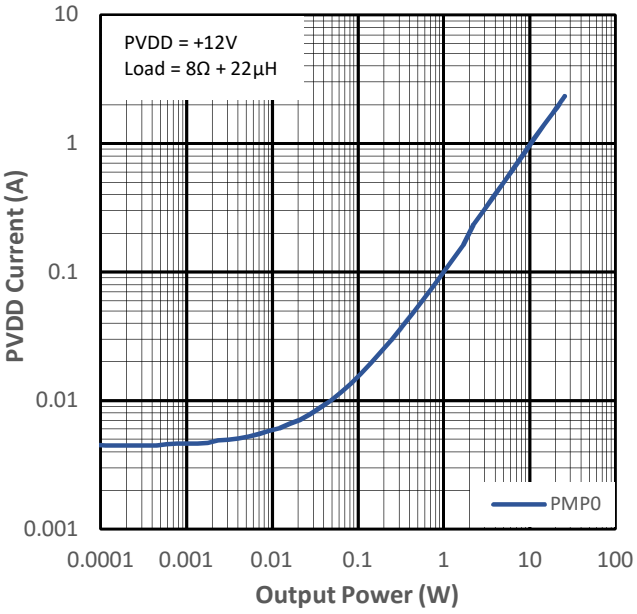


Figure 15-17 PVDD Current vs Output Power for PMP0

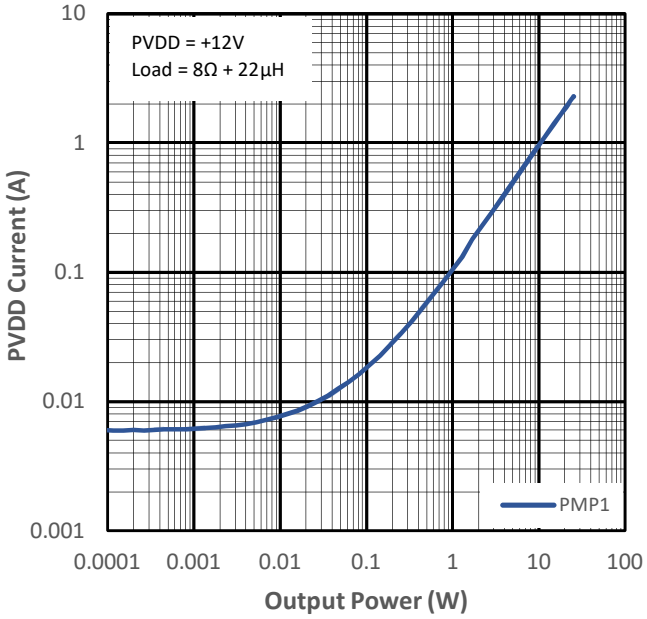


Figure 15-18 PVDD Current vs Output Power for PMP1

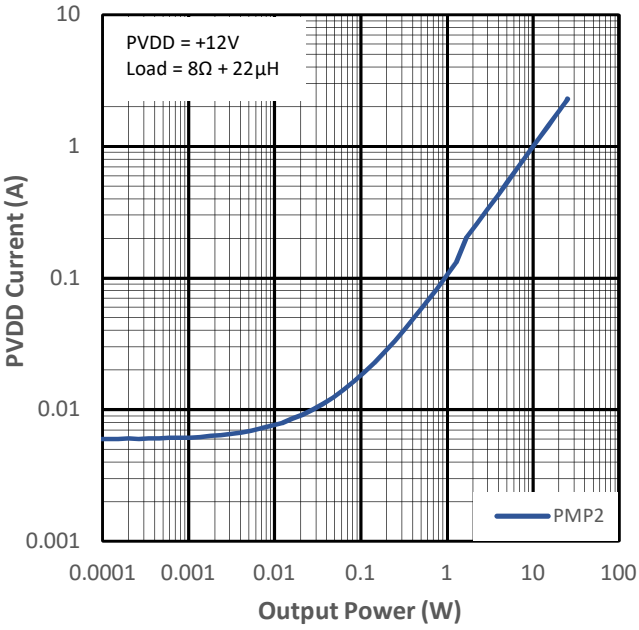


Figure 15-19 PVDD Current vs Output Power for PMP2

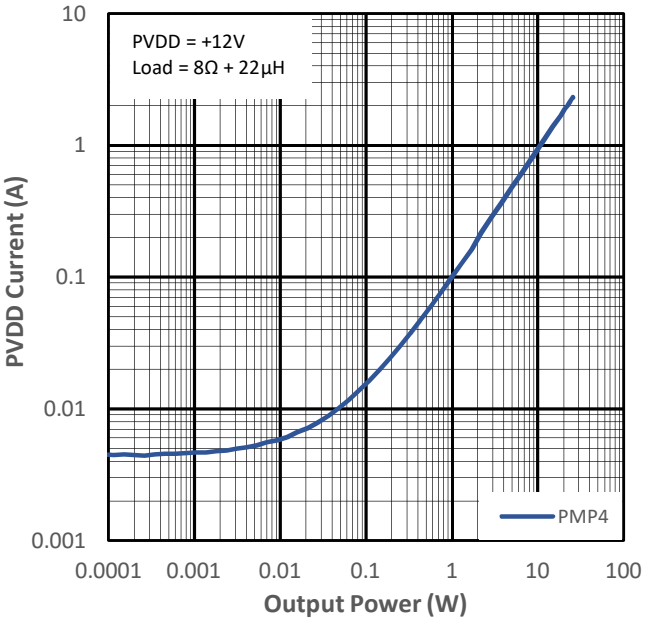


Figure 15-20 PVDD Current vs Output Power for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

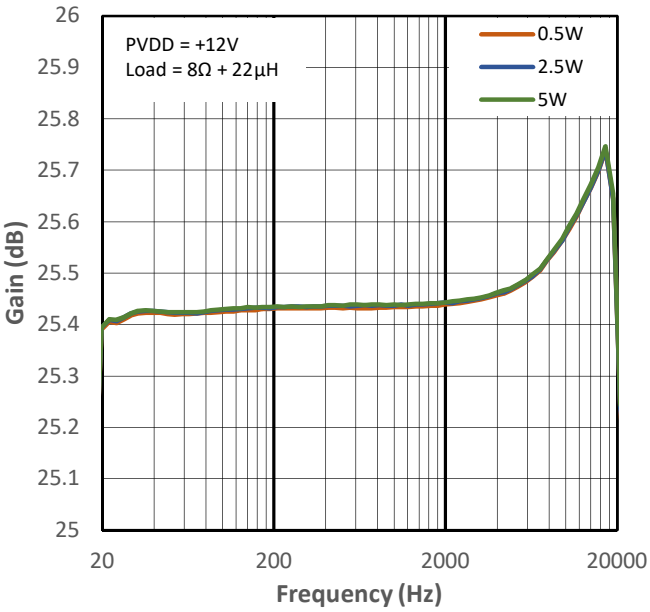


Figure 15-21 Gain vs Frequency for PMP0

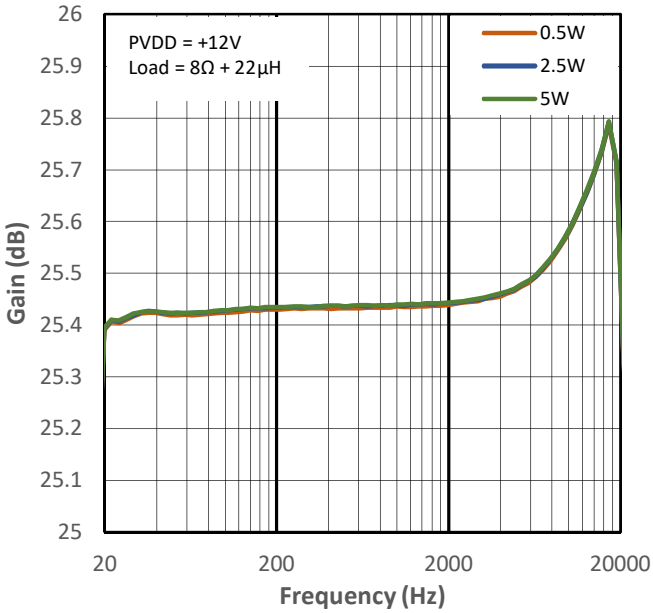


Figure 15-22 Gain vs Frequency for PMP1

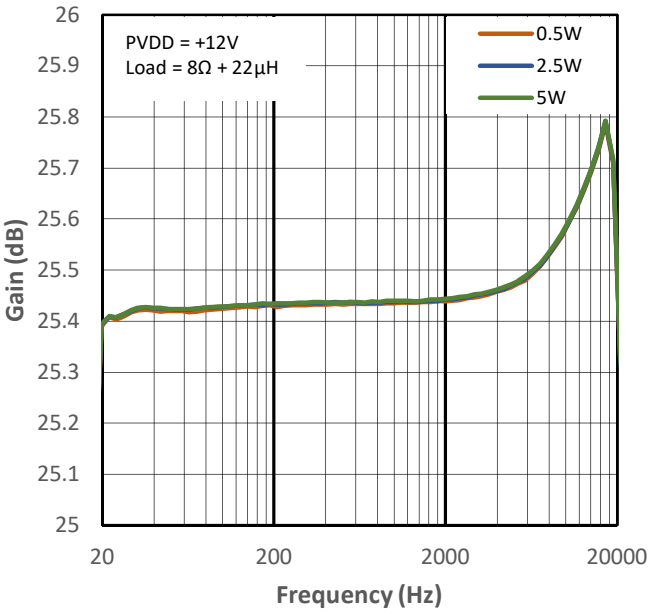


Figure 15-23 Gain vs Frequency for PMP2

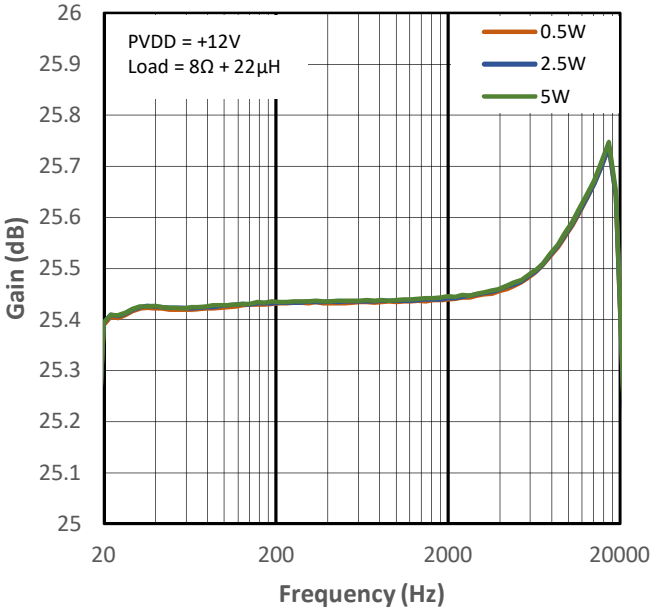


Figure 155-24 Gain vs Frequency for PMP4

BTL configuration; Load = 8Ω + 22µH; Measurements carried out with APx 515 + AUX-0025 input filter; APx uses AES17 brick-wall filter.

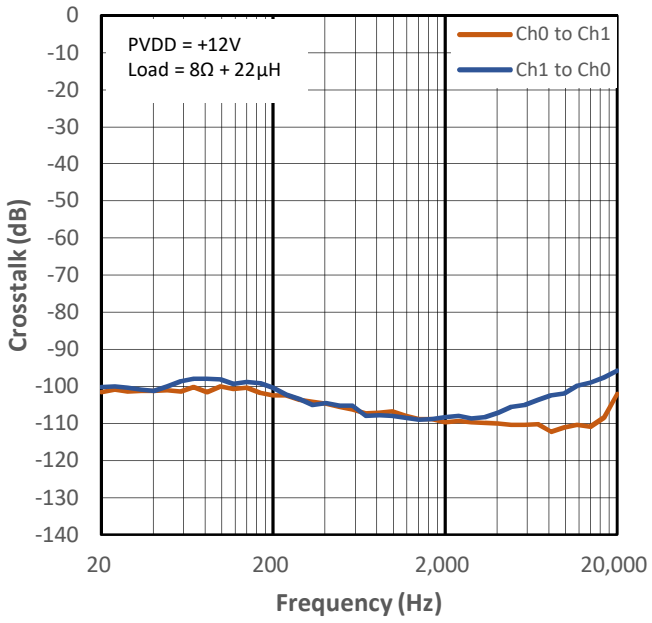


Figure 15-25 Crosstalk vs Frequency for PMP0

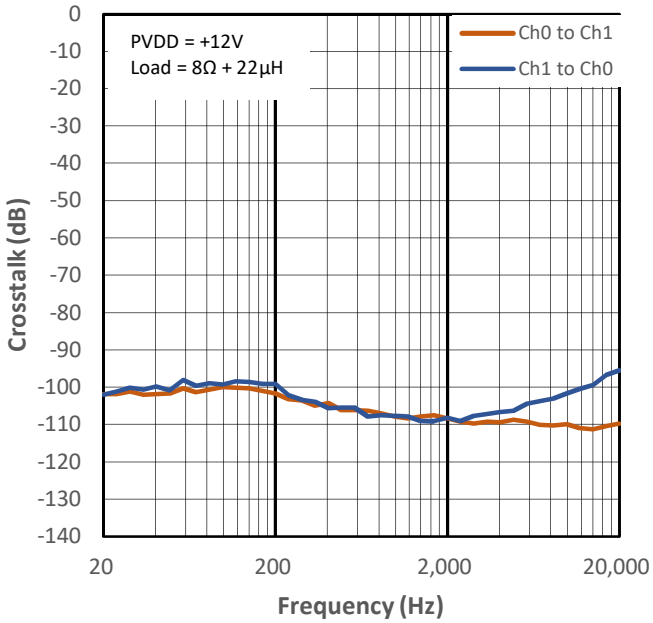


Figure 15-26 Crosstalk vs Frequency for PMP1

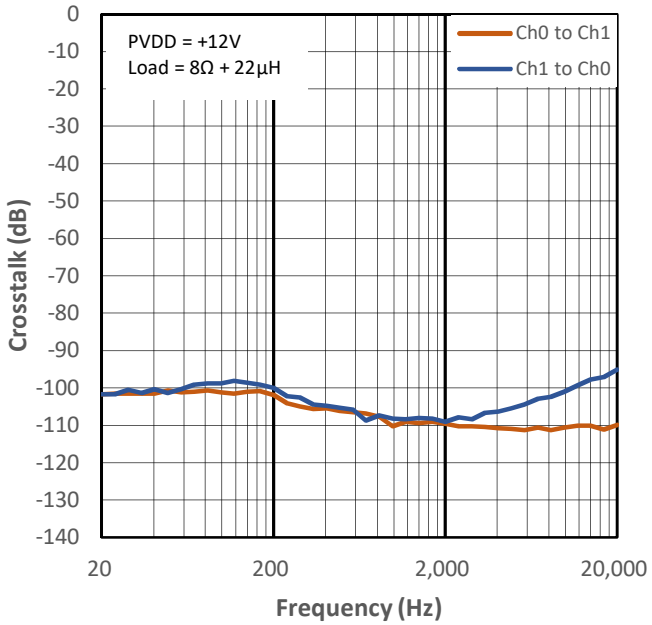


Figure 15-27 Crosstalk vs Frequency for PMP2

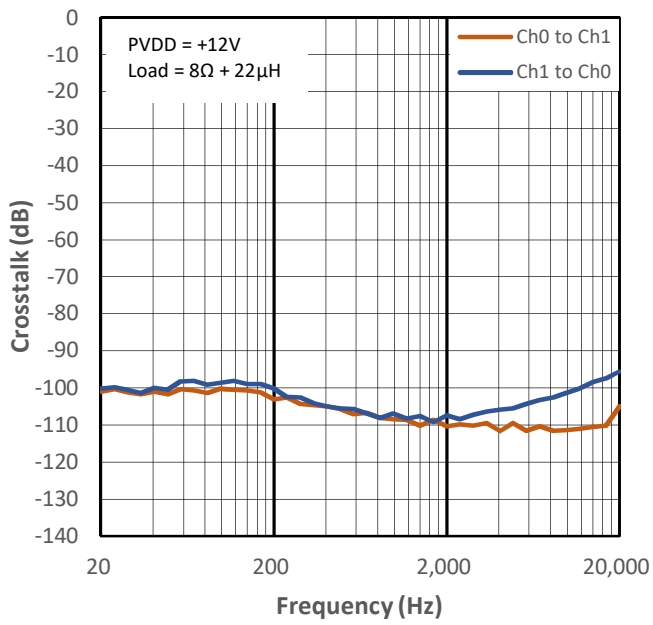


Figure 15-28 Crosstalk vs Frequency for PMP4

16 Register map

For all register map:

" f " : Don't Care condition

" – " : Reserved bits configured during factory settings.

Read / Write Access (Power Mode Settings):

Address	Default Address Value	Description	Name	Bit(s)	Value	Function
0x00	0x3D	Power Mode Control	manualPM	6	- 0 1 1 - - - -	Select manual Power Mode control. Default the device will operate in automatic Power Mode control. This bit can be set to 1 if manual Power Mode control is required.
			PM_man	5:4	- 0 1 1 - - - -	Manual selected power mode. These two bits can be used selecting the Power Mode of the device when it is in manual Power Mode control.
					- - 0 0 - - - -	*Reserved*
					- - 0 1 - - - -	*Power Mode 1*
					- - 1 0 - - - -	*Power Mode 2*
					- - 1 1 - - - -	*Power Mode 3*
0x01	0x3C	Threshold for Power Mode change PM1=>PM2	Mthr_1to2	7:0	0 0 1 1 1 1 0 0	Threshold value for PM1=>PM2 change. This value will set the threshold for when automatic Power Mode changes from PM1 to PM2. It can be programmed from 0 - 255; this maps to 0 output power – max output power.
0x02	0x32	Threshold for Power Mode change PM2=>PM1	Mthr_2to1	7:0	0 0 1 1 0 0 1 0	Threshold value for PM2=>PM1 change. This value will set the threshold for when automatic Power Mode changes from PM2 to PM1. It can be programmed from 0 - 255; this maps to 0 output power – max output power.
0x03	0x5A	Threshold for Power Mode change PM2=>PM3	Mthr_2to3	7:0	0 1 0 1 1 0 1 0	Threshold value for PM2=>PM3 change. This value will set the threshold for when automatic Power Mode changes from PM2 to PM3. It can be programmed from 0 - 255; this maps to 0 output power – max output power.
0x04	0x50	Threshold for Power Mode change PM3=>PM2	Mthr_3to2	7:0	0 1 0 1 0 0 0 0	Threshold value for PM3=>PM2 change. This value will set the threshold for when automatic Power Mode changes from PM3 to PM2. It can be programmed from 0 - 255; this maps to 0 output power – max output power.
0x0A	0xC	Soft-clipping and over-current protection latching	lf_clamp_en	7	0 - - - - - 0 -	Enables soft-clipping. High to enable. Low to disable.
			ocp_latch_en	1	0 - - - - - 0 -	High to use permanently latching OCP.

Read / Write Access (Power Mode Profile Settings):

Address	Default Address Value	Description	Name	Bit(s)	Value	Function
0x1D	0x00	Select Power Mode Profile setting	PMprofile	2:0	f f f f f 0 0 0	Power Mode Profile select. With this register the user can selects the appropriate Power Mode Profile.
					- - - - - 0 0 0	*Power Mode Profile 0*
					- - - - - 0 0 1	*Power Mode Profile 1*
					- - - - - 0 1 0	*Power Mode Profile 2*
					- - - - - 0 1 1	*Power Mode Profile 3*
					- - - - - 1 0 0	*Power Mode Profile 4*
0x1E	0x2F	Power Mode Profile configuration	PM3_man	5:4	f f 1 0 - - - -	Custom profile PM3 content
					- - 0 0 - - - -	*Assign scheme A to PM3*
					- - 0 1 - - - -	*Assign scheme B to PM3*
					- - 1 0 - - - -	*Assign scheme C to PM3*
					- - 1 1 - - - -	*Assign scheme D to PM3*
			PM2_man	3:2	f f - - 1 1 - -	Custom profile PM2 content
					- - - - 0 0 - -	*Assign scheme A to PM2*
					- - - - 0 1 - -	*Assign scheme B to PM2*
					- - - - 1 0 - -	*Assign scheme C to PM2*
					- - - - 1 1 - -	*Assign scheme D to PM2*
			PM1_man	1:0	f f - - - - 1 1	Custom profile PM1 content
					- - - - - - 0 0	*Assign scheme A to PM1*
					- - - - - - 0 1	*Assign scheme B to PM1*
					- - - - - - 1 0	*Assign scheme C to PM1*
					- - - - - - 1 1	*Assign scheme D to PM1*
0x20	0x1F	Over-current protection latch clear	ocp_latch_clear	7	0 - - - - - - -	Clears over current protection latch. A low to high toggle clears the current OCP latched condition.
0x25	0x10	Audio in mode	audio_in_mode	6:5	- 0 0 - - - - -	Audio input mode. Sets the input mode of the amplifier. This means the amplifier overall gain setting.
					- 0 0 - - - - -	*Audio in mode 0: 20dB gain*
					- 0 1 - - - - -	*Audio in mode 1: 26dB gain*
0x26	0x05	DC protection	Eh_dcShdn	2	f f f f - 1 - -	Enables or disables DC protection. High to enable. Low to disable.
0x27	0x08	Audio in mode overwrite	audio_in_mode_ext	5	0 0 0 0 - 0 - -	Enables audio in mode default overwrite. High to enable. Low to disable. Should enabled for address 0x25 to have effect.
0x2D	0x30	Error handler clear	eh_clear	2	- - 0 - - 0 - -	Clears error handler. A low-to-high-to-low toggle clears the error handler.

Read / Write Access (I2S format configuration)

Address	Default Address Value	Description	Name	Bit(s)	Value	Function
0x35	0x01	PCM word format	i2s_format	2:0	0 0 0 0 0 0 0 0	i2s standard
					0 0 0 0 0 0 0 1	Left justified
					0 0 0 0 0 1 0 0	Right justified **16bits**
					0 0 0 0 0 1 1 0	Right justified **18bits**
					0 0 0 0 0 0 0 0	Right justified **20bits**
					0 0 0 0 0 1 1 1	Right justified **24bits**
0x36	0x01	Left/right order of PCM words	i2s_rightfirst	5	0 0 0 0 0 0 0 1	**Left** PCM data word (of a simultaneously sampled PCM data pair) is send first
					0 0 0 1 0 0 0 1	**Right** PCM data word (of a simultaneously sampled PCM data pair) is send first
		Number of data bits per frame	i2s_framesize	4:3	0 0 0 0 0 0 0 1	**64** serial clock (SCK) cycles are present in each period of the word select signal (WS)
					0 0 0 0 1 0 0 1	**48** serial clock (SCK) cycles are present in each period of the word select signal (WS)
					0 0 0 1 0 0 0 1	**32** serial clock (SCK) cycles are present in each period of the word select signal (WS)
		Bit order of PCM data words	i2s_order	2	0 0 0 0 0 0 0 1	**Most** significant bit of the PCM data word is transmitted first
					0 0 0 0 0 1 0 1	**Least** significant bit of the PCM data word is transmitted first
		Pairing of data words	i2s_ws_pol	1	0 0 0 0 0 0 0 1	First word of a simultaneously sampled PCM data pair is transmitted while word select (WS) is **low**
					0 0 0 0 0 0 1 1	First word of a simultaneously sampled PCM data pair is transmitted while word select (WS) is **high**
		Clocking edge of the serial clock signal (SCK)	i2s_sck_pol	0	0 0 0 0 0 0 0 0	Serial data (SDX) and word select (WS) are changing at **rising** edge of the serial clock signal (SCK). The MA12040P will capture data at the falling edge of the serial clock signal SCK
					0 0 0 0 0 0 0 1	Serial data (SDX) and word select (WS) are changing at **falling** edge of the serial clock signal (SCK). The MA12040P will capture data at the rising edge of the serial clock signal SCK

Read / Write Access (Volume control and limiter)

Address	Default Address Value	Description	Name	Bit(s)	Value	Function
0x35	0x01	Limiter attack time control	audio_proc_release	7:6	0 0 0 0 0 0 0 1	**Slow** attack time
					0 1 0 0 0 0 0 1	**Normal** attack time
					1 0 0 0 0 0 0 1	**Fast** attack time
		Limiter release time	audio_proc_attack	5:4	0 0 0 0 0 0 0 1	**Slow** release time
					0 0 0 1 0 0 0 1	**Normal** release time
					0 0 1 0 0 0 0 1	**Fast** release time
		Processor bypass mux	audio_proc_enable	3	0 0 0 0 0 0 0 1	Bypass the audio processor
					0 0 0 0 1 0 0 1	Use the audio processor
0x36	0x01	Mute mux control	audio_proc_mute	7	1 0 0 0 0 0 0 1	Mute audio
					0 0 0 0 0 0 0 1	Play audio
		Limiter bypass mux	audio_proc_limiterEnable	6	0 0 0 0 0 0 0 1	Bypass the limiter
					0 1 0 0 0 0 0 1	Use the limiter
0x40	0x18	Master integer dB volume	vol_db_master	7:0	0 0 0 1 1 0 0 0	Control of integer value master dB volume (see Table 8-9 for mapping overview)
0x41	0x00	Master fract dB volume	vol_lsb_master	1:0	f f f f f f 0 0	Control of fractional value dB volume (see Table 8-9 for mapping overview)
0x42	0x18	Ch0L integer dB volume	vol_db_ch0	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0L dB volume (see Table 8-9 for mapping overview)
0x43	0x18	Ch0R integer dB volume	vol_db_ch1	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0R dB volume (see Table 8-9 for mapping overview)
0x44	0x18	Ch1L integer dB volume	vol_db_ch2	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0L dB volume (see Table 8-9 for mapping overview)
0x45	0x18	Ch1R integer dB volume	vol_db_ch3	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0R dB volume (see Table 8-9 for mapping overview)
0x46	0x00	Ch0L fract dB volume	vol_lsb_ch0	1:0	0 0 0 0 0 0 0 0	Control of fractional value ch0L dB volume (see Table 8-9 for mapping overview)
		Ch0R fract dB volume	vol_lsb_ch1	3:2	0 0 0 0 0 0 0 0	Control of fractional value ch0R dB volume (see Table 8-9 for mapping overview)
		Ch1L fract dB volume	vol_lsb_ch2	5:4	0 0 0 0 0 0 0 0	Control of fractional value ch1L dB volume (see Table 8-9 for mapping overview)
		Ch0R fract dB volume	vol_lsb_ch3	7:6	0 0 0 0 0 0 0 0	Control of fractional value ch1R dB volume (see Table 8-9 for mapping overview)
0x47	0x18	Ch0L integer dBFS limiter	thr_db_ch0	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0L dBFS limiter threshold (see section “Limiter”)
0x48	0x18	Ch0R integer dBFS limiter	thr _db_ch1	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0R dBFS limiter threshold (see section “Limiter”)
0x49	0x18	Ch1L integer dBFS limiter	thr _db_ch2	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0L dBFS limiter threshold (see section “Limiter)
0x4A	0x18	Ch1R integer dBFS limiter	thr _db_ch3	7:0	0 0 0 1 1 0 0 0	Control of integer value ch0R dBFS limiter threshold (see section “Limiter”)
0x4B	0x00	Ch0L fract dBFS limiter	thr _lsb_ch0	1:0	0 0 0 0 0 0 0 0	Control of fractional value ch0L dBFS limiter threshold (see section “Limiter”)
		Ch0R fract dBFS limiter	thr _lsb_ch1	1:0	0 0 0 0 0 0 0 0	Control of fractional value ch0R dBFS limiter threshold (see section “Limiter”)
		Ch1L fract dBFS limiter	thr _lsb_ch2	1:0	0 0 0 0 0 0 0 0	Control of fractional value ch1L dBFS limiter threshold (see section “Limiter”)
		Ch0R fract dBFS limiter	thr _lsb_ch3	1:0	0 0 0 0 0 0 0 0	Control of fractional value ch1R dBFS limiter threshold (see section “Limiter”)

Read Only Access (Volume control and limiter monitor)

Address	Default Address Value	Description	Name	Bit(s)	Value	Function
0x7E	0x00	Indicates if limiters are active	audio_proc_limiter_mon	7:4	0 0 0 0 0 0 0 0	Bit 4 high: limiter is active on channel 0L
						Bit 5 high: limiter is active on channel 0R
						Bit 6 high: limiter is active on channel 1L
						Bit 7 high: limiter is active on channel 0R
0x7E	0x00	Indicates if clipping occurs on the VLP output signals	audio_proc_clip_mon	3:0	0 0 0 0 0 0 0 0	Bit 0 high: clipping is present on channel 0L
						Bit 1 high: clipping is present on channel 0R
						Bit 2 high: clipping is present on channel 1L
						Bit 3 high: clipping is present on channel 0R

Read Only Access (Monitor Channel 0 and Channel 1)

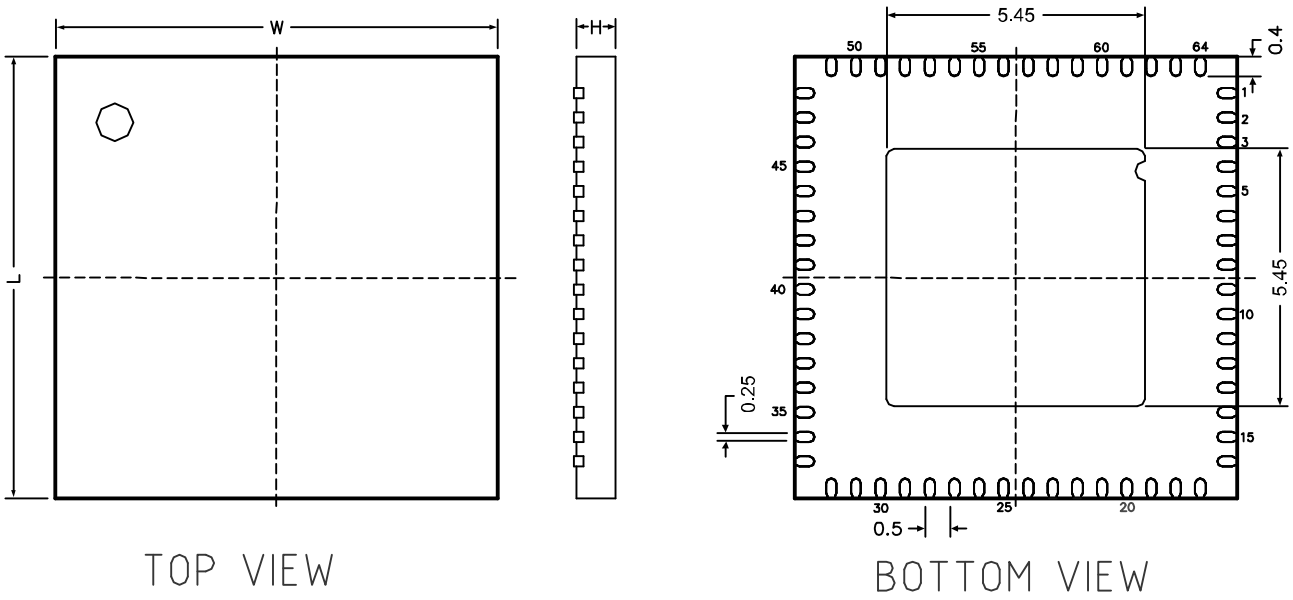
Address	Default Address Value	Description	Name	Bit(s)	Value	Function
0x60	0x00	Monitor register channel 0 (Frequency and Power Mode)	dcu_mon0.freqMode	6:4	-000ff00	Frequency mode monitor channel 0. Register to read out in which frequency mode channel 0 of the device is currently operating in.
			dcu_mon0.PM_mon	1:0	----ff00	Power mode monitor channel 0. Monitor to read out in which Power Mode channel 0 of the device is currently operating in.
0x61	0x00	Monitor register channel 0	dcu_mon0.mute	5	ff0000000	Channel 0 mute monitor. Monitor to read out if channel 0 is in mute or in unmute.
			dcu_mon0.vdd_ok	4	ff0000000	Channel 0 VDD monitor. Monitor to read out if VDD for channel 0 is ok.
			dcu_mon0.pvdd_ok	3	ff0000000	Channel 0 PVDD monitor. Monitor to read out if PVDD for channel 0 is ok.
			dcu_mon0.Vcfly2_ok	2	ff0000000	Channel 0 Cfly2 protection monitor. Monitor to read out if Cfly2 for channel 0 is ok.
			dcu_mon0.Vcfly1_ok	1	ff0000000	Channel 0 Cfly1 protection monitor. Monitor to read out if Cfly1 for channel 0 is ok.
			OCP Monitor channel 0	0	ff0000000	Channel 0 over current protection monitor. Monitor to read out if an over current protection event has occurred.
0x62	0x00	Monitor register channel 0 (Modulation Index)	dcu_mon0.M_mon	7:0	00000000	Channel 0 modulation index monitor. Monitor to read out live modulation index. Modulation index from 0 to 1 maps on the 8-bits register from 0 to 255.
0x64	0x00	Monitor register channel 1 (Frequency and Power Mode)	dcu_mon1.freqMode	6:4	-000ff00	Frequency mode monitor channel 1. Register to read out in which frequency mode channel 1 of the device is currently operating in.
			dcu_mon1.PM_mon	1:0	----ff00	Power mode monitor channel 1. Monitor to read out in which Power Mode channel 1 of the device is currently operating in.
0x65	0x00	Monitor register channel 1	dcu_mon1.mute	5	ff0000000	Channel 1 mute monitor. Monitor to read out if channel 1 is in mute or in unmute.
			dcu_mon1.vdd_ok	4	ff0000000	Channel 1 VDD monitor. Monitor to read out if VDD for channel 1 is ok.
			dcu_mon1.pvdd_ok	3	ff0000000	Channel 1 PVDD monitor. Monitor to read out if PVDD for channel 1 is ok.
			dcu_mon1.Vcfly2_ok	2	ff0000000	Channel 1 Cfly2 protection monitor. Monitor to read out if Cfly2 for channel 1 is ok.
			dcu_mon1.Vcfly1_ok	1	ff0000000	Channel 1 Cfly1 protection monitor. Monitor to read out if Cfly1 for channel 1 is ok.
			OCP Monitor channel 1	0	ff0000000	Channel 1 over current protection monitor. Monitor to read out if an over current protection event has occurred.
0x66	0x00	Monitor register channel 1 (Modulation Index)	dcu_mon1.M_mon	7:0	00000000	Channel 1 modulation index monitor. Monitor to read out live modulation index. Modulation index from 0 to 1 maps on the 8-bits register from 0 to 255.

Read Only Access (Error Register Monitoring):

Address	Default Address Value	Description	Name	Bit(s)	Value	
0x6D	0x00	Error accumulated register	error_acc	7:0	0 0 0 0 0 0 0 0	Error monitor register. Gives the accumulated status of every potential error source. This register should be cleared by using the error handler clear register.
						All bits will be 0 in default/normal operation and 1 when triggered
						Bit 0: flying capacitor over-voltage error
						Bit 1: over-current protection
						Bit 2: pll error
						Bit 3: PVDD under-voltage protection
						Bit 4: over-temperature warning
						Bit 5: over-temperature error
						Bit 6: pin-to-pin low impedance protection
						Bit 7: DC protection
0x75	0x00	Monitor MSEL register	msel_mon	2:0	f f f f f 0 0 0	MSEL[2:0] monitor register. Monitor to read out which output configuration the device is in: BTL, SE, BTL/SE or PBTL
0x7C	0x00	Error register	error	7:0	0 0 0 0 0 0 0 0	Error monitor register. Gives the live status of every potential error source.
						All bits will be 0 in default/normal operation and 1 when triggered
						Bit 0: flying capacitor over-voltage error
						Bit 1: over-current protection
						Bit 2: pll error
						Bit 3: PVDD under-voltage protection
						Bit 4: over-temperature warning
						Bit 5: over-temperature error
						Bit 6: pin-to-pin low impedance protection
						Bit 7: DC protection

17 Package Information

QFN pad-down 64-pin mechanical data

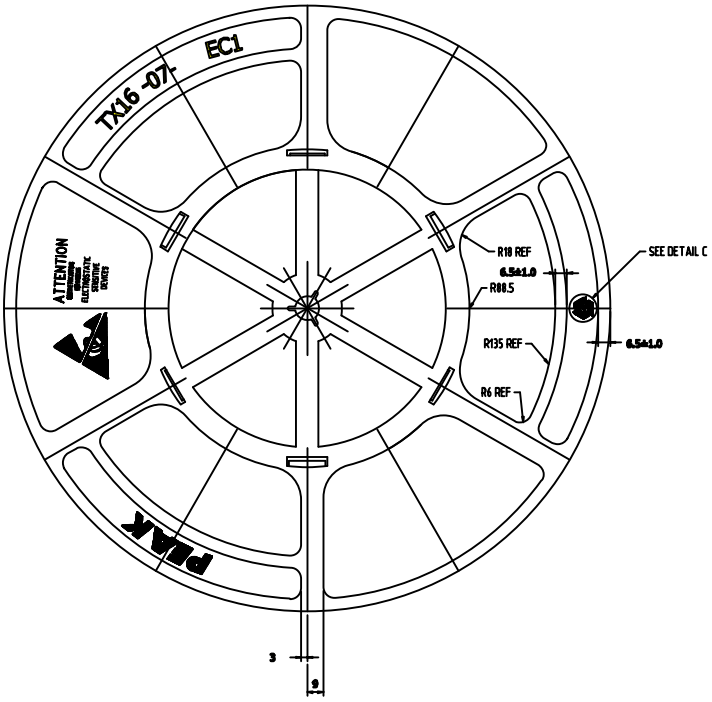


Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	9.00	±0.1
Width [W]	9.00	±0.1
Height [H]	0.90	MAX

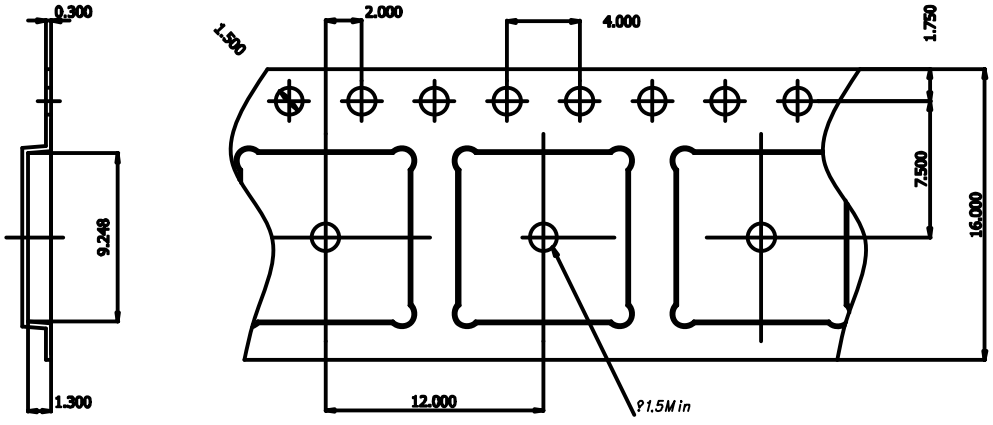
18 Tape and Reel Information



VIEW B

DETAIL C
M4:1

NOTES:
1. FLANGE WARPAGE: 3 MM MAXIMUM
2. ALL DIMENSIONS ARE IN MM
3. ESD-SURFACE RESISTIVITY
10^5 TO 10^{11} OHMS/SQ.
4. GENERAL TOLERANCE: ±0.25 MM
5. TOTAL THICKNESS OF REEL : 22.4 MAX.
6. PART NO. TX16-07-EC1
(PLEASE INDICATE ON PURCHASE ORDER)
7. TAPE SLOT WIDTH: 5.0±0.5



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm
3. Material: Black conductive Polystyrene
4. Ao and Bo measured on the seating plane of the package
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be same position.

19 Revision History

Doc. Rev.	Date	Comments
V 1.0	July 2018	Initial release in Infineon format

20 Contents

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE
The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Audio Amplifiers ***category:***

Click to view products by Infineon ***manufacturer:***

Other Similar products are found below :

LV3313PM-TLM-E LV47002P-E LV4924VH-MPB-H LV4924VH-TLM-H AZ386MTR-E1 NCP2811AFCT1G NCP2890AFCT2G FAB3102UCX STK404-070N-E STK404-140N-E STK433-840N-E STK433-890N-E IS31AP4915A-QFLS2-TR TDA1591T AS3561-BWLT-500 TDA7563AH TDA7850H TS2012EIJT NCP2809BMUTXG NJW1157BFC2 TPA6201A1ZQVR IS31AP4996-GRLS2-TR NCP2823BFCT1G LA4450L-E IS31AP2036A-CLS2-TR TDA7563ASMTR STPA001AH MP1720DH-12-LF-P SABRE9601K THAT1646W16-U PAM8965ZLA40-13 TSDP10XX1NLGXZBX TSDP11XX1NBGIZBX TSDP10XX1NBGIZBX NJM4580CV-TE1 BD5638NUX-TR BD37543FS-E2 BD3814FV-E2 TPA3110LD2PWPR AS3435-EQFP AW88194ACSR TAS5766MDCAR TAS5766MRMTR TAS5766MRMTT TPA3136AD2PWP TPA3140D2PWPR TS2007EIJT MP7748DF-LF IS31AP2005-DLS2-TR TAS5766MDCA