30 W high-efficiency auxiliary SMPS for refrigerator using ICE5QR1680BG

REF_5QR1680BG_30W1

About this document

Scope and purpose

This document is a reference design for a high-efficiency 30 W auxiliary SMPS for a refrigerator with the latest fifth-generation Infineon QR CoolSET™ **ICE5QR1680BG**. The power supply is designed with a universal input compatible with most geographic regions and three outputs (isolated +12 V/2.2 A, +5 V/0.2 A and non-isolated 15 V/0.15 A) as typically employed in most home appliances.

Highlights of this auxiliary power supply for a refrigerator:

- Overall high efficiency to meet energy efficiency requirements
- Simplified circuitry with good integration of power and protection features
- Auto restart protection scheme to minimize interruption to enhance end user experience
- Add-in AC zero-crossing detection (ZCD) circuit
- Add-in LDO enable circuit to reduce standby loss

Intended audience

This document is intended for power supply design or application engineers, etc. who want to design auxiliary power supplies for refrigerators that are efficient, reliable and easy to design.

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1 System introduction

With the growing household trend for internet-connected devices, the new generation of home appliances such as refrigerators are equipped with advanced features which often include communication capability, such as wireless communication, touchscreen display and sensors. These will transform a static product into an interactive and intelligent home appliance, capable of adapting to the smart-home theme. Infineon has introduced the latest fifth-generation QR CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules and sensors, which typically operate from a stable DC voltage source. The Infineon CoolSET™ (as shown in **Figure 1**) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

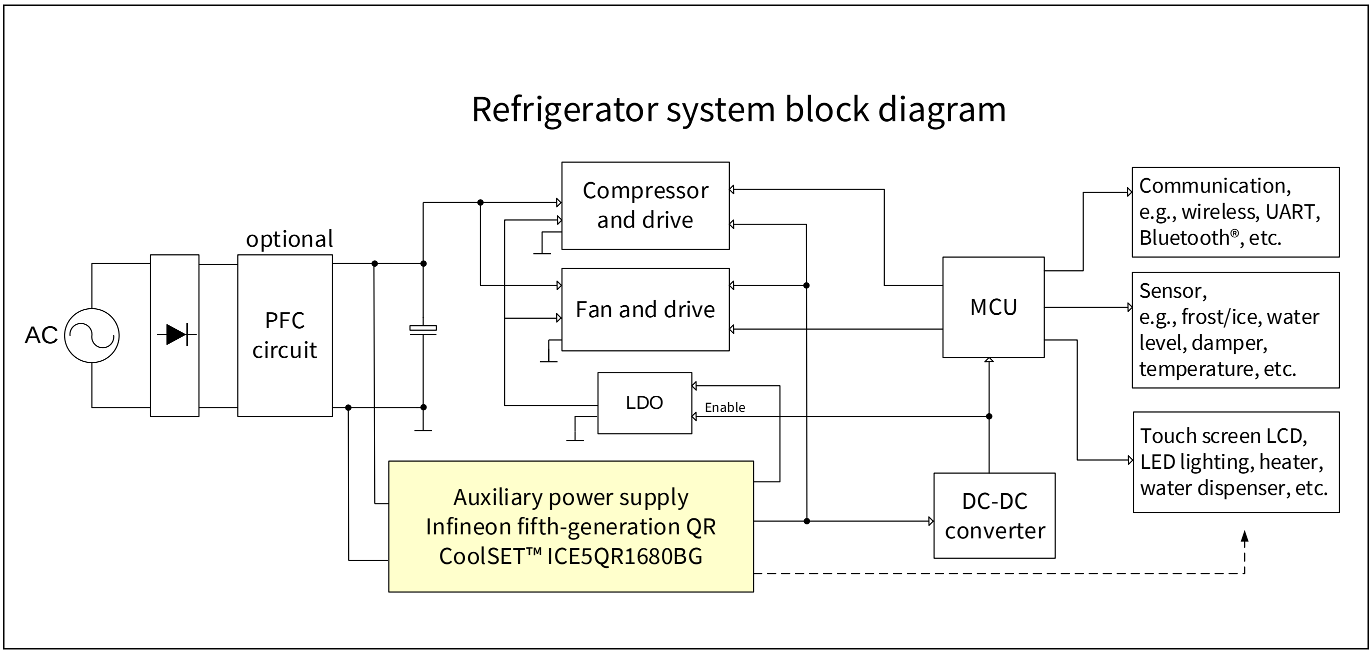


Figure 1 Simplified refrigerator system block diagram

Table 1 lists the system requirements for a refrigerator, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and reference board solutions

	System requirement for a refrigerator	Reference board solution – ICE5QR1680BG
1	High efficiency to meet various energy efficiency requirements	Primary QR control and secondary synchronous rectifier control
2	Simplified circuitry with good integration of power and protection features	Embedded 800 V MOSFET and controller in DSO-12 package
3	Auto restart protection scheme to minimize interruption to enhance end user experience	All abnormal protections are in auto restart mode

1.1 High efficiency under light-load conditions to meet ENERGY STAR requirements

During typical refrigerator operation, the power requirement fluctuates according to various use cases. However, in most cases, the refrigerator will reside in an idle state in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for a prolonged period. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency play a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5QR1680BG was primarily chosen due to its QR switching scheme. Compared with a traditional flyback switching scheme, the CoolSET™ will attempt to turn on its integrated high-voltage (HV) MOSFET in the valley of the resonant period, thereby minimizing switching losses. Additionally, the fifth-generation QR series suports up to 10 valleys, thereby lowering the switching frequency further along with a reduction in load. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, CoolSET™ is a highly integrated device with both a controller and a HV MOSFET integrated in a single, space-saving DSO-12 package. These certainly help the designer to reduce component count as well as simplifying the layout into a single-layer PCB design for ease of manufacturing, using the traditional, cost-effective wave-soldering process.

To counter abnormal line input conditions, CoolSET™ has integrated line input overvoltage (OV) as well as brown-out protection to increase the robustness of the auxiliary power. In the event of such faults, the controller within the CoolSET™ will halt the switching operation of the integrated HV MOSFET, thereby preventing permanent damage. These features allow the designer to reduce the complexity of introducing additional external circuitry and yield a saving of many components.

1.3 Auto restart protection scheme to minimize interruption to enhance end user experience

For a refrigerator it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the CoolSET™ implements auto restart mode for all protections.

2 Reference board

This document provides complete design details including specifications, schematics, bill of materials (BOM), and PCB layout and transformer design and construction information. This information includes performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans, etc.

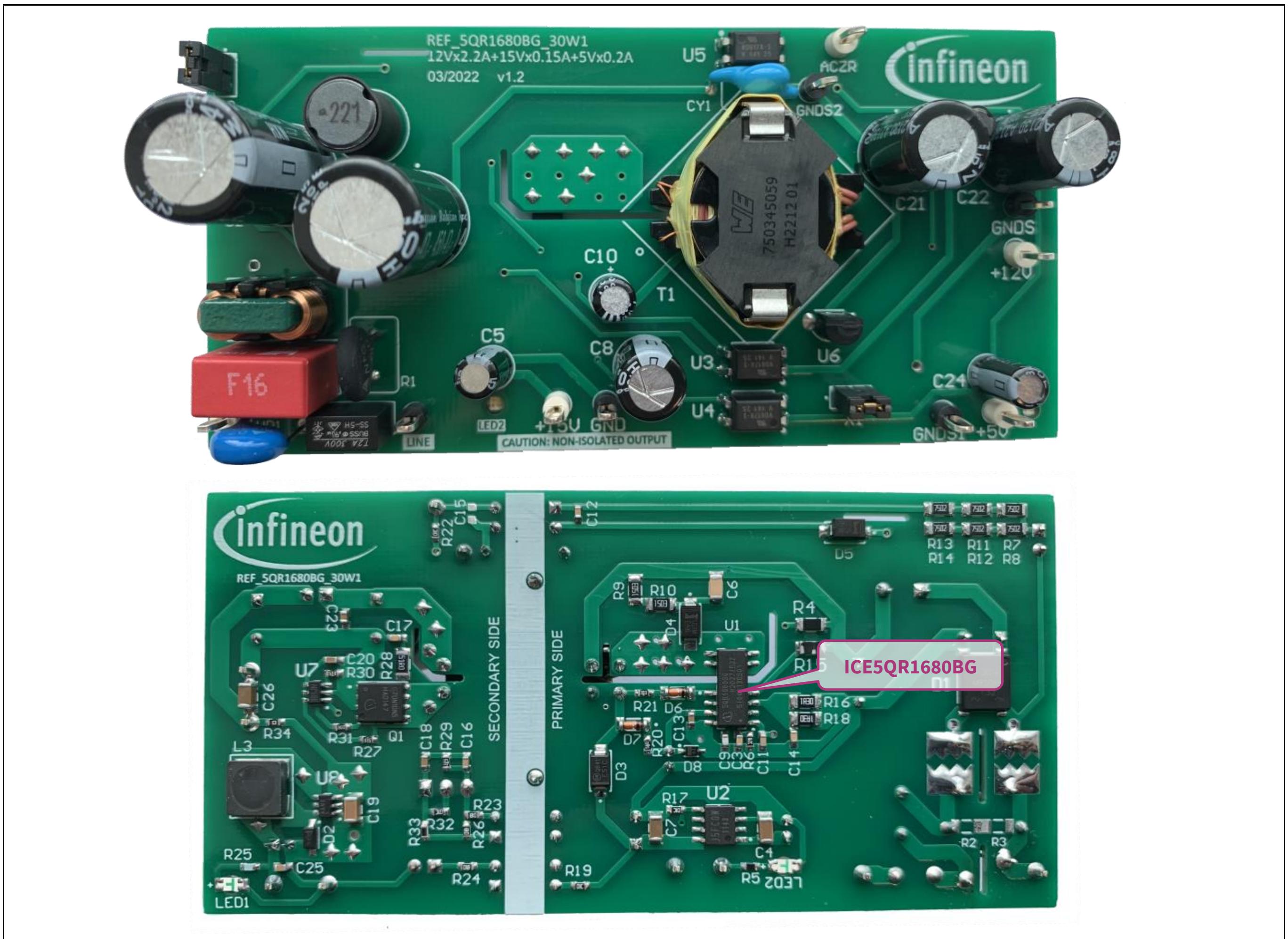


Figure 2 **REF_5QR1680BG_30W1**

3 Power supply specifications

The table below represents the minimum acceptance performance of the design. The actual performance is listed in the measurements section.

Table 2 Specifications of REF_5QR1680BG_30W1

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	85	–	264	V AC	Two wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	0.5	–	W	Enabled LDO at 230 V AC
Line OV	V_{IN_OVP}	–	300	–	V AC	
Output						
Output voltage 1	V_{OUT1}	–	12	–	V	±1 percent
Output current 1	I_{OUT1}	–	2.2	–	A	
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	120	mV	
Output voltage 2	V_{OUT2}	–	5	–	V	Tapped from 12 V output via DC-DC converter
Output current 2	I_{OUT2}	–	0.2	–	A	
Output voltage 3	V_{OUT3}	–	15	–	V	Tapped from 18 V output via LDO
Output current 3	I_{OUT3}	–	0.15	–	A	
Overcurrent protection (12 V)	I_{OCP}	–	–	3.3	A	With full load on other outputs
Efficiency						
Maximum load efficiency	η	–	84	–	%	115 V AC/230 V AC
Average efficiency	η_{avg}	–	83	–	%	115 V AC/230 V AC
Average efficiency for single output configuration	η_{avg_s}	–	89	–	%	115 V AC/230 V AC
Environmental						
Conducted EMI			10		dB	Margin, CISPR 22 class B
ESD						EN 61000-4-2
Contact discharge			±6		kV	
Air discharge			±8		kV	
Surge immunity						EN 61000-4-5
Differential mode			±1		kV	
Common mode			±2		kV	
PCBA form factor			110 x 54 x 30		mm^3	L x W x H

4 Circuit diagram

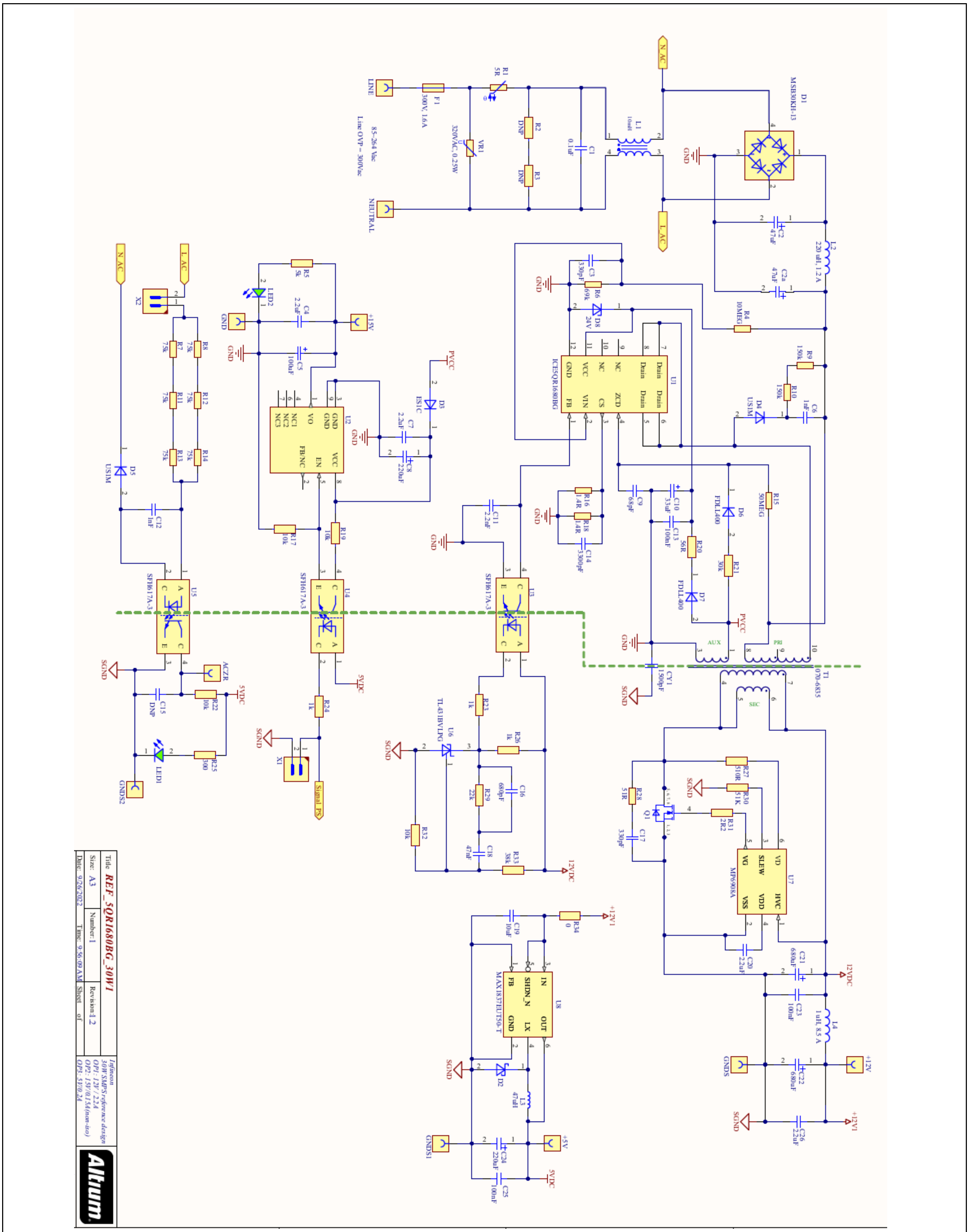


Figure 3 **Schematic of REF_5QR1680BG_30W1**

5 Circuit description

In this section, the reference design circuit for refrigerator auxiliary power will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide **[2]** and calculation tool **[3]**.

5.1 EMI filtering and line rectification

The input of the refrigerator auxiliary power unit is taken from the AC power grid, which is in the range of 85 V AC ~ 264 V AC. The fuse F1 is right at the entrance to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VR1, which is connected across L and N to absorb the line surge transient. Common mode (CM) choke L1 and X-capacitor C1 form a basic filter to attenuate the DM and CM conducted EMI noise. The bridge rectifier D1 rectifies the AC input into DC voltage, filtered by the π filter (capacitor C2, C2a and L2). The above is not applicable if the power-factor correction (PFC) circuit is used as shown in **Figure 1**.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer T1, a primary HV MOSFET (integrated into ICE5QR1680BG), secondary synchronous rectifier (SR) MOSFET Q1, secondary output capacitors and filtering component (C21, C22 and L4).

When the integrated CoolMOS™ turns on, some energy is stored in the transformer. When it turns off, the stored energy would release to the output capacitors and the output loading through the output SR MOSFET Q1.

Sandwich winding structure for the transformer T1 is used to reduce the leakage inductance, and so the loss in the clamper circuit is reduced. T1 has two output windings; one primarily for the V_{OUT1} (12 V) and the other for the V_{OUT3} (15 V). All the secondary output capacitors should be the low-ESR type, which can effectively reduce the switching ripple. Together with the Y-capacitor CY1 across the primary and secondary side, the EMI noise can be further reduced to comply with CISPR 22 specifications.

5.3 Control of flyback converter through fifth-generation QR CoolSET™ ICE5QR1680BG

5.3.1 Integrated HV power MOSFET

The ICE5QR1680BG CoolSET™ is a 12-pin device in a DSO-12 package. It has been integrated with the new QR PWM controller and all necessary features and protections, and most importantly the 800 V power MOSFET, Infineon superjunction CoolMOS™. Hence, the schematic is much simplified and the circuit design becomes much easier.

5.3.2 Current sensing

The ICE5QR1680BG is a CM controller. The peak current is controlled cycle-by-cycle through the current sensing (CS) resistors R16 and R18 in the CS pin (pin 3), so transformer saturation can be avoided and the system is more robust and reliable.

5.3.3 Feedback and compensation network

Resistors R32 and R33 are used to sense the V_{OUT1} and send reference voltage to the feedback (FB) pin (pin 2) via error amplifier TL431 (U6) and optocoupler (U3). A Type II compensation network (C16, C18 and R29) is implemented to stabilize the system.

The FB pin of ICE5QR1680BG is a multifunction pin which is used to select the entry burst power level (there are two levels available) through R_{sel} and also the burst-on/burst-off sense input during active burst mode (ABM).

5.4 Unique features of the fifth-generation QR CoolSET™ ICE5QR1680BG to support the requirements of refrigerator auxiliary power

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. The zero-crossing detection (ZCD) pin (pin 4) is a multifunction pin and it serves as the start-up pin with the connection of pull-up resistors R15, which has the other end connecting to the bus voltage during the start-up phase. At first, $I_{VCC\_Charge1}$ is used to charge the V_{CC} capacitor from 0 V to V_{CC_SCP}. This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of $I_{VCC\_Charge2}$ will charge the V_{CC} capacitor until the V_{CC_ON} is reached.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer T1, which needs to support the V_{CC} to be above undervoltage lockout (UVLO) voltage (10 V typ.). In this reference board, the V_{CC} supply is tapped from the +18 V winding.

5.4.2 QR switching with valley sensing

ICE5QR1680BG is a QR flyback controller, which always turns on at the lowest valley point of the drain voltage. The IC senses the valley point through the ZCD pin (pin 4), which monitors auxiliary winding voltage by R21, D6 and C9 to the ZCD pin (pin 4) together with the internal resistor R_{ZCD}. The IC detects the valley crossing signal. When the ZCD voltage drops below 100 mV (typ.), the CoolMOS™ is allowed to switch on. With QR switching, the lowest switching losses can be achieved for good efficiency.

5.4.3 System robustness and reliability through protection features

5.4.3.1 Input voltage monitoring and protection

To avoid system damage due to the high AC input transient, refrigerator auxiliary power requires the input line overvoltage protection (LOVP) to stop the flyback converter switching whenever the V_{Bus} voltage exceeds the operating range. The IC has a V_{IN} pin (pin 2), which can sense V_{Bus} voltage through voltage dividers R4 and R6. When the V_{IN} pin exceeds the protection threshold 2.9 V (typ.), the IC stops switching. With the same V_{IN} sensing, ICE5QR1680BG also implements input undervoltage (UV) protection (brown-in/brown-out) to prevent the overcurrent (OC) stress of the power stage components when the input voltage is too low.

5.4.3.2 Other protections with auto restart

Besides input OV and UV protection, ICE5QR1680BG has more comprehensive protection features to protect the system, such as V_{CC} OV, V_{CC} UV, overload, open-loop protection, output OV, overtemperature, V_{CC} short-to-GND, etc.

5.5 Clamper circuit

A clamper network (D4, C6 and R9, R10) is used to reduce the switching spikes on the drain pin, which are generated from the leakage inductance of the transformer T1. This is a dissipative circuit and the selection of the R9, R10 needs to be fine-tuned.

5.6 AC zero-crossing detection and LDO enable circuit

A ZCD circuit is usually required in home appliances that supply power from an AC outlet to detect the zero-cross point (which is the 0 V point of the AC waveform) in order to efficiently control motors. Thus, a conventional ZCD circuit was built in here to output a zero-cross signal from 85 V AC to 264 V AC input at the ACZR pin. This circuit can be disabled by removing jumper X2.
The LDO enable function is controlled via an optocoupler U4 by 5 V output, which can reduce standby power loss if LDO output is not required. By removing jumper X1, LDO can be disabled.

5.7 PCB design tips

For a good PCB design layout, there are several points to highlight.

- The power loop needs to be as small as possible (see **Figure 4**). There are two power loops in the reference design; one from the primary side and the other from the secondary side. For the primary side, it starts from the bulk capacitor (C2a) positive to the bulk capacitor negative. The power loop components include C2a, the main primary transformer winding (pin 8 and pin 10 of T1), the drain pin and CS pin of the CoolSET™ U1 and CS resistors R16 and R18. For the secondary side, the 12 V output starts from the secondary transformer windings (pin 6 and 7 of T1), SR MOSFET Q1 and output capacitors C21 and C22.
- Star-ground concept should be used to avoid unexpected HF noise coupling to affect the proper control. The ground of the small-signal components, e.g., C3, C9, C11, C13 and R6, and emitter of optocoupler (pin 3 of U3) etc. should connect directly to the IC ground (pin 12 of U1). Then it connects to the negative terminal of the C2a capacitor directly.

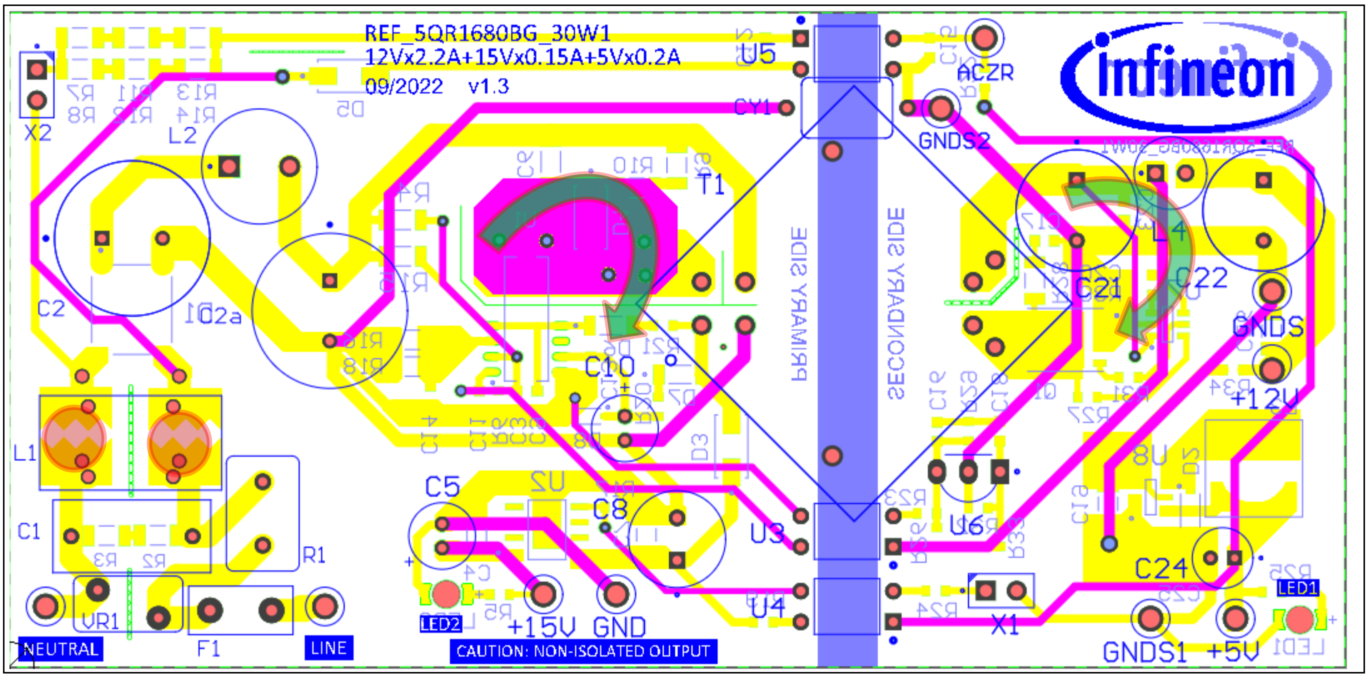


Figure 4 PCB layout tips

- Adding a certain amount of drain PCB copper area can increase the margin of power capability of the CoolSET™.
- Adding spark-gap (PCB sawtooth, 0.5 mm separation) pattern under the input CM choke L1 can improve system input line surge and ESD immunity.

5.8 EMI reduction tips

EMI compliance is always a challenge for a power supply. There are several critical points to consider in order to achieve satisfactory EMI performance.

- Good transformer winding coupling is very important. Without this it would lead to high leakage inductance and incur a lot of switching spike and high-frequency (HF) noise. The most effective method is to adopt sandwich winding (refer to **Figure 8**) where the secondary winding is in the middle of the winding and covered by the primary winding on the bottom and top layer. Shielding the transformer can reduce the HF noise. The outermost shield wrapped around the transformer cores with copper foil can help to reduce leakage flux and reduce the noise coupling to nearby components. The inner shield (copper foil or copper wire winding) between the transformer windings can help to reduce the parasitic capacitance and reduce the HF noise coupling. Both shields need to tie to the negative of C2a to achieve the best performance, but note that the inner shield approach would result in more energy loss.
- Short power loop design in the PCB (as described in section **5.6**) and terminating to the low ESR capacitor such as C2 and C2a for primary-side loop and C21 and C22 for the secondary-side loop can help to reduce the switching ripple, which comes out to the input terminals V_{IN}. In addition, adding a low-ESR ceramic capacitor in parallel may help to further reduce the switching ripple.
- Sufficient input filter (C1, L1, L2, C2 and C2a) design is important to pass the EMI requirement.
- The Y-capacitor CY1 has a function to return the HF noise to the source (negative of C2a) and reduce the overall HF noise going out to the input terminals. The greater capacitance is more effective. However, a higher value would introduce more leakage current and may fail the safety requirement.

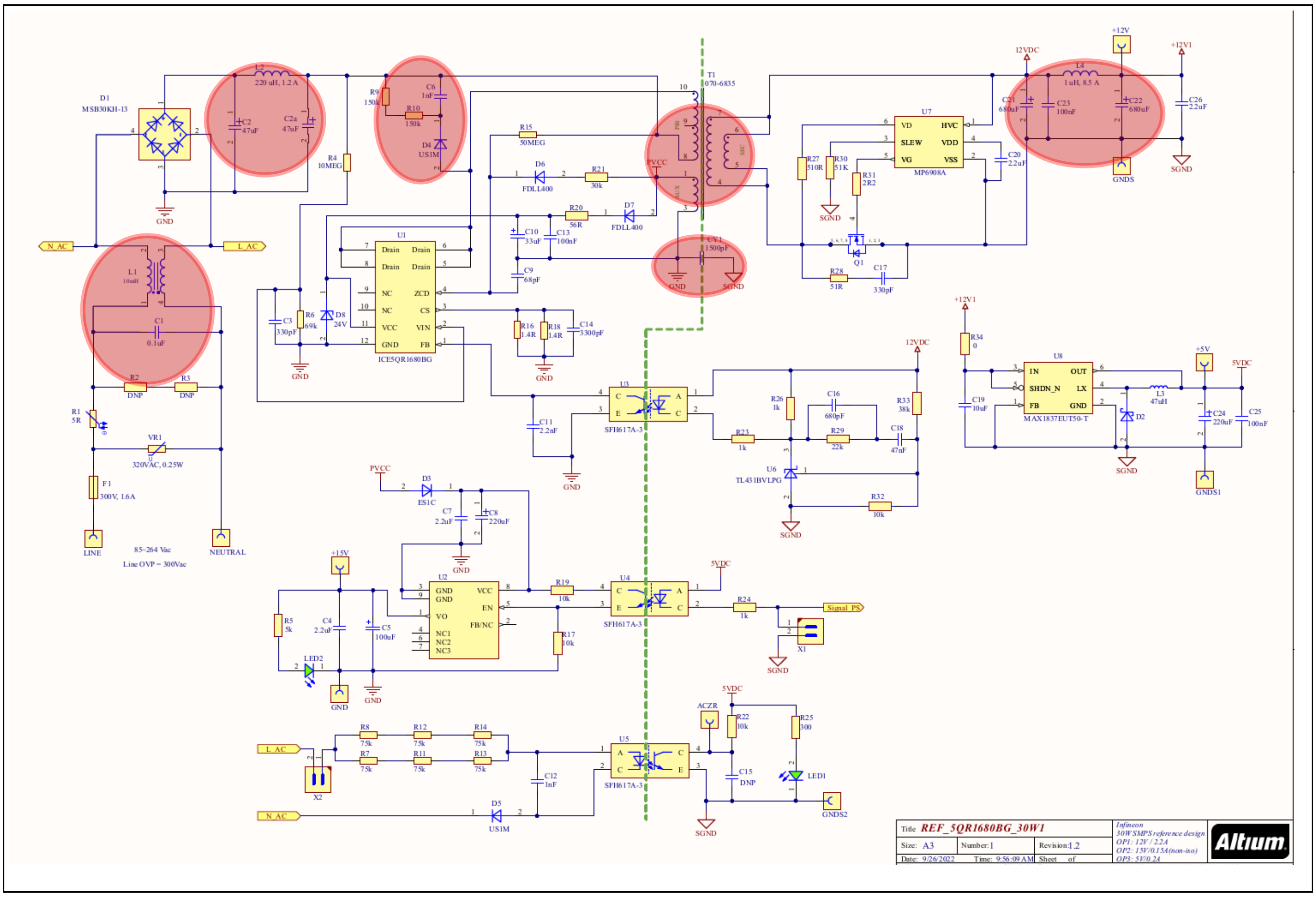


Figure 5 **EMI reduction tips**

6 PCB layout

6.1 Top side

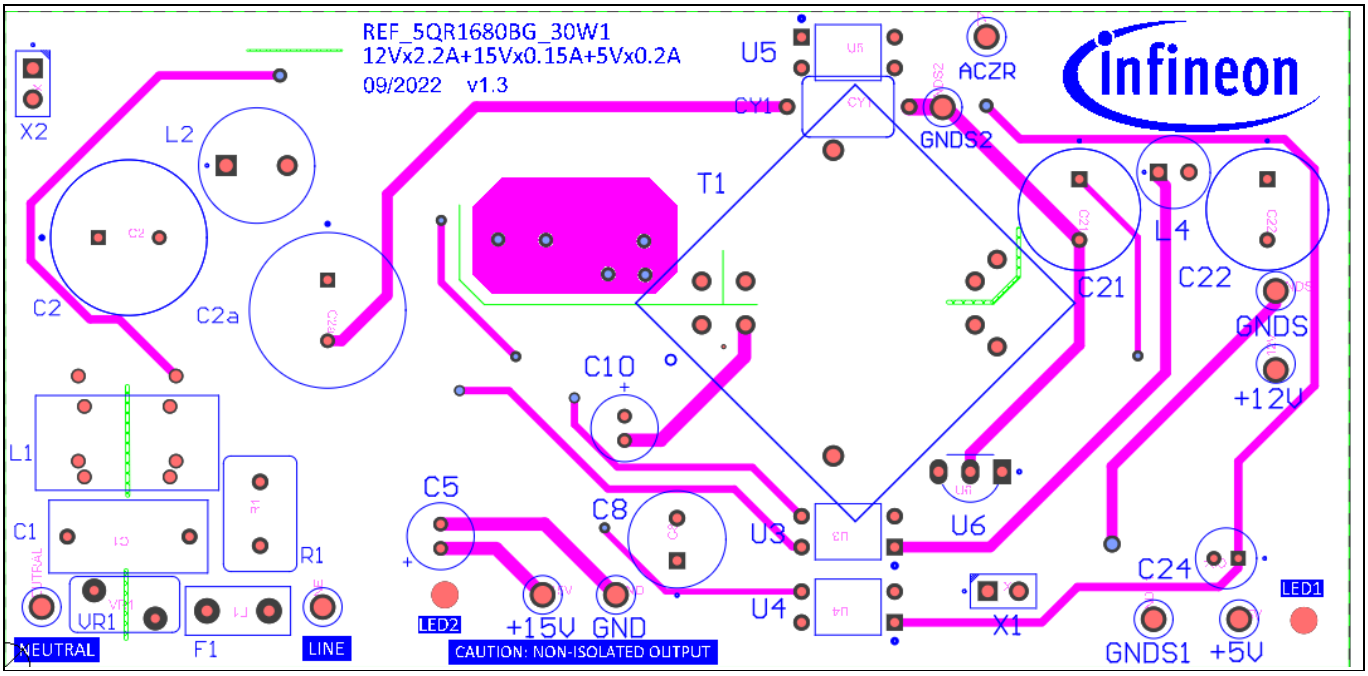


Figure 6 Top-side component legend

6.2 Bottom side

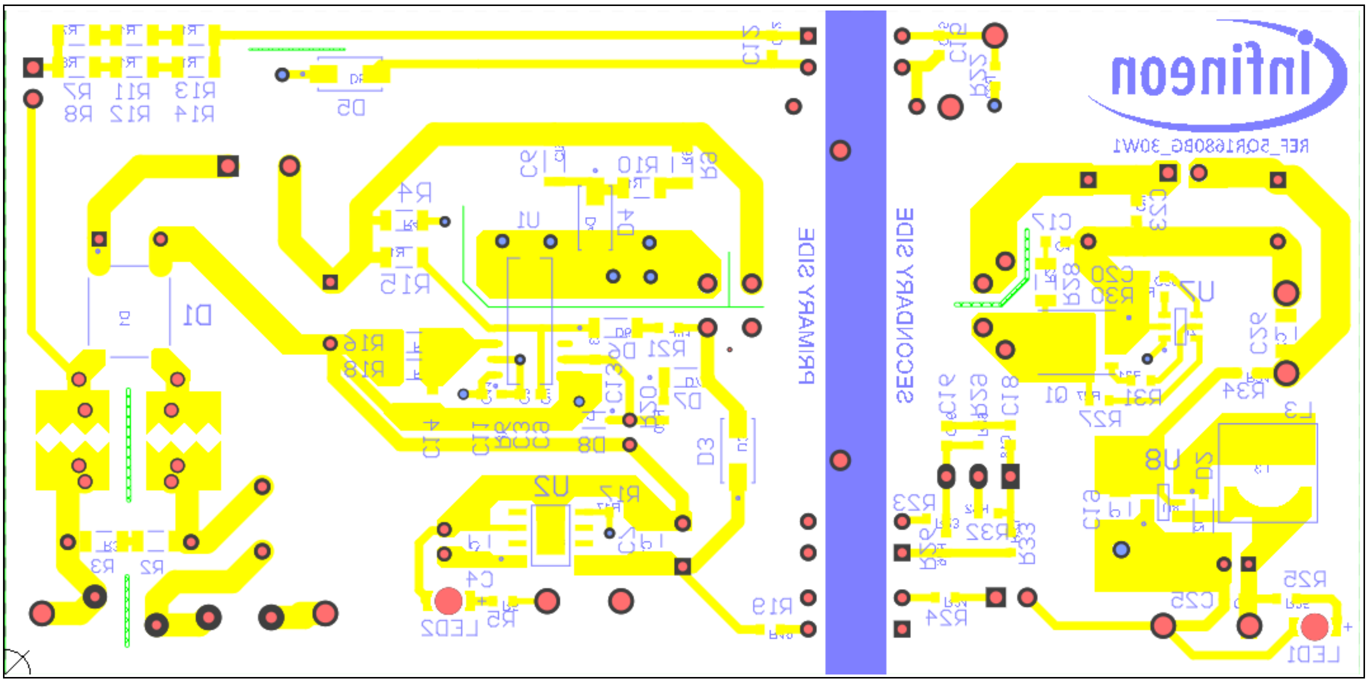


Figure 7 Bottom-side component legend

7 Bill of materials

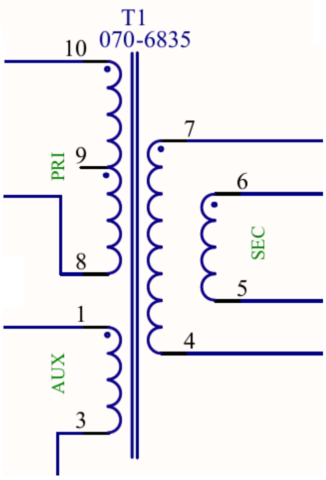
Table 3 BOM

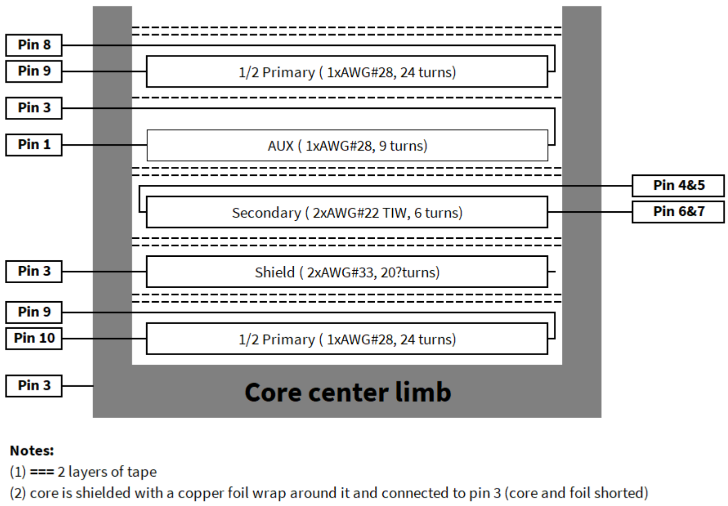
No.	Designator	Description	Manufacturer	Part number	Quantity
1	C1	Safety capacitors 0.1 µF 310 V 10%	Würth Elektronik	890334023023	1
2	C2, C2a	Aluminum capacitor 47 µF 10% 450 V radial	Rubycon	450HXW47MEFR12.5X25	2
3	C3, C17	Ceramic capacitor 330 pF 100 V CH 0603	AVX	06031C331KAZ2A	3
4	C4, C7, C26	Ceramic capacitor 2.2 µF 50 V X7R 1206			3
5	C13, C23, C25	Ceramic capacitor 100 nF 50 V X7R 0603			3
6	C5	Aluminum capacitor 100 µF 20% 25 V radial	Rubycon	25YXJ100M5X11	1
7	C6	Ceramic capacitor 1206 1 nF 500 V X7R 10% FL	Kemet	C1206X102KCRACAUTO	1
8	C8	Aluminum capacitor 220 µF 20% 35 V radial	United Chemi-Con	EKZE350ELL221MH15D	1
9	C9	Ceramic capacitor 68 pF 50 V X7R 0603			1
10	C10	Aluminum capacitor 33 µF 20% 35 V radial			1
11	C11	Ceramic capacitor 0603 2.2 nF 16 V X7R 10%			1
12	C12	Ceramic capacitor 0603 1 nF 50 V X7R 10%			1
13	C14	Ceramic capacitor 0603 3.3 nF 50 V X7R 10%			1
14	C16	Ceramic capacitor 680 pF 50 V X7R 0603			1
15	C18	Ceramic capacitor 0603 47 nF 16 V X7R 10%			1
16	C19	Ceramic capacitor 10 µF 25 V X7R 1206			1
17	C20	Ceramic capacitor 2.2 µF 10 V X7R 0603			1
18	C21, C22	Aluminum capacitor 680 µF 20% 25 V radial	Rubycon	25ZLH680MEFC10X16	2
19	C24	Aluminum capacitor 220 µF 20% 10 V radial	Rubycon	10YXJ220M5X11	1
20	CY1	Ceramic capacitor 1500 pF 250 V radial	Murata	DE1E3KX152MA4BN01F	1
21	D1	Bridge rectifier single-phase 800 V 3 A 4MSBL	Diodes Inc	MSB30KH-13	1
22	D2	Schottky diode 30 V 1 A SOD-123	ON Semiconductor	MBR130T3G	1
23	D3	General-purpose diode 150 V 1 A SMA	ON Semiconductor	ES1C	1
24	D6, D7	General-purpose diode 150 V 200 mA SOD-80	ON Semiconductor	FDLL400	2
25	D4, D5	General-purpose diode 1 kV 1 A SMA	ON Semiconductor	US1M	2
26	D8	Zener diode 24 V 300 mW SOD-323	Nexperia	BZX384-C24,115	1
27	F1	Time-lag fuse 300 V 1.6A	Littelfuse	36911600000	1
28	L1	CMC 10 mH 2LN TH	Tengda	TD1010-10.0mH	1
29	L2	Fixed inductor 220 µ H 1.2A 290 mΩ TH	Würth Elektronik	7447452221	1
30	L3	Fixed inductor 47µH 730 mA 280 mΩ SMD	Würth Elektronik	744062470	1
31	L4	Inductor WE-TI size 5075 1 µH 8.5 A	Würth Elektronik	7447462010	1
32	LED1, LED2	Clear green LED two SMD bottom entry	Würth Elektronik	156120VS82500	2
33	Q1	MOSFET N-channel 100 V 80 A TDSON-8	Infineon	BSC070N10NS5	1
34	R1	ICL 5 Ω 20% 4.2 A 9.5 mm	TDK	B57235S0509M000	1
35	R4	SMD resistor 10 mΩ 1% 1206	Vishay	RCV120610M0FKEA	1
36	R5	SMD resistor 5 kΩ 1% 1/10 W 0603			1
37	R6	SMD resistor 69 kΩ 1% 1/10 W 0603			1
38	R7, R8, R11, R12, R13, R14	SMD resistor 75 kΩ 1% 1/4 W 1206			6
39	R9, R10	SMD resistor 150 kΩ 1% 1/4 W 1206			2
40	R15	SMD resistor 50 mΩ 1% 1206	Vishay	CRHA1206AF50M0FKEF	1
41	R16, R18	SMD resistor 1.3 Ω 1% 1/4 W 1206			2
42	R17, R19, R22, R32	SMD resistor 10 kΩ 1% 1/10 W 0603			4
43	R20	SMD resistor 56 Ω 1% 1/10 W 0603			1
44	R21	SMD resistor 30 kΩ 1% 1/10 W 0603			1
45	R23, R24, R26	SMD resistor 1 kΩ 1% 1/10 W 0603			3

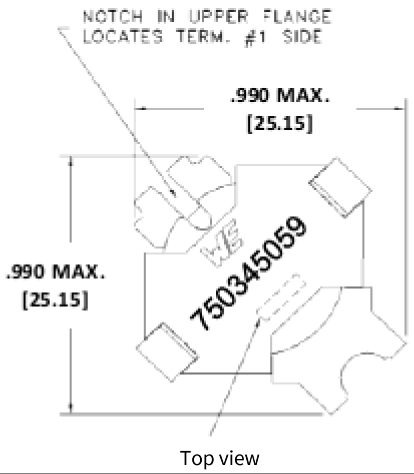
No.	Designator	Description	Manufacturer	Part number	Quantity
46	R25	Resistor 300 Ω 1% 1/8 W 0603			1
47	R27	SMD resistor 510 Ω 1% 1/10 W 0603			1
48	R28	SMD resistor 51 Ω 5% 1/4 W 1206			1
49	R29	SMD resistor 22 kΩ 1% 1/10 W 0603			1
50	R30	SMD resistor 51 kΩ 1% 1/10 W 0603			1
51	R31	SMD resistor 2.2 Ω 1% 1/10 W 0603			1
52	R33	SMD resistor 38 kΩ 1% 1/10 W 0603			1
53	R34	SMD resistor 0 Ω 1% 1/10 W 0603			1
54	T1	Transformer RM style, RM8, Rev01	Würth Elektronik	750345059	1
55	U1	QR 800 V CoolSET™	Infineon	ICE5QR1680BG	1
56	U2	35 V withstand voltage 1 A LDO regulators	Rohm	BDJ5FC0WEFJ-E2	1
57	U3, U4, U5	Opto-isolator 5.3 kV transformer 4DIP	Vishay	SFH617A-3	3
58	U6	IC V_{REF} shunt ADJ 0.4% TO92-3		TL431BVLPG	1
59	U7	Synchronous rectifier controller	MPS	MP6908A	1
60	U8	Step-down converter	Maxim Integrated	MAX1837EUT50-T	1
61	VR1	Varistor 510 V 1.75 kA disc 7 mm	Epcos	B72207S2321K101	1
62	X1, X2	Vertical header connector two-position 2.54 mm	Samtec	TSW-102-08-G-S	2
63	X1, X2	Shunt connector two-position	Samtec	SNT-100-BK-G	2
64	+5 V, +12 V, +15 V, NEUTRAL, ACZR	Test-point multipurpose THT, white	Keystone	5012	5
65	GND, LINE, GNDS, GNDS1, GNDS2	Test-point multipurpose THT, black	Keystone	5011	5

8 Transformer specification

- Core and materials: RM8, TP4A (TDG)
- Bobbin: 070-6835 (10-pin, THT, horizontal version)
- Primary inductance: L_p = 450 µH (±10 percent), measured between pin 8 and pin 10
- Manufacturer and part number: Würth Elektronik Midcom (750345059)
- Refer to Appendix A for transformer design and Appendix B for WE transformer specification







Wire size requirement :

Start	Stop	No. of turns	Wire size	Layer
Pin 10	Pin 9	24	1 x AWG#27	1/2 Primary
Pin 3	NC		2 x AWG#33	Shield
Pin 6&7	Pin 4&5	6	2 x AWG#22 TIW	Secondary
Pin 1	Pin 3	9	1 x AWG#28	AUX
Pin 9	Pin 8	24	1 x AWG#27	1/2 Primary

Figure 8 Transformer specification

9 Measurement data and graphs

Table 4 Efficiency data

Input (V AC/Hz)	Load percentage	P_{IN} (W)	V_{O1} (V)	I_{O1} (A)	V_{O2} (V)	I_{O2} (A)	V_{O3} (V)	I_{O3} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)	OLP P_{IN} (W)	OLP I_{O1} (A)
85 V AC/60 Hz	25%	8.92	12.000	0.545	4.96	0.045	15.06	0.038	7.335	82.24	82.74	38.34	2.40
	50%	17.73	12.000	1.096	4.94	0.090	15.05	0.078	14.771	83.31			
	75%	26.75	11.984	1.644	4.91	0.148	15.04	0.119	22.218	83.06			
	100%	35.81	11.984	2.195	4.88	0.193	15.03	0.149	29.486	82.34			
115 V AC/60 Hz	25%	8.88	12.000	0.545	4.96	0.045	15.06	0.038	7.335	82.61	83.81	43.34	2.75
	50%	17.54	12.000	1.096	4.94	0.090	15.05	0.078	14.771	84.21			
	75%	26.41	11.984	1.644	4.91	0.148	15.04	0.119	22.218	84.13			
	100%	34.99	11.984	2.195	4.89	0.193	15.03	0.149	29.488	84.28			
230 V AC/50 Hz	25%	8.96	12.000	0.545	4.96	0.045	15.06	0.038	7.335	81.87	84.20	44.89	2.96
	50%	17.45	12.000	1.096	4.94	0.090	15.05	0.078	14.771	84.64			
	75%	26.19	11.984	1.644	4.91	0.148	15.04	0.118	22.203	84.78			
	100%	34.48	11.984	2.195	4.89	0.193	15.03	0.149	29.488	85.52			
263 V AC/50 Hz	25%	9.07	12.000	0.545	4.96	0.045	15.06	0.038	7.335	80.88	83.79	46.21	3.05
	50%	17.54	12.000	1.096	4.94	0.090	15.05	0.078	14.771	84.21			
	75%	26.26	12.000	1.644	4.91	0.148	15.04	0.118	22.229	84.65			
	100%	34.52	11.984	2.195	4.89	0.193	15.03	0.149	29.488	85.42			

Note: AC ZCD circuit was disabled (open X2) during efficiency test.

Table 5 Single-output (+12 V) configuration efficiency data

Input (V AC/Hz)	Load percentage	P_{IN} (W)	V_{O1} (V)	I_{O1} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
85 V AC/60 Hz	0	0.038	12.000	0.000	0.000		
	10%	3.020	12.000	0.216	2.592	85.83	
	25%	7.331	12.000	0.545	6.540	89.21	88.66
	50%	14.772	12.000	1.096	13.152	89.03	
	75%	22.210	12.000	1.644	19.728	88.82	
	100%	30.040	11.984	2.195	26.305	87.57	
115 V AC/60 Hz	0	0.041	12.000	0.000	0.000		
	10%	3.050	12.000	0.216	2.592	84.98	
	25%	7.290	12.000	0.544	6.528	89.55	89.90
	50%	14.590	12.000	1.096	13.152	90.14	
	75%	21.910	12.000	1.644	19.728	90.04	
	100%	29.310	12.000	2.195	26.340	89.87	
230 V AC/50 Hz	0	0.053	12.000	0.000	0.000		
	10%	3.048	12.000	0.216	2.592	85.04	
	25%	7.436	12.000	0.544	6.528	87.79	89.67
	50%	14.630	12.000	1.096	13.152	89.90	
	75%	21.860	12.000	1.644	19.728	90.25	
	100%	29.020	12.000	2.195	26.340	90.76	
264 V AC/50 Hz	0	0.057	12.000	0.000	0.000		
	10%	3.085	12.000	0.216	2.592	84.02	
	25%	7.510	12.000	0.544	6.528	86.92	89.23
	50%	14.690	12.000	1.096	13.152	89.53	
	75%	21.920	12.000	1.644	19.728	90.00	
	100%	29.120	12.000	2.195	26.340	90.45	

Note: *Single-output (+12 V) configuration efficiency measurement was done by removing the LDO circuit (open X1) and DC-DC circuit (remove R34), and also shorting R20 on board. The overall circuit is not optimized for single-output configuration; the above efficiency data is for illustration only.*

Table 6 Standby power measurement

Test condition	Input condition	P_{IN}	V_{O1} (+12 V)	V_{O2} (+5 V)	V_{O3} (+15 V)	AC_ZR detection circuit
	(V AC/Hz)	(W)	(V)	(V)	(V)	(On/Off)
Condition 1	85 V AC/60 Hz	0.341	12.000	4.963	15.097	On
	115 V AC/60 Hz	0.368	12.000	4.965	15.097	
	230 V AC/50 Hz	0.566	12.000	4.963	15.100	
	264 V AC/50 Hz	0.649	12.000	4.965	15.100	
Condition 2	85 V AC/60 Hz	0.304	12.000	4.963	15.100	Off
	115 V AC/60 Hz	0.306	12.000	4.963	15.100	
	230 V AC/50 Hz	0.323	12.000	4.963	15.100	
	264 V AC/50 Hz	0.335	12.000	4.965	15.100	
Condition 3	85 V AC/60 Hz	0.169	12.000	4.965	Disabled	
	115 V AC/60 Hz	0.172	12.000	4.968		
	230 V AC/50 Hz	0.186	12.000	4.968		
	264 V AC/50 Hz	0.191	12.000	4.968		
Condition 4	85 V AC/60 Hz	0.038	12.000	Disabled		
	115 V AC/60 Hz	0.041	12.000			
	230 V AC/50 Hz	0.053	12.000			
	264 V AC/50 Hz	0.057	12.000			

Note: Standby power was measured under four different test conditions, below; there is no load at any output throughout testing:

- Condition 1: power on as per original board delivered with all features and outputs enabled;
- Condition 2: disable AC ZCD circuit, enable 12 V, 5 V and 15 V outputs;
- Condition 3: disable AC ZCD circuit and 15 V LDO circuit, enable 12 V and 5 V outputs;
- Condition 4: test under single output (+12 V) configuration.

9.1 Efficiency curve

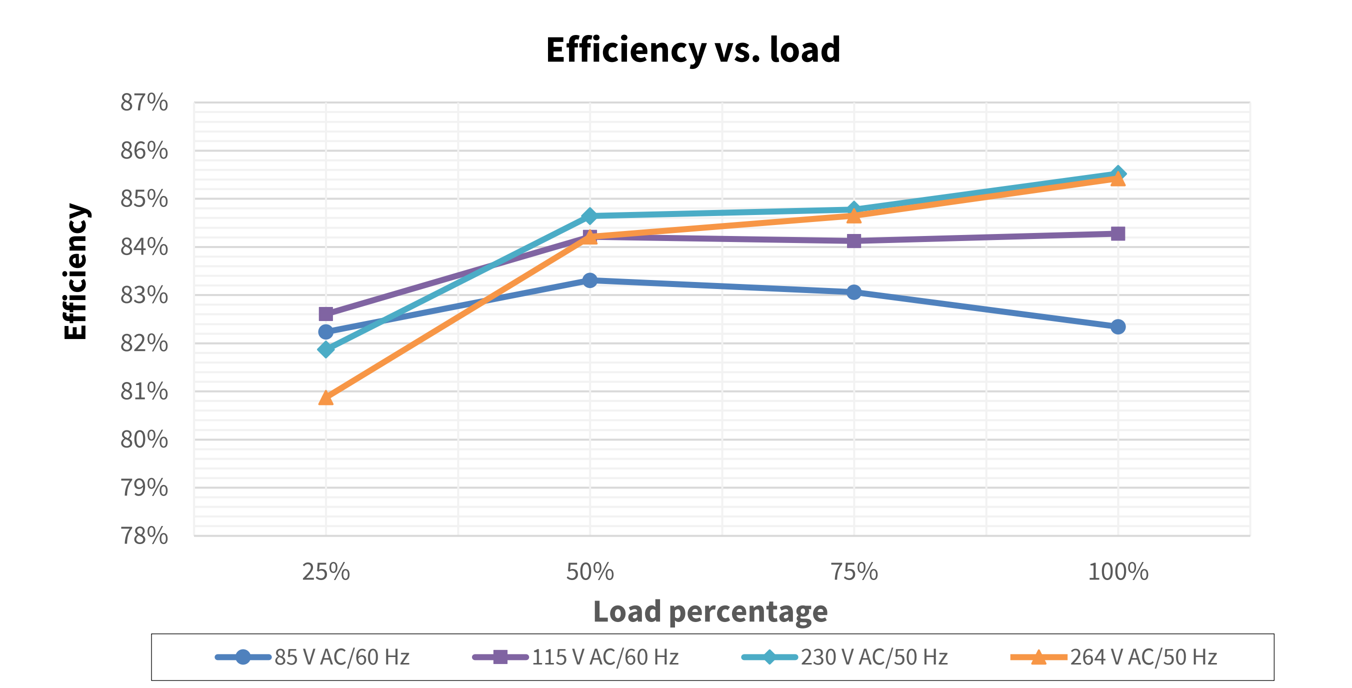


Figure 9 **Efficiency curve**

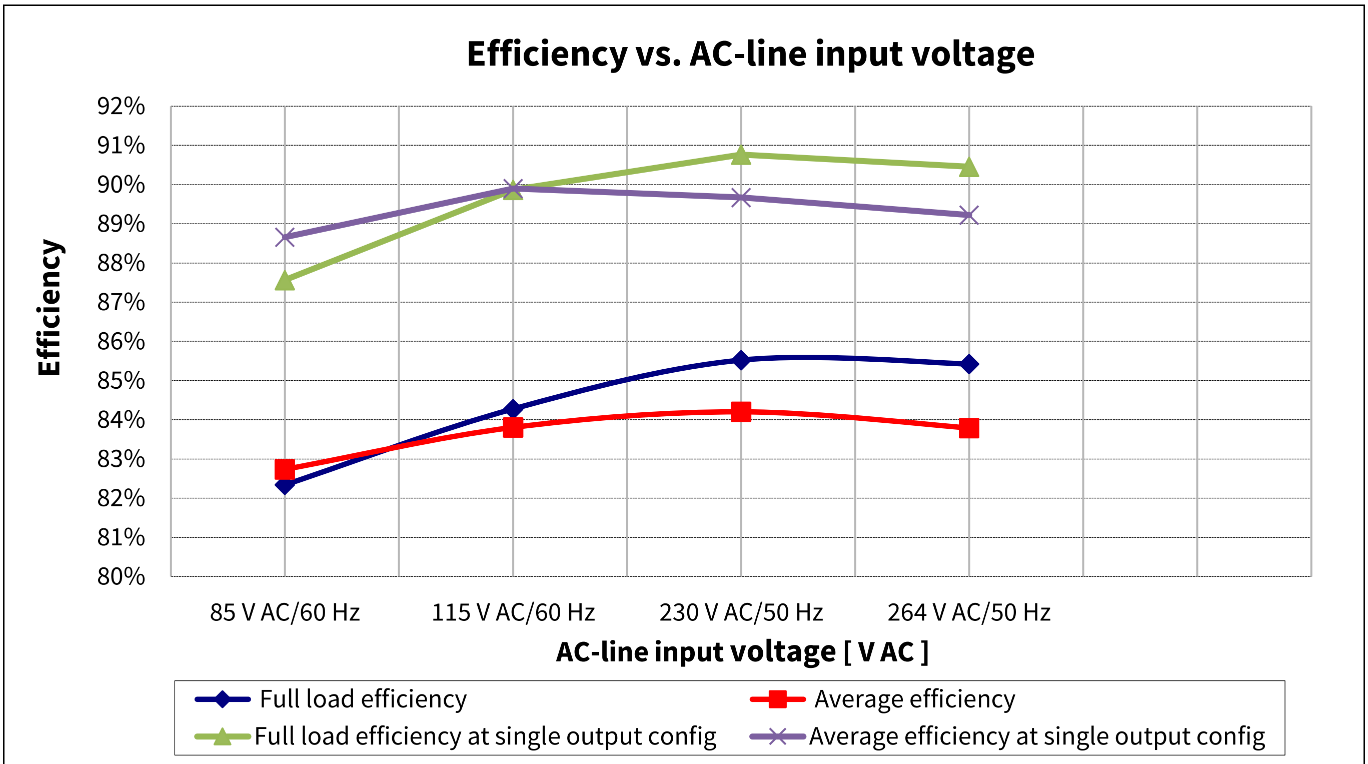


Figure 10 **Efficiency vs. AC-line input voltage**

9.2 Line and load regulation

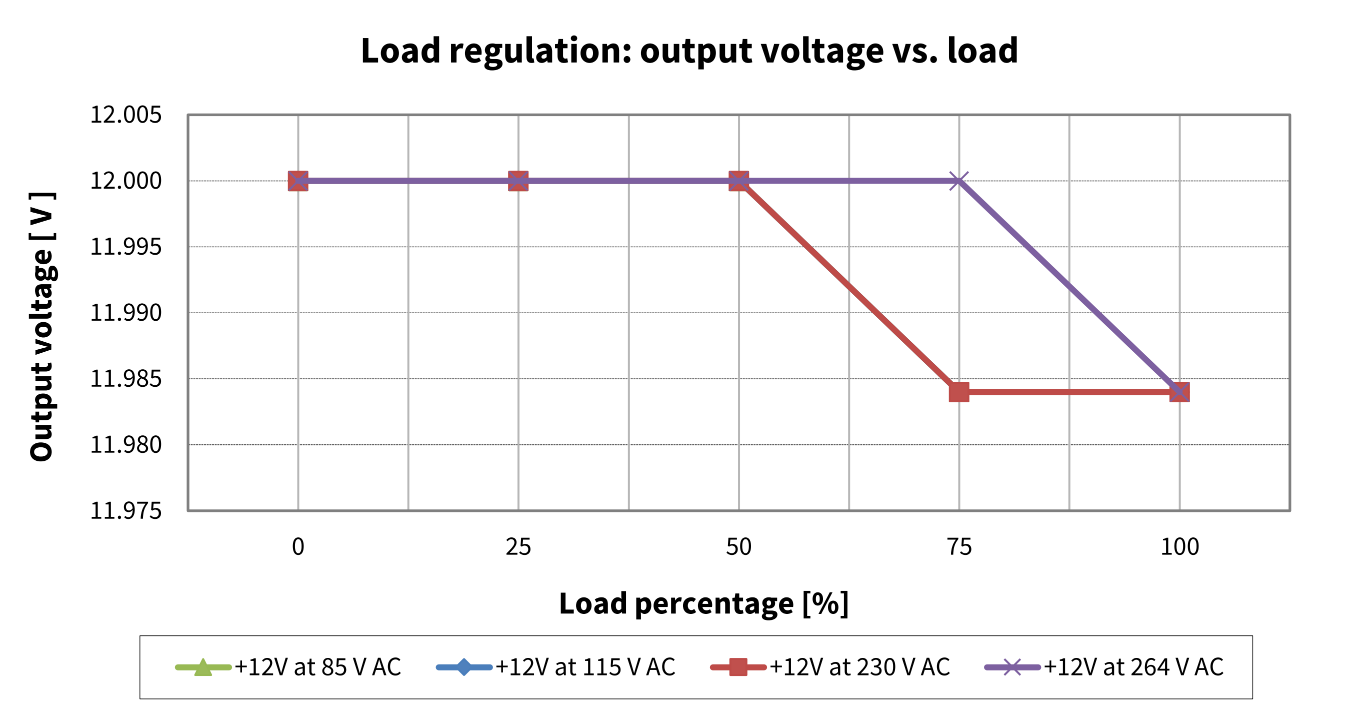


Figure 11 Line and load regulation (+12 V output)

9.3 Standby power

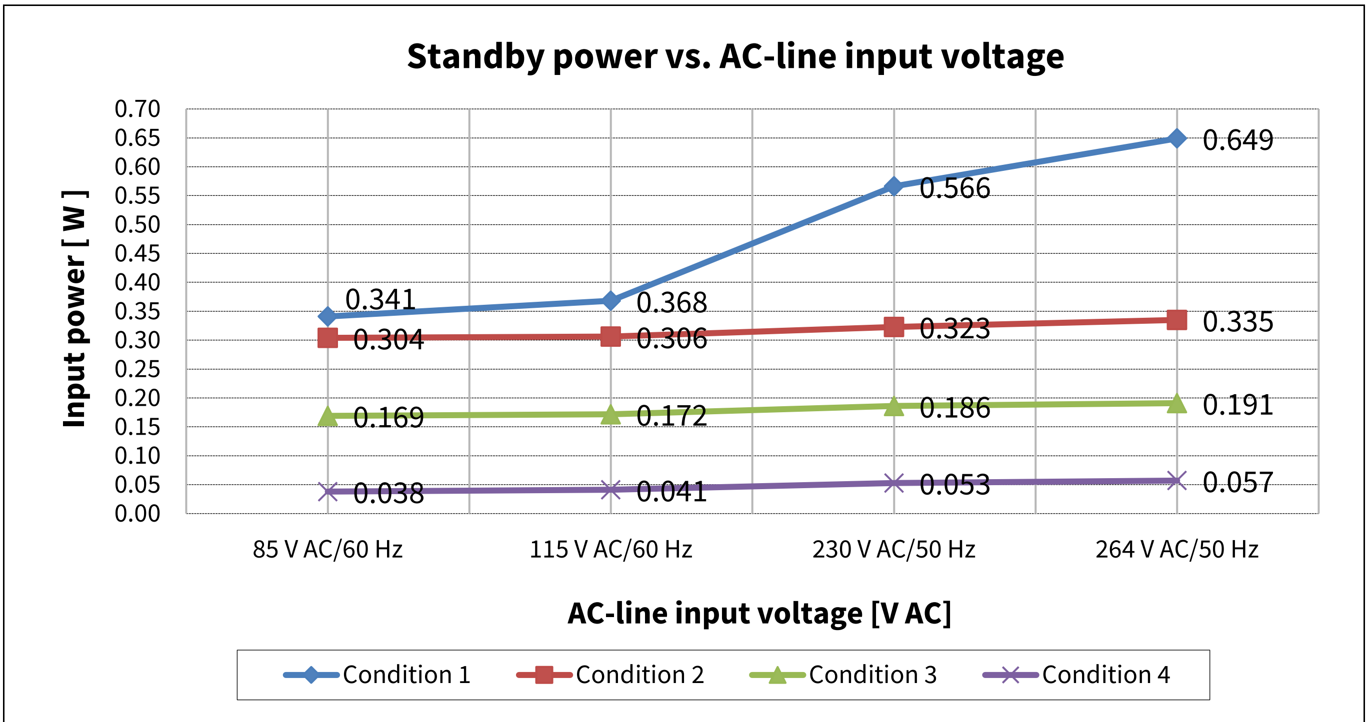


Figure 12 Standby power vs. AC-line input voltage (refer to page 18 for all conditions)

9.4 Maximum input power

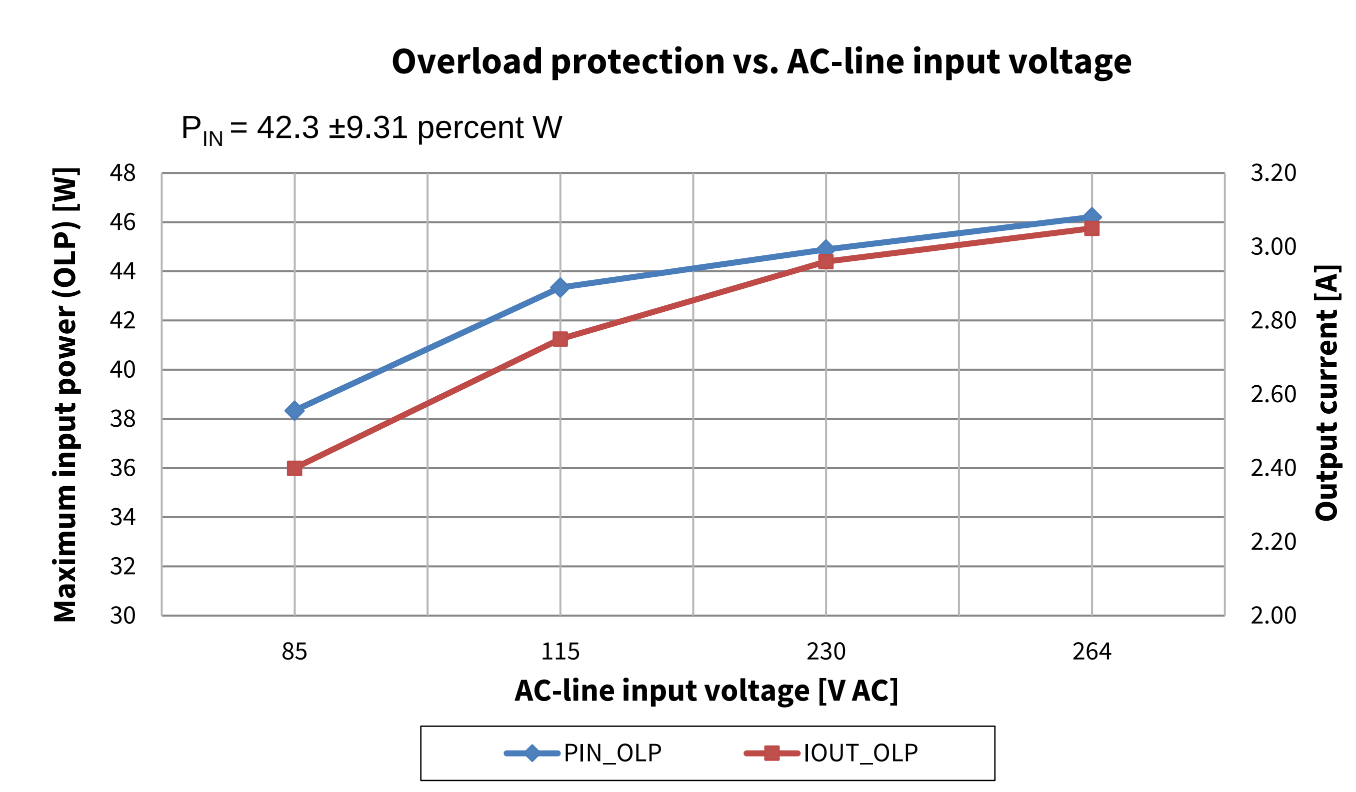


Figure 13 Maximum input power (before overload protection) vs. AC-line input voltage

9.5 ESD immunity (EN 61000-4-2)

This system was subjected to ESD testing according to EN 61000-4-2 level 3 (±6 kV contact and ±8 kV air discharge). It was tested at full load (resistive load). A test failure was defined as non-recoverable.

Table 7 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			V_{OUT1}	Com	
115/230 V AC, 30 W	Contact	±6 kV	10	10	Pass
	Air	±8 kV	10	10	Pass

9.6 Surge immunity (EN 61000-4-5)

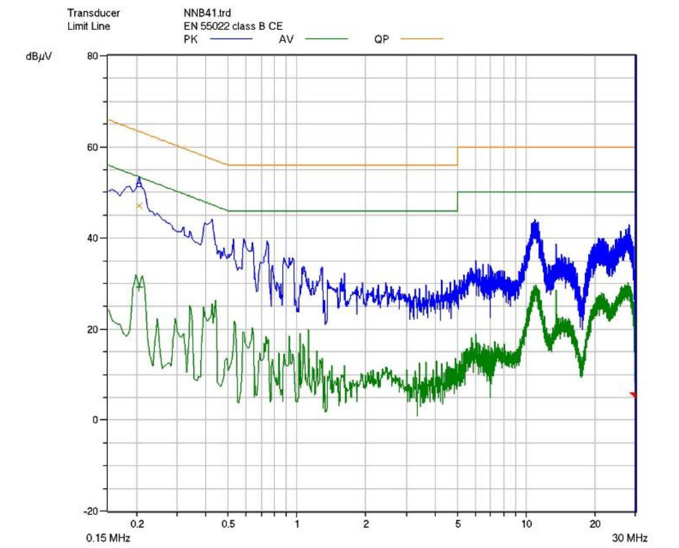
The reference board was subjected to a surge immunity test (±2 kV DM and ±4 kV CM) according to EN 61000-4-5. It was tested at full load (resistive load). A test failure was defined as non-recoverable.

Table 8 System lightning surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
115/230 V AC, 30 W	DM	±2 kV	L → N	3	3	3	3	Pass
	CM	±4 kV	L → G	3	3	3	3	Pass
		±4 kV	N → G	3	3	3	3	Pass

9.7 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board was tested at full load (resistive load) at input voltages of 115 V AC and 230 V AC.



Final Measurement Results: * = Limit exceeded

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2040	L	51.8	L	29.2	L	47.2	53.4	63.4

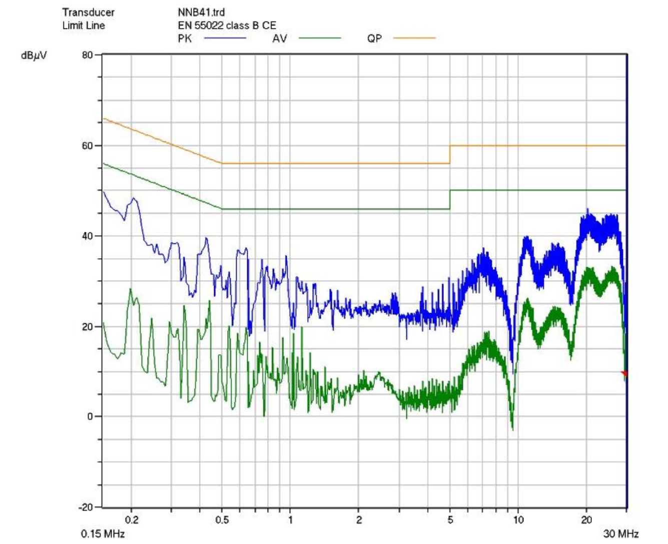
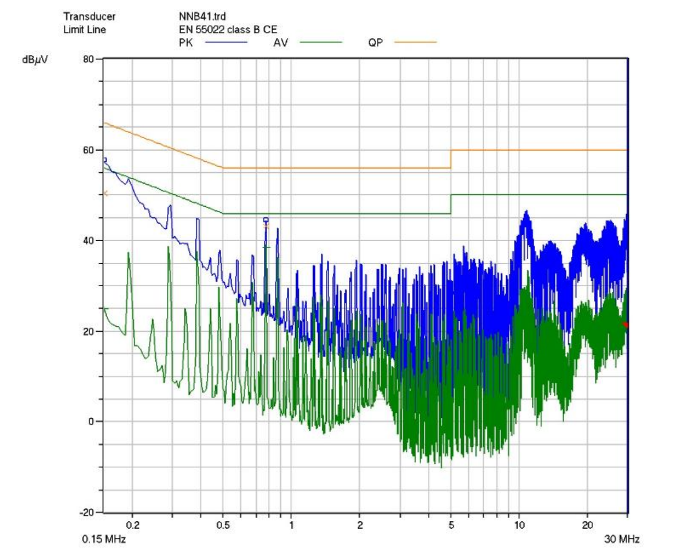
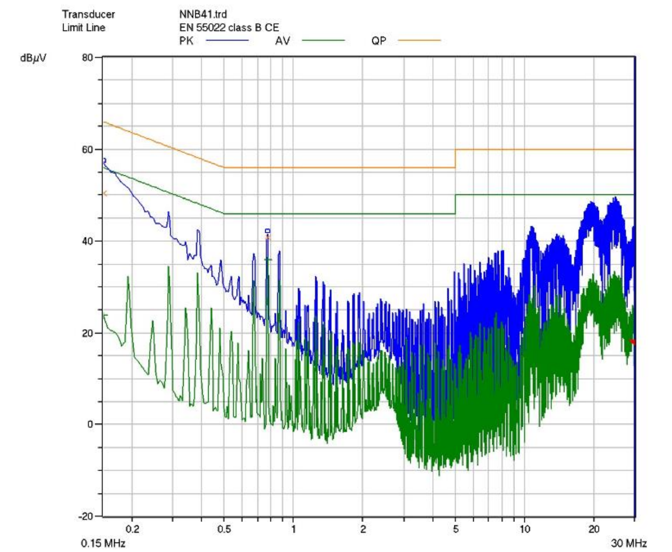


Figure 14 Conducted emissions at 115 V AC and full load on line (left) and neutral (right)



Final Measurement Results: * = Limit exceeded

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.1500	L	57.8	L	24.8	L	50.4	56.0	66.0
0.7680	L	44.5	L	38.5	L	43.2	46.0	56.0



Final Measurement Results: * = Limit exceeded

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.1500	L	57.6	L	23.9	L	50.4	56.0	66.0
0.7680	L	42.1	L	36.0	L	40.8	46.0	56.0

Figure 15 Conducted emissions at 230 V AC and full load on line (left) and neutral (right)

9.8 Thermal measurement

The thermal testing of the reference board was done in the open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of particular components. The measurements were taken at the maximum load running for one hour. The tested input voltages were 85 V AC and 264 V AC.

Table 9 Component temperature at full load under T_{amb} = 25°C

Circuit code	Major component	85 V AC (°C)	264 V AC (°C)
L1	Input CMC choke	56.3	38.5
TR1	Main transformer	61.8	70.5
D1	Bridge diode	63.1	45.9
U1	ICE5QR1680BG	95.2	82.6
Q1	SR MOSFET	59.3	63.5

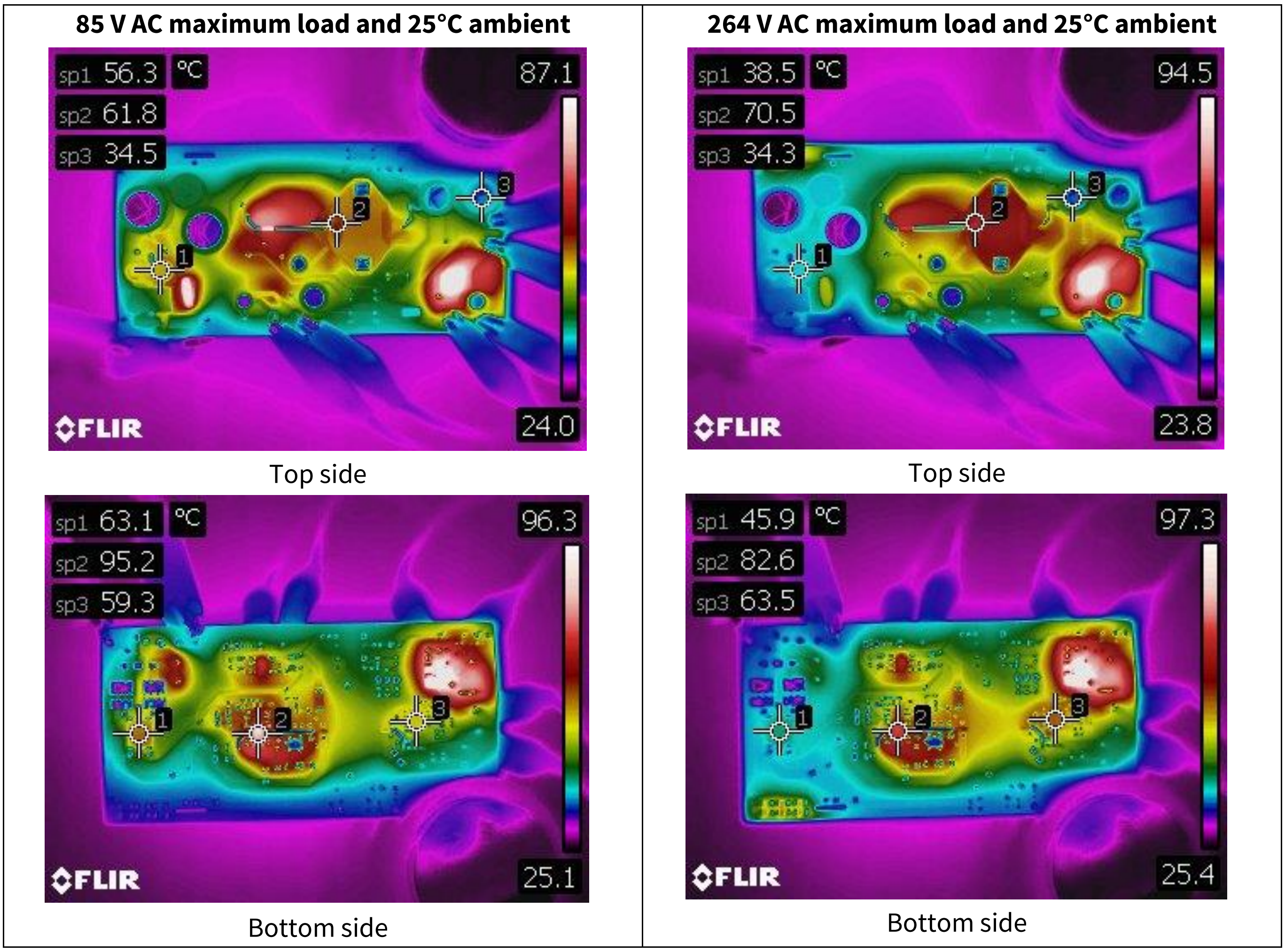
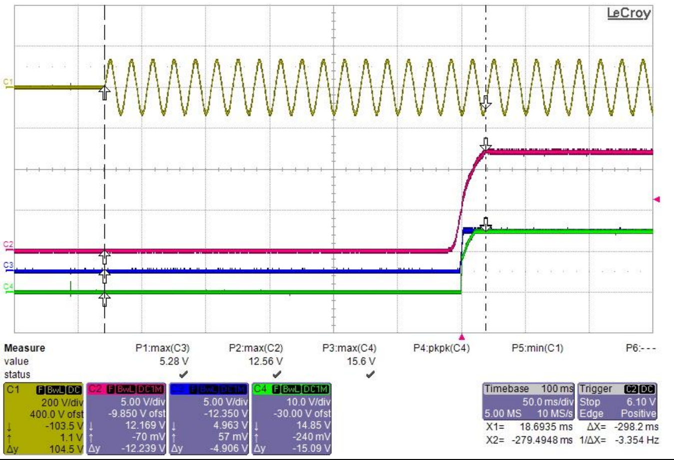


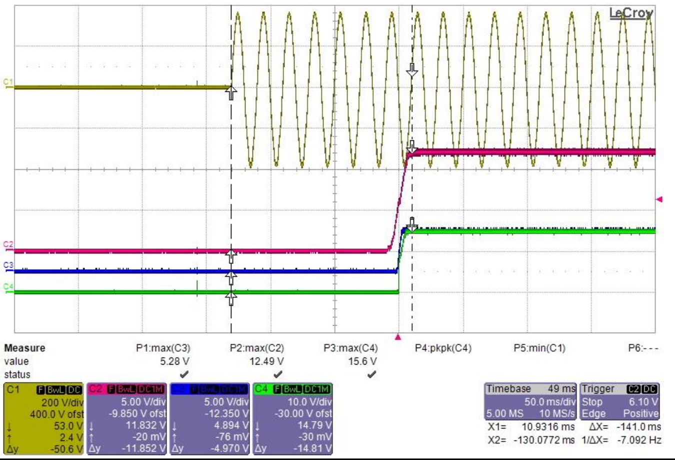
Figure 16 Infrared thermal image of REF_5QR1680BG_30W1

10 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 44Xi oscilloscope.

10.1 Start-up at full load

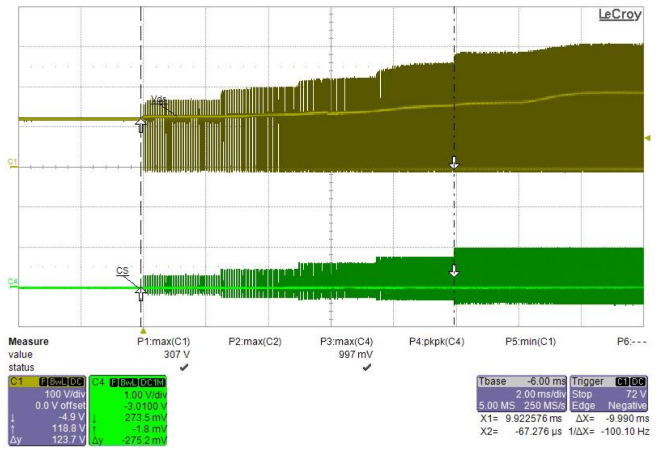


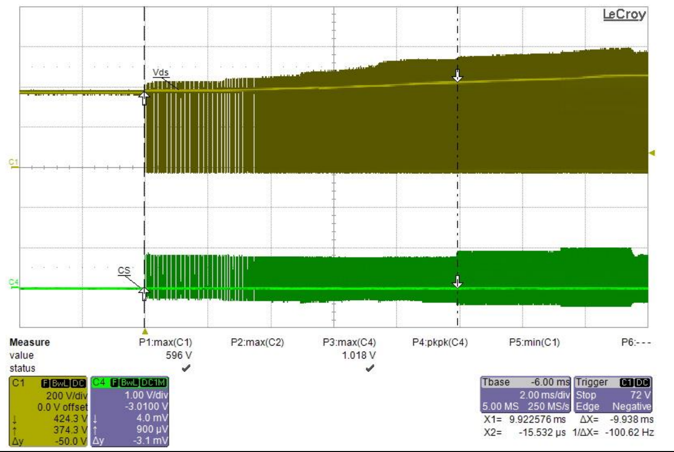


C1 (yellow) : AC-line voltage C2 (purple) : +12 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +15 V output voltage	C1 (yellow) : AC-line voltage C2 (purple) : +12 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +15 V output voltage
85 V AC start-up time at full load is around 298 ms	264 V AC start-up time at full load is around 141 ms

Figure 17 Start-up at full load

10.2 Soft-start at full load

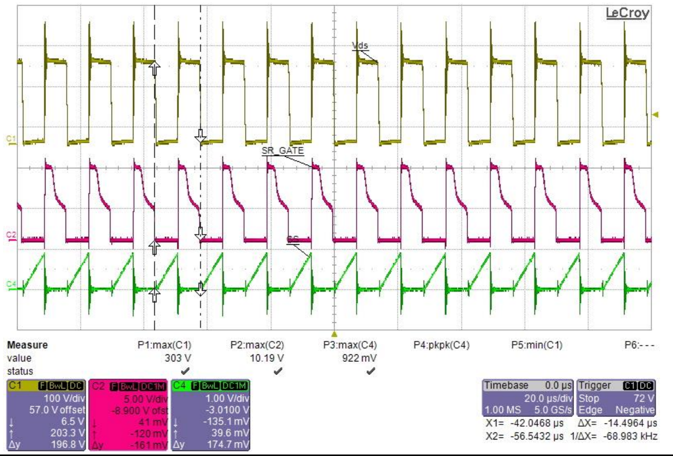


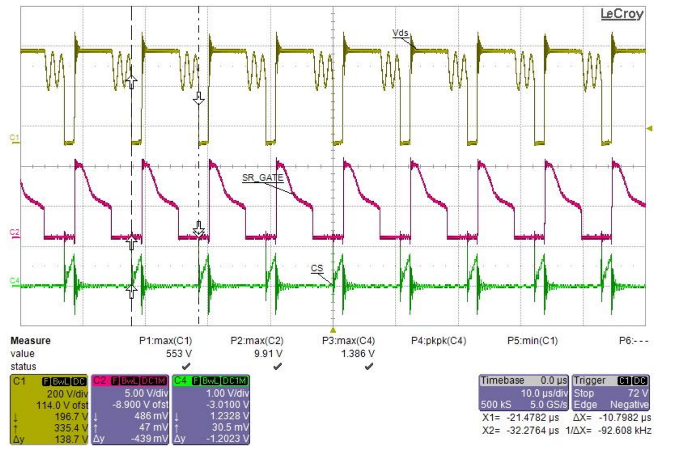


C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
85 V AC soft-start at full load within ~10 ms	264 V AC soft-start time at full load within ~10 ms

Figure 18 Soft-start at full load

10.3 Switching waveform at full load

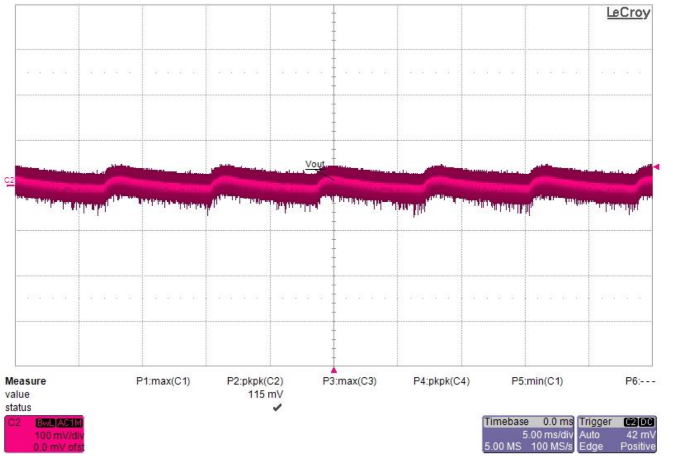


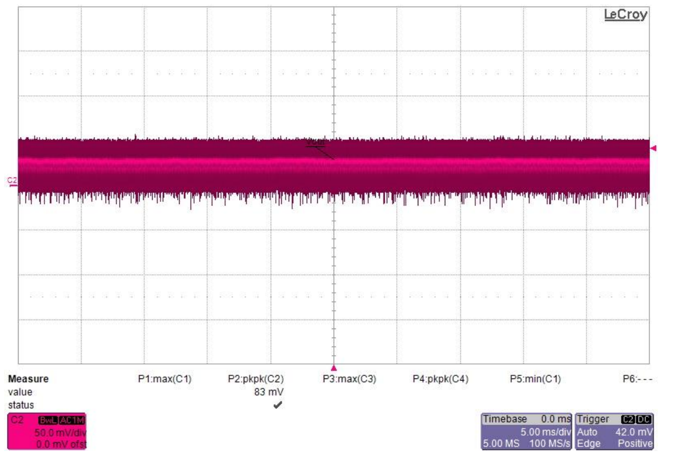


C1 (yellow) : Drain voltage (V_D) C2 (purple) : SR gate signal C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : SR gate signal C4 (green) : CS voltage (V_{CS})
V_{IN} = 85 V AC, full load; the first ZC is measured (highest ZC at low-line) Switching frequency is around 69 kHz	V_{IN} = 264 V AC, full load; the third ZC is measured (highest ZC at high-line) Switching frequency is around 92 kHz

Figure 19 Switching waveform at full load

10.4 Output ripple voltage at full load





C2 (purple) : +12 V output ripple voltage	C2 (purple) : +12 V output ripple voltage
Input 85 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 115 mV	Input 264 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 83 mV

Figure 20 Output ripple voltage at full load (20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.5 Output ripple voltage in ABM

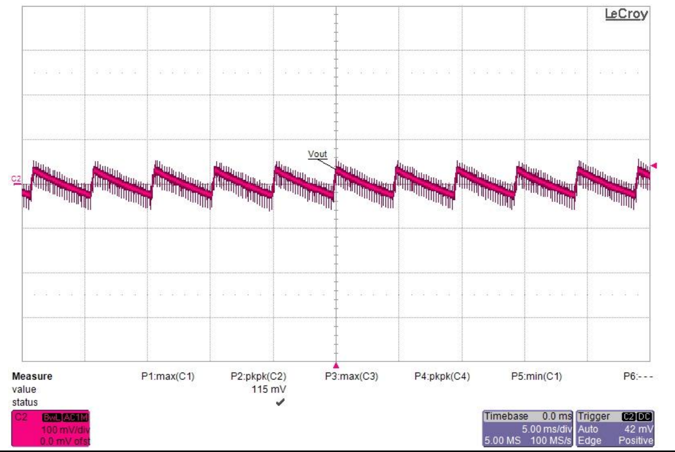
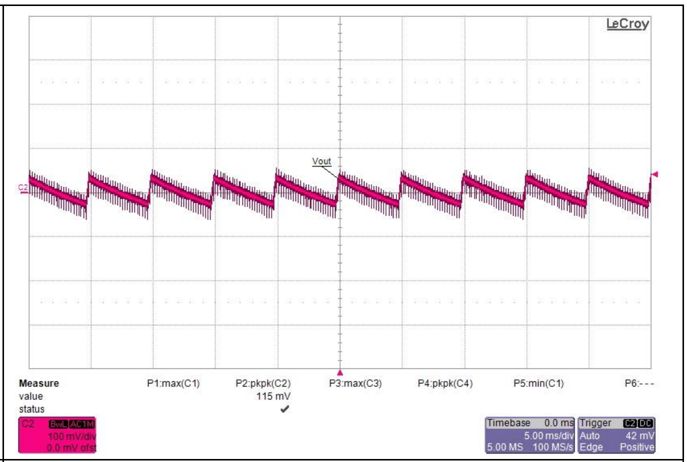
	
C2 (purple) : +12 V output ripple voltage	C2 (purple) : +12 V output ripple voltage
Input 85 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 115 mV	Input 264 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 115 mV

Figure 21 Output ripple voltage in ABM (20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.6 Load-transient response

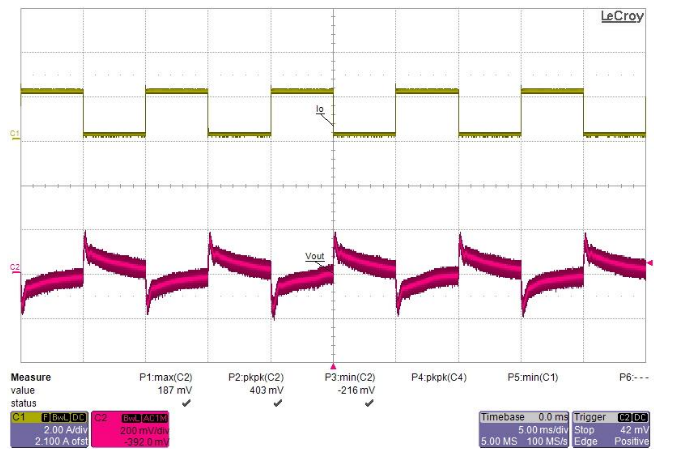
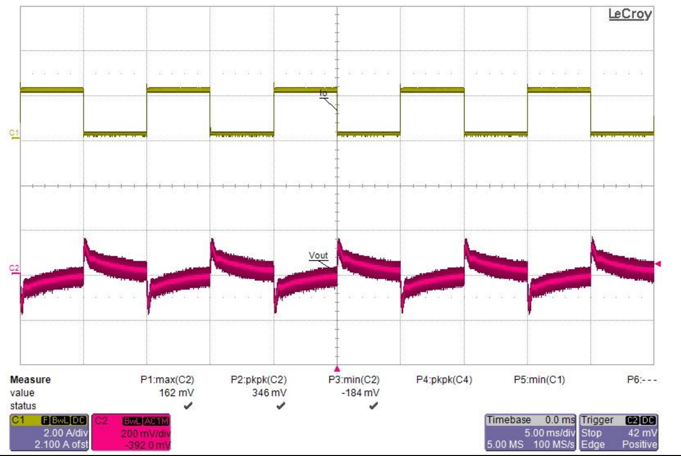
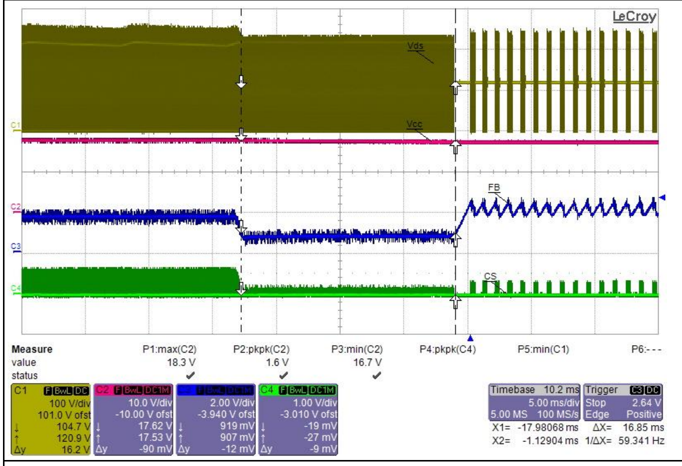
	
C4 (yellow) : Load current C2 (purple) : +12 V output voltage	C4 (yellow) : Load current C2 (purple) : +12 V output voltage
Input 85 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 216 mV	Input 264 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 184 mV

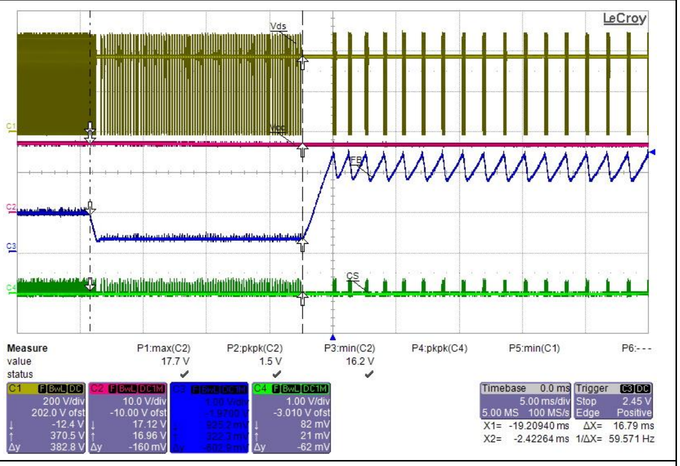
Figure 22 Load-transient response (+12 V output load change from 10 percent to 100 percent at 0.4 A/µs slew rate, 100 Hz, +15 V output and +5 V output load are fixed at full load; 20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.7 Entering ABM



C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : Feedback voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

Condition to enter ABM level 1: V_{FB} less than 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = ~20 ms
(load change from 5 W to 0.5 W at 85 V AC)

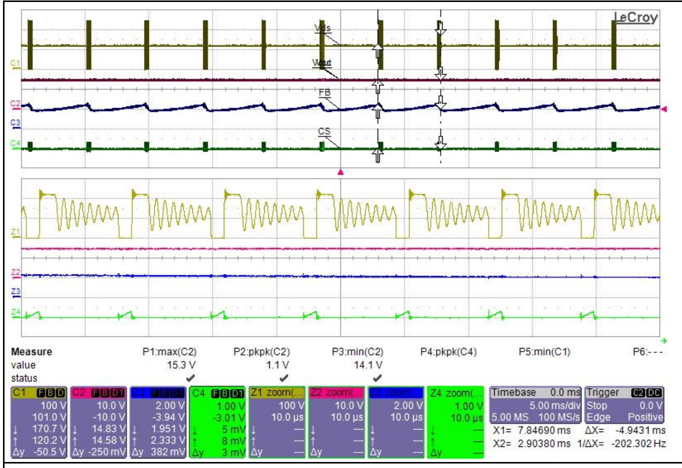


C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : Feedback voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

Condition to enter ABM level 1: V_{FB} less than 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = ~20 ms
(load change from 5 W to 0.5 W at 264 V AC)

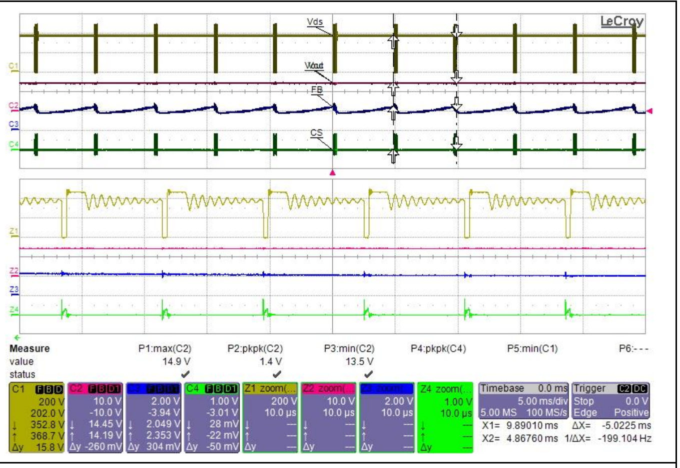
Figure 23 **Entering ABM**

10.8 During ABM



C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : Feedback voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

During ABM level 1: V_{FB_Bon} = 2.4 V
V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8
(no load at 85 V AC)



C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : Feedback voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

During ABM level 1: V_{FB_Bon} = 2.4 V
V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10
(no load at 264 V AC)

Figure 24 **During ABM**

10.9 Leaving ABM

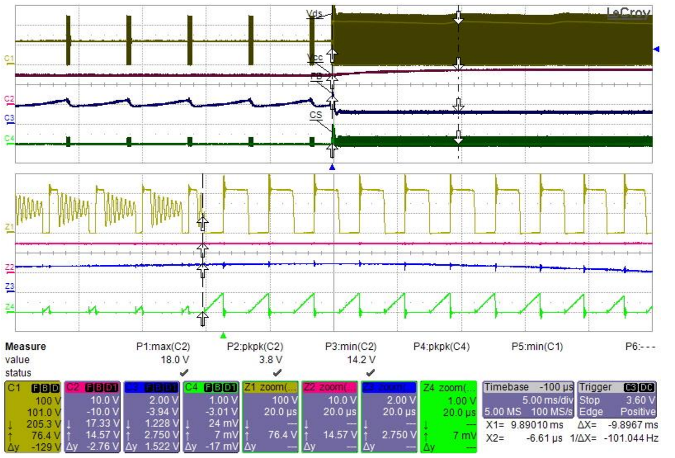
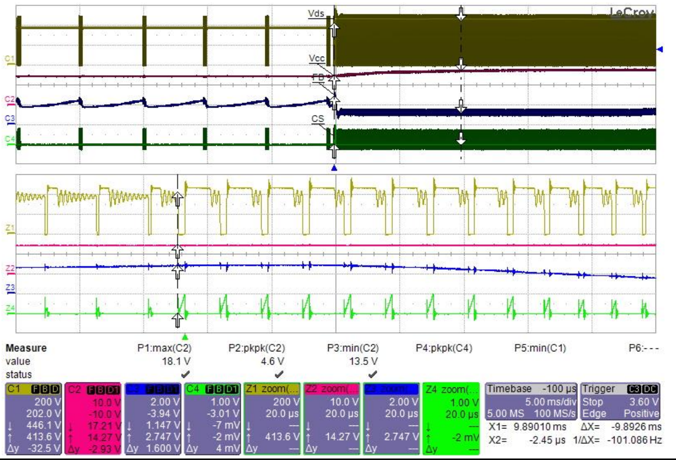
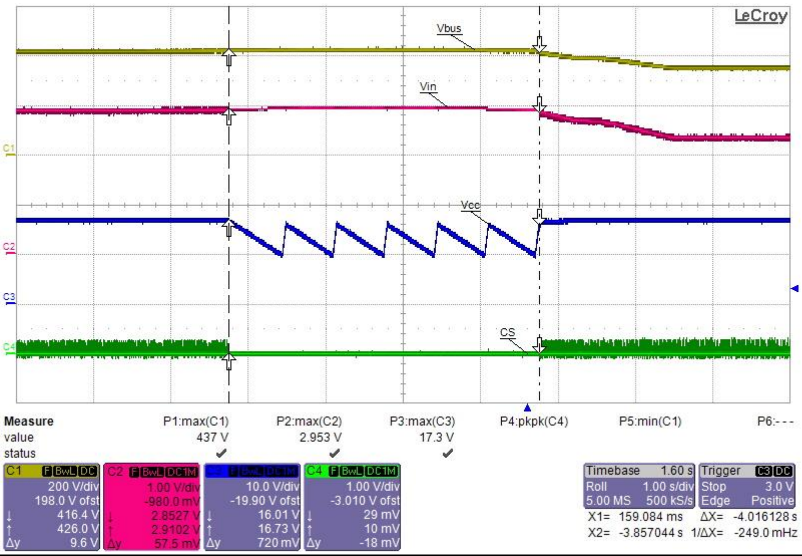
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : Feedback voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : Feedback voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Condition to leave ABM: V_{FB} more than 2.75 V (load change from no load to full load at 85 V AC)	Condition to leave ABM: V_{FB} more than 2.75 V (load change from no load to full load at 264 V AC)

Figure 25 **Leaving ABM**

10.10 LOVP

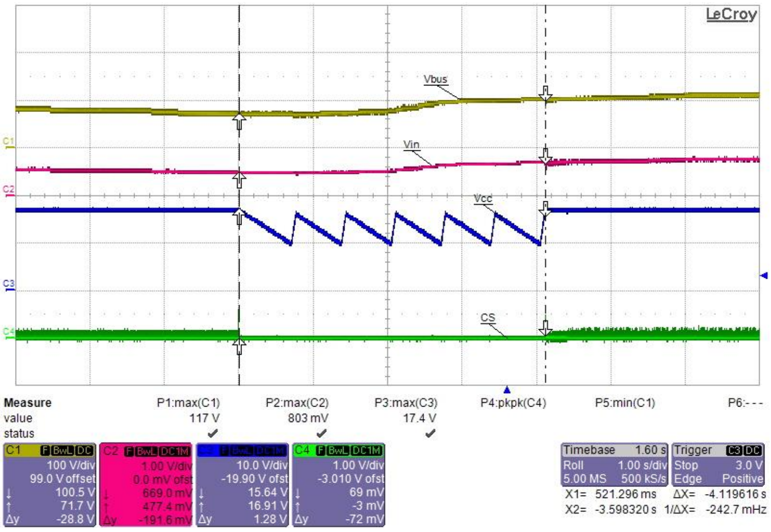


C1 (yellow) : Bulk capacitor voltage (V_{Bulk})
C2 (purple) : V_{IN} voltage (V_{VIN})
C3 (blue) : Supply voltage (V_{VCC})
C4 (green) : CS voltage (V_{CS})

Condition to detect LOVP: V_{VIN} more than 2.9 V
Condition to reset LOVP: V_{VIN} less than 2.9 V

Figure 26 **LOVP**

10.11 Brown-out protection

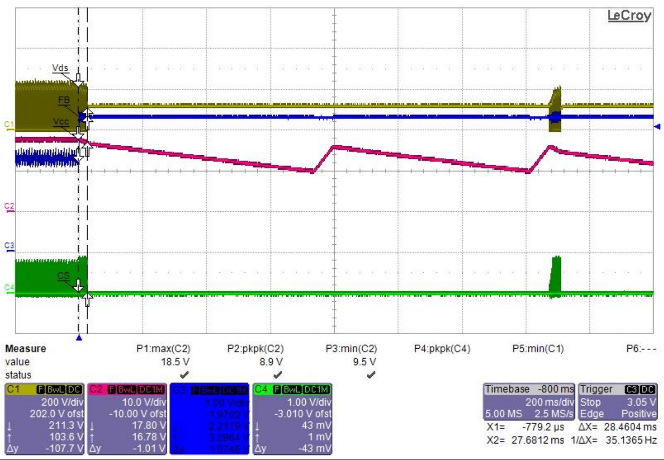


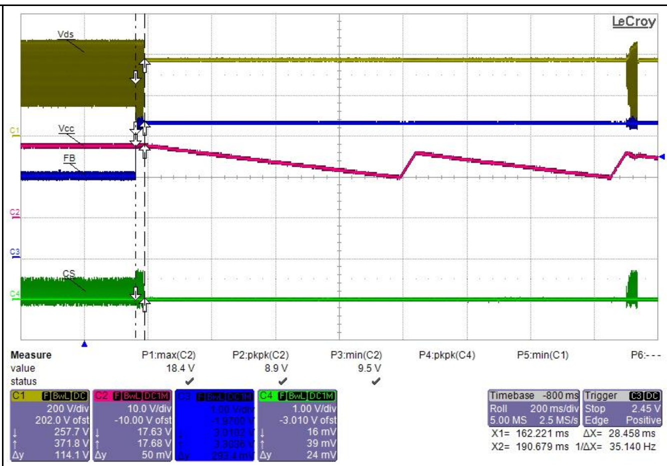
C1 (yellow)	: Bulk capacitor voltage (V_{Bulk})
C2 (purple)	: V_{IN} pin voltage (V_{VIN})
C3 (blue)	: Supply voltage (V_{VCC})
C4 (green)	: CS voltage (V_{CS})

Condition to reset brown-out protection (brown-in): V_{VIN} more than 0.66 V
Condition to detect brown-out protection: V_{VIN} less than 0.4 V and $t_{blanking}$ = ~250 µs

Figure 27 Brown-out protection

10.12 Overload protection

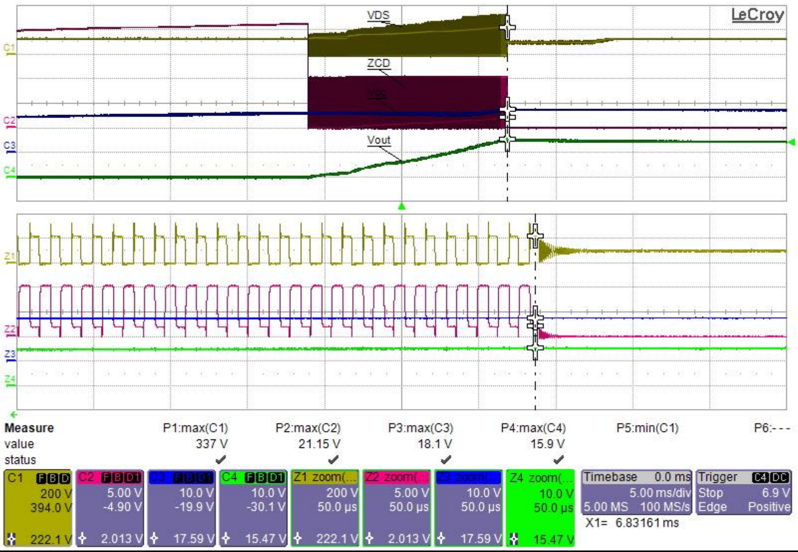




C1 (yellow) : Drain voltage C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC Trigger protection at FB pin voltage greater than 2.75 V (V_{FB_OLP}) for approximate 30 ms ($t_{FB\_OLP\_B}$)	264 V AC Trigger protection at FB pin voltage greater than 2.75 V (V_{FB_OLP}) for approximate 30 ms ($t_{FB\_OLP\_B}$)

Figure 28 OLP

10.13 Output OV protection

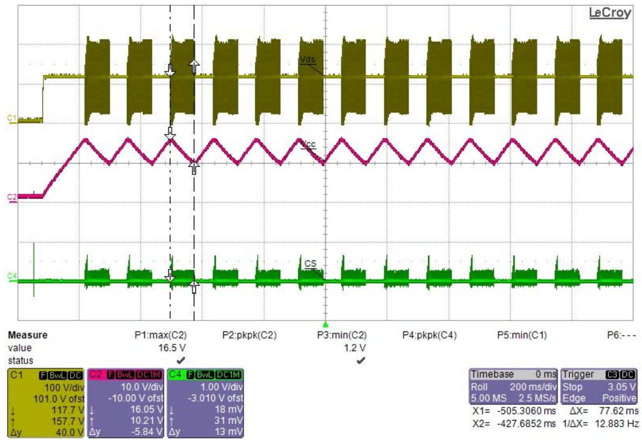


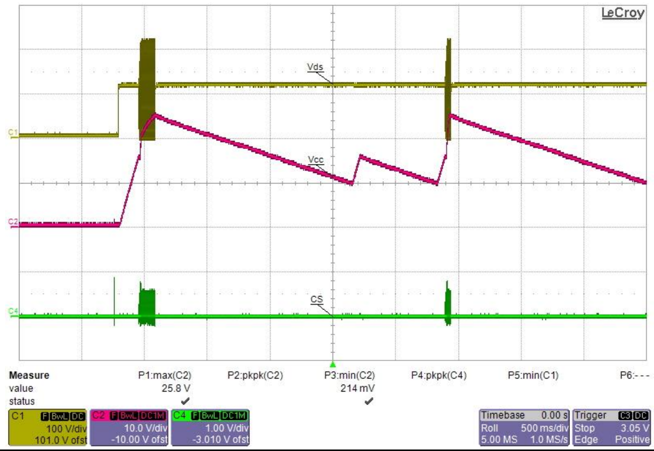
C1 (yellow) : Drain voltage (V_D)
C2 (purple) : ZCD voltage (V_{ZCD})
C3 (blue) : Supply voltage (V_{VCC})
C4 (green) : +12 V output voltage (V_{O1})

Condition to enter output OVP: V_{ZCD} more than 2 V for 10 consecutive pulses (V_{O1} more than ~15 V)
(85 V AC, short R32 during system operation at no load)

Figure 29 Output OVP

10.14 V_{CC} OV/UV protection





C1 (yellow) : Drain voltage C2 (purple) : Supply voltage (V_{VCC}) C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : Supply voltage (V_{VCC}) C4 (green) : CS voltage
85 V AC at full load Trigger V_{CC} UVP at V_{CC} voltage less than 10 V (V_{VCC_OFF}) Auto restart mode (open R20)	85 V AC start-up at full load Trigger V_{CC} OVP at V_{CC} voltage greater than 25.5 V (V_{VCC_OVP}), odd-skip auto restart mode (short R20 and remove D8)

Figure 30 V_{CC} OVP/UVP

10.15 ZCD

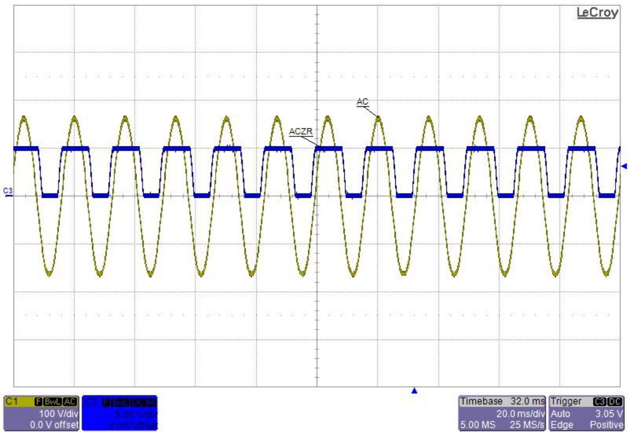
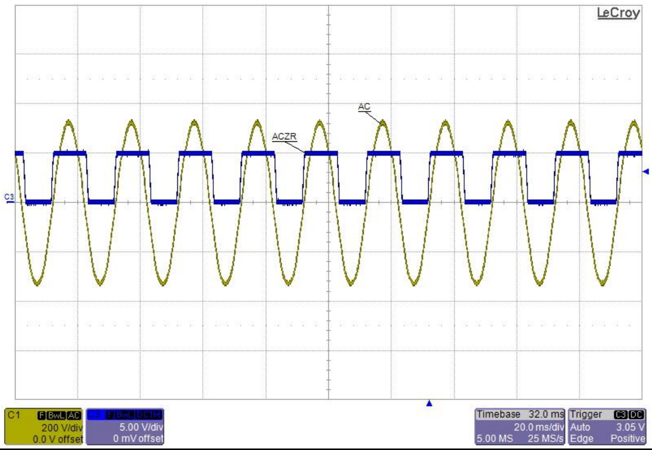
	
C1 (yellow) : AC input C2 (purple) : ACZR	C1 (yellow) : AC input C2 (purple) : ACZR
Input 115 V AC	Input 230 V AC
AC ZCD circuit is an optional circuit, which can be disabled by removing X2	

Figure 31 AC zero-crossing signal

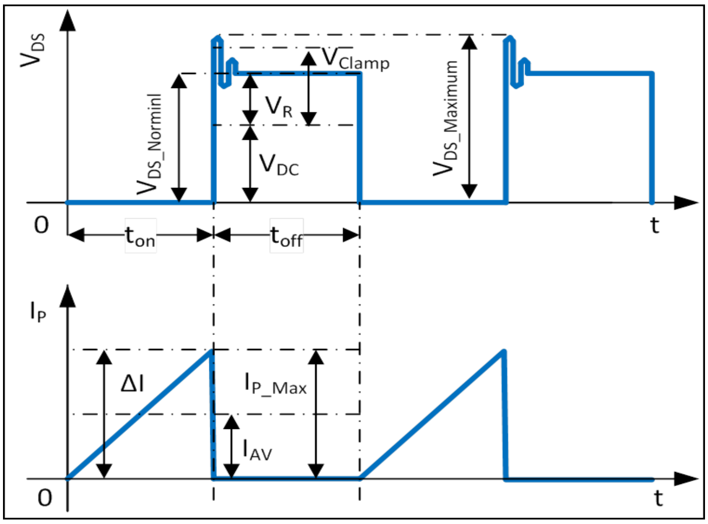
11 Appendix A: Transformer design and spreadsheet [2]

Design procedure for QR flyback converter using Q5 CoolSET™ 5QRxxxxAx (version 1.1)

Project:	ICE5QR1680BG
Application:	30 W aux SMPS for refrigerator application
CoolSET™:	ICE5QR1680BG
Date:	Feb. 22, 2022
Revision:	1.0
Note:	AC zero-crossing circuit, LDO-related circuit and DC-DC circuit are not taken into consideration in this spreadsheet

Enter design variables in orange-colored cells
Read design results in green-colored cells
Equation numbers are according to the application note; some changes are made for this specified design

			Unit	Value
Input	Minimum AC input voltage	V_{ACMin}	[V]	85
Input	Maximum AC input voltage	V_{ACMax}	[V]	264
Input	Line frequency	f_{AC}	[Hz]	60
Input	Bus capacitor (C13) DC ripple voltage	$V_{DCRIPPLE}$	[V]	25
Input	Output voltage 1	V_{OUT1}	[V]	12
Input	Output current 1	I_{OUT1}	[A]	2.2
Input	Output ripple voltage	$V_{OUT\ Ripple}$	[V]	0.12
Input	Maximum output power for start-up, transient response and OLP	P_{OUTMax}	[W]	33
Input	Nominal output power	P_{OUTNor}	[W]	29.10
Input	Minimum output power	P_{OUTMin}	[W]	0.5
Input	Efficiency	η		0.87
Result	Drain-to-source capacitance of MOSFET (including $Co_{(er)}$ of MOSFET)	$C_{DS}+Co_{(er)}$	[pF]	8.00



			Unit	Value
Input	Reflection voltage	V_R	[V]	96
Input	V_{CC} voltage	V_{VCC}	[V]	18
Input	Forward voltage of V_{CC} diode (D12)	$V_{FDiodeVCC}$	[V]	0.3
Input	CoolSET™ -Q5	CoolSET™ -Q5		ICE5QR1680BG
Input	Low-line min. switching frequency	f_S	[Hz]	65000
Input	Targeted max. drain-source voltage	V_{DSMax}	[V]	700
Input	Max. ambient temperature	T_a	[°C]	50
Diode bridge (BR1)				
Result	Eq 1	P_{INMax}	[W]	37.93
Result	Eq 2	I_{AC_RMS}	[A]	0.744
Result	Eq 3	$V\ DC_{Max\_Pk}$	[V]	373.35
Result	Eq 4	$V\ DC_{Min\_Pk}$	[V]	120.21
Result	Eq 10	$V\ DC_{Min}$	[V]	95.55

Result	Eq 6	T_D	[ms]	6.59
Result	Eq 7	W_{IN}	[Ws]	0.25
Result	Eq11	D_{Max}		0.5012
Input capacitor (C13)				
Result	Eq 8	C_{IN} (C13)	[µF]	92.85
Input	Select input capacitor	C_{IN} (C13)	[µF]	94
Transformer (TR1)				
Result	Eq 12	L_P	[H]	4.537E-04
Result	Eq 13	I_{AV}	[A]	0.79
Result	Eq 14	ΔI	[A]	1.624
Result	Eq 15	I_{P_Max}	[A]	1.60
Result	Eq 16	I_{Valley}	[A]	0.0
Result	Eq 17	I_{P_RMS}	[A]	0.65
Select core type				
Input	Select core type			10
		Core type		User-defined core
		Core material		0
	Maximum flux density	B_{Max}	[T]	0.3
	Effective magnetic cross-section	A_e	[mm²]	52
	Bobbin width	BW	[mm]	9.14
	Winding cross-section	A_N	[mm²]	31.35
	Average length of turn	l_N	[mm]	44.6
Winding calculation				
Result	Eq 18	N_P	Turns	46.65
Input	Choose number of primary turns	N_P	Turns	48
Result	Eq 19	N_{S1}	Turns	6.00
Input	Choose number of secondary turns	N_{S1}	Turns	6
Result	Eq 20	N_{VCC}	Turns	9.15
Input	Choose number of auxiliary turns	N_{VCC}	Turns	9
Result	Auxiliary supply voltage (Eq 21)	V_{VCC}	[V]	17.70
Post calculation				
Result	Eq 23	V_R	[V]	96.0
Result	Eq 24	D_{Max}		0.50
Result	Eq 25	D_{Max}'		0.49
Result	Eq 26	B_{Max}	[T]	0.292
CS resistor				
Input	CS threshold value from datasheet	V_{csth}	[V]	1
Result	Eq 21	R_{Sense}	[Ω]	0.62
Result	Eq 22	P_{SR}	[W]	0.26
Input	PWM-OP gain from datasheet	G_{PWM}		2.05
Result	Eq 94	Z_{PWM}	[V/A]	1.3
Transformer winding design				
Input	Margin according to safety standard	M	[mm]	0
Input	Copper space factor	f_{Cu}		0.4
Primary				
Input	Insulation thickness	INS	[mm]	0.02
Result	Eq 32	A_p (area of primary wire)	[mm²]	0.13
Result	Eq 36	Dia. (diameter of primary wire)	[mm]	0.41
Result	Eq 35	AWG		26
Input	Selected wire size	AWG		27
Input	Number of parallel wires	Np		1
Result	Eq 37	Dia. (diameter of primary wire)	[mm]	0.36
Result	Eq 38	(Eff. copper area of primary)	[mm²]	0.1034
Result	Eq 39	Sp (primary current density)	[A/mm²]	6.30
Result	Eq 30	BW_e (effective bobbin width)	[mm]	9.1
Result	Eq 40	Od_p (diameter of primary wire including insulation)	[mm]	0.40
Result	Eq 41	NL_P (max. primary turns/layer)	Turns/layer	22
Result	Eq 42	Ln_P (primary layers)	Layers	3

Secondary				
Input	Insulation thickness	INS	[mm]	0.02
Result	Eq 33	A_S (area of secondary wire)	[mm²]	0.94
Result	Eq 36	Dia. (diameter of secondary wire)	[mm]	1.09
Result	Eq 35	AWG		17
Input	Selected wire size	AWG		22
Input	Number of parallel wires	Np		2
Result	Eq 37	Dia. (diameter of secondary wire)	[mm]	0.65
Result	Eq 38	(Eff. copper area of secondary)	[mm²]	0.6564
Result	Eq 39	S_S (secondary current density)	[A/mm²]	7.92
Result	Eq 30	BW_E (effective bobbin width)	[mm]	9.1
Result	Eq 40	Od_S (diameter of secondary wire including insulation)	[mm]	0.69
Result	Eq 41	NL_S (max. secondary turns/layer)	Turns/layer	6
Result	Eq 42	Ln_S (secondary layers)	Layers	1
Leakage inductance				
Input		Leakage inductance as percentage of L_P	[%]	1
Result	Eq 45	L_{LK}	[H]	4.54E-06
RCD clamper circuit				
Result	Eq 44	V_{clamp}	[V]	230.65
Result	Eq 46	C_{clamp} (C15)	[nF]	0.2
Input	Selected C_{clamp} capacitor value	C_{clamp} (C15)	[nF]	1
Result	Eq 47	R_{clamp} (R11)	[kΩ]	257
Input	Selected R_{clamp} value	R_{clamp} (R11)	[kΩ]	300
Output and V_{CC} diodes				
Result	Eq 43a	V_{SR_MOS} (for output SR MOSFET)	[V]	58.67
Result	Eq 28	I_{S_Max1}	[A]	12.83
Result	Eq 29	I_{S_RMS1}	[A]	5.20
Result	Eq 43b	V_{RDiode} (for V_{CC} diode)	[V]	88.00
Output capacitors				
Input	Max. voltage overshoot at output capacitor (C22, C23)	ΔV_{OUT1}	[V]	0.5
Input	Number of clock periods	n_{cp}		20
Result	Eq 49	$I_{RIPPLE1}$	[A]	4.71
Result	Eq 50	C_{OUT1}	[µF]	1354
Input	Selected output capacitor value	C22	[µF]	1360
Input	Number of parallel capacitors	n_c		2
Soft-start time				
Input	Selected soft-start time from datasheet	$t_{softstart}$	[ms]	12
V_{CC} capacitor (C16) and start-up time				
Input	Selected $I_{VCC,Charge3}$ from datasheet	$I_{VCC,Charge3}$	[mA]	3
Input	Selected V_{VCChys} from datasheet	V_{VCChys}	[mV]	6
Result	Eq 56A	C_{VCC}	[µF]	6.00
Input	Selected V_{CC} capacitor	C_{VCC} (C16)	[µF]	22
Input	Selected $V_{VCC,STG}$ from datasheet	$V_{VCC,STG}$	[V]	1.1
Input	Selected $I_{VCC,Charge1}$ from datasheet	$I_{VCC,Charge1}$	[mA]	0.2
Input	Selected $V_{VCC,ON}$ from datasheet	$V_{VCC,ON}$	[V]	16
Result	Eq 56B	$t_{StartUp}$	[ms]	238.33
Calculation of losses				
Input diode bridge				
Input	Select V_{F_Bridge} from datasheet	V_{F_Bridge}	[V]	1
Result	Eq 57	P_{DIN}	[W]	1.49
Transformer copper losses				
Result	Eq 58	R_{PCu}	[mΩ]	355.99
Result	Eq 58	R_{SCu1}	[mΩ]	7.01
Result	Eq 58	R_{SCu2}	[mΩ]	151.14
Result	Eq 59	P_{PCu}	[mW]	189.63
Result	Eq 60	P_{SCu1}	[mW]	0.3408
Output rectifier MOSFET				
Input	R_{DSON} from datasheet	R_{DSON} at T_J = 125°C	[Ω]	0.02

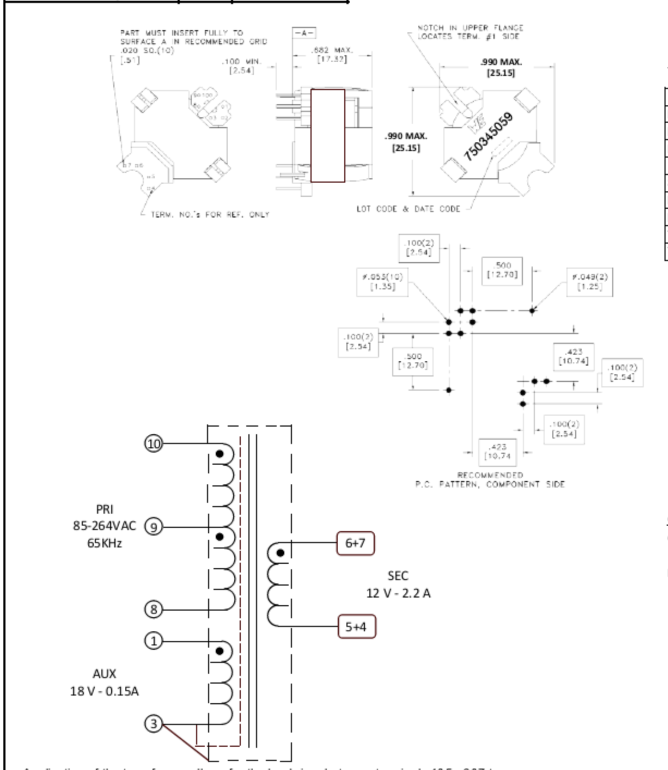
Result		P_{OUT_MOSFET}	[W]	0.54
RCD clamper circuit				
Result	Eq 63	P_{clamp}	[W]	0.54
MOSFET				
Input	R_{DSON} from datasheet	R_{DSON} at T_J = 90°C (T_J by measurement)	[Ω]	3.01
Input	$Co_{(er)}$ from datasheet	$Co_{(er)}$	[pF]	7
Input	External drain-to-source capacitance of MOSFET	C_{DS}	[pF]	0
MOSFET losses at V AC_{Min} + P_{Max}				
Result	Eq 65	P_{SON}	[W]	0.000000045
Result	Eq 66	P_{cond}	[W]	1.2779
Result	Eq 67	MOSFET losses	[W]	1.2779
MOSFET losses at V AC_{Max} + P_{Max}				
Result	Eq 68	P_{SON}	[W]	0.0228
Result	Eq 69	P_{cond}	[W]	0.4252
Result	Eq 70	MOSFET losses	[W]	0.4479
Temperature calculation				
Input	Enter MOSFET losses	MOSFET losses	[W]	1.28
Input	Enter thermal resistance junction – ambient	R_{th}	[°K/W]	75
Result	Eq 74	ΔT	[°K]	95.8
Result	Eq 75	T_{jmax}	[°C]	145.8
Note: estimated T_{jmax} is based on maximum drain-source turn-on resistance; actual thermal measurement will be needed.				
Controller				
Result	$I_{VCC,Normal}$XV_{VCC}	Controller losses	[W]	0.0157
Sum of losses (excluding LDO circuit-related loss and DC-DC loss)				
Result	Eq 77	P_{Losses}	[W]	4.20
Efficiency after losses (NOT considering LDO and DC-DC related circuit)				
Result	Eq 78	η_L		0.8871
Calculation of the regulation loop				
Input	Minimum current for TL431 reference	I_{KAmin}	[mA]	1
Input	Optocoupler gain	G_C (200%)		2
Input	Maximum current for optocoupler diode	I_{Fmax}	[mA]	10
Input	Second resistor of TL431 voltage divider	R26	[kΩ]	10
Input	0 dB crossover frequency	fg	[kHz]	3
Input	Eq 81	R25	[kΩ]	38.00
Input	Selected value of R25	R25	[kΩ]	38
Input	Eq 82	R22	[kΩ]	0.8250
Result	Selected value of R22	R22	[kΩ]	1
Input	V_{REF} from datasheet	V_{REF}	[V]	3.3
Result	$V_{FB,OLP}$ from datasheet (overload/open-loop detection limit at FB pin)	$V_{FB,OLP}$	[V]	2.75
Input	R_{FB} from datasheet	R_{FB}	[kΩ]	3
Result	Eq 83	R23	[kΩ]	1.34
Input	Selected value of R23	R23	[kΩ]	1
Result	Eq 84	V_{Out_RL}	[V]	12.0
Input	Eq 85	K_{FB}		6.00
Input	Eq 86	G_{FB}	[dB]	15.56
Input	Eq 87	K_{VD}		0.21
Input	Eq 88	G_{VD}	[dB]	-13.62
Result	Eq 89	R_{LH}	[Ω]	4.36
Input	Eq 90	R_{LL}	[Ω]	1440.00
Result	Eq 91	f_{OH}	[Hz]	26.82
Result	Eq 92	f_{OL}	[Hz]	0.08
Result	Eq 93	f_{OM}	[Hz]	1.48
Result	Eq 95	$\lvert F_{PWR}(fg)\rvert$		0.052
Result	Eq 96	$G_{PWR}(fg)$	[dB]	-25.62
Result	Eq 99	Gr	[dB]	23.687
Result	Eq 100	R24	[kΩ]	121.03
Result	Selected value of R24	R24	[kΩ]	22
Result	Eq 101	C26	[nF]	2.411

Result	Selected value of C26	C26	[nF]	1
Result	Eq 102	C25	[nF]	4899.29
Result	Selected value of C25	C25	[nF]	47
ZCD and output OVP calculation				
Input	Designed V_{OUT_OVP}	V_{OUT_OVP}	[V]	15
Input	$V_{ZC\_OVP\_MIN}$ from datasheet	$V_{ZC\_OVP\_MIN}$	[V]	1.9
Input	R_{ZCD_MIN} from datasheet	R_{ZCD}	[kΩ]	3
Result	Eq 103	R_{ZC}(R15)	[kΩ]	32.53
Input	Selected value of R15	R_{ZC} (R15)	[kΩ]	30
Input	f_{OSC2} by measurement	f_{OSC2}	[kHz]	900
Result	Eq 104	C_{ZC} (C19)	[pF]	101
Input	Selected value of C_{ZC} (C19)	C_{ZC} (C19)	[pF]	68
LOVP is the first priority and its associated brown-out, brown-in and line selection				
Input		R_{I1} (R18)	[Ω]	10,000,000
Input		LOV (V_{OVP_AC})	[V AC]	300
Input		V DC_{RIPPLE}	[V]	25
Result	Eq 105A	R_{I2} (R19)	[Ω]	68,824
Input	Selected value of R19 (R_{I2})	R_{I2} (R19)	[Ω]	69,000
Result	Eq 106	Brown-in voltage ($V_{Brownin\_AC}$)	[V AC]	68
Result	Eq 107	Brown-out voltage for full load which considers V DC_{RIPPLE} ($V_{Brownout\_AC}$)	[V AC]	59
Result	Eq 107	Brown-out voltage for light load which neglects V DC_{RIPPLE} ($V_{Brownout\_AC}$)	[V AC]	41
Result	Eq 108	Line selection threshold with V DC_{RIPPLE} (V_{VIN} = 1.52 V)	[V AC]	175
Result	Eq 108	Line selection threshold without V DC_{RIPPLE} (V_{VIN} = 1.52 V)	[V AC]	157

Electrical			
Minimum AC voltage		[V]	85
Maximum AC voltage		[V]	264
Maximum input current		[A]	0.45
Minimum DC voltage		[V]	96
Maximum DC voltage		[V]	373
Maximum output power		[W]	33.0
Output voltage		[V]	12.0
Inductor peak current		[A]	1.60
Maximum duty cycle			0.50
Reflected output voltage		[V]	96
Copper losses		[W]	0.34
MOSFET losses		[W]	1.28
Sum losses		[W]	4.20
Efficiency			0.89

Transformer			
Core type			RM8
Core material			0
Effective core area		[mm²]	52
Maximum flux density		[mT]	292
Inductance		[uH]	454
Margin		[mm]	0
Primary turns		Turns	48
Primary copper wire size		AWG	27
Secondary turns (N_{S1})		Turns	6
Secondary copper wire size		AWG	22
Number of parallel secondary wires			2
Secondary turns (N_{S2})		Turns	0
Auxiliary turns		Turns	9
Leakage inductance		[µH]	4.5
Turns ratio			8.00
Primary layers		Layer	3
Secondary layers		Layer	1

12 Appendix B: WE transformer specification



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-3	@20°C	0.12 ohms max.
D.C. RESISTANCE	8-10	@20°C	0.50 ohms max.
D.C. RESISTANCE	4-7	tie(4+5,6+7), @20°C	0.02 ohms max.
INDUCTANCE	8-10	10kHz, 100mV, Ls	450.00µH ±10%
SATURATION CURRENT	8-10	20% rolloff from initial	2A
LEAKAGE INDUCTANCE	8-10	tie(4+5+6+7),100kHz, 100mV, Ls	12µH max.
DIELECTRIC	10-7	tie(1+10,4+5+6+7), 3750VAC, 1 second	3000VAC, 1 minute
TURNS RATIO		(10-8):(1-3)	5.33:1
TURNS RATIO		(10-8):(7-4),tie (4+5,6+7)	8.00:1

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC62368-1, EN62368-1, UL62368-1/CSA62368-1 and AS/NZS62368.1:

- Reinforced insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, OVC II, Pollution Degree 2.

Application of the transformer allows for the leadwires between terminals 4&5, 6&7 to solder bridge.

Customer to tie terminals 4 + 5 and 6 + 7 on PC board.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability. Marking method, font and color may vary on preproduction samples.

DFM		Packaging Specifications	Tolerances unless otherwise specified:	DRAWING TITLE: TRANSFORMER
DATE		Method: Tray	Angles: ±1° Decimals: ±.005 [.13]	
ENG	NWU	PKG-0027	Fractions: ±1/64 Footprint: ± .001 [.03]	PART NO. 750345059
REV.	01	CONVENTION PLACEMENT	This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	
DATE	2021/10/25	www.we-online.com/midcom		SPECIFICATION SHEET 1 OF 1

Figure 32 WE transformer specification

13 References

[1] **ICE5QRxxxxBG datasheet, Infineon Technologies AG**

[2] **Design Guide Quasi Resonant CoolSET™ Generation 5**

[3] **Calculation Tool Quasi Resonant CoolSET™ Generation 5**

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-07-27	Initial release
V 1.1	2022-10-19	Schematic and PCB layout updated

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