# XDPL8219 40 W reference design with IPD80R900P7

## For high-power-factor flyback converter with constant voltage output

## About this document

### Scope and purpose

This document is an engineering report for a reference design, REF-XDPL8219-U40W, which is based on Infineon's **XDPL8219** high-power-factor (HPF) flyback controller and **IPD80R900P7** MOSFET. This is a reference design for a 40 W front-stage HPF flyback converter with secondary-side regulated constant voltage output of 54 V, which can be used to supply a second-stage constant current converter for LED lighting applications.

### Intended audience

Power supply design engineers and field application engineers.

## Table of contents

# 1 Introduction and safety information

The **XDPL8219** 40 W reference design is a digitally configurable front-stage HPF flyback converter with secondary-side regulated (SSR) constant voltage (CV) output of 54 V. The CV output should not be used to directly drive the LEDs. For LED lighting applications, it should be converted to constant current (CC) output by a second-stage DC-DC switching or linear regulator.

The 40 W reference design sample is ready to be tested out of the box, with its main board already connected to a 54 V CV SSR plug-in board via connectors X200-A and X200-B, as shown in **Figure 1**. No pre-programming is needed, as it has already been burned with the first full configuration set of working parameters.

A simple test setup can be done by connecting the board's AC input (L – live, N – neutral) to the AC source, and the 54 V CV output (+, -) from connector X300-A to an electronic load in CC mode, based on **Figure 1**. Additionally, to capture and decode the UART reporting data packets, the connector X2 pin 2 (UART) can be connected to the oscilloscope via a voltage probe, with the grounding on the connector X2 pin 3 (PGND).

***Attention:*** ***Lethal voltages are present on this reference design. Do not operate the board unless you are trained to handle HV circuits. Do not leave this board unattended when it is powered up.***

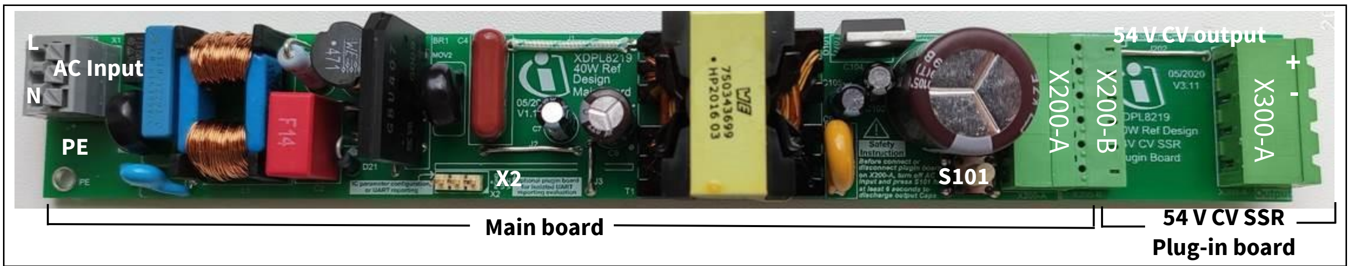



**Figure 1** **XDPL8219 40 W reference design main board and 54 V CV SSR plug-in board**

If the 54 V CV SSR plug-in board is not connected to the reference design main board, the flyback output voltage of the main board will become unregulated with either the $V_{CC}$ or output overvoltage (OV) protection of **XDPL8219** being triggered.

An isolated UART reporting evaluation plug-in board (see **Figure 2**) is included in the **XDPL8219** 40 W reference design packaging box. This plug-in board has an isolated optocoupler-based circuit, which can be evaluated optionally, by connecting it to the **XDPL8219** 40 W reference design main board. The recommended evaluation setup and procedures are written at the bottom layer of this plug-in board (see **Figure 9**).

***Attention:*** ***For safety purposes, before disconnecting or connecting any plug-in board, the connected AC source or DC source must be switched off and followed by the output voltage discharge. A tactile switch S101 provides an option to discharge the flyback secondary output voltage, by pressing and holding it until the output voltages are at safe levels based on measurement. When disconnecting or connecting a plug-in board, the user should only hold onto either the main board connector X200-A or the PCB edges just next to this connector.***

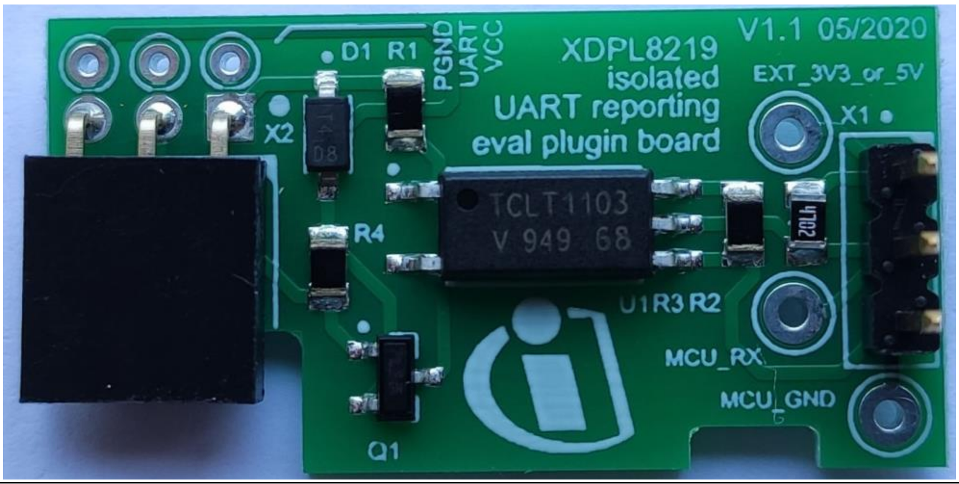



**Figure 2** **XDPL8219 isolated UART reporting evaluation plug-in board**

# 2 Design features

- Secondary-side regulated (SSR) constant voltage (CV) output
- Supports universal input with 90 $V_{rms}$ to 305 $V_{rms}$ and DC input with 127 V to 432 V
- High-power-factor (HPF) and low total harmonic distortion (iTHD), across wide AC input voltage range (120 $V_{rms}$ to 277 $V_{rms}$) and wide output load range (33 percent to 100 percent of full load)
- High efficiency with quasi-resonant (QR) mode, switching in valley n (QRMn), across wide input and output load range
- No-load standby power, as low as less than 100 mW with active burst mode (ABM)
- Input overvoltage protection (OVP) and input undervoltage protection (UVP)
- Power limitation during brown-out, to better protect primary components, e.g., the flyback MOSFET, from overheating and magnetics from saturation
- Output power limitation and output UVP, under single fault condition where the second-stage constant current DC-DC converter MOSFET drain pin is shorted to the source pin
- Output and $V_{CC}$ OVP, under feedback open condition
- Output short protection
- $V_{CC}$ UVP
- Configurable parameters, e.g., brown-out power limitation slope, protection thresholds and reaction (auto restart/latch)
- Reporting of system information, e.g., input voltage, line frequency, controller temperature, input voltage loss, and error code of last triggered protection, via unidirectional UART communication

# 3 Board specifications

**Table 1** and **Table 2** respectively list the electrical specifications and system protection parameter values of the reference design.

**Table 1 Electrical specifications**

| Specification | Symbol | Value | Unit |
|---|---|---|---|
| Normal operational AC input voltage | V AC | 90 ~ 305 | $V_{rms}$ |
| Normal operational AC input frequency | $F_{line}$ | 47 ~ 63 | Hz |
| Normal operational DC input voltage | V DC | 127 ~ 300 | V |
| SSR CV output set-point | $V_{out,setpoint}$ | 54 | V |
| Steady-state output load current | $I_{out}$ | 0 ~ 800 | mA |
| Steady-state full-load output power | $P_{out,full}$ | 43.2 | W |
| Total line, load regulation of $V_{out}$ | $\Delta V_{out}$ | ± 1 | % |
| Power efficiency 1<br>(V AC = 230 $V_{rms}$; $I_{out}$ = 600 mA to 800 mA) | $\eta_1$ | More than 92 | % |
| Power efficiency 2<br>(V AC = 230 $V_{rms}$; $I_{out}$ = 400 mA to 600 mA) | $\eta_2$ | More than 91 | % |
| Power efficiency 3<br>(V AC = 120 $V_{rms}$ to 277 $V_{rms}$; $I_{out}$ = 400 mA to 800 mA) | $\eta_3$ | More than 91 | % |
| Power efficiency 4<br>(V AC = 120 $V_{rms}$ to 277 $V_{rms}$; $I_{out}$ = 265 mA to 400 mA) | $\eta_4$ | More than 90 | % |
| Power factor 1<br>(V AC = 230 $V_{rms}$; $F_{line}$ = 50 Hz; $I_{out}$ = 400 mA to 800 mA) | $PF_1$ | More than 0.98 | – |
| Power factor 2<br>(V AC = 230 $V_{rms}$; $F_{line}$ = 50 Hz; $I_{out}$ = 265 mA to 400 mA) | $PF_2$ | More than 0.96 | – |
| Power factor 3<br>(V AC = 120 $V_{rms}$ and 277 $V_{rms}$; $F_{line}$ = 60 Hz; $I_{out}$ = 400 to 800 mA) | $PF_3$ | More than 0.96 | – |
| Power factor 4<br>(V AC = 120 $V_{rms}$ and 277 $V_{rms}$; $F_{line}$ = 60 Hz; $I_{out}$ = 265 to 400 mA) | $PF_4$ | More than 0.9 | – |
| Total harmonic distortion 1<br>(V AC = 230 $V_{rms}$; $F_{line}$ = 50 Hz; $I_{out}$ = 265 to 800 mA) | $iTHD_1$ | Less than 10 | % |
| Total harmonic distortion 2<br>(V AC = 120 $V_{rms}$ and 277 $V_{rms}$; $F_{line}$ = 60 Hz; $I_{out}$ = 400 to 800 mA) | $iTHD_2$ | Less than 10 | % |
| Total harmonic distortion 3<br>(V AC = 120 $V_{rms}$ and 277 $V_{rms}$; $F_{line}$ = 60 Hz; $I_{out}$ = 265 to 400 mA) | $iTHD_3$ | Less than 15 | % |

**Table 2 System protection parameter values**

| System protection parameter | Symbol | Value | Unit |
|---|---|---|---|
| Input OVP level[1] | $V_{inOV}$ | 350 | $V_{rms}$ |
| Maximum input voltage level for start-up[1] | $V_{in,start,max}$ | 326 | $V_{rms}$ |
| Brown-in/Minimum input voltage level for start-up[1] | $V_{in,start,min}$ | 82 | $V_{rms}$ |
| Brown-out/Input UVP level[1] | $V_{inUV}$ | 70 | $V_{rms}$ |
| Output OVP level[1] | $V_{outOV}$ | 65 | V |
| Start-up output UVP (short) level[1] | $V_{out,start}$ | 31 | V |
| Regulated mode output UVP level[1] | $V_{outUV}$ | 33 | V |
| Regulated mode output UVP blanking time[1] | $t_{VoutUV,blank}$ | 500 | ms |
| $V_{CC}$ OVP level[1] | $V_{VCC,max}$ | 23 | V |
| Regulated mode $V_{CC}$ UVP level[1] | $V_{VCC,min}$ | 7.5 | V |
| Regulated mode CS pin maximum voltage at the lowest operational input voltage[1] | $V_{OCP1,at,V,in,low}$ | 0.52 | V |
| Lowest operational input voltage[1] | $V_{in,low}$ | 82 | $V_{rms}$ |
| Regulated mode CS pin maximum voltage at the highest operational input voltage[1] | $V_{OCP1,at,V,in,high}$ | 0.43 | V |
| Highest operational input voltage[1] | $V_{in,high}$ | 326 | $V_{rms}$ |
| IC overtemperature protection level[2] | $T_{critical}$ | 119 | °C |
| Maximum IC temperature for start-up | $T_{start,max}$ | $T_{critical} - 4 = 115$ | °C |
| Input OVP reaction | $Reaction_{OVP,Vin}$ | Auto restart | – |
| Input UVP reaction | $Reaction_{UVP,Vin}$ | Auto restart | – |
| Output OVP reaction[1] | $Reaction_{OVP,Vout}$ | Auto restart | – |
| Start-up output UVP reaction | $Reaction_{UVP,Vout,start}$ | Auto restart | – |
| Regulated mode output UVP reaction[1] | $Reaction_{UVP,Vout}$ | Auto restart | – |
| $V_{CC}$ OVP reaction[1] | $Reaction_{VCC,OVP}$ | Latch mode | – |
| Regulated mode $V_{CC}$ UVP reaction | $Reaction_{VCC,UVP}$ | Auto restart | – |
| IC overtemperature protection reaction | $Reaction_{TP}$ | Auto restart | – |
| Auto restart time[1] | $t_{auto,restart}$ | 1.2 | s |

*Note:* *The input and output sensing voltages for these protections are estimated from ZCD pin switching signals. To improve the input voltage estimation accuracy, CS pin switching signal is also sensed.*

*Note:* *Regulated mode is a controller operating state, which is entered after the start-up phase, to regulate the output based on the feedback voltage signal.*

[1] Configurable

[2] Configurable up to 143°C (lifetime is not guaranteed when IC operating junction temperature is above 125°C)

# 4 Schematic and PCB layout

**Figure 3** and **Figure 4** respectively show the main board schematic and 54 V CV SSR plug-in board schematic of this reference design.

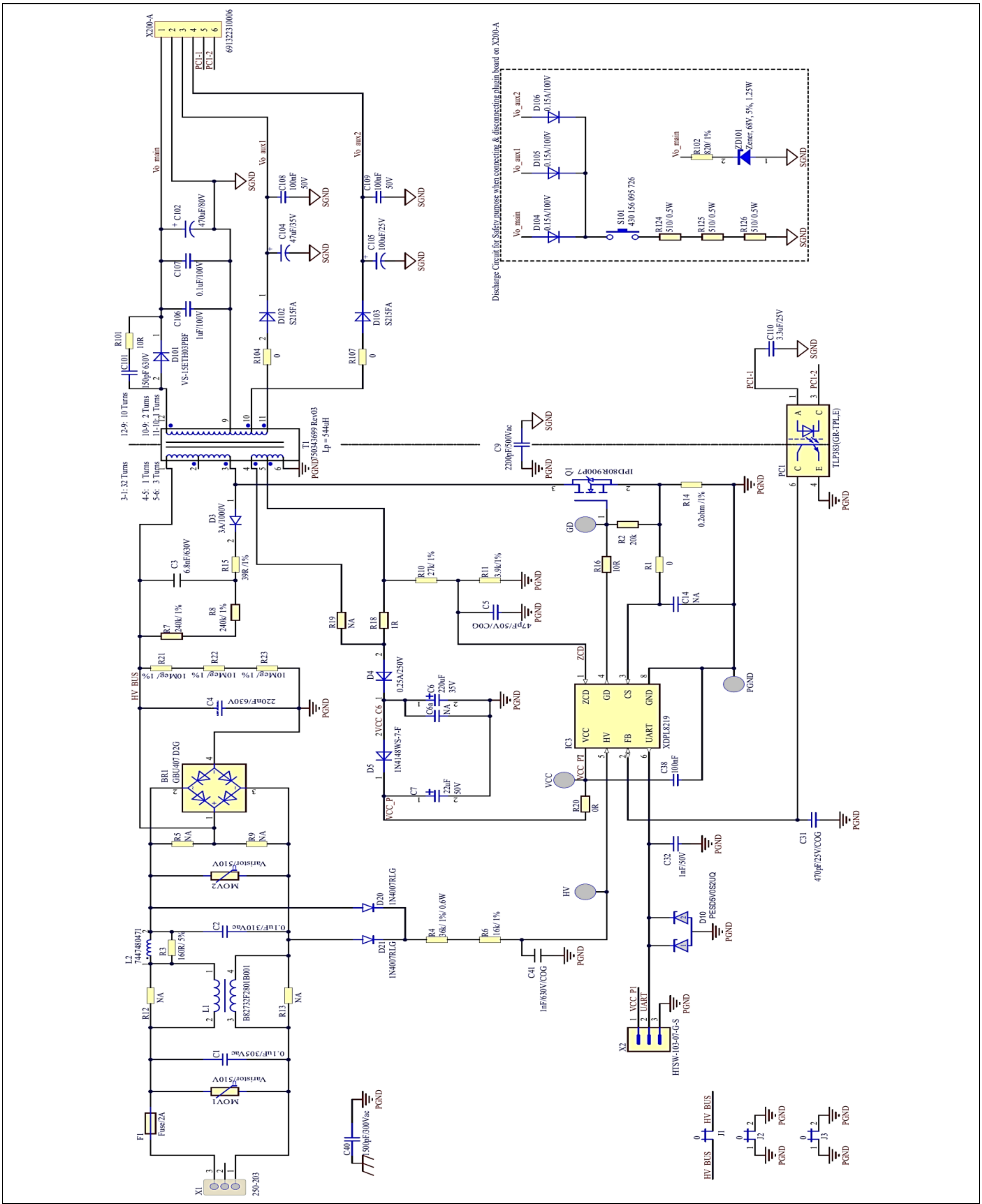
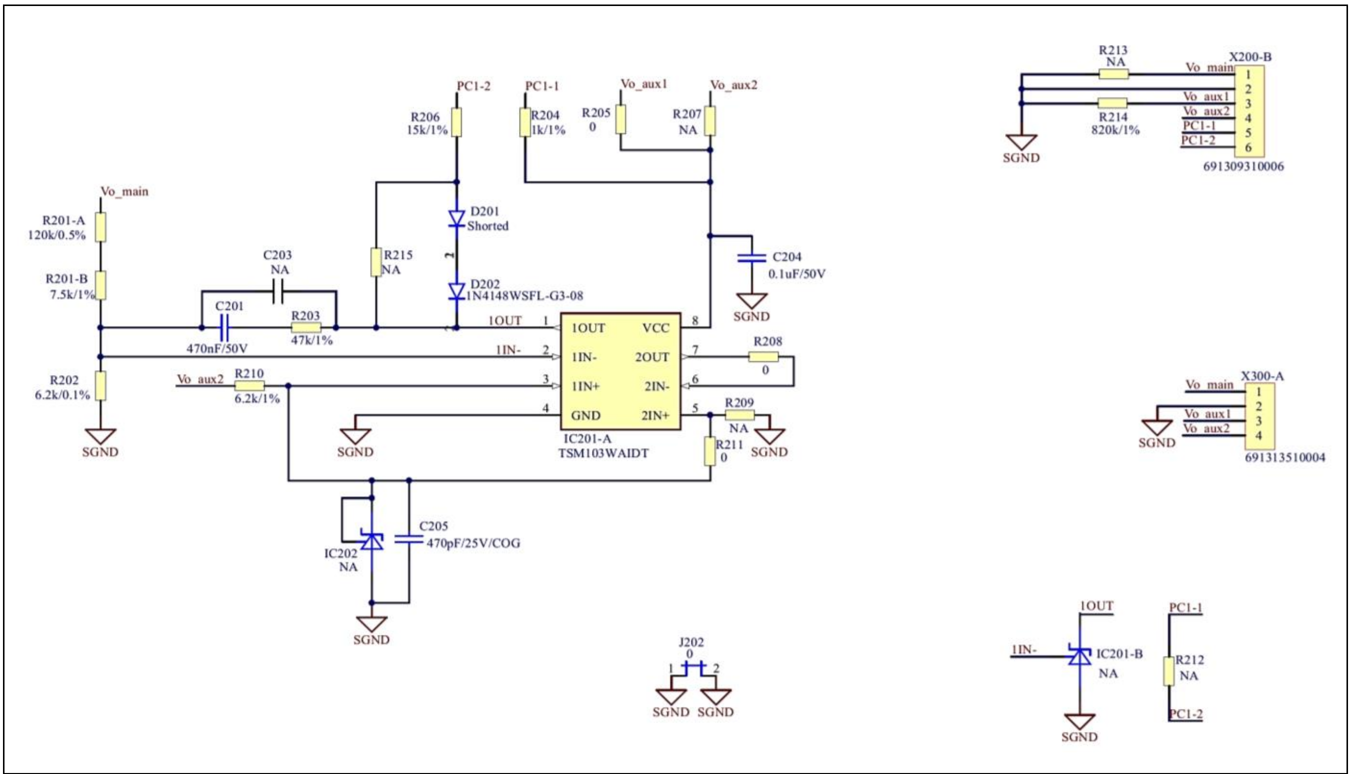
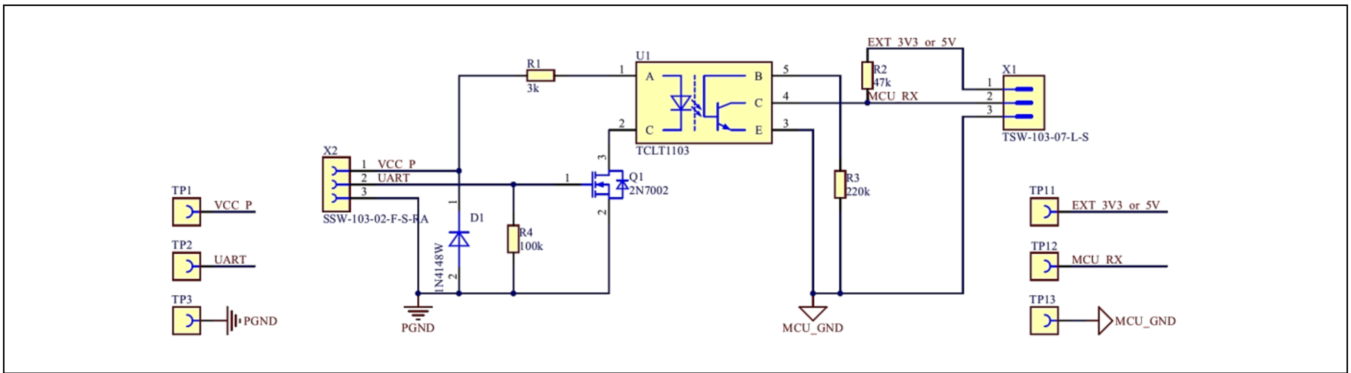



**Figure 3** **XDPL8219 40 W reference design main board schematic**



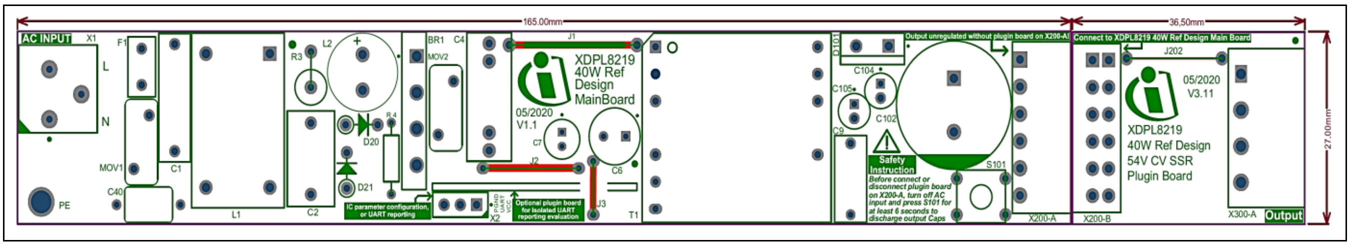

## Figure 4 54 V CV SSR plug-in board schematic

**Figure 5** shows the isolated UART reporting evaluation plug-in board schematic of this reference design.




## Figure 5 Isolated UART reporting evaluation plug-in board schematic

Both the **XDPL8219** 40 W reference design main board and 54 V CV SSR plug-in board have single-layer PCB layout design. **Figure 6** and **Figure 7** respectively show the PCB top layout (with dimensions) and bottom layout.




## Figure 6 PCB top layout of main board and 54 V CV SSR plug-in board

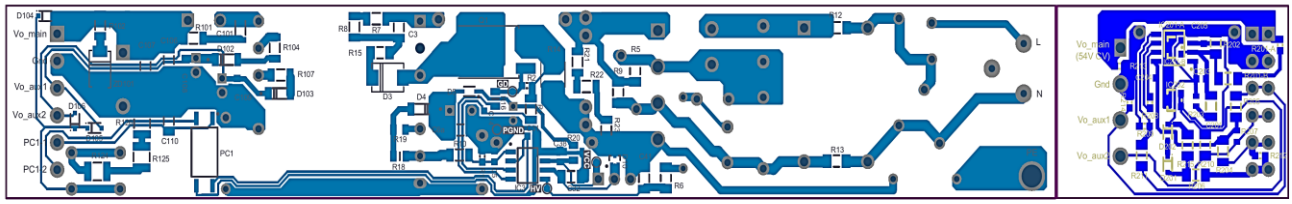


**Figure 7 PCB bottom layout of main board and 54 V CV SSR plug-in board**

The isolated UART reporting evaluation plug-in board has double-layer PCB layout design. **Figure 8** and **Figure 9** respectively show the PCB top layout (with dimensions) and bottom layout.

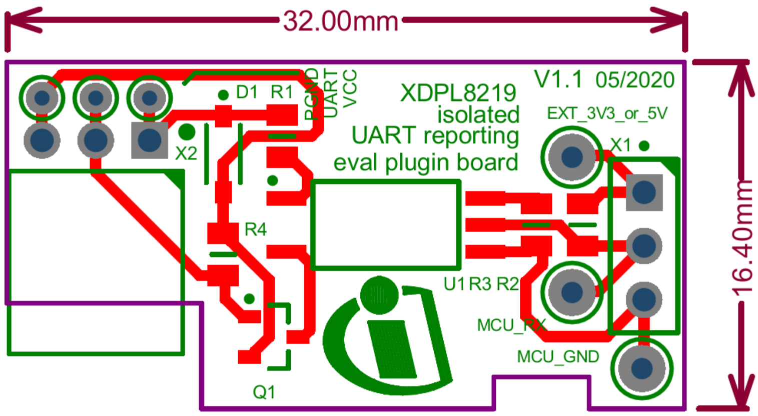



**Figure 8 PCB top layout of isolated UART reporting evaluation plug-in board**

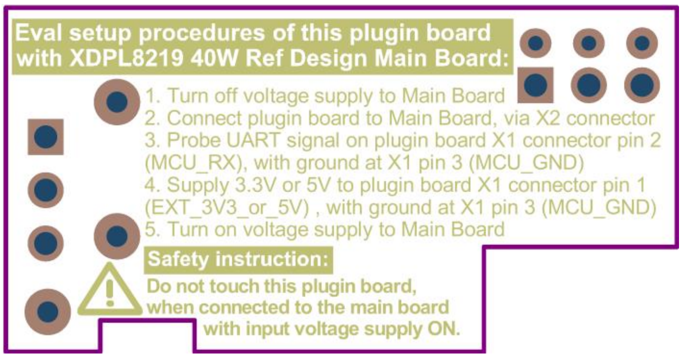



**Figure 9 PCB bottom layout of isolated UART reporting evaluation plug-in board**

# 5 Performance

The results shown in this section are based on the evaluation of a single reference board, at room temperature.

## 5.1 Line and load regulation

The total line and load regulation of $V_{out}$ is within ±1 percent, as shown in **Figure 10**.

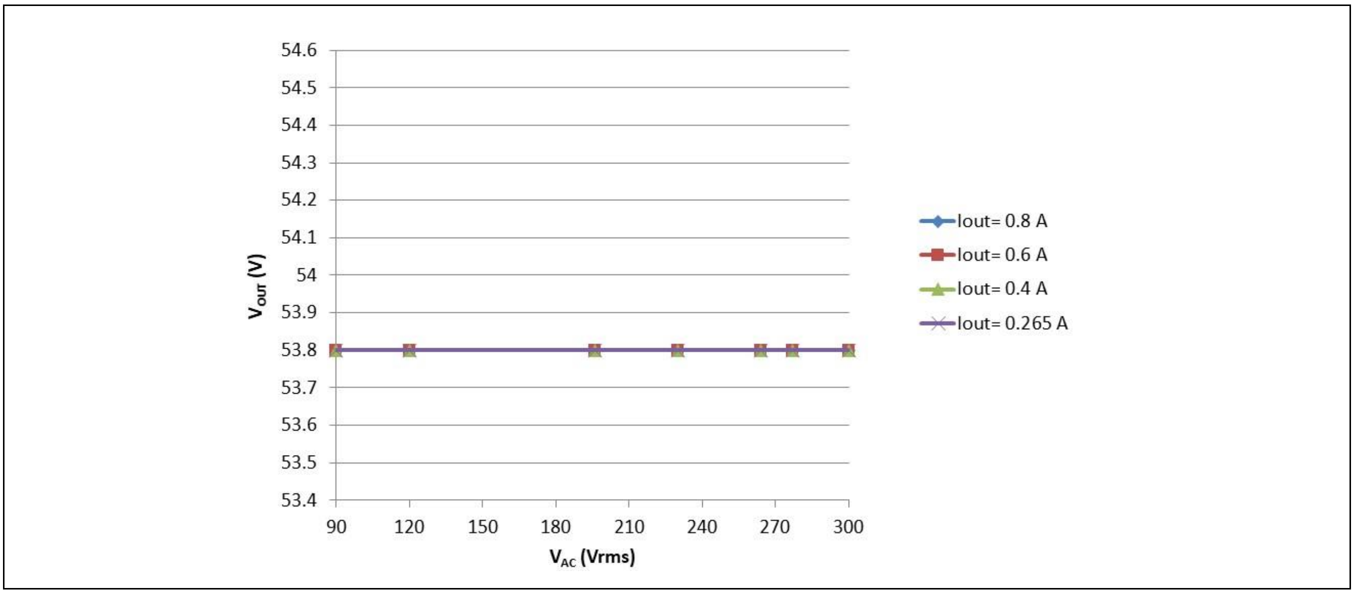



**Figure 10 Line and load regulation test result**

## 5.2 Power efficiency

The power efficiency is measured in the range of 90 percent to 93 percent, with a combination of wide output load range ($I_{out}$ = 265 mA to 800 mA) and wide AC input voltage range (V AC = 120 $V_{rms}$ to 277 $V_{rms}$), as shown in **Figure 11**.

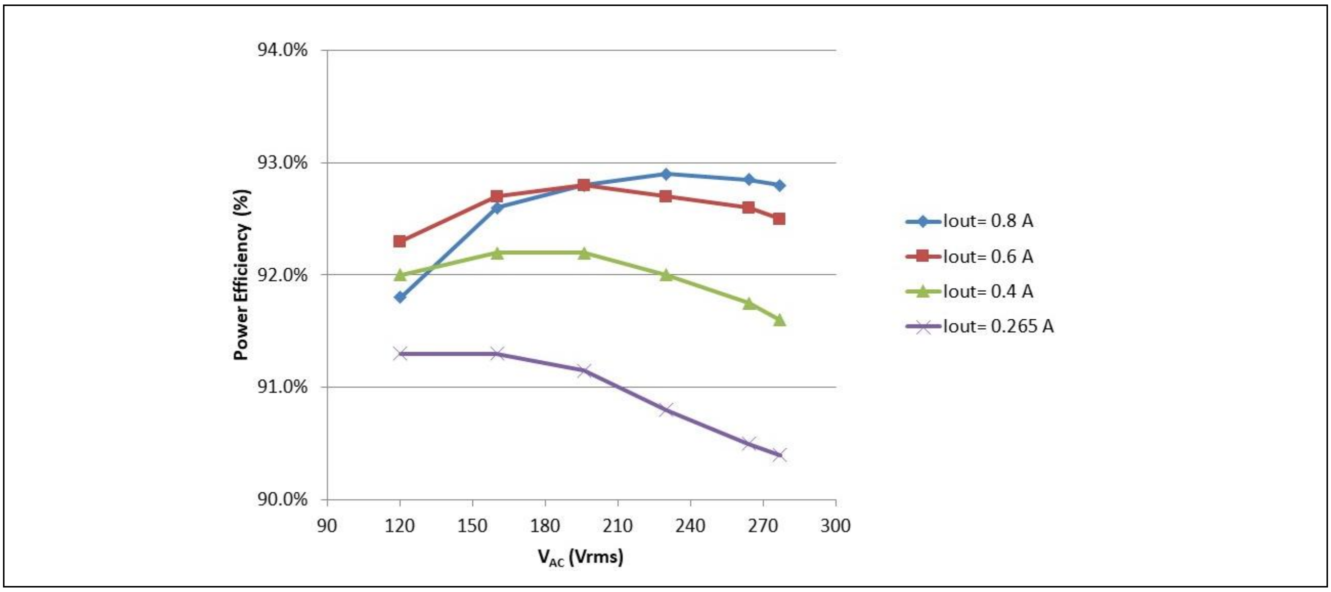



**Figure 11 System efficiency test result**

## 5.3 Standby power

The standby power under no-load condition is less than 100 mW, as shown in **Figure 12**.

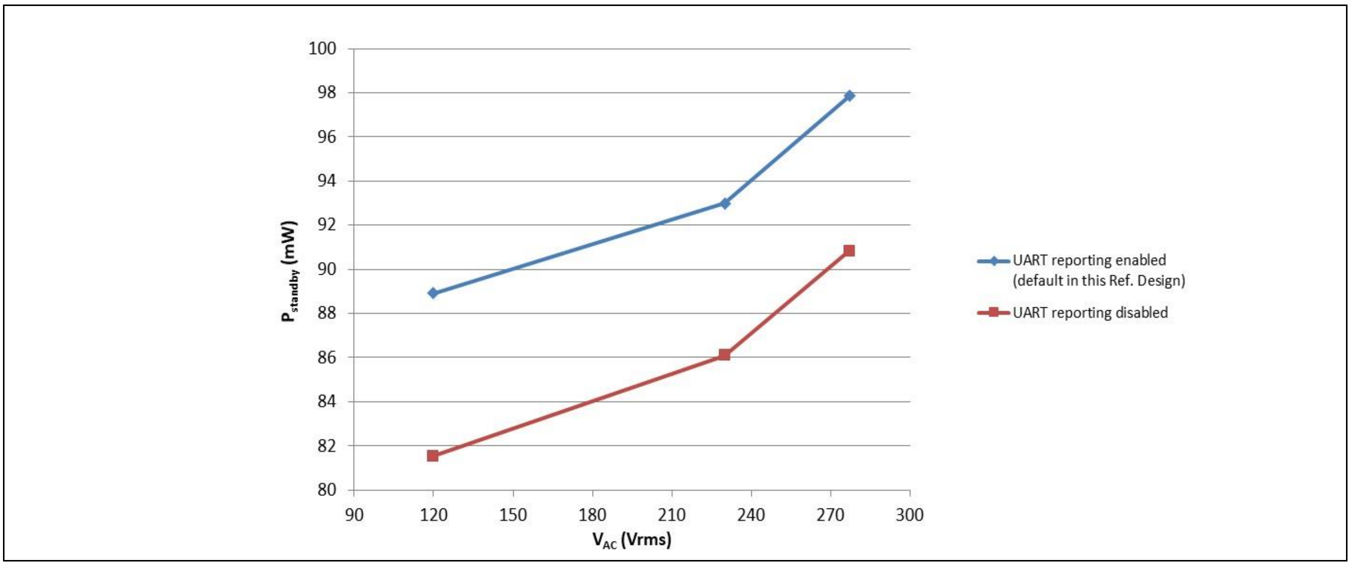



**Figure 12 Standby power test result**

## 5.4 Power factor and total harmonic distortion

Across both wide output load range ($I_{out}$ = 265 mA to 800 mA) and wide input voltage (V AC = 90 $V_{rms}$ to 277 $V_{rms}$), the PF stays above 0.9, as shown in **Figure 13**.

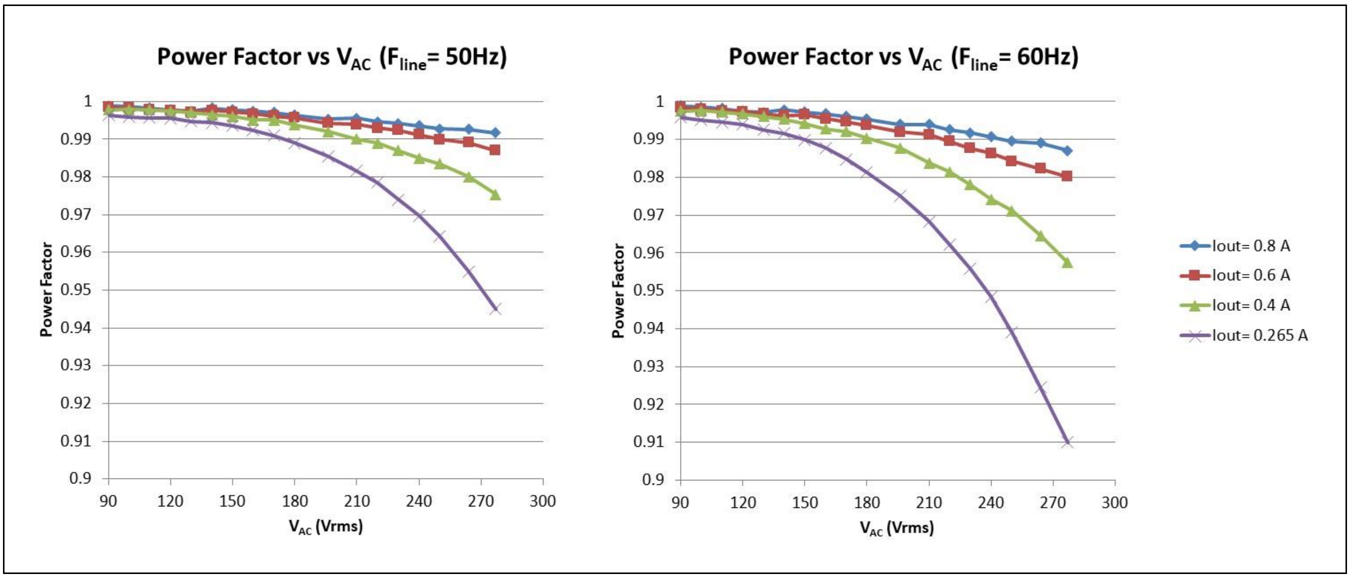



**Figure 13 PF test result**

Across wide output load range ($I_{out}$ = 265 mA to 800 mA), the iTHD measurements shown in **Figure 14** are:

- Less than 10 percent with V AC = 230 $V_{rms}$ ($F_{line}$ = 50 Hz)
- Less than 15 percent with V AC = 120 $V_{rms}$ and 277 $V_{rms}$ ($F_{line}$ = 60 Hz)

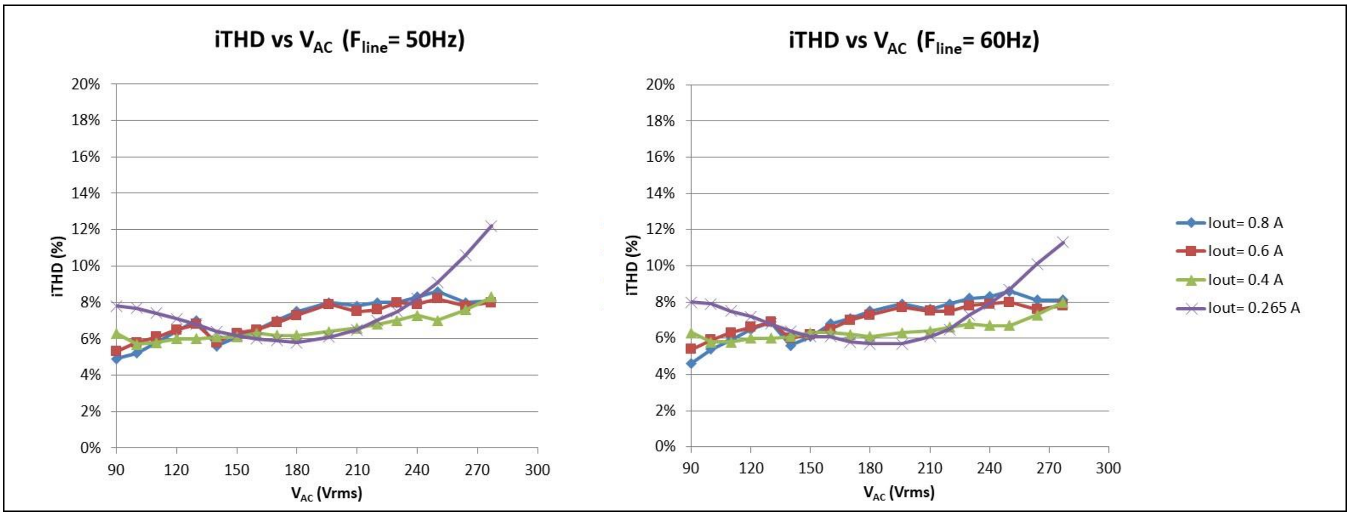



**Figure 14** Total harmonic distortion (iTHD) test result

## 5.5 Current harmonics

**Figure 15**, **Figure 16** and **Figure 17** show the current harmonics measurement (IHD) compared to the IEC61000-3-2 Class C limits ($IHD_{Limits}$).

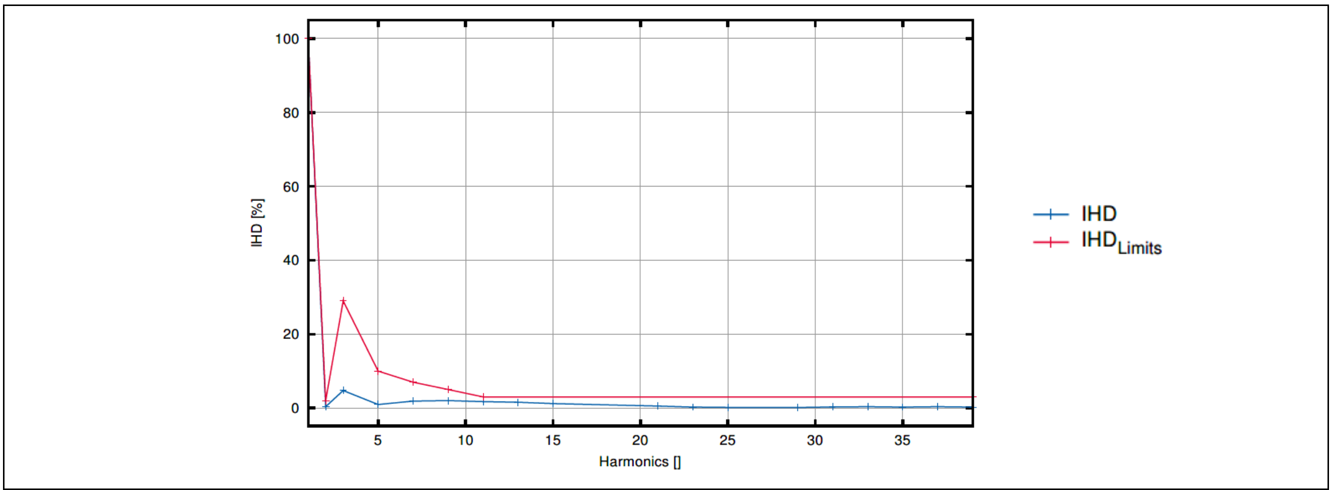



**Figure 15** Current harmonics at V AC = 120 $V_{rms}$, $F_{line}$ = 60 Hz and $I_{out}$ = 0.8 A

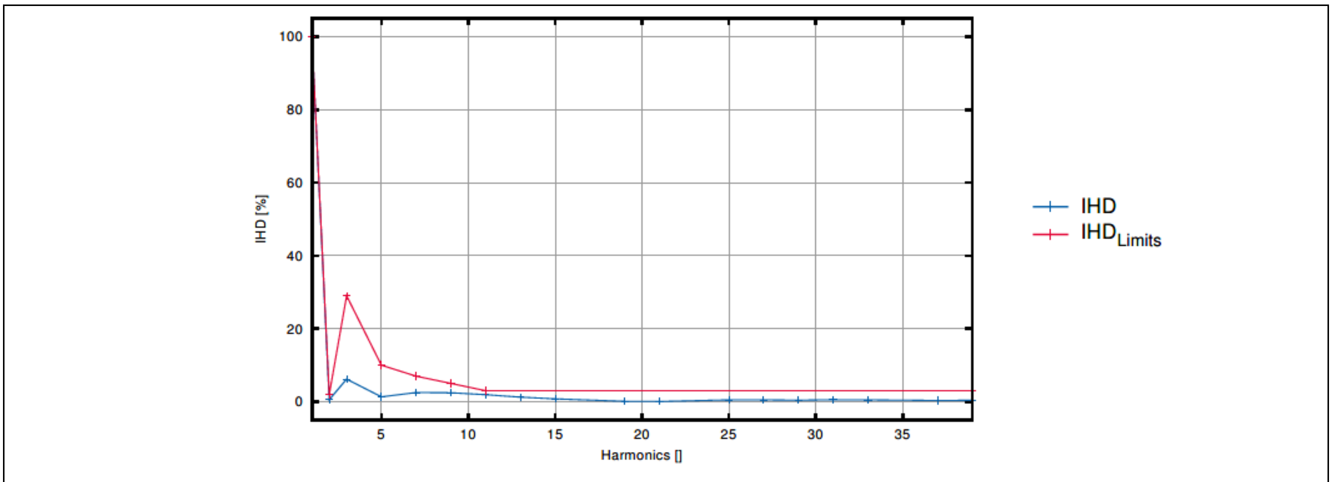



**Figure 16** Current harmonics at V AC = 230 $V_{rms}$, $F_{line}$ = 50 Hz and $I_{out}$ = 0.8 A

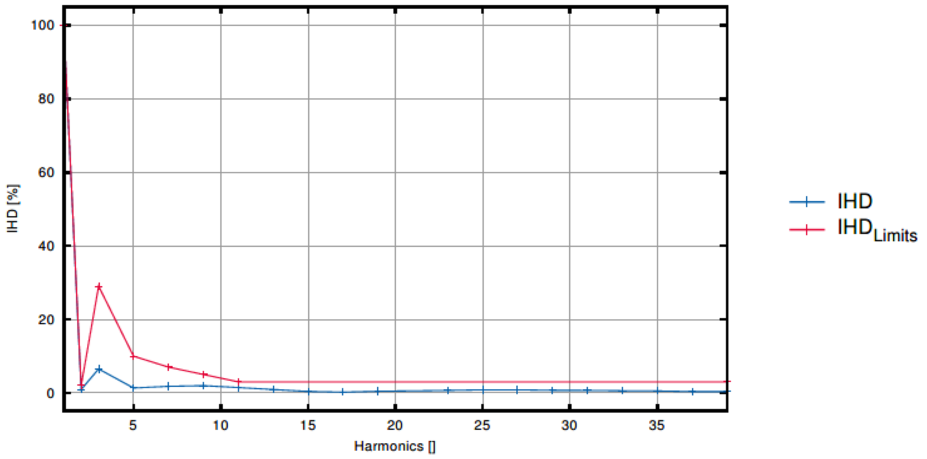



**Figure 17** **Current harmonics at V AC = 277 $V_{rms}$, $F_{line}$ = 60 Hz and $I_{out}$ = 0.8 A**

## 5.6 Input UV protection and brown-out power limitation

To better protect the primary components, e.g., the flyback MOSFET, from overheating and the magnetics from saturation, **XDPL8219** features not only an input UVP (via ZCD and CS pin signal sensing) with configurable threshold for output on/off, but also a configurable brown-out power limitation slope. **Figure 18** shows the $t_{on,max,at,V,in,low}$, $t_{on,max,at,V,in,UV}$, $V_{inUV}$ and $V_{in,low}$ parameter configuration in this reference design, which affects the maximum on-time reduction slope, and the brown-out power limitation slope test result.

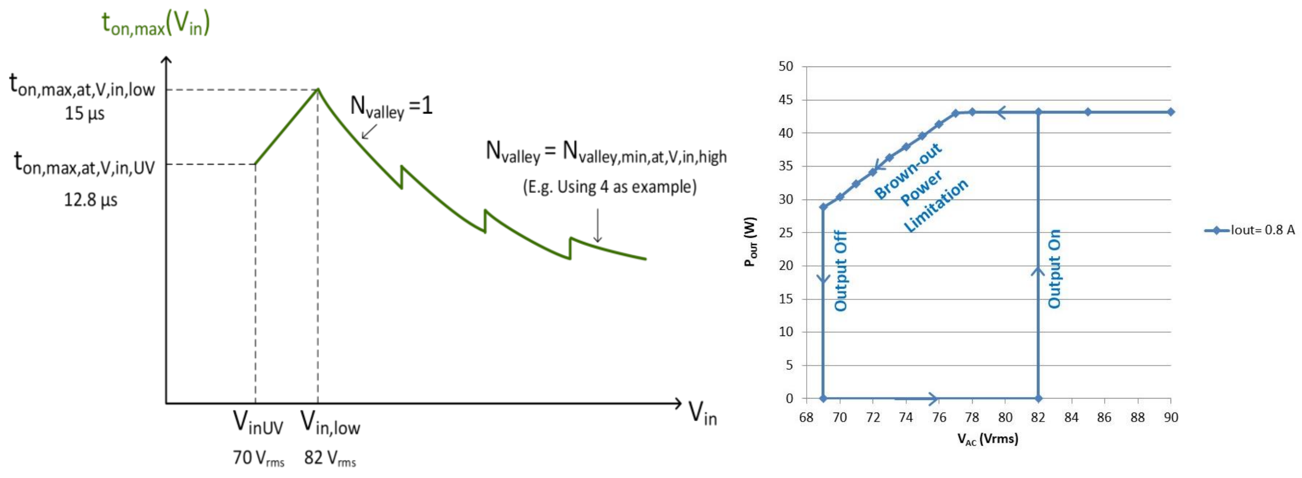



**Figure 18** **Input UV protection and brown-out power limitation with maximum on-time reduction**

## 5.7 Regulated mode output UV protection and output power limitation under single fault condition

Under the single fault condition of second-stage CC converter MOSFET drain and source pins being shorted, the connected output LEDs could clamp the flyback output voltage below its constant voltage regulation set-point.

To limit the flyback output power to the LEDs below 100 VA as per UL1310 requirements under such a fault condition, especially at high input voltage, **XDPL8219** regulated mode features the regulated mode CS pin maximum voltage limit $V_{OCP1}$ ($V_{in}$) and minimum valley number limit $N_{valley}$ ($V_{in}$), which are adaptive based on the estimated input voltage $V_{in}$.

**Figure 19** shows the $V_{OCP1,at,V,in,low}$, $V_{OCP,at,V,in,high}$, $N_{valley,min,at,V,in,high}$, $V_{in,low}$ and $V_{in,high}$ parameter configuration in this reference design, which affects the output power limitation curve test result, under such a single fault condition.

In case the single fault condition mentioned above occurs in conjunction with low-output LED voltage, **XDPL8219** also features a regulated mode output UVP (via ZCD pin signal sensing), which can be triggered to prevent the flyback MOSFET from continuously operating in the saturation region with low gate drive and $V_{CC}$ voltages, as shown in the test result in **Figure 19**.

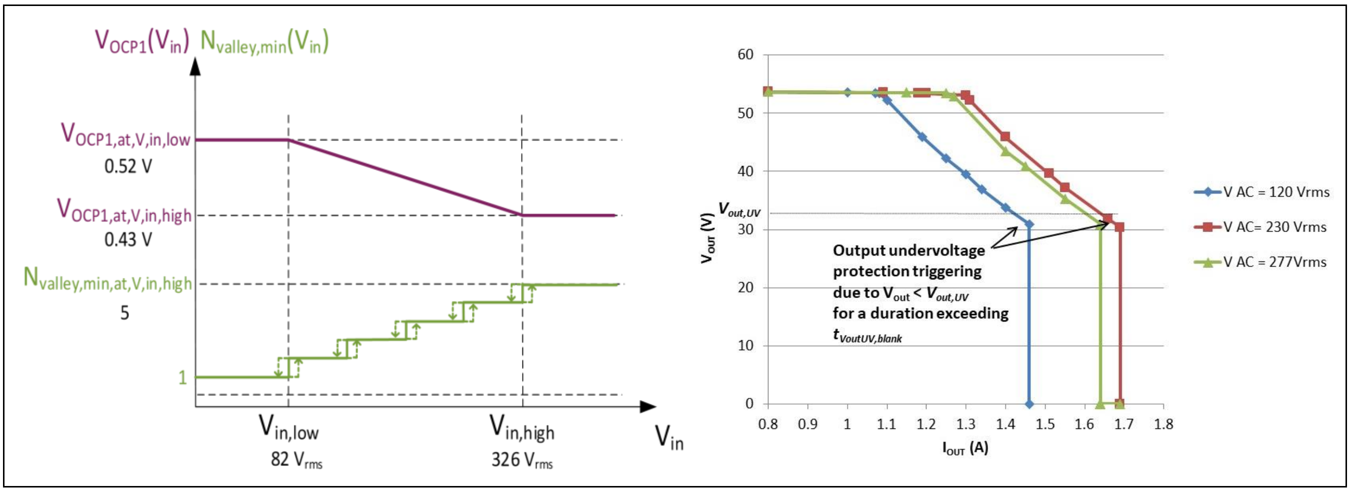



**Figure 19** **Regulated mode output UV protection, and output power limitation based on regulated mode CS pin maximum voltage limit and minimum valley number limit**

## 5.8 UART reporting

The **XDPL8219** UART pin reporting signals can be probed from the main board's X2 connector pin 2, with the grounding on X2 connector pin 3. With the default $UART_{polarity}$ = "Low" parameterization in this reference design, the oscilloscope settings for data decoding should be based on logic level of low = 1 and high = 0, with a baud rate of 9600 bps.

The captured UART signals in **Section 5.8.1**, **Section 5.8.2** and **Section 5.8.3** are based on such a setup.

### 5.8.1 Regular data reporting

With the $EN_{UART,REPORTING}$ parameter enabled by default in this reference design, the **XDPL8219** UART pin transmits a regular data packet once every 14 operation cycles, which contains the following information:

- Last detected line frequency or input voltage type based on $F_{line,UART}$
- Last estimated input voltage rms value $V_{in}$
- Last measured IC junction temperature $T_{J,UART}$, based on its internal sensor

*Note: In ABM, the $F_{line,UART}$ cannot be synchronized with the input voltage frequency, for power savings. It only shows the last detected values before entering ABM.*

The UART reporting system information is useful for power monitoring, and also for improving reliability, for example reducing the second-stage CC regulator maximum output power, when the $V_{in}$ drops too low or $T_{J,UART}$ rises too high.

**Figure 20** shows an example of the captured and decoded regular data packet.

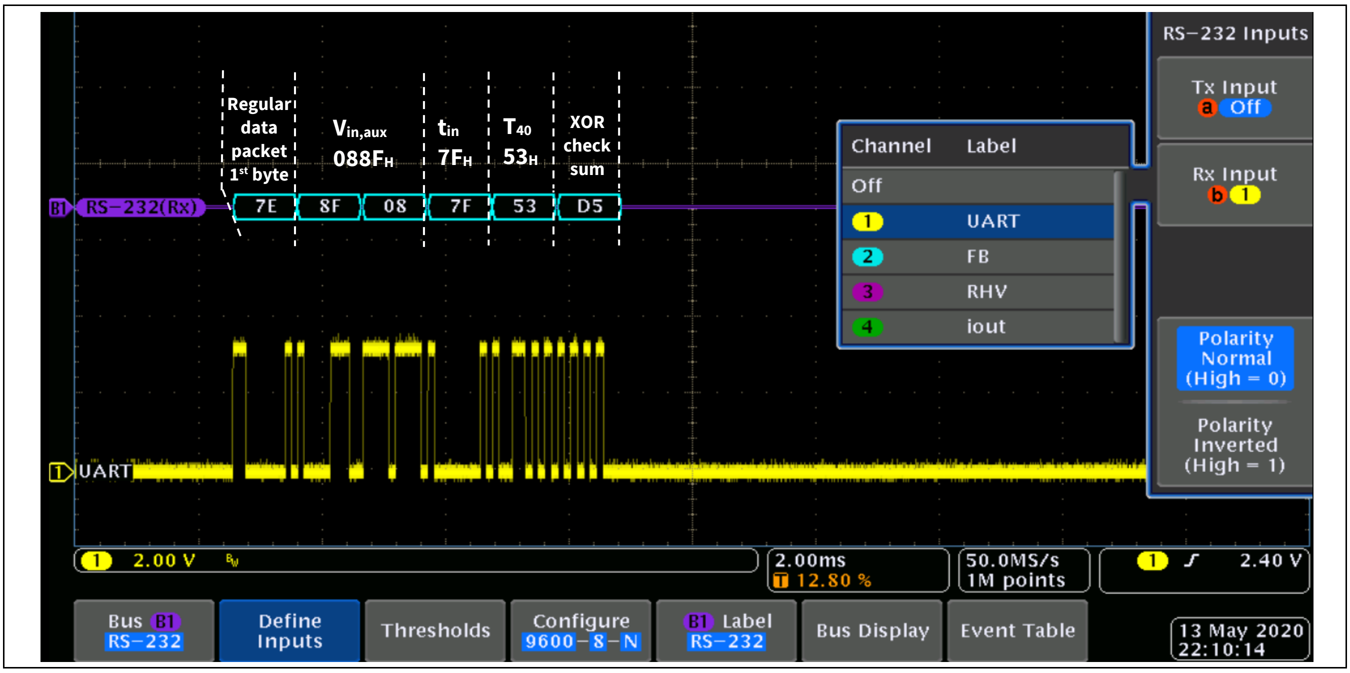



**Figure 20 UART regular data packet capturing and decoding**

Based on **Table 3**, the decoded UART regular data ($V_{in,aux}$, $t_{in}$ and $T_{40}$) can be interpreted to obtain the system information (e.g., line frequency $F_{line,UART}$, input voltage $V_{in}$ and IC junction temperature $T_{J,UART}$).

**Table 3 Interpretation of the decoded regular data**

| UART data | Data interpretation | Example of data interpretation based on the decoded data in Figure 20 |
|---|---|---|
| $t_{in}$ | If $t_{in}$ = $FF_H$, the input voltage type has not been detected.<br>If $t_{in}$ = $00_H$, the last detected input voltage type is constant DC.<br>If $t_{in} \neq FF_H$ and $t_{in} \neq 00_H$, the last detected input voltage type is AC and the $F_{line,UART}$ (unit: Hz) can be calculated based on:<br>$F_{line,UART} = \begin{cases} 5828/t_{in}, & T_{critical} > 119°C \\ 7726/t_{in}, & T_{critical} \leq 119°C \end{cases}$<br>Where $T_{critical}$ is the IC overtemperature protection level parameter setting. | Based on **$t_{in} = 7F_H \neq FF_H \neq 00_H$**, the **last detected input voltage type is AC**.<br>Based on **$T_{critical} = 119°C$** configuration in this reference design, the AC input frequency $F_{line,UART}$ equation is selected:<br>$F_{line,UART} = 7726/t_{in}$<br>Based on **$t_{in} = 7F_H = 127$**,<br>$F_{line,UART} = 60.83\ Hz$ |
| $V_{in,aux}$ | $V_{in} = \begin{cases} 0.005460 \cdot V_{in,aux} \cdot N_p/N_a, & t_{in} \neq FF_H \text{ and } t_{in} \neq 00_H \\ 0.007722 \cdot V_{in,aux} \cdot N_p/N_a, & t_{in} = 00_H \end{cases}$ | Based on **$t_{in} = 7F_H \neq FF_H \neq 00_H$**, the $V_{in}$ equation is selected:<br>$V_{in} = 0.005460 \cdot V_{in,aux} \cdot N_p/N_a$<br>Based on **$V_{in,aux} = 088F_H = 2191$**, with **$N_p = 32$ and $N_a = 3$** configuration in this reference design,<br>$V_{in} = 0.005460 \cdot 2191 \cdot 32/3 = 127.6\ V_{rms}$ |
| $T_{40}$ | $T_{J,UART} = T_{40} - 40$ | Based on **$T_{40} = 53_H = 83$**,<br>$T_{J,UART} = T_{40} - 40 = 43\ °C$ |

The single board test result shows that the UART reporting input voltage $V_{in}$ averaging value deviates in the range of 0.2 percent to 6.4 percent from the actual input voltage, as shown in **Figure 21**.

For higher input voltage monitoring accuracy, the microcontroller should store the necessary calibration data for its post-processing, to compensate for the offset on $V_{in}$, which varies based on the IC and system tolerances of each board.

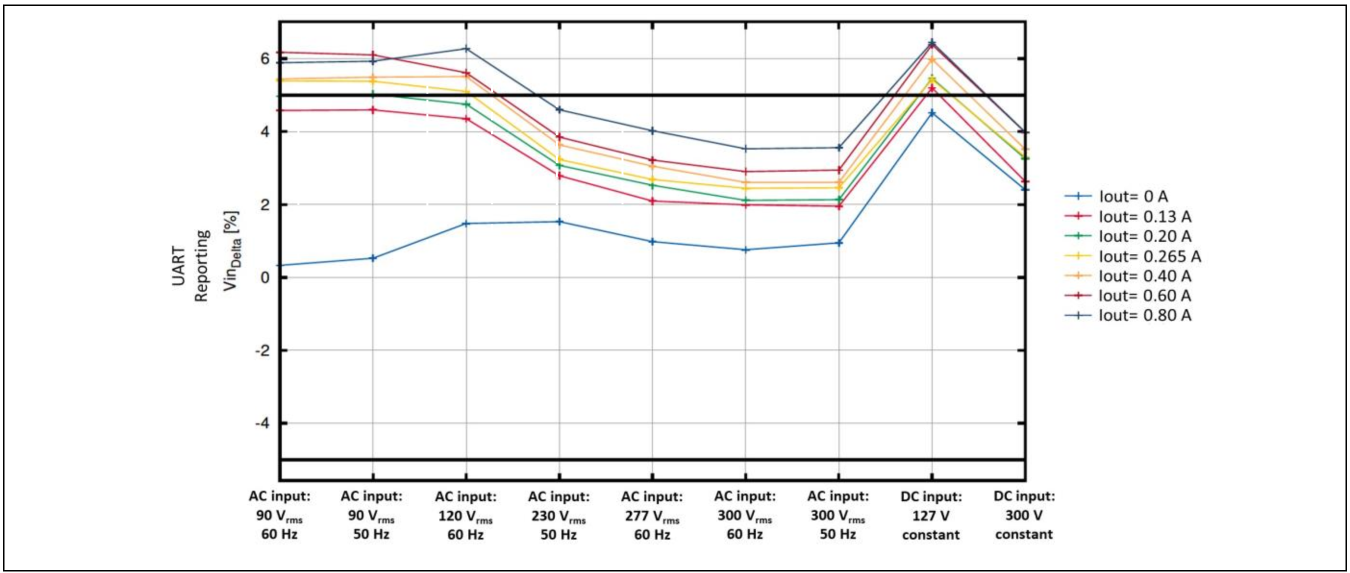



**Figure 21 UART reporting input voltage deviation test result**

The single board test result shows that the UART reporting line frequency $F_{line,UART}$ averaging value deviates in the range of -0.4 percent to 1.3 percent from the actual AC input frequency, as shown in **Figure 22**. It is important to note that the $F_{line,UART}$ deviation data below is measured with static input and output conditions applied from start-up to steady-state. As the $F_{line,UART}$ cannot be synchronized with the AC input frequency in ABM, some $F_{line,UART}$ deviation data below obtained under ABM operation (e.g., with $I_{out}$ = 0 A) can therefore become invalid, if the line frequency changes (e.g., from 50 Hz to 60 Hz, or vice-versa) after start-up.

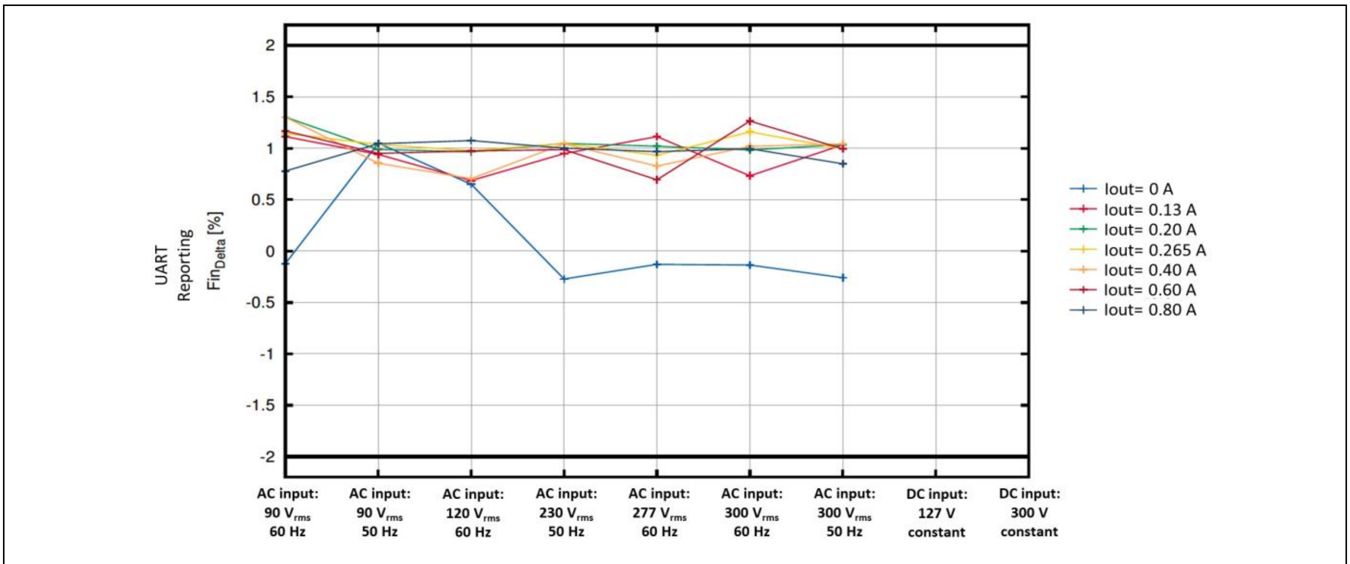



**Figure 22 UART reporting line frequency deviation test result**

The UART reporting IC junction temperature $T_{J,UART}$ sample deviates in the range of -6 percent to 6 percent from the actual IC junction temperature.

### 5.8.2 Input voltage loss reporting

With both $EN_{UART,REPORTING}$ and $EN_{SEND,V,IN,LOSS}$ parameters enabled by default in this reference design, the **XDPL8219** UART pin transmits either $40_H$ data packet(s), or a number of $ED_H$ data within the regular data packet, or both, to indicate the input voltage loss, if the consecutive number of too-low ZCD pin clamping current $-I_{IV}$ sampling values have exceeded a limit.

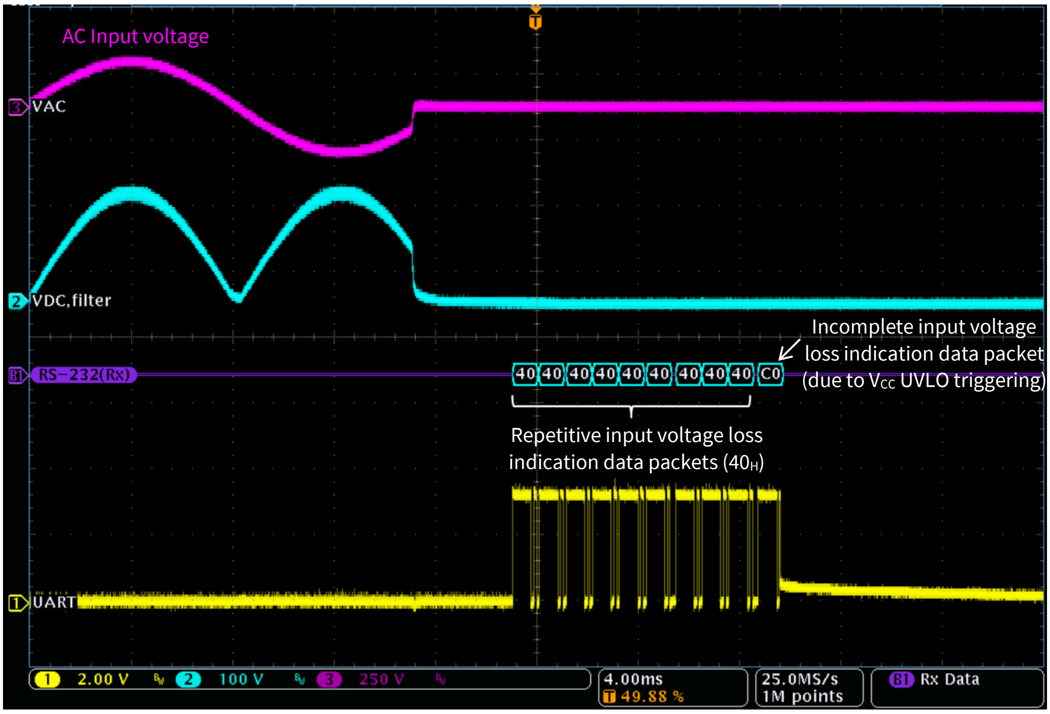



**Figure 23 Typical input voltage loss indication – data packets capturing and decoding ($40_H$)**

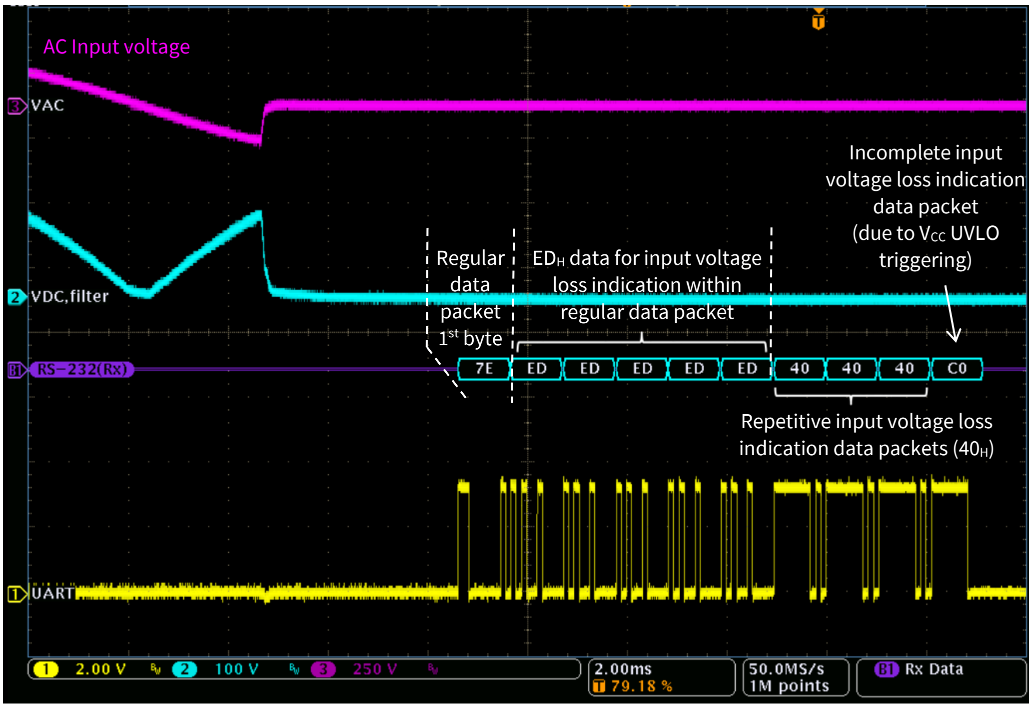



**Figure 24 Input voltage loss indication within regular data packet capturing and decoding ($ED_H$)**

### 5.8.3 Error code reporting

With both $EN_{UART,REPORTING}$ and $EN_{SEND,LAST;ERROR;CODE}$ parameters enabled by default in this reference design, the **XDPL8219** UART pin transmits a data packet which contains the error code of the last triggered protection, right before every auto restart.

If the triggered protection reaction is hardware restart, stop-mode or latch-mode, the error code will not be sent out. For example, if the $V_{CC}$ OVP has been triggered, with the default $V_{CC}$ OVP reaction parameter setting of $Reaction_{VCC,OVP}$ = “Latch-Mode” in this reference design, the UART reporting error code data packet will not be sent out.

**Figure 25** shows an example of capturing and decoding the error code data packet, by zooming into the UART signal at auto restart, after the protection has been triggered. According to **Table 4**, the obtained error code of $FFEF_H$ shows that the last triggered protection is start-up output UVP.

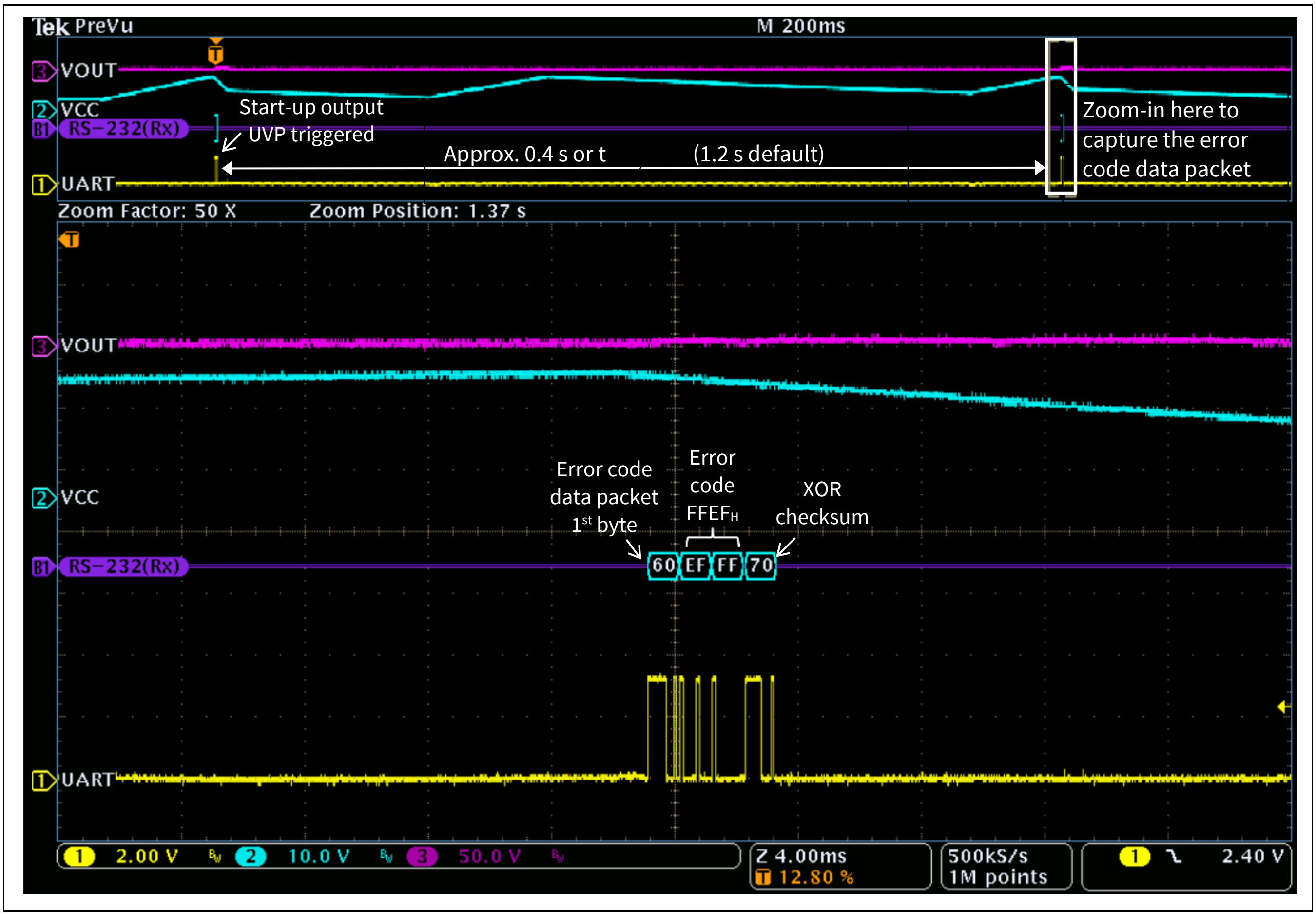



**Figure 25** **Error code data packet capturing and decoding ($FFEF_H$, as an example)**

**Table 4** **UART reporting error code data interpretation**

| Error code data | | Last triggered protection |
|---|---|---|
| $UART_{polarity}$ = high | $UART_{polarity}$ = low | |
| $0000_H$ | $FFFF_H$ | None |
| $0001_H$ | $FFFE_H$ | Output OVP |
| $0008_H$ | $FFF7_H$ | Regulated mode output UVP |
| $0010_H$ | $FFEF_H$ | Start-up output UVP |

| Error code | | Last triggered protection |
|---|---|---|
| $UART_{polarity}$ = high | $UART_{polarity}$ = low | |
| $0020_H$ | $FFDF_H$ | Transformer demagnetization time shortage protection |
| $0040_H$ | $FFBF_H$ | Input UVP |
| $0080_H$ | $FF7F_H$ | Input OVP |
| $0100_H$ | $FEFF_H$ | IC overtemperature protection |
| $0200_H$ | $FDFF_H$ | $V_{CC}$ OVP |
| $0400_H$ | $FBFF_H$ | Interrupt watchdog protection (may get triggered for input UVP) |
| $0800_H$ | $F7FF_H$ | MOSFET over-current protection |
| $4000_H$ | $BFFF_H$ | ADC watchdog protection (may get triggered for input UVP) |
| $8000_H$ | $7FFF_H$ | Regulated mode $V_{CC}$ UVP |

## 5.9 Isolated UART reporting

If the UART reporting signals are to be probed from the isolated UART reporting evaluation plug-in board's connector X1 (based on the recommended setup and procedures printed on the PCB), the default $UART_{polarity}$ = "Low" parameter setting in this reference design must be used, so the captured UART signals shown in **Section 5.8.1**, **Section 5.8.2** and **Section 5.8.3** will be inverted.

For such a setup, the oscilloscope settings for data decoding should be based on logic level of low = 0 and high = 1, with a baud rate of 9600 bps.

## 5.10 Thermal test

The open-frame thermal test was done on the reference design using an infrared thermography camera at an ambient temperature of approximately 25°C. The temperature measurements of the following main components (see **Table 5**) were taken after 2 hours' running.

**Table 5 Main components for temperature measurement**

| PCB bottom | | | PCB top | | |
|---|---|---|---|---|---|
| **Measure point** | **Component** | **Description** | **Measure point** | **Component** | **Description** |
| sp1 | Q1 | Flyback MOSFET (IPD80R900P7) | sp1 | T1 | Flyback transformer |
| sp2 | IC3 | Flyback controller (XDPL8219) | sp2 | D101 | Secondary main output diode |
| | | | sp3 | PCB | PCB above Q1 |

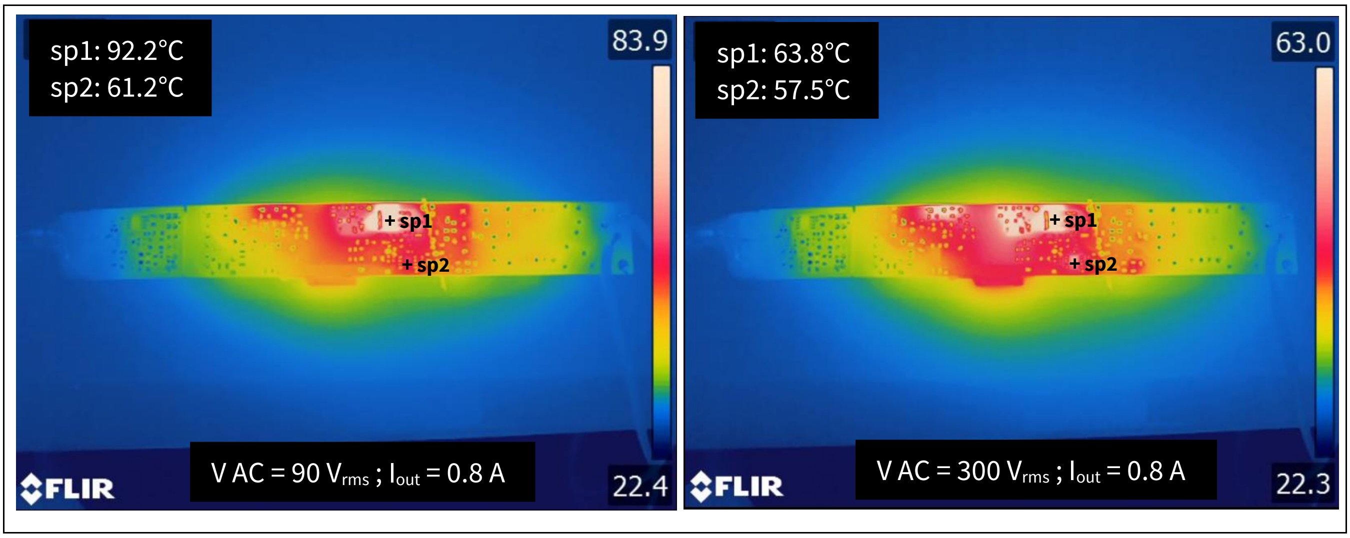



**Figure 26 Infrared thermal image result of PCB bottom components**

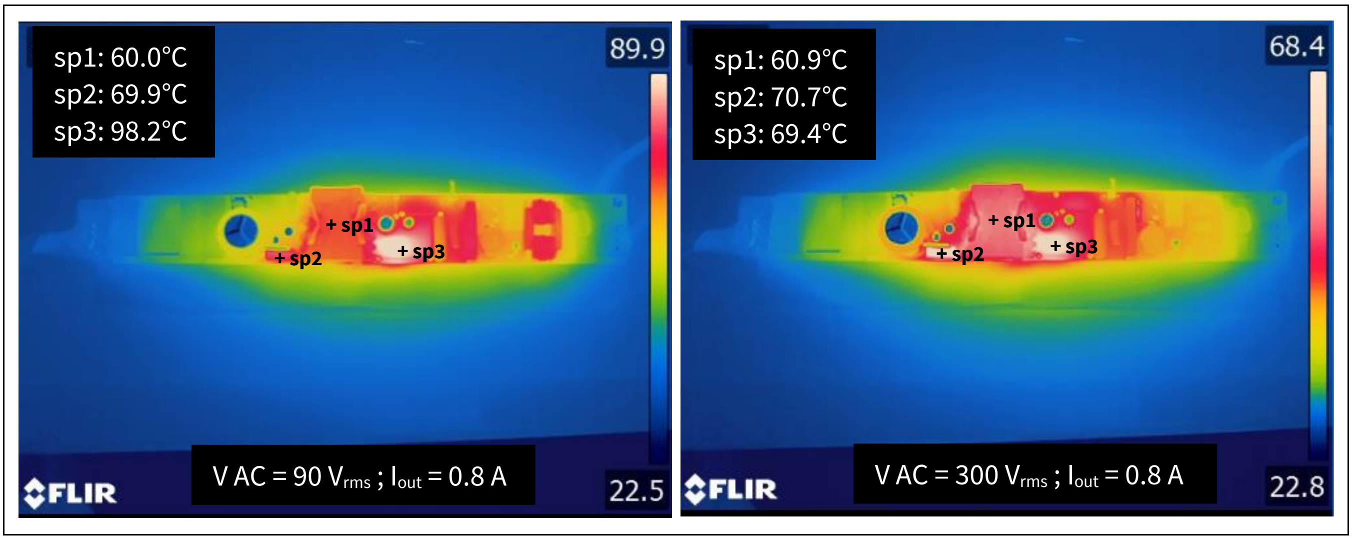



**Figure 27 Infrared thermal image result of PCB top components**

# 6 BOM and transformer specifications

This section provides the BOM and the transformer specifications.

## 6.1 BOM

**Table 6 BOM of main board**

| Designator | Value | Part number | Manufacturer |
|---|---|---|---|
| BR1 | Bridge rectifier/4 A/1000 V | GBU407 D2G | Taiwan Semiconductor |
| C1 | 0.1 µF/305V AC | B32922C3104K | EPCOS |
| C2 | 0.1 µF/310 V AC | 890334023023CS | Würth |
| C3 | 6.8 nF/630 V | GRM31BR72J682KW01L | Murata |
| C4 | 220 nF/630 V | ECW-FA2J224J | Panasonic |
| C5 | 47 pF/50 V/C0G | CL10C470JB8NNNC | Samsung Electro-Mechanics |
| C6 | 220 µF/35 V/20 percent | EKMG350EC3221MHB5D | Nippon Chemi-Con |
| C7 | 22 µF/50 V/20 percent | 50PX22MEFC5X11 | Rubycon |
| C9 | 2200 pF/500 V AC | VY1222M47Y5UQ63V0 | Vishay |
| C31 | 470 pF/25 V/COG | 06033A471JAT2A | AVX |
| C32 | 1 nF/50 V | 12065C102KAT2A | AVX |
| C38, C108, C109 | 100 nF/50 V/X7R/10 percent | CL10B104KB8NNNC | Samsung Electro-Mechanics |
| C40 | 1500 pF/300 V AC | DE1E3KX152MN4AP01F | Murata |
| C41 | 1 nF/630 V/COG | GRM31B5C2J102JW01L | Murata |
| C101 | 150 pF/630 V/C0G/5 percent | GRM31A5C2J151JW01 | Murata |
| C102 | 470 µF/80 V | EKZE800ELL471MM20S | United Chemi-Con |
| C104 | 47 µF/35 V | ECA1VHG470 | Panasonic |
| C105 | 100 µF/25 V | UVY1E101MDD | Nichicon |
| C106 | 1 µF/100 V/X7R/10 percent | 12061C105K4Z2A | AVX |
| C107 | 0.1 µF/100 V | 12061C104KAT2A | AVX |
| C110 | 3.3 µF/25V | CGA5L1X7R1E335K160AC | TDK |
| D3 | Fast diode/3 A/1 kV | RS3MB-13-F | DIODES |
| D4 | Fast diode/0.25 A/250 V | BAV103,115 | Nexperia |
| D102, D103 | Schottky diode/2 A/150 V | S215FA | Onsemi |
| D5 | Fast diode/0.15 A/100 V | 1N4148WS-7-F | Diodes Incorporated |
| D10 | ESD diode/6.8 V | PESD5V0S2UQ,115 | Nexperia |
| D20, D21 | Standard diode/1 A/1000 V | 1N4007RLG | ON Semi |
| D101 | Hyper-fast diode/15 A/300 V | VS-15ETH03PBF | Vishay |
| D104, D105, D106 | Fast diode/0.15 A/100 V | 1N4148WS-E3-18 | Vishay |
| F1 | Fuse/2 A | MCMSF 2 A 250 V | Multicomp |
| IC3 | Flyback controller | XDPL8219 | Infineon |
| J1 | 20 mm pitch jumper with insulated sleeving | TCW21 250G | PRO Power |
| J2 | 15 mm pitch jumper | TCW21 250G | PRO Power |
| J3 | 7.5 mm pitch jumper | TCW21 250G | PRO Power |
| L1 | Common mode choke/39 mH/0.8 A | B82732F2801B001 | Epcos |
| L2 | Differential choke/470 µH/1.15 A | 7447480471 | Würth |

| Designator | Value | Part number | Manufacturer |
|---|---|---|---|
| MOV1, MOV2 | Varistor/510 V/10 percent | ERZE08A511 | Panasonic |
| PC1 | Optocoupler/100 percent CTR | TLP383(GR-TPL,E) | Toshiba |
| Q1 | MOSFET/0.9 Ω/800 V | IPD80R900P7 | Infineon |
| R1, R104, R107 | 0 R | RC1206JR-070RL | Yageo/Phycomp |
| R2 | 20 k | AC0603FR-0720KL | Yageo/Phycomp |
| R3 | 160 R/2 W/5 percent | ERG-2SJ161V | Panasonic |
| R4 | 36 k | LR1F36K | TE |
| R6 | 16 k | ERJ-8ENF1602V | Panasonic |
| R7, R8 | 240 k | WCR1206-240KFI | Welwyn |
| R10 | 27 k | MCSR12X2702FTL | Multicomp |
| R11 | 3.9 k | MCWR06X3901FTL | Multicomp |
| R14 | 0.2 | LR2010-R20FW | Welwyn |
| R15 | 39 R | ERJ-8ENF39R0V | Panasonic |
| R16 | 10 R | CRCW080510R0FK | Vishay |
| R18 | 1 R | CRCW08051R00FK | Vishay |
| R20 | 0 R | RC0805JR-070RL | Yageo |
| R21, R22, R23 | 10 Meg | CRCW120610M0FKEB | Vishay |
| R101 | 10 R | RC1206FR-0710RL | Yageo/Phycomp |
| R102 | 820 R | RMCF1206FT820R | Stackpole Electronics Inc |
| R124, R125, R126 | 510 R | ERJU14F5100U | Panasonic |
| S101 | Tactile switch | 430 156 095 726 | Würth |
| T1 | PQ2620; 544 µH; Np = 32; Ns = 10; Na(5-6) = 3; Na(4-5) = 1; Na,sec(11-10) = 1; Na,sec(10-9) = 2 | 750343699 Rev03 | Würth |
| X1 | Terminal strip/3 pins/3.5 mm pitch | 250-203 | WAGO |
| X2 | Header/3 pins/2.54 mm pitch | HTSW-103-07-G-S | Samtec |
| X200-A | Terminal block/6 pins/3.81 mm pitch | 691322310006 | Würth |
| ZD101 | Zener/68 V/5 percent/1.25 W | SML4760A-E3/61 | Vishay |

**Table 7 BOM of 54 V CV SSR plug-in board**

| Designator | Value | Part number | Manufacturer |
|---|---|---|---|
| C201 | 470 nF/50 V | 12065C474KAT2A | AVX |
| C204 | 0.1 µF/50 V | MC0603B104K500CT | Multicomp |
| C205 | 470 pF/25 V/COG | 06033A471JAT2A | AVX |
| D201 | 0 R | RC0603JR-070RL | Yageo/Phycomp |
| D202 | Fast diode/0.15 A/100 V | 1N4148WS-E3-18 | Vishay |
| IC201-A | Op-amp IC with reference voltage | TSM103WAIDT | ST |
| J202 | 15 mm pitch jumper | TCW21 250G | PRO Power |
| R201-A | 120 k | RR0816P-124D | Susumu |
| R201-B | 7.5 k | MCMR12X7501FTL | Multicomp |
| R202 | 6.2 k | ERA-8AEB622V | Panasonic |
| R203 | 47 k | CRCW060347K0FK | Vishay |

| Designator | Value | Part number | Manufacturer |
|---|---|---|---|
| R204 | 1 k | MCWR12X1001FTL | Multicomp |
| R205, R211 | 0 R | RC1206JR-070RL | Yageo/Phycomp |
| R206 | 15 k | RC1206FR-0715KL | Yageo/Phycomp |
| R208 | 0 R | RC0603JR-070RL | Yageo/Phycomp |
| R210 | 6.2 k | MCWR12X6201FTL | Multicomp |
| R214 | 820 k | MCWR06X8203FTL | Multicomp |
| X200-B | Terminal block/6 pins/3.81 mm pitch | 691309310006 | Würth |
| X300-A | Terminal block/4 pins/5.08 mm pitch | 691313510004 | Würth |

**Table 8 BOM of Isolated UART evaluation plug-in board**

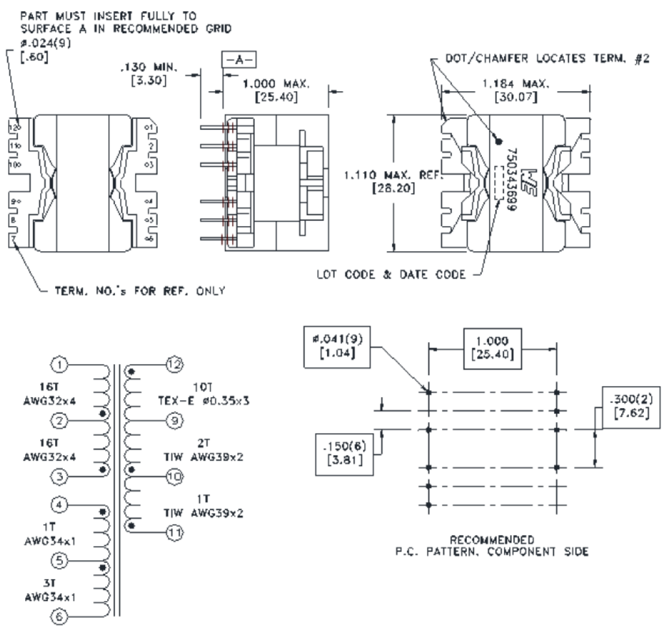
| Designator | Value | Part number | Manufacturer |
|---|---|---|---|
| D1 | Fast diode/0.15 A/100 V | Diodes Incorporated | 1N4148W-7-F |
| Q1 | Small-signal MOSFET/60 V | Infineon Technologies | 2N7002 |
| R1 | 3 k | Vishay | CRCW08053K00FK |
| R2 | 47 k | Vishay | CRCW080547K0FK |
| R3 | 220 k | Vishay | CRCW0805220KFK |
| R4 | 100 k | Vishay | CRCW0805100KFK |
| U1 | Optocoupler, phototransistor output | Vishay | TCLT1103 |
| X1 | Board-to-board connector/3 pin/2.54 mm pitch | Amphenol ICC (FCI) | 68001-103HLF |
| X2 | Header/3 pins/2.54 mm pitch | Sullins | PPPC031LGBN-RC |

## 6.2 Transformer specifications

| CUSTOMER TERMINAL | RoHS | LEAD(Pb)--FREE |
|---|---|---|
| Sn 96%, Ag 4% | Yes | Yes |

more than you expect

WÜRTH ELEKTRONIK




ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

| PARAMETER | | TEST CONDITIONS | VALUE |
|---|---|---|---|
| D.C. RESISTANCE | 1-3 | @20°C | 0.275 ohms max. |
| D.C. RESISTANCE | 4-5 | @20°C | 0.080 ohms max. |
| D.C. RESISTANCE | 5-6 | @20°C | 0.205 ohms max. |
| D.C. RESISTANCE | 9-10 | @20°C | 0.235 ohms max. |
| D.C. RESISTANCE | 9-12 | @20°C | 0.042 ohms max. |
| D.C. RESISTANCE | 10-11 | @20°C | 0.138 ohms max. |
| INDUCTANCE | 3-1 | 10kHz, 100mV, Ls | 544.00uH ±7% |
| LEAKAGE INDUCTANCE | 3-1 | tie(4 THRU 12),100kHz, 100mV, Ls | 4.50μH max. |
| DIELECTRIC | 1-12 | tie(3+4), 2300VAC, 1 second | 1840VAC, 1 minute |
| DIELECTRIC | 12-CORE | 2300VAC, 1 second | 1840VAC, 1 minute |
| TURNS RATIO | | (3-1):(4-5) | 32:1, ±2% |
| TURNS RATIO | | (3-1):(5-6) | 10.67:1, ±2% |
| TURNS RATIO | | (3-1):(10-9) | 16:1, ±2% |
| TURNS RATIO | | (3-1):(12-9) | 3.2:1, ±2% |
| TURNS RATIO | | (3-1):(11-10) | 32:1, ±2% |

**GENERAL SPECIFICATIONS:**

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by UL1310 and UL8750:

- Reinforced insulation for a primary circuit at a working voltage of 300Vrms (operating frequency of <2MHz).

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

| | | | | | | |
|---|---|---|---|---|---|---|
| DFM | | Packaging Specifications | CONVENTION PLACEMENT | Tolerances unless otherwise specified: | DRAWING TITLE | PART NO. |
| DATE | | Method: Tray | | Angles: ±1° Decimals: ±.005 [.13] | TRANSFORMER | 750343699 |
| ENG | HJH | PKG-0253 | | Fractions: ±1/64 Footprint: ± .001 [.03] | | |
| REV. | 03 | | | This drawing is dual dimensioned. Dimensions in brackets are in millimeters. | | |
| DATE | 2020/1/14 | www.we-online.com/midcom | | | | SPECIFICATION SHEET 1 OF 1 |

**Figure 28 Flyback transformer (T1) specifications**

# 7 References

[1] XDPL8219 datasheet
[2] XDPL8219 design guide

# 8 Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| V 1.0 | 2020-07-13 | Initial version |
| V 1.1 | 2020-07-24 | Section 5.9:<br>Correction of text from ".. logic level of low = **1** and high = **0**, .." to "..logic level of low = **0** and high = **1**,..". |
| | | |

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