

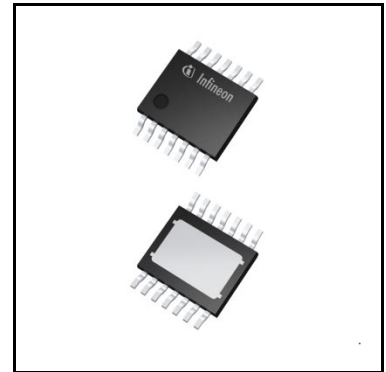
# TLD2132-1EP

## LITIX™ Basic+



### Features

- Single channel device with integrated and protected output stage (current source), optimized to drive LEDs as additional low cost current source
- High output current (up to 240 mA)
- Very low current consumption in sleep mode
- Very low output leakage when channel is “off”
- Low current consumption during fault
- Output currents’ control via external low power resistor
- Additional output current demand supported by LITIX™ Companion direct drive without additional components
- Very high precision digital dimming supported
- Intelligent fault management: up to 16 and more devices can share a common error network with only one external resistor
- Reverse polarity protection allows reduction of external components and improves system performance at low battery/input voltages
- Overload protection
- Wide temperature range:  $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$
- Output current control via external low power resistor
- Green product (RoHS compliant)



### Potential applications

- Cost effective “stop”/ “tail” function implementation with shared and separated LEDs per function
- Turn indicators
- Position, fog, rear lights and side markers
- Animated light functions like wiping indicators and “welcome/goodbye” functions
- Day Running Light
- Interior lighting functions like ambient lighting (including RGB color control), illumination and dash board lighting
- LED indicators for industrial applications and instrumentation

### Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

## Description

The LITIX™ Basic+ TLD2132-1EP is a single channel high-side driver IC with integrated output stage. It is designed to control LEDs with a current up to 240 mA. In typical automotive applications the device is capable of driving 3 red LEDs with a current up to 180 mA and even above, if not limited by the overall system thermal properties. Practically, the output current is controlled by an external resistor or reference source, independently from load and supply voltage changes.

**Table 1 Product summary**

Parameter	Symbol	Values
Operating voltage	$V_{S(nom)}$	5.5 V ... 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUT(max)}$	40 V
Nominal output (load) current	$I_{OUT(nom)}$	180 mA (nominal) when using the automotive supply voltage range 8 V - 18 V. Currents up to $I_{OUT(max)}$ are possible with low thermal resistance $R_{thJA}$
Maximum output (load) current	$I_{OUT(max)}$	240 mA depending on $R_{thJA}$
Current accuracy at $R_{SET} = 10\text{ k}\Omega$	$K_{LT}$	900 ±5%
Current consumption in sleep mode	$I_{S(sleep, typ)}$	0.1 µA
Maximum current consumption during fault	$I_{S(fault, ERRN)}$	850 µA or less when fault is detected from another device (disabled via ERRN)

Type	Package	Marking
TLD2132-1EP	PG-TSDSO-14	TLD2132

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Block diagram

1 Block diagram

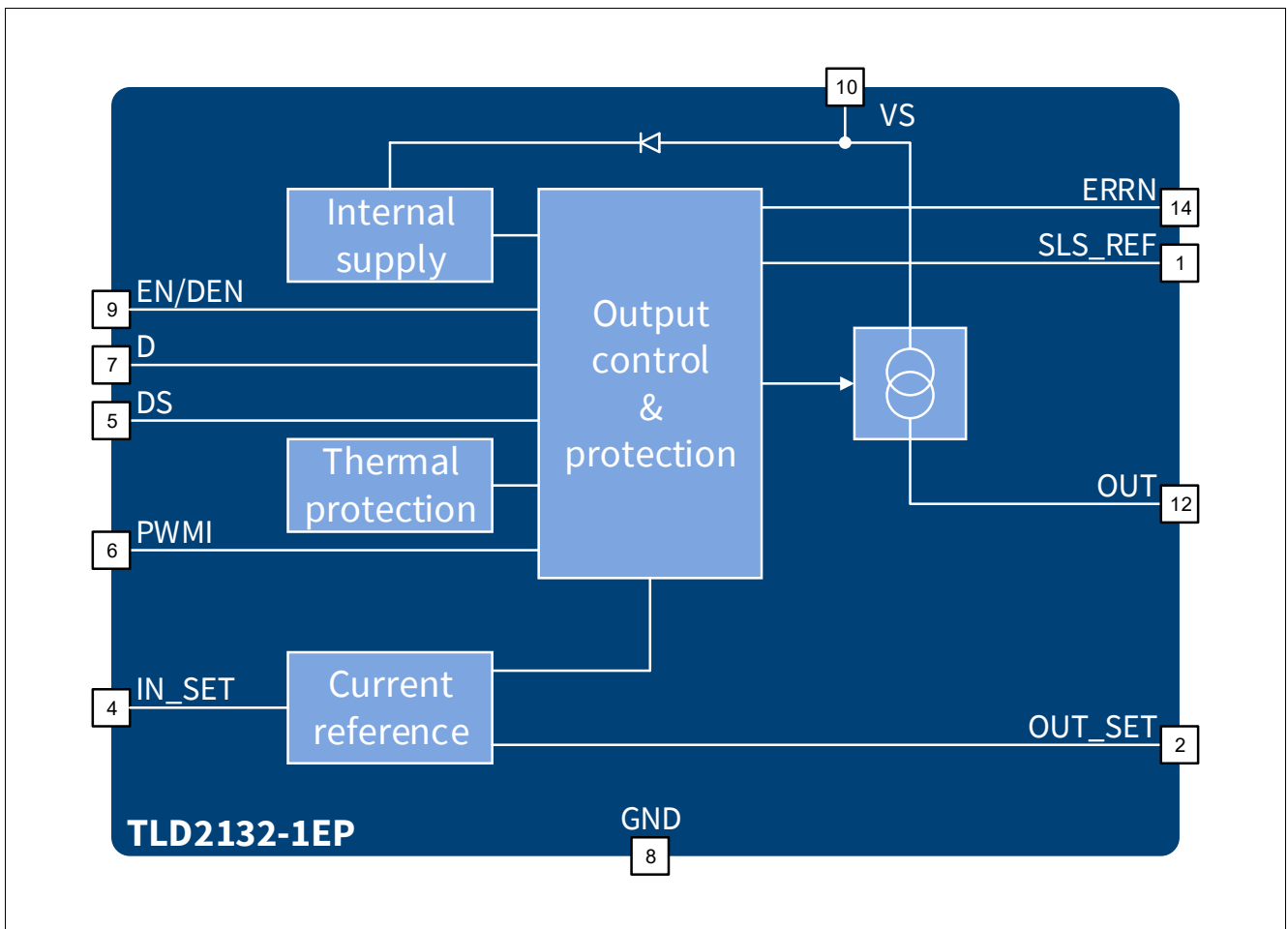


Figure 1 Block diagram

Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment

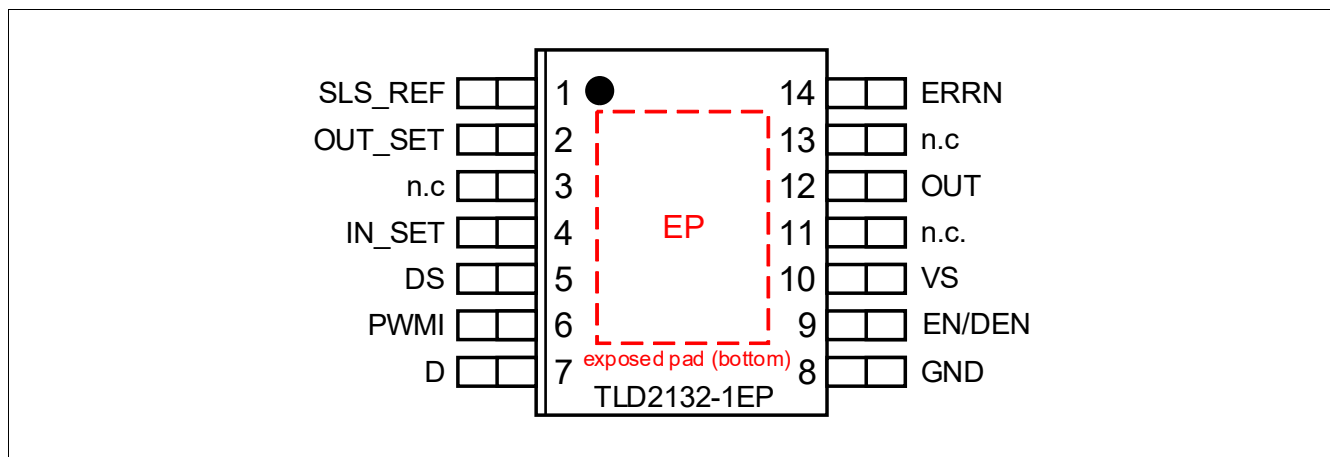


Figure 2 Pin configuration

### 2.2 Pin definitions and functions

Pin	Symbol	Function
10	VS	<b>Supply voltage;</b> Connected to battery or supply control switch, with EMC filter
8	GND	<b>Ground;</b> Signal ground
4	IN_SET	<b>Control input for OUT channel;</b> Connect to a low power resistor to adjust OUT output current. Alternatively, a different current reference (i.e. the OUT_SET of another LITIX™ Basic+ LED Driver) may be connected
2	OUT_SET	<b>Control output for additional current source;</b> If an additional channel or output current with same input control is needed, connect this pin to the IN_SET pin of the additional LED driver. If not used, leave the pin open
6	PWMI	<b>PWM input;</b> Connect to an external PWM controller. If not used, connect to GND
1	SLS_REF	<b>Single LED short reference input;</b> Connect to a low power resistor or a voltage reference to adjust Internal SLS threshold. If not used, connect to GND
5	DS	<b>Single LED short delay/restart input;</b> Connect to a capacitor, leave open or connect to GND, depending on the required diagnosis management for single LED short detection (see <a href="#">Chapter 6</a> for further details)
7	D	<b>Disable/delay error input;</b> Connect to a capacitor, leave open or connect to GND, depending on the required diagnosis management (see <a href="#">Chapter 6</a> for further details)
14	ERRN	<b>ERROR flag I/O;</b> Open drain, active low. Connect to a pull-up resistor

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**Pin configuration**

<b>Pin</b>	<b>Symbol</b>	<b>Function</b>
9	EN/DEN	<b>Output enable and diagnosis control input;</b> Connect to a control input (i.e. to VS via a resistor divider or a Zener diode) to enable OUT control and diagnosis capability
12	OUT	<b>Channel output;</b> Connect to the target load
3, 11, 13	n.c.	<b>Not connected;</b> Leave these pins open
Exposed Pad	EP	<b>Exposed Pad;</b> Connected to GND-pin in application

General product characteristics

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltage</b>							
Supply voltage	$V_S$	-18	–	40	V	–	P_4.1.1
EN/DEN voltage	$V_{EN/DEN}$	-18	–	40	V	–	P_4.1.3
EN/DEN voltage related to $V_S$ : $V_{EN/DEN} - V_S$	$V_{EN/DEN(VS)}$	-40	–	18	V	–	P_4.1.4
EN/DEN voltage related to $V_{OUT}$ : $V_{EN/DEN} - V_{OUT}$	$V_{EN/DEN(VOUT)}$	-18	–	40	V	–	P_4.1.5
Output voltage	$V_{OUT}$	-1	–	40	V	–	P_4.1.10
Output voltage related to $V_S$ : $V_S - V_{OUT}$	$V_{OUT(VS)}$	-18	–	40	V	–	P_4.1.11
IN_SET voltage	$V_{IN\_SET}$	-0.3	–	6	V	–	P_4.1.12
OUT_SET voltage	$V_{OUT\_SET}$	-0.3	–	6	V	–	P_4.1.13
PWMI voltage	$V_{PWMI}$	-0.3	–	6	V	–	P_4.1.14
ERRN voltage	$V_{ERRN}$	-0.3	–	40	V	–	P_4.1.18
D Voltage	$V_D$	-0.3	–	6	V	–	P_4.1.19
DS voltage	$V_{DS}$	-0.3	–	6	V	–	P_4.1.42
SLS_REF voltage	$V_{SLS\_REF}$	-0.3	–	6	V	–	P_4.1.43
<b>Current</b>							
Output current	$I_{OUT}$	0	–	250	mA	–	P_4.1.23
PWMI current	$I_{PWMI}$	-0.5	–	0.5	mA	–	P_4.1.26
IN_SET current	$I_{IN\_SET}$	0	–	300	$\mu\text{A}$	–	P_4.1.30
D current	$I_D$	-0.5	–	0.5	mA	–	P_4.1.31
DS current	$I_{DS}$	-0.5	–	0.5	mA	–	P_4.1.44
SLS_REF current	$I_{SLS\_REF}$	-0.5	–	0	mA	–	P_4.1.45
OUT_SET current	$I_{OUT\_SET}$	0	–	0.5	mA	–	P_4.1.32
<b>Temperature</b>							
Junction temperature	$T_J$	-40	–	150	$^\circ\text{C}$	–	P_4.1.33
Storage temperature	$T_{stg}$	-55	–	150	$^\circ\text{C}$	–	P_4.1.34
<b>ESD susceptibility</b>							
ESD susceptibility all pins to GND	$V_{ESD}$	-2	–	2	kV	HBM <sup>2)</sup>	P_4.1.36

**General product characteristics**

**Table 2 Absolute maximum ratings<sup>1)</sup>** (cont'd)

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility all pins to GND	$V_{ESD}$	-500	–	500	V	CDM <sup>3)</sup>	P_4.1.37
ESD susceptibility Pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	CDM <sup>3)</sup>	P_4.1.38

- 1) Not subject to production test, specified by design
- 2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
- 3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**3.2 Functional range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage range for normal operation	$V_{S(nom)}$	5.5	–	18	V	–	P_4.2.1
Extended supply voltage for functional range	$V_{S(ext)}$	$V_{SUV(ON)}$	–	40	V	–	P_4.2.2
Junction temperature	$T_J$	-40	–	150	°C	–	P_4.2.4

*Note: Within the Normal Operation range, the IC operates as described in the circuit description. Within the Extended Operation range, parameters deviations are possible. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*



**General product characteristics**

**3.3 Thermal resistance**

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	$R_{thJC}$	–	–	10	K/W	<sup>1)2)</sup>	P_4.3.1
Junction to Ambient 1s0p board	$R_{thJA1}$	–	61 56	–	K/W	<sup>1)3)</sup> $T_A = 85^\circ\text{C}$ $T_A = 135^\circ\text{C}$	P_4.3.3
Junction to Ambient 2s2p board	$R_{thJA2}$	–	45 43	–	K/W	<sup>1)4)</sup> $T_A = 85^\circ\text{C}$ $T_A = 135^\circ\text{C}$	P_4.3.4

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and exposed pad are fixed to ambient temperature).  $T_A = 85^\circ\text{C}$ . Total power dissipation = 1.5 W
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. The product (chip+package) was simulated on a  $76.2 \times 114.3 \times 1.5$  mm board with  $70 \mu\text{m}$  Cu,  $300 \text{ mm}^2$  cooling area. Total power dissipation 1.5 W distributed statically and homogenously over all power stages
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a  $76.2 \times 114.3 \times 1.5$  mm board with 2 inner copper layers ( $2 \times 70 \mu\text{m}$  Cu,  $2 \times 35 \mu\text{m}$  Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over all power stages

Internal supply

## 4 Internal supply

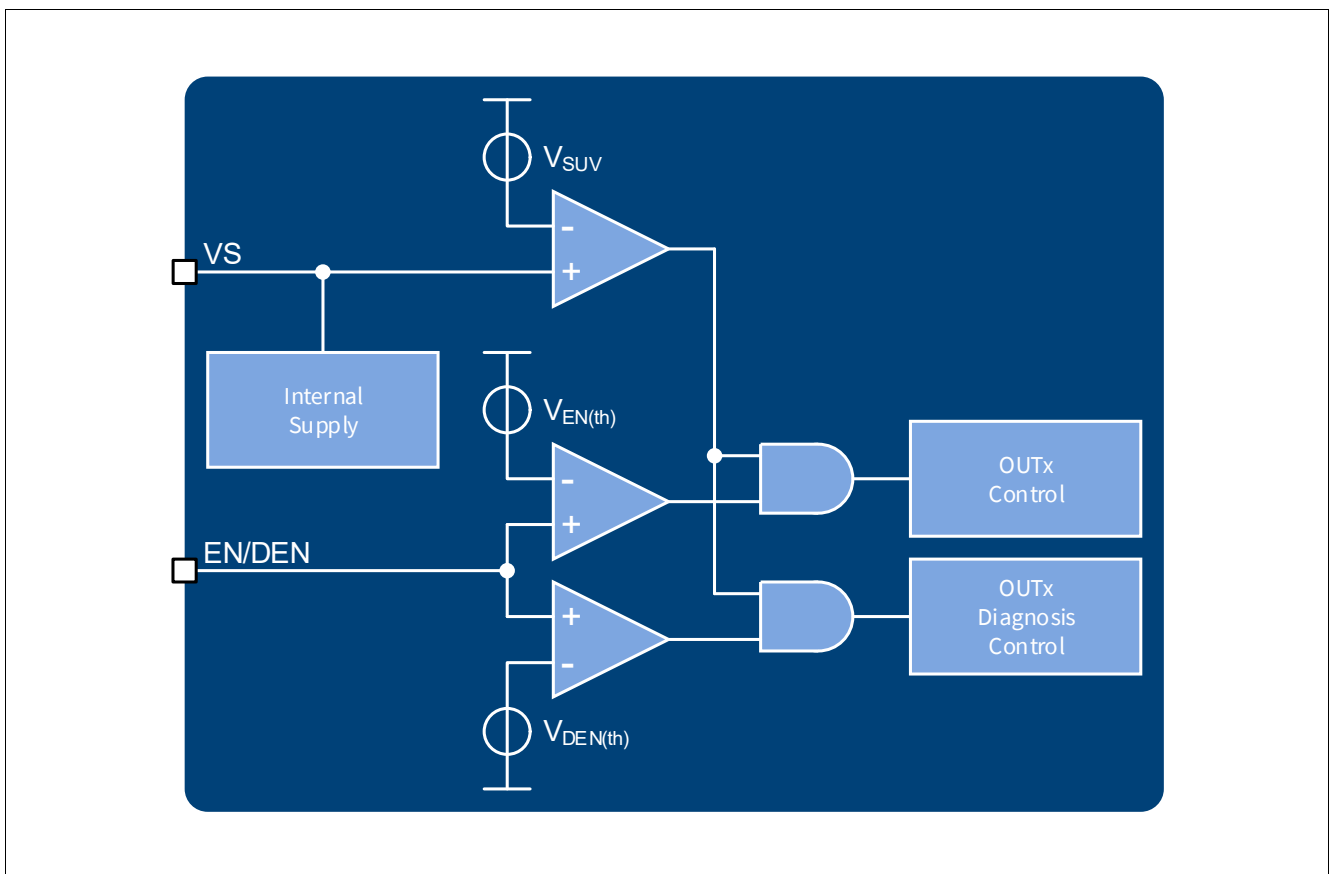
This chapter describes the internal supply in its main parameters and functionality.

### 4.1 Description

The internal supply principle is highlighted in the concept diagram of [Figure 3](#).

If the voltage applied at the EN/DEN pin is below  $V_{EN(th)}$  the device enters sleep mode. In this state all internal functions are switched off and the current consumption is reduced to  $I_{S(sleep)}$ .

As soon as the voltage applied at the supply pin  $V_S$  is above  $V_{SUV(ON)}$  and the voltage applied at the EN/DEN pin is above  $V_{EN(th)}$ , after the power-on reset time  $t_{POR}$ , the device is ready to deliver output current from the output stage. The power on reset time  $t_{POR}$  has to be taken into account also in relevant application conditions, i. e. with PWM control from  $V_S$  or EN/DEN lines.



**Figure 3** Internal supply

Furthermore, as soon as the voltage applied at the supply pin  $V_S$  is above  $V_{SUV(ON)}$  and the voltage applied to the EN/DEN pin  $V_{EN}$  is above  $V_{DEN(th)}$ , the device is ready to detect and report fault conditions via ERRN (error network pin) as described in [Chapter 6](#).

To program output enable and diagnosis enable via EN/DEN pin there are several possibilities, like a resistor divider from  $V_S$  to GND, a Zener diode from EN/DEN to  $V_S$  and also a logic control pin (e.g. from a microcontroller output).

Internal supply

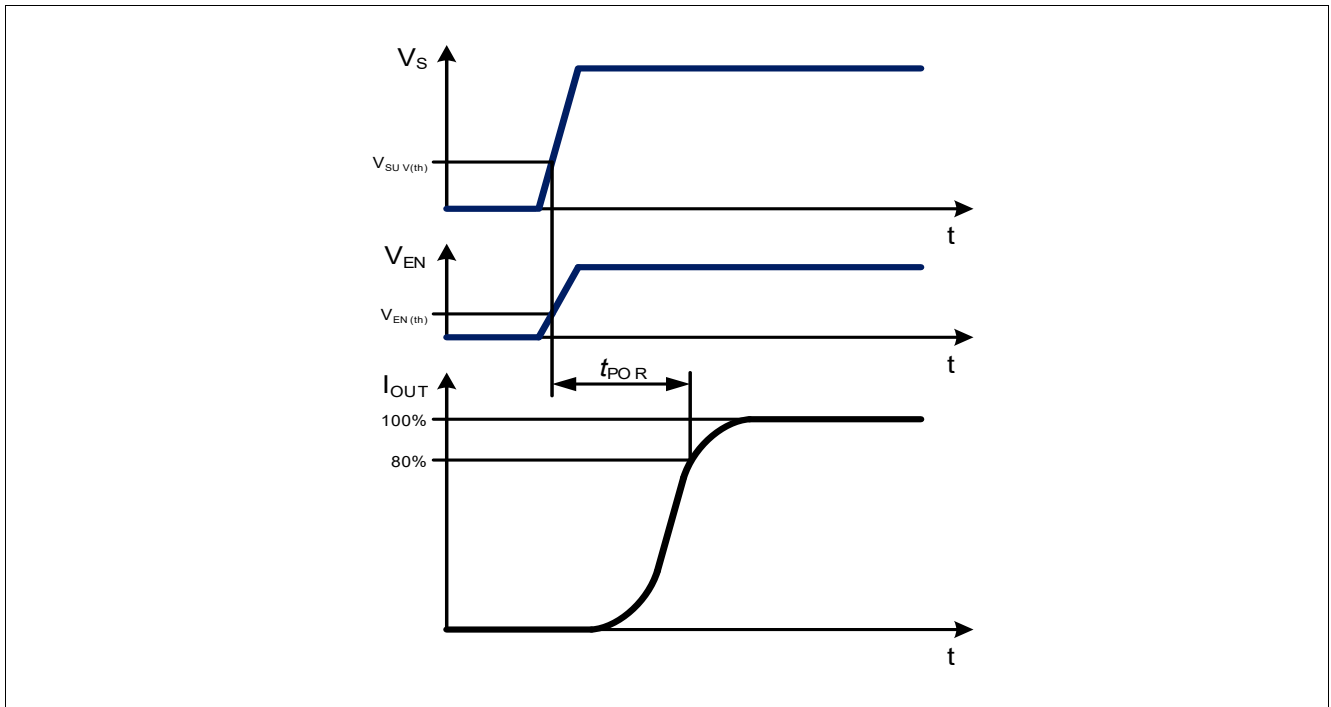


Figure 4 Power on reset timing diagram

**Internal supply**

**4.2 Electrical characteristics internal supply and EN pin**

**Table 5 Electrical characteristics: Internal supply and EN pin**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{S(\text{sleep})}$	–	0.1	2	$\mu\text{A}$	<sup>1)</sup> $V_{EN} = 0\text{ V}$ $T_J < 85^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUT} = 3.6\text{ V}$	P_5.2.1
Current consumption, active mode (no fault)	$I_{S(\text{active})}$	–	1.5	3	mA	$V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\ \mu\text{A}$ $T_J < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUT} = 3.6\text{ V}$	P_5.2.3
Current consumption during fault condition triggered from another device sharing ERRN bus	$I_{S(\text{fault, ERRN})}$	–	–	850	$\mu\text{A}$	$V_{EN} = 5.5\text{ V}$ $T_J < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{ERRN} = 0\text{ V}$ $V_{OUT} = 3.6\text{ V}$ D open	P_5.2.4
Current consumption during fault condition	$I_{S(\text{fault, OUT})}$	–	–	1.25	mA	$V_{EN} = 5.5\text{ V}$ $T_J < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUT} = 0\text{ V}$ $V_{OUT}$ D open	P_5.2.16

**Supply thresholds**

Required supply voltage for output activation	$V_{SUV(\text{ON})}$	–	–	5.5	V	$V_{EN} = V_S$ $V_{OUT} = 3\text{ V}$ $R_{IN\_SET} = 6.8\text{ k}\Omega$ $I_{OUT} > 50\% I_{OUT(\text{nom})}$	P_5.2.5
Required supply voltage for output deactivation	$V_{SUV(\text{OFF})}$	4.5	–	–	V	$V_{EN} = V_S$ $V_{OUT} = 3\text{ V}$ $R_{IN\_SET} = 6.8\text{ k}\Omega$ $I_{OUT} < 50\% I_{OUT(\text{nom})}$	P_5.2.6
Supply voltage activation hysteresis: $V_{SUV(\text{ON})} - V_{SUV(\text{OFF})}$	$V_{SUV(\text{hys})}$	–	200	–	mV	<sup>1)</sup> $V_{EN} > V_{EN(\text{th})}$	P_5.2.8

**EN pin**

EN output enable threshold	$V_{EN(\text{th})}$	1.4	1.65	1.8	V	$V_S = 5.5\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{IN\_SET} = 6.8\text{ k}\Omega$ $I_{OUT} = 50\% I_{OUT(\text{nom})}$	P_5.2.9
DEN diagnosis enable threshold	$V_{DEN(\text{th})}$	2.4	2.5	2.8	V	$V_S = 5.5\text{ V}$	P_5.2.11

**Internal supply**

**Table 5 Electrical characteristics: Internal supply and EN pin (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
DEN diagnosis enable hysteresis	$V_{DEN(hys)}$	–	120	–	mV	<sup>1)</sup> $R_{IN\_SET} = 6.8\text{ k}\Omega$	P_5.2.12
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	60	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN/DEN} = 2.8\text{ V}$	P_5.2.17
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	110	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN/DEN} = 5.5\text{ V}$	P_5.2.14
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	350	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN/DEN} = V_S$	P_5.2.15

**Timing**

Power on reset delay time	$t_{POR}$	–	–	25	$\mu\text{s}$	<sup>1)</sup> $V_S$ rising from $0\text{ V}$ to $13.5\text{ V}$ $V_{OUT} = 3.6\text{ V}$ $R_{IN\_SET} = 6.8\text{ k}\Omega$ $I_{OUT} = 80\% I_{OUT(nom)}$	P_5.2.13
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1) Not subjected to production test: specified by design

Power stage

## 5 Power stage

The output stage is realized as high-side current source with an output current up to 240mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.

The maximum output current is limited by the power dissipation and used PCB cooling areas.

For an operating output current control loop, the supply and output voltage have to be considered according to the following parameters:

- Required supply voltage for current control  $V_{S(CC)}$
- Voltage drop over through the output stage during current control  $V_{PS(CC)}$
- Required output voltage for current control  $V_{OUT(CC)}$

### 5.1 Protection

The device provides embedded protective functions, which are designed to prevent IC damage under fault conditions described in this datasheet. Fault conditions are considered as “outside” normal operating range. Protective functions are not designed for continuous nor for repetitive operations.

#### 5.1.1 Thermal protection

A thermal protection circuitry is integrated in the device. It is realized by a temperature monitoring of the output stages.

As soon as the junction temperature exceeds the current reduction temperature threshold  $T_{J(CRT)}$  the output current can be reduced by the device by reducing the IN\_SET reference voltage  $V_{IN\_SET(ref)}$ . This feature greatly helps to avoid LEDs flickering during static output overload conditions. Furthermore, it helps to protect the LEDs, which are mounted thermally close to the device, against overtemperature. If the device temperature still increases, the three output currents decrease close to 0 A. As soon as the device cools down the output currents rise again.

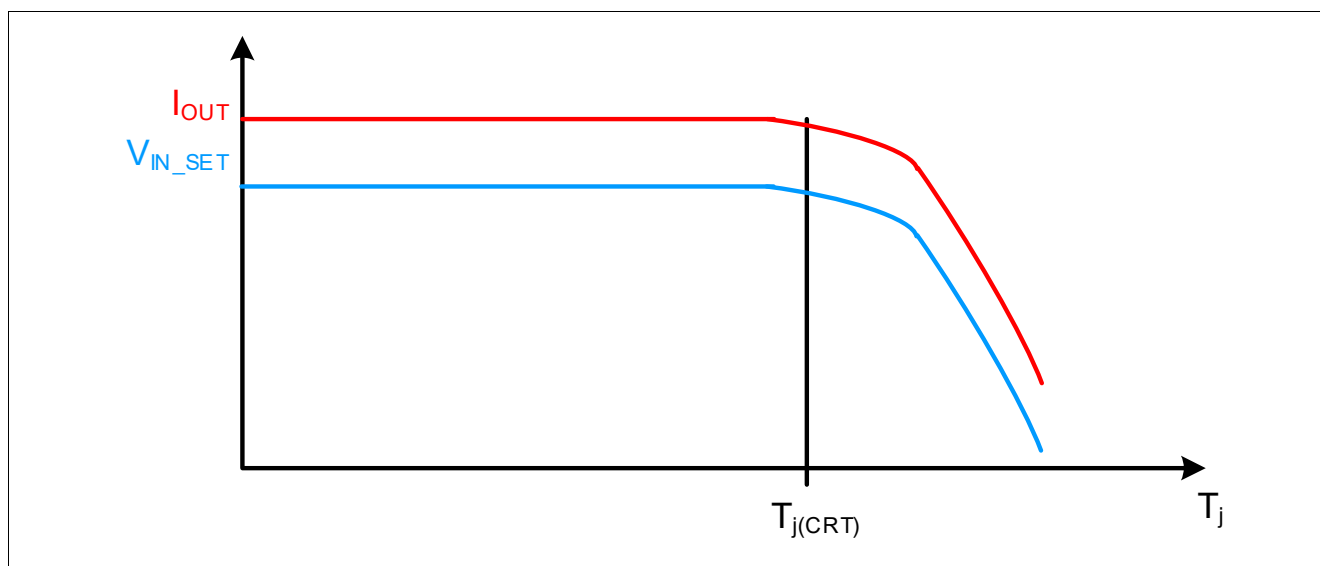


Figure 5 Output current reduction at high temperature (qualitative diagram)

Note: It is assumed that a configuration resistor  $R_{SET}$  is applied from IN\_SET to GND, and not a current source, to make the protection effective.

Power stage

### 5.1.2 Reverse battery protection

The device has an integrated reverse battery protection feature. This feature protects the driver IC itself and, potentially, also connected LEDs. The output reverse current is limited to  $I_{OUT(REV)}$  by the reverse battery protection.

## 5.2 Output configuration via IN\_SET, OUT\_SET and PWMI pins

Outputs current can be defined via IN\_SET and OUT\_SET (to drive additional devices without further external components) pin.

### 5.2.1 IN\_SET pin

The IN\_SET pin is a multiple function pin for the output current definition and input control.

Output current definition and analog dimming control can be done defining accordingly the IN\_SET current.

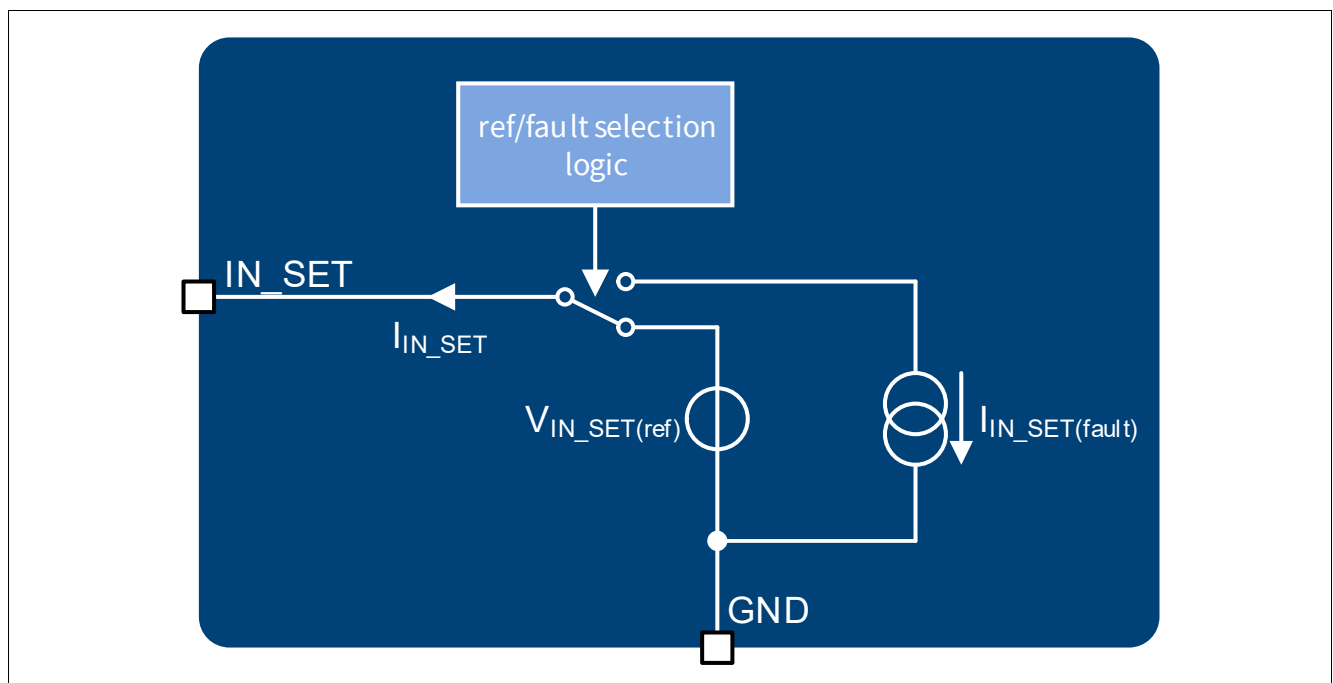


Figure 6 IN\_SET pin block diagram

### 5.2.2 Output current adjustment via $R_{SET}$

The output current for the channel can be defined connecting a low power resistor ( $R_{SET}$ ) between the IN\_SET pin and GND. The dimensioning of the resistor can be done using the formula:

$$I_{OUT} = k \cdot I_{IN\_SET} = k \cdot V_{IN\_SET(ref)} / R_{SET} \quad (5.1)$$

The gain factor  $k$  (defined as the ratio  $I_{OUT}/I_{IN\_SET}$ ) is graphically described in [Figure 7](#).

The current through the  $R_{SET}$  is defined by the resistor itself and the reference voltage  $V_{IN\_SET(ref)}$ , which is applied to the IN\_SET pin when the device is supplied and the channel enabled.

Power stage

### 5.2.3 Output control via IN\_SET

The IN\_SET pin can be connected via  $R_{SET}$  to the open-drain output of a microcontroller or to an external NMOS transistor as described in [Figure 9](#). This signal can be used to turn off the relative output stages of the IC.

A minimum IN\_SET current of  $I_{IN\_SET(Act)}$  is required to turn on the output stages. This feature is implemented to prevent glowing of LEDs caused by leakage currents on the IN\_SET pin, see again [Figure 7](#) for details.

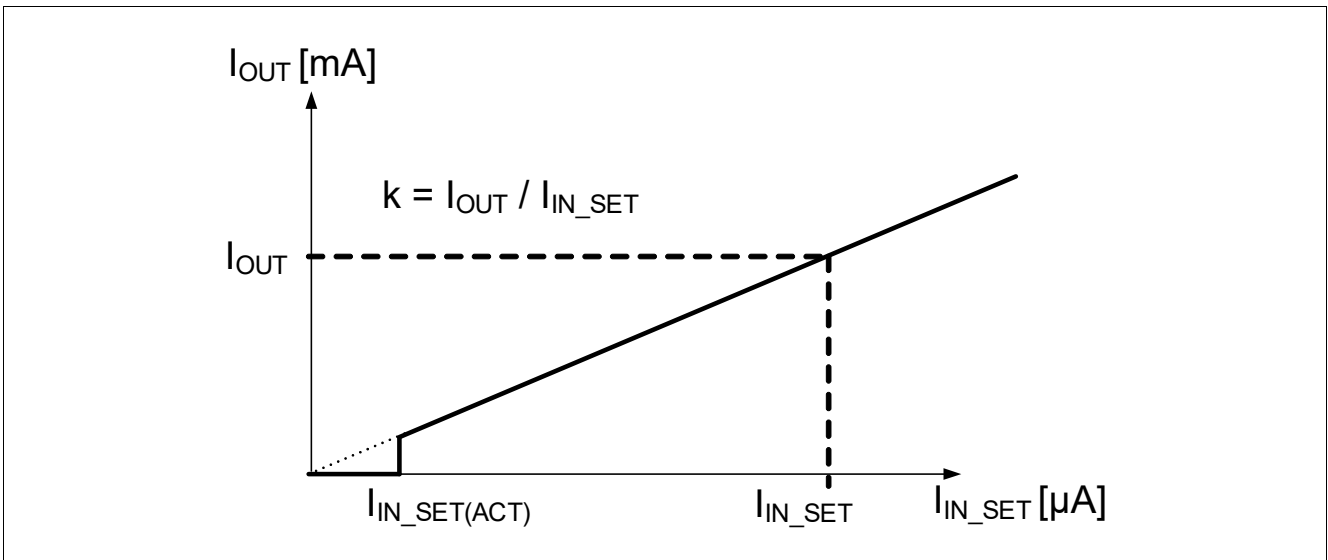


Figure 7  $I_{OUT}$  vs  $I_{IN\_SET}$

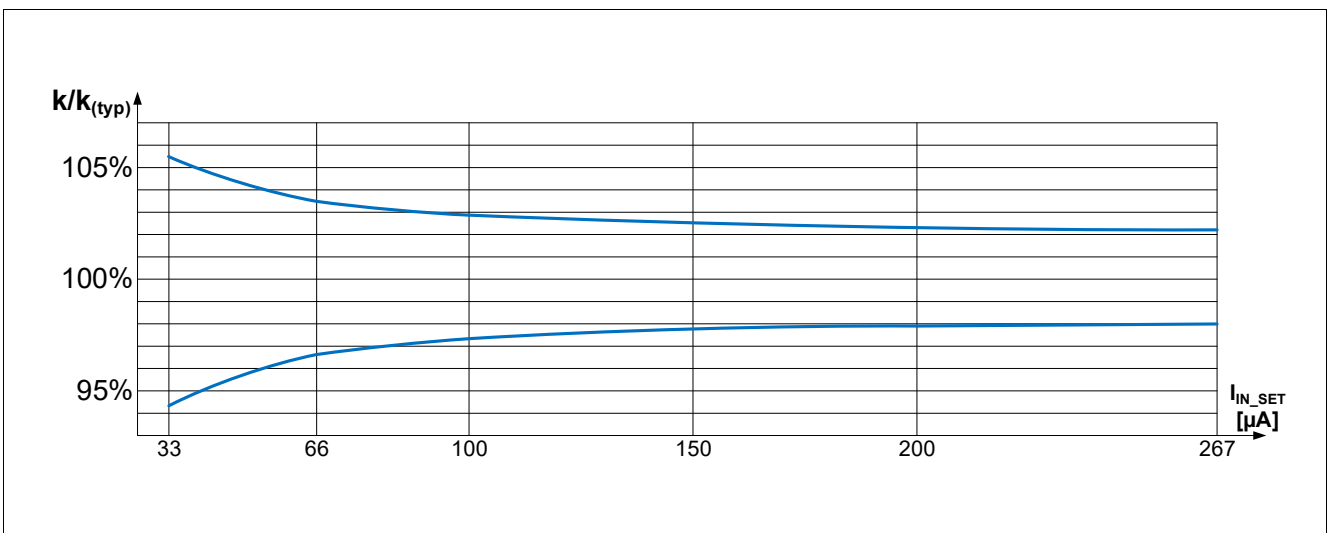


Figure 8 Typical output current accuracy  $I_{OUT} / I_{IN\_SET}$  at  $T_J = 25^\circ C$



Power stage

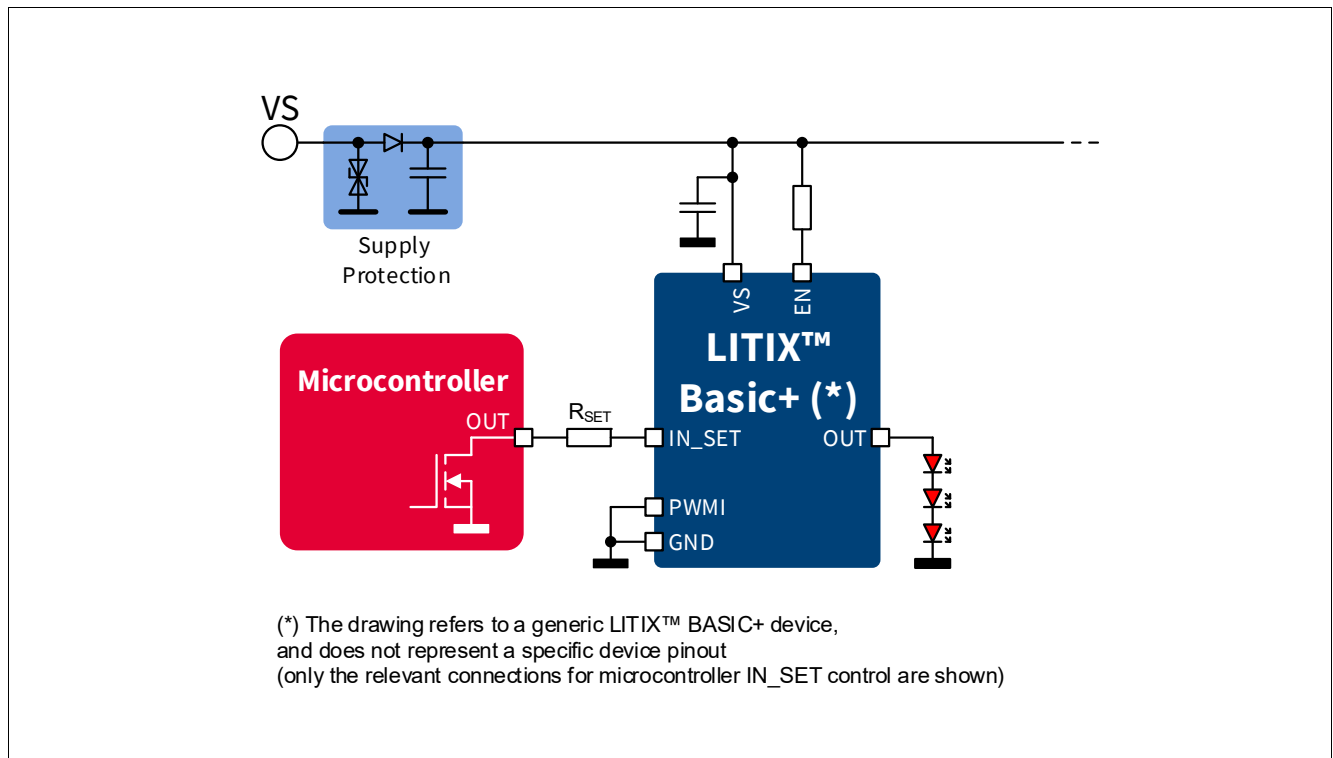


Figure 9 Output control via IN\_SET pin and open-drain microcontroller out (simplified diagram)

### 5.2.4 IN\_SET pin behavior during device fault management

If a fault condition arises on the channel controlled by the IN\_SET pin, once the D-pin reaches the high level threshold  $V_{D(th)}$ , the current of the IN\_SET pin is reduced to  $I_{IN\_SET(fault)}$ , in order to minimise the current consumption of the whole device under fault condition (detailed description is in the load diagnosis section, [Chapter 6](#)).

### 5.2.5 OUT\_SET pin

The OUT\_SET pin, mirroring the IN\_SET current defined by the external resistor  $R_{SET}$ , can be used to define the IN\_SET current of an additional companion device.

If minimum IN\_SET activation current  $I_{IN\_SET(act)}$  is not reached or if the D-pin reaches the high level threshold  $V_{D(th)}$  the OUT\_SET current is reduced to  $I_{OUT\_SET(OFF)}$ . This allows to drive other devices via OUT\_SET, even when digital dimming is required, without external components (see application drawing example in [Chapter 7](#)).

Power stage

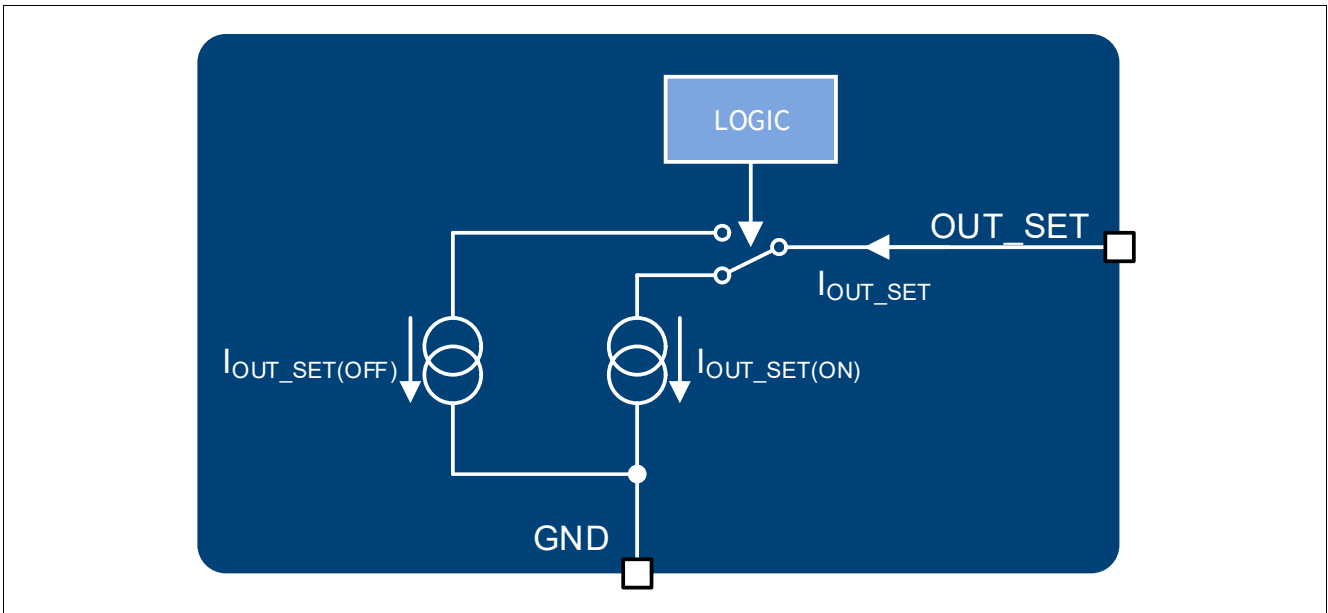


Figure 10 OUT\_SET pin block diagram

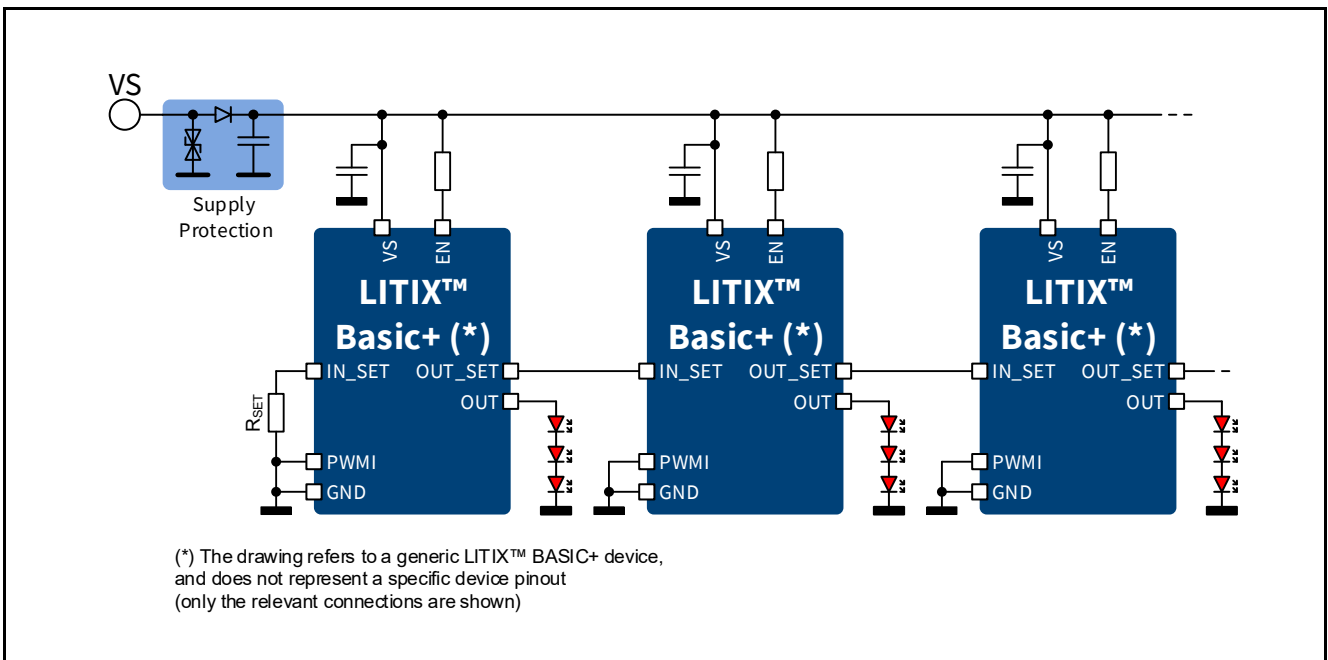


Figure 11 IN\_SET to OUT\_SET serial connection example

### 5.2.6 Direct control of PWMI

PWMI input can be controlled by the PWMO output of another device of LITIX™ Basic+ family or, alternatively, a push-pull output stage of a microcontroller: the host device decides the digital dimming characteristics by applying the proper control cycle in order to set the “on”/“off” timing, according to the chosen dimming function.

### 5.2.7 Timing diagrams

In the following diagrams (Figure 12, Figure 13, Figure 14) the influences of different driving inputs on output activation delays are shown.

Power stage

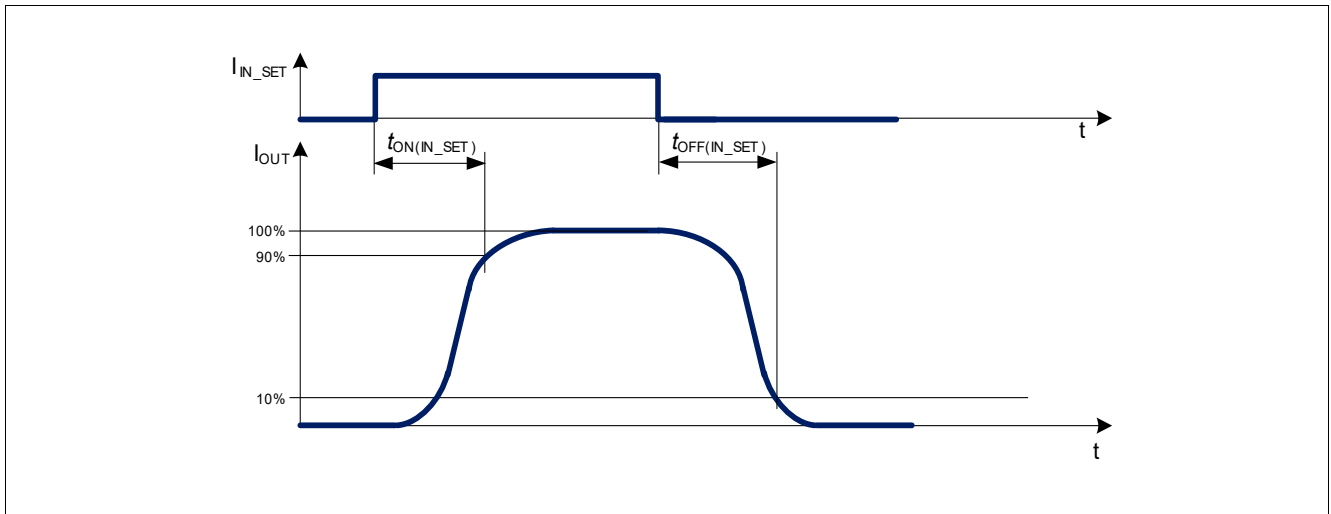


Figure 12 IN\_SET turn on and turn off delay timing diagram

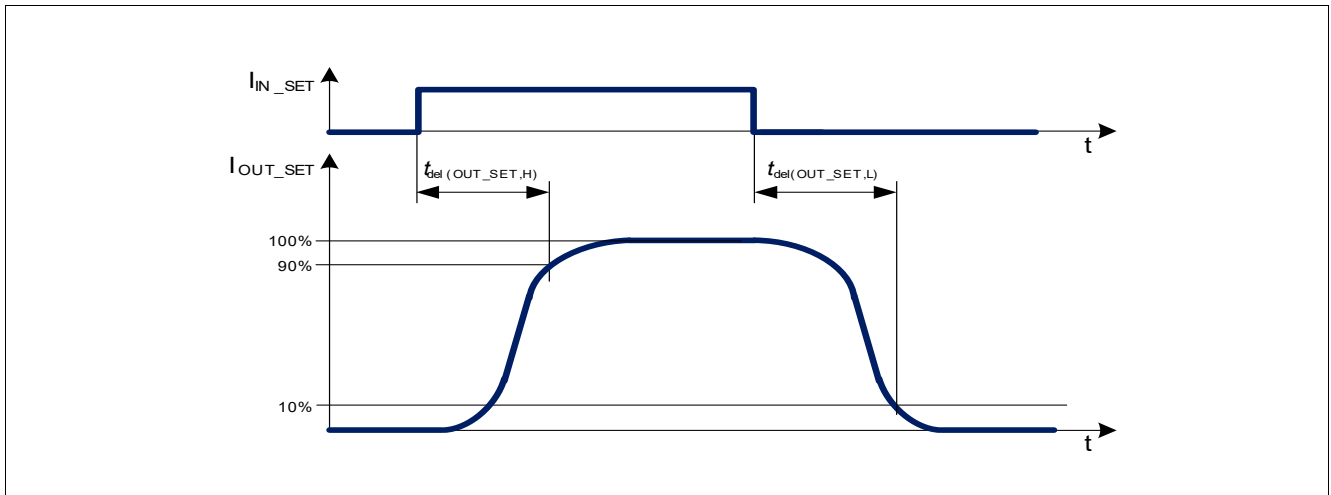


Figure 13 IN\_SET to OUT\_SET activation and deactivation delay timing diagram

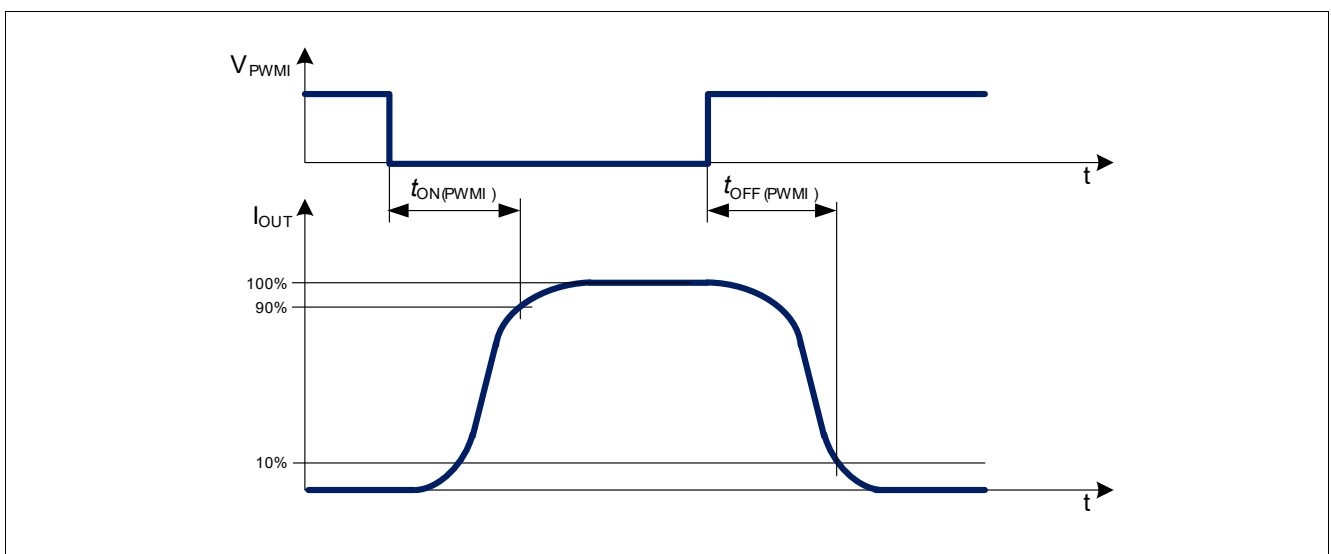


Figure 14 PWMI turn on and turn off timing diagram

Power stage

### 5.3 Electrical characteristics power stage

**Table 6 Electrical characteristics: Power stage**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current	$I_{OUT(Leak)}$	–	–	9	$\mu\text{A}$	<sup>1)</sup> $V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\ \mu\text{A}$ $V_{OUT} = 2.5\text{ V}$ $T_J = 85^\circ\text{C}$	P_6.5.51
Output leakage current	$I_{OUT(Leak)}$	–	–	21	$\mu\text{A}$	<sup>1)</sup> $V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\ \mu\text{A}$ $V_{OUT} = 2.5\text{ V}$ $T_J = 150^\circ\text{C}$	P_6.5.60
Reverse output current	$I_{OUT(rev)}$	–	–	3	$\mu\text{A}$	<sup>1)</sup> $V_{EN} = V_S$ $V_S = -18\text{ V}$ Output load: LED with break down voltage $< -0.6\text{ V}$	P_6.5.2

#### Output current accuracy

Output current accuracy	$K_{LT}$	837	900	963	–	<sup>1)</sup> $T_J = 25\dots 115^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS} = 2\text{ V}$ $I_{IN\_SET} = 33\ \mu\text{A}$	P_6.5.53
Output current accuracy	$K_{ALL}$	801	900	999	–	<sup>1)</sup> $T_J = -40\dots 115^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS} = 2\text{ V}$ $I_{IN\_SET} = 33\ \mu\text{A}$	P_6.5.54
Output current accuracy	$K_{LT}$	855	900	945	–	<sup>1)</sup> $T_J = 25\dots 115^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS} = 2\text{ V}$ $I_{IN\_SET} = 66\ \mu\text{A}$	P_6.5.55
Output current accuracy	$K_{ALL}$	837	900	963	–	<sup>1)</sup> $T_J = -40\dots 115^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS} = 2\text{ V}$ $I_{IN\_SET} = 66\ \mu\text{A}$	P_6.5.56
Output current accuracy	$K_{LT}$	864	900	936	–	<sup>1)</sup> $T_J = 25\dots 115^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS} = 2\text{ V}$ $I_{IN\_SET} = 200\ \mu\text{A}$	P_6.5.57
Output current accuracy	$K_{ALL}$	855	900	945	–	<sup>1)</sup> $T_J = -40\dots 115^\circ\text{C}$ $V_S = 8\dots 18\text{ V}$ $V_{PS} = 2\text{ V}$ $I_{IN\_SET} = 200\ \mu\text{A}$	P_6.5.58

**Power stage**

**Table 6 Electrical characteristics: Power stage (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	1.0	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{OUT} > 90\%$ of $K_{(typ)} * I_{IN\_SET}$	P_6.5.36
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.65	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{IN\_SET} = 133\ \mu\text{A}$ $I_{OUT} > 90\%$ of $K_{(typ)} * I_{IN\_SET}$ $T_J = -40^\circ\text{C}$	P_6.5.37
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.75	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{IN\_SET} = 133\ \mu\text{A}$ $I_{OUT} > 90\%$ of $K_{(typ)} * I_{IN\_SET}$ $T_J = 25^\circ\text{C}$	P_6.5.38
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.85	–	–	V	<sup>2)</sup> $V_S = 8\dots 18\text{ V}$ $I_{IN\_SET} = 133\ \mu\text{A}$ $I_{OUT} > 90\%$ of $K_{(typ)} * I_{IN\_SET}$ $T_J = 150^\circ\text{C}$	P_6.5.39
Required supply voltage for current control	$V_{S(CC)}$	5.5	–	–	V	$V_{EN} = 5.5\text{ V}$ $V_{OUT} = 3\text{ V}$ $R_{IN\_SET} = 6.8\text{ k}\Omega$ $I_{OUT} > 90\%$ of $K * I_{IN\_SET}$	P_6.5.40
Required output voltage for current control	$V_{OUT(CC)}$	1.4	–	–	V	$V_S = 8\dots 18\text{ V}$ $I_{OUT} > 90\%$ of $K * I_{IN\_SET}$	P_6.5.41
Current reduction temperature threshold	$T_{J(CRT)}$	–	140	–	$^\circ\text{C}$	<sup>1)</sup>	P_6.5.44
Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of $I_{OUT(typ)}$	–	–	mA	<sup>1)</sup> $T_J = 150^\circ\text{C}$	P_6.5.45

1) Not subjected to production test: specified by design

2) In these test conditions, the parameter  $K_{(typ)}$  represents the typical value of output current accuracy.

Power stage

## 5.4 Electrical characteristics IN\_SET, OUT\_SET and PWMI pins for output settings

**Table 7 Electrical characteristics: IN\_SET, OUT\_SET and PWMI pins**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.195	1.22	1.245	V	<sup>1)</sup> $V_{EN} = 5.5\text{ V}$ $T_J = 25^\circ\text{C}$	P_6.6.1
IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.184	1.22	1.256	V	<sup>1)</sup> $V_{EN} = 5.5\text{ V}$ $T_J = -40\dots 115^\circ\text{C}$	P_6.6.17
IN_SET output activation current	$I_{IN\_SET(ACT)}$	-	-	15	$\mu\text{A}$	$V_{EN} = 5.5\text{ V}$ $V_{PS} = 3\text{ V}$ $I_{OUT} > 50\%$ of $K_{(typ)} * I_{IN\_SET}$	P_6.6.2
OUT_SET output current matching	$\Delta I_{OUT\_SET(ON)}/I_{IN\_SET}$	-4	-	4	%	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{OUT\_SET} = 1.2\text{ V}$ $I_{IN\_SET} = 267\text{ }\mu\text{A}$	P_6.6.3
PWMI low threshold	$V_{PWMI(L)}$	1.5	1.7	2	V	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{EN} = 5.5\text{ V}$	P_6.6.6
PWMI high threshold	$V_{PWMI(H)}$	2.5	2.7	3	V	$V_S = 8\text{ V}$ to $18\text{ V}$ $V_{EN} = 5.5\text{ V}$	P_6.6.7

### Timing

IN_SET turn on time	$t_{ON(IN\_SET)}$	-	-	20	$\mu\text{s}$	<sup>1)2)</sup> $V_S = 13.5\text{ V}$ $V_{PS} = 4\text{ V}$ $I_{IN\_SET}$ rising from 0 to $180\text{ }\mu\text{A}$ $I_{OUT} = 90\%$ of $K * I_{IN\_SET}$	P_6.6.8
IN_SET turn off time	$t_{OFF(IN\_SET)}$	-	-	10	$\mu\text{s}$	<sup>1)2)</sup> $V_S = 13.5\text{ V}$ $V_{PS} = 4\text{ V}$ $I_{IN\_SET}$ falling from $180$ to $0\text{ }\mu\text{A}$ $I_{OUT} = 10\%$ of $K * I_{IN\_SET}$	P_6.6.9
OUT_SET activation time	$t_{del(OUT\_SET,H)}$	-	-	5	$\mu\text{s}$	<sup>1)3)</sup> $V_S = 13.5\text{ V}$ $I_{IN\_SET}$ rising from 0 to $180\text{ }\mu\text{A}$ $I_{OUT\_SET} = 90\%$ of $I_{IN\_SET}$	P_6.6.10
OUT_SET deactivation time	$t_{del(OUT\_SET,L)}$	-	-	5	$\mu\text{s}$	<sup>1)3)</sup> $V_S = 13.5\text{ V}$ $I_{IN\_SET}$ falling from $180$ to $0\text{ }\mu\text{A}$ $I_{OUT\_SET} = 10\%$ of $I_{IN\_SET}$	P_6.6.11

Power stage

**Table 7 Electrical characteristics: IN\_SET, OUT\_SET and PWMI pins (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI turn on time	$t_{ON(PWMI)}$	–	–	15	$\mu\text{s}$	<sup>1)4)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{PWMI}$ falling from $5\text{ V}$ to $0\text{ V}$ $I_{OUT} = 90\%$ of $K \cdot I_{IN\_SET}$ $T_J = -40 \dots 115^\circ\text{C}$	P_6.6.12
PWMI turn off time	$t_{OFF(PWMI)}$	–	–	10	$\mu\text{s}$	<sup>1)4)</sup> $V_S = 8\text{ V}$ to $18\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{PWMI} = 0$ rising from $0\text{ V}$ to $5\text{ V}$ $I_{OUT} = 10\%$ of $K \cdot I_{IN\_SET}$ $T_J = -40 \dots 115^\circ\text{C}$	P_6.6.13

- 1) Not subjected to production test: specified by design
- 2) Refer to [Figure 12](#)
- 3) Refer to [Figure 13](#)
- 4) Refer to [Figure 14](#)

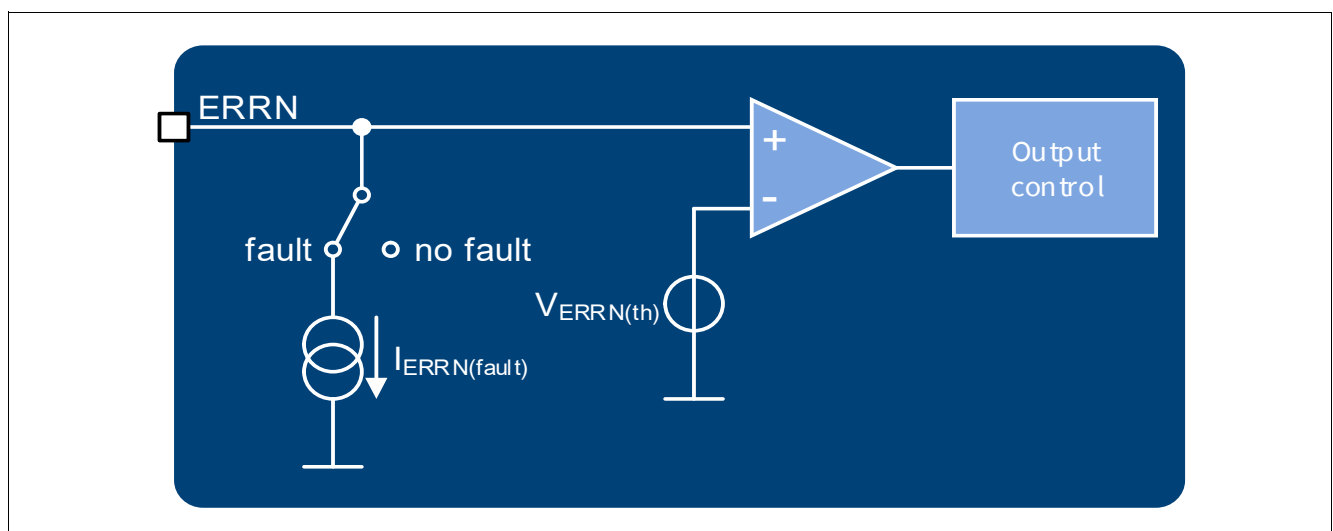
## 6 Load diagnosis

### 6.1 Error management via ERRN and D-pins

Several diagnosis features are integrated in the TLD2132-1EP:

- Open load detection (OL).
- Short circuit OUT-GND (SC).
- Single LED Short detection (SLS).

#### 6.1.1 ERRN pin

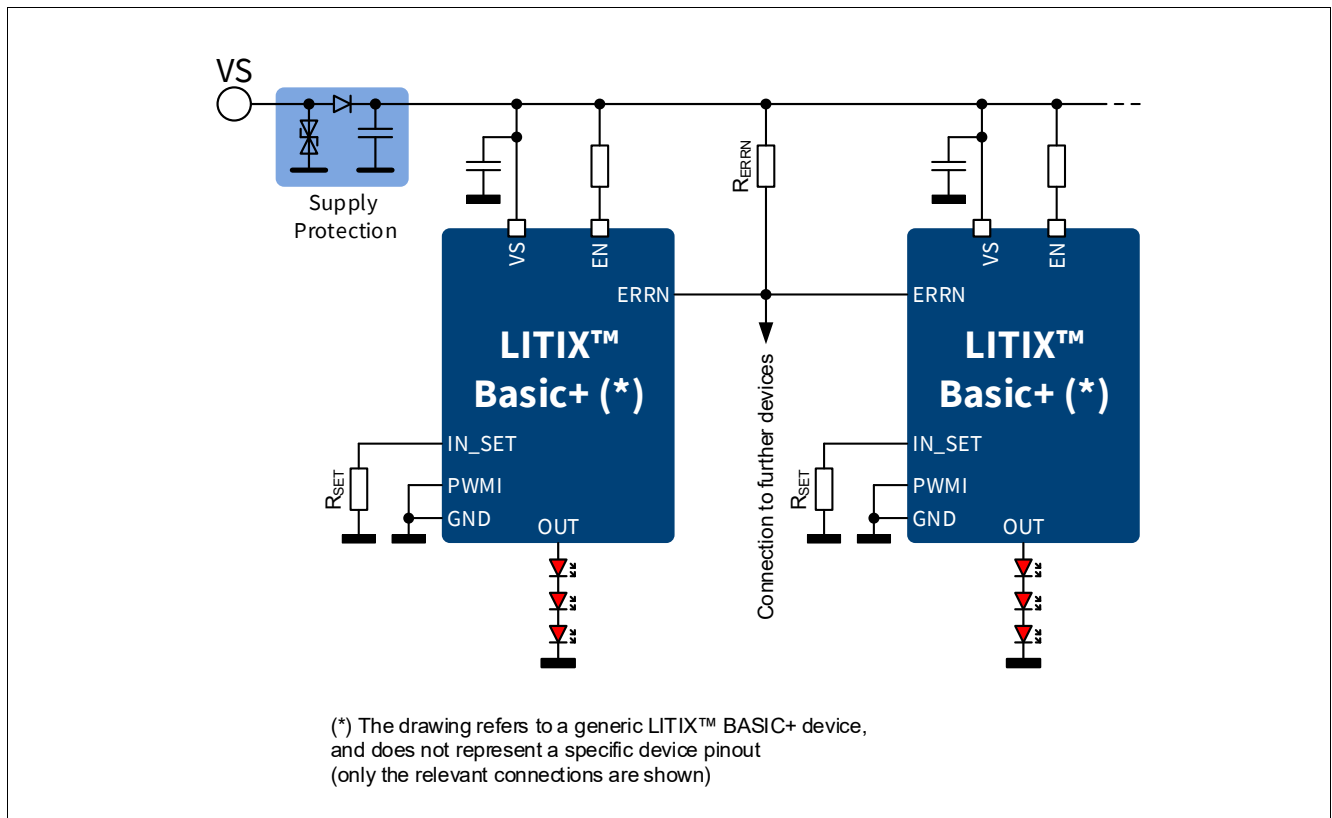


**Figure 15** ERRN pin (block diagram)

The device is able to report a detected failure in its driven load and react to a fault detected by another LED driver in the system if a shared error network is implemented (i. e. driving LED chains of the same light function). This is possible with the usage of an external pull-up resistor, allowing multiple devices to share the open drain diagnosis output pin ERRN. All devices sharing the common error network are capable to detect the fault from any of the channels driven by the LITIX™ Basic+ LED drivers and, if desired, to switch multiple loads off.



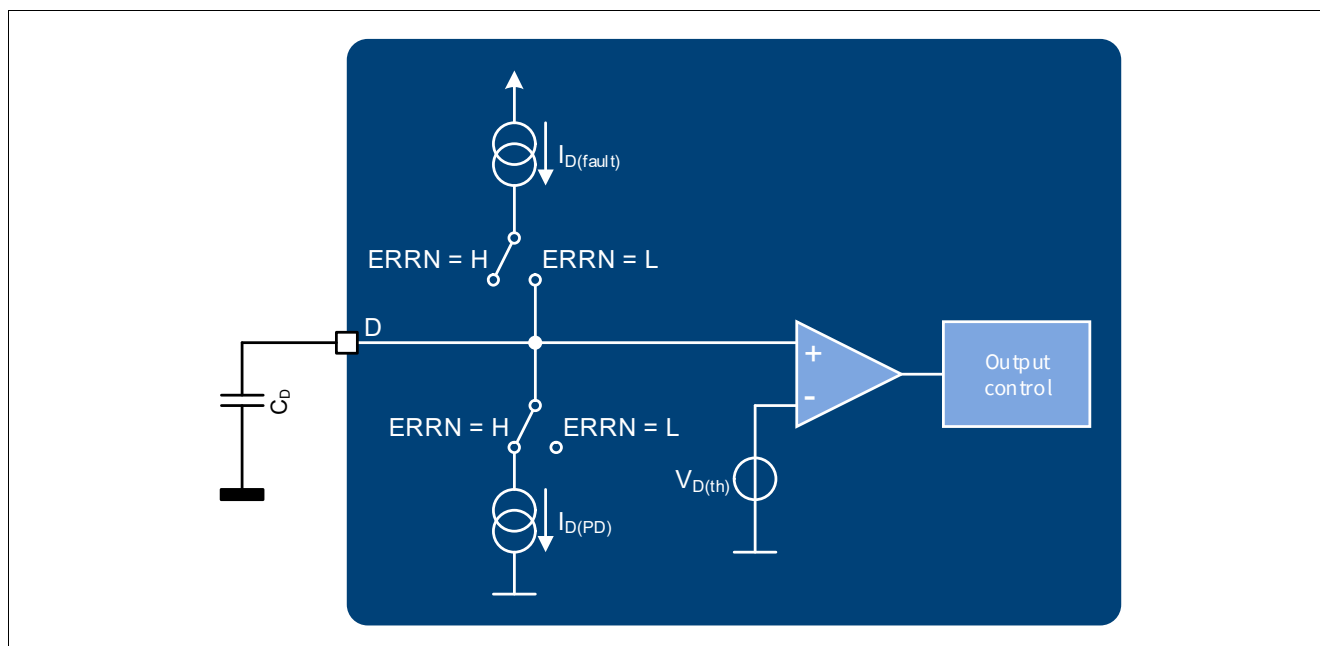
Load diagnosis



**Figure 16 Shared error network principle between LITIX™ Basic+ family devices**

When the channel is detected to be under fault conditions (for, at least, a filter time  $t_{\text{fault}}$ ), the open-drain ERRN pin sinks a pull-down current  $I_{\text{ERRN(fault)}}$  toward GND. Therefore an active low state can be detected at ERRN pin when  $V_{\text{ERRN}} < V_{\text{ERRN(fault)}}$  and if this condition is reached, provided the proper setup of the delay pin D, the channel is switched off. Similarly, when the fault is removed, ERRN pin is put back in high impedance state, and the channels reactivation procedure can be completed once D-pin voltage is below the value  $V_{\text{D(th)}}$ , as illustrated in the timing diagrams in this chapter.

### 6.1.2 D-pin



**Figure 17 D-pin (block diagram).**

The D-pin is designed for 2 main purposes:

- To react to error conditions in LED arrays according to the implemented fault management policy, in systems where multiple LED chains are used for a given light function.
- To extend the channel deactivation delay time of a value  $t_D$ , adding a small signal capacitor from the D-pin to GND. In this way, an unstable or noisy fault condition may be prevented from switching off all the channels of a given light function (i.e. driven by several driver ICs sharing the same error network).

The functionality of the D-pin is shown in the **Figure 17** simplified block diagram:

If one LED within one chain fails in open load condition or the device output is shorted to GND, the respective LED chain is off. Different automotive applications require a complete deactivation of a light function, if the desired brightness of the function (LED array) can not be achieved due to an internal error condition.

In normal operative status (no fault) a pull-down current  $I_{D(PD)}$  is sunk from the D-pin to GND. If there is a fault condition (for, at least, a filter time  $t_{fault}$ ) in one of the LED channels driven by the IC or in any of the devices sharing the same ERRN error network line, a pull-up current  $I_{D(fault)}$  is instead sourced from the D-pin. As a consequence, if a capacitive or open load is applied at this pin, its voltage starts rising.

When  $V_{D(th)}$  is reached at D-pin, all the channels driven by the device are switched off and if other devices share the same ERRN and D-pins nodes, all the devices turn their outputs off.

Alternatively, if the D-pin is tied to GND, only the channel that has been detected with a fault is safely deactivated.

The capacitor value used at the D-pin,  $C_D$ , sets the delay times  $t_{D(set/reset)}$  according to the following equations:

$$t_{D(set)} = \frac{C_D \cdot V_{D(th)}}{I_{D(fault)}} \quad (6.1)$$

$$t_{D(reset)} = \frac{C_D \cdot (V_{D(CL)} - V_{D(th)})}{I_{D(PD)}} \quad (6.2)$$

## Load diagnosis

*Note:* If the device detects a Single LED Short failure, the D-pin behavior and the overall fault management is slightly different (allows periodical retries with load reactivation, according to DS pin settings too), as described in [Chapter 6.3](#).

### 6.2 Open Load (OL) and short OUT to GND (SC)

The behavior of the device during overload conditions that lead to an excess of internal heating up to overtemperature condition, is already described in [Chapter 5](#).

Open load (OL) and OUT shorted to GND (SC) diagnosis features are also integrated in the TLD2132-1EP.

An open load condition is detected if the voltage drop over the output stage  $V_{PS}$  is below the threshold  $V_{PS(OL)}$  at least for a filter time  $t_{fault}$ .

A short to GND condition is detected if the voltage of the output stages  $V_{OUT}$  is below the threshold  $V_{OUT(SC)}$  at least for a filter time  $t_{fault}$ .

#### 6.2.1 Fault management (D-pin open or connected with a capacitor to GND)

With D-pin open or connected with a capacitor to GND configuration, it is possible to switch off all the channels which share a common error network, without the need of an auxiliary microcontroller. For more details refer also to the timing diagram of [Figure 18](#), [Figure 19](#).

If there is an OL or SC condition on the output, a pull-up current  $I_{OUT(fault)}$  then flows out from the channel, replacing the configured output current (but limited by the actual load impedance, e.g. reduced to zero with an ideal open load). Under these conditions, the ERRN pin starts sinking a current  $I_{ERRN(fault)}$  toward GND and (with proper dimensioning of the external pull-up resistor) reaches a voltage level below  $V_{ERRN(fault)}$ .

After  $t_{D(set)}$ , the voltage  $V_{D(th)}$  is reached at D-pin, the IN\_SET goes in a weak pull-down state with a current consumption  $I_{IN\_SET(fault)}$  after an additional latency time  $t_{IN\_SET(del)}$ . The ERRN low voltage can also be used as input signal for a microcontroller to perform the desired diagnosis policy.

The OL and SC error conditions are not latched: as soon as the fault condition is no longer present (at least for a filter time  $t_{fault}$ ) ERRN goes back to high impedance. When its voltage is above  $V_{ERRN(fault)}$ , the D-pin voltage starts decreasing and after  $t_{D(reset)}$  goes below  $(V_{D(th)} - V_{D(th,hys)})$ . Then the IN\_SET voltage goes up to  $V_{IN\_SET(ref)}$ , again after a time  $t_{IN\_SET(del)}$ : at this point, the output stage are activated again. The total time between the fault removal and the IN\_SET reactivation  $t_{ERR(reset)}$  is extended by an additional latency which depends on the external ERRN pin pull-up and filter circuitry.

Load diagnosis

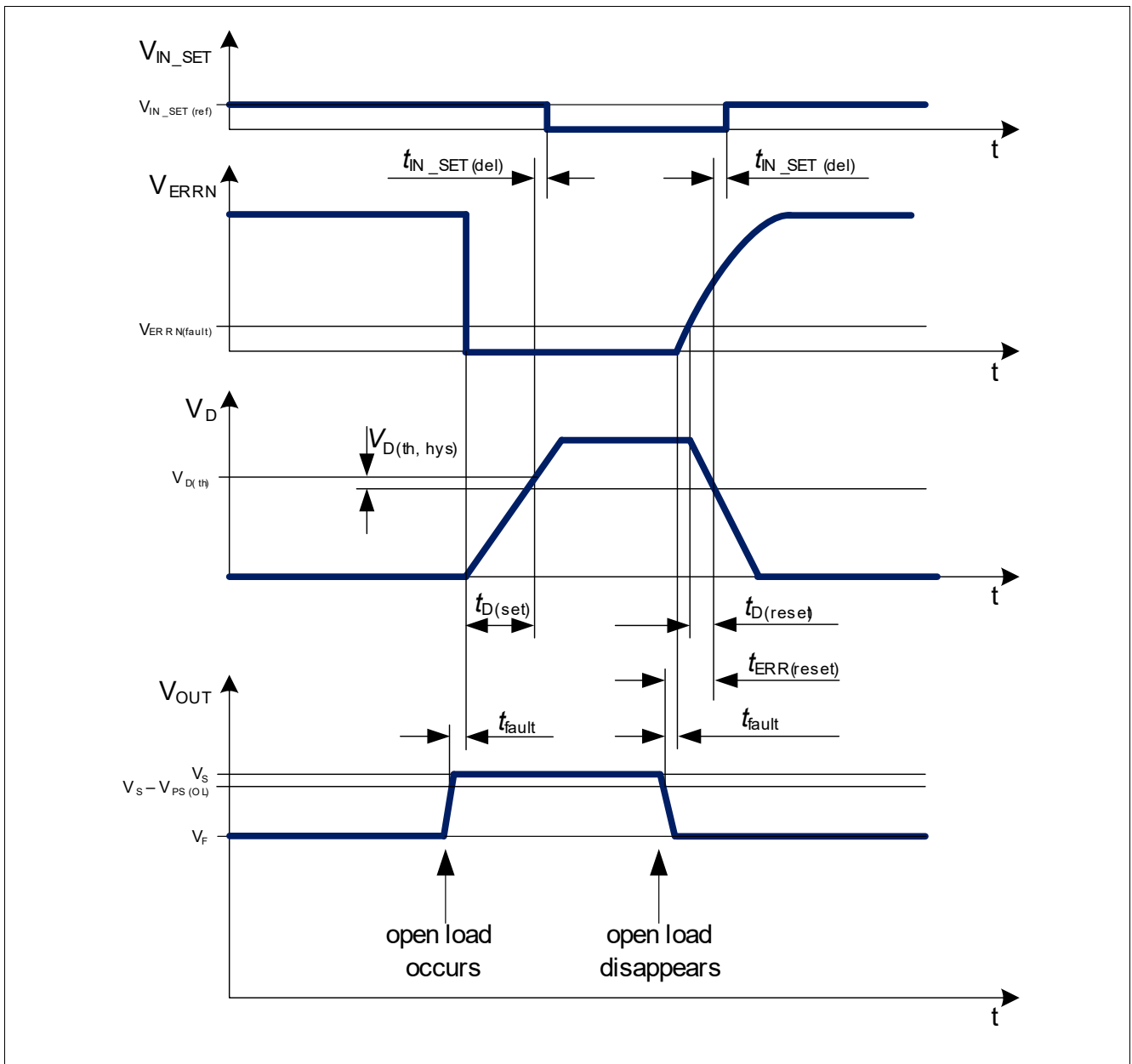
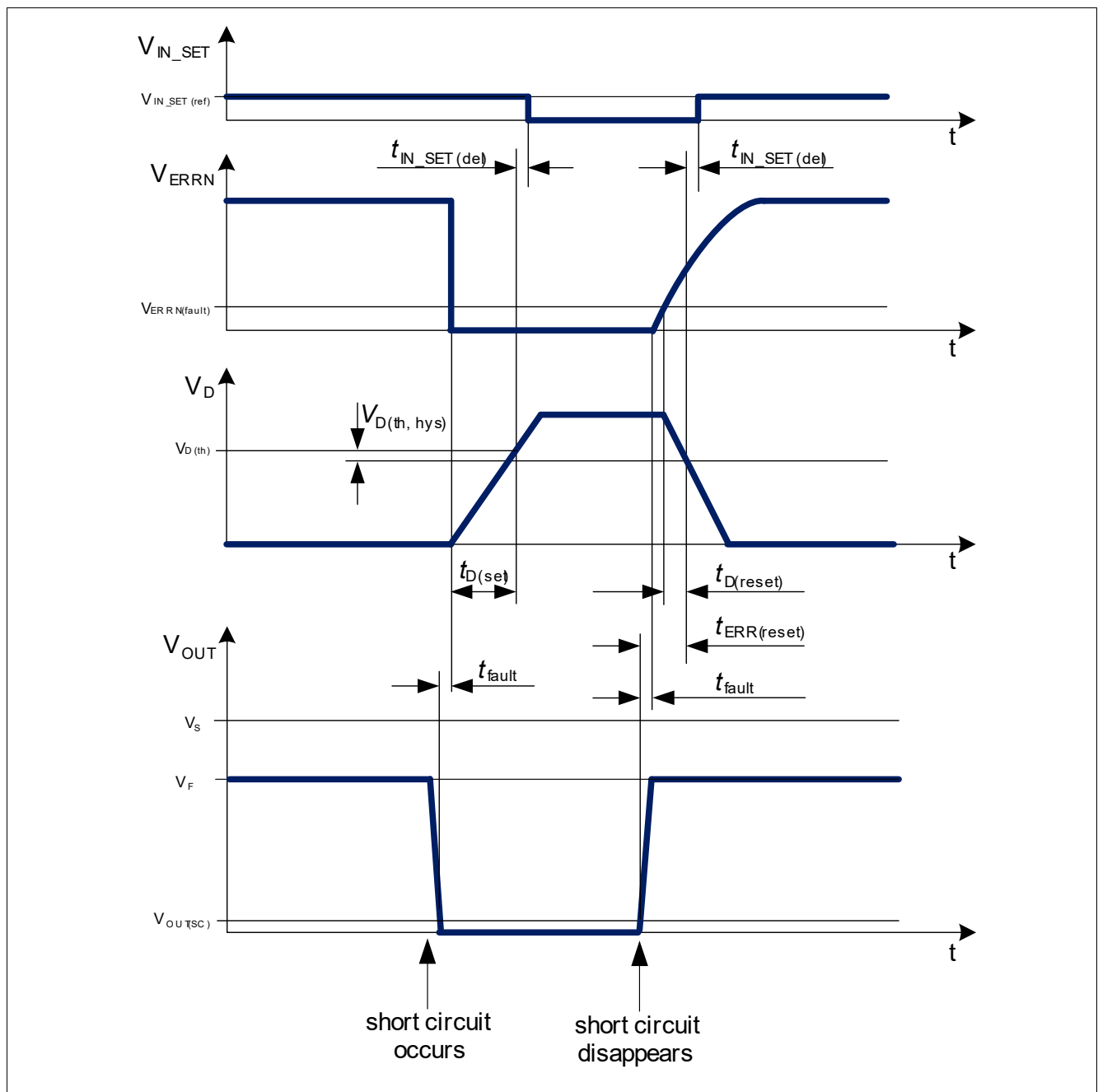


Figure 18 Open load condition timing diagram example (D-pin unconnected or connected to external capacitor to GND,  $V_F$  represents the typical forward voltage of the output load)

Load diagnosis



**Figure 19 Short circuit to GND condition timing diagram example (D-pin not connected or connected to external capacitor to GND,  $V_{Fxyz}$  represents the forward voltage of the output loads)**

**6.2.2 Fault management (D-pin connected to GND)**

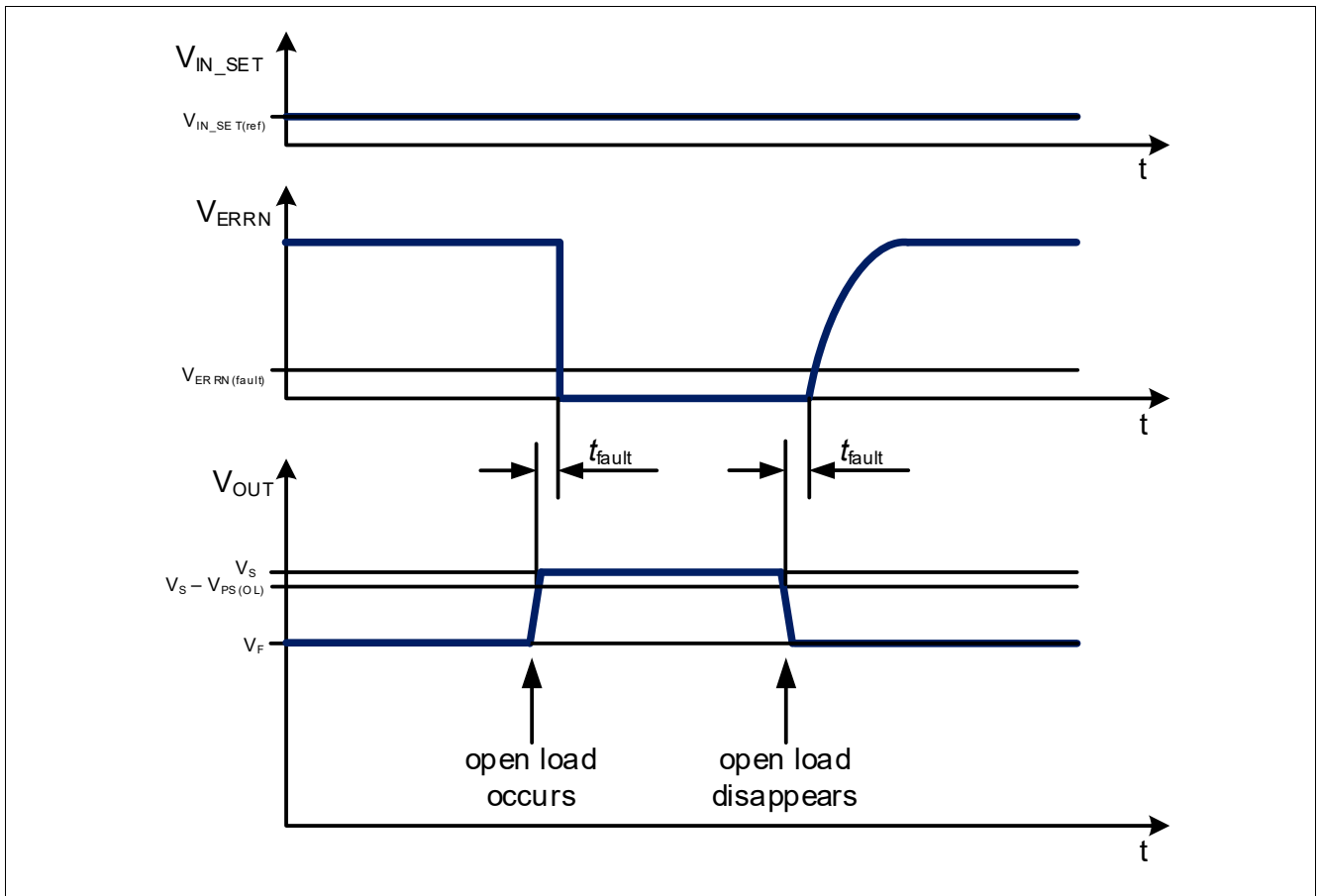
With D-pin connected to GND configuration, it is possible to deactivate only the channel under fault conditions, still sharing ERRN pin in a common error network with other devices of LITIX™ Basic+ family.

If there is fault condition on the output, a pull-up current  $I_{OUT(fault)}$  flows out from the channel, replacing the configured output current (but limited by the actual load impedance, e.g. reduced to zero with an ideal open load). Under fault conditions the ERRN pin starts sinking a current  $I_{ERRN(fault)}$  to ground and the voltage level on this pin will drop below  $V_{ERRN(fault)}$  if the external pull-up resistor is properly dimensioned. The ERRN low voltage can also be used as input signal for a  $\mu C$  to perform the desired diagnosis policy.

**Load diagnosis**

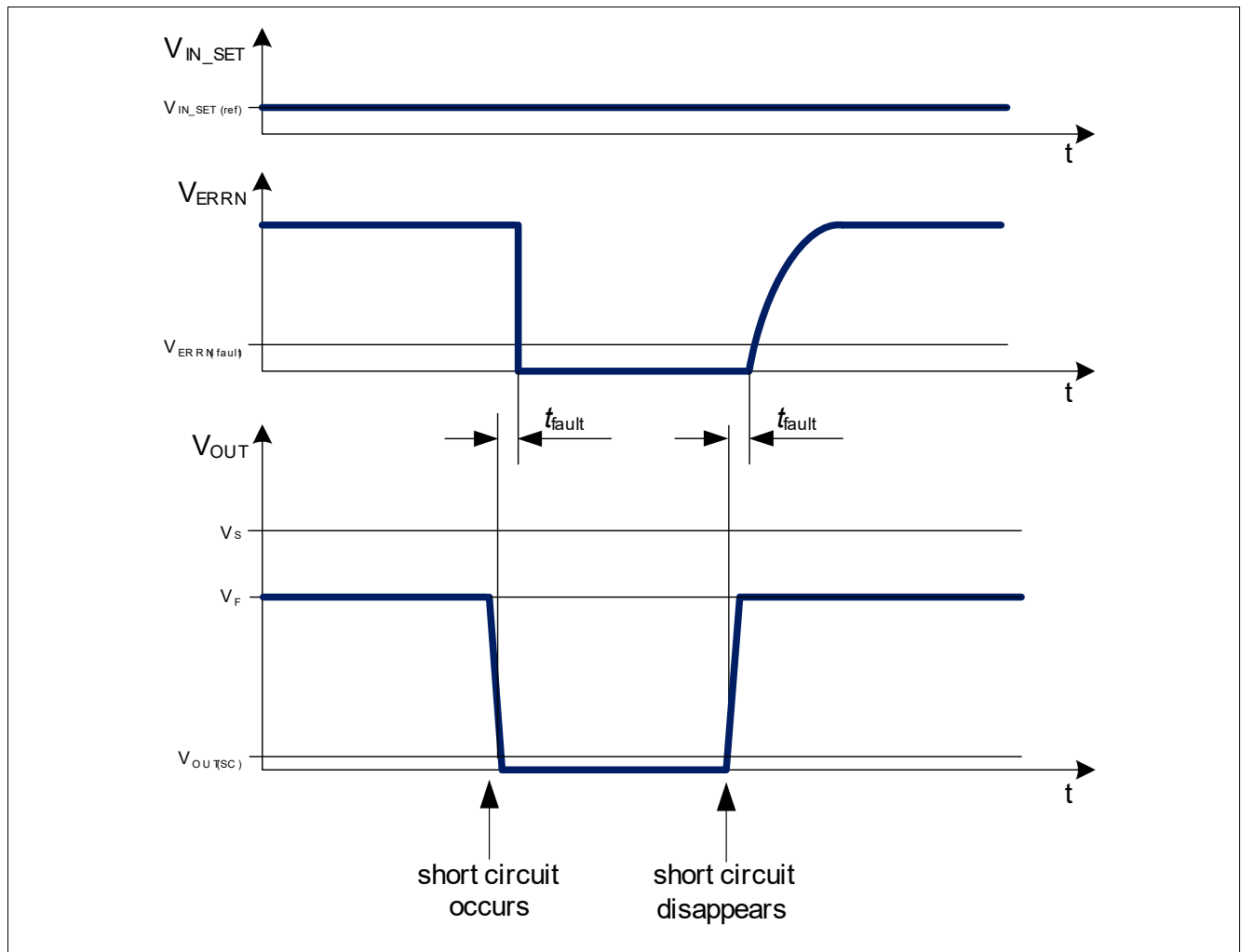
The fault status is not latched: as soon as the fault condition is no longer present (at least for a filter time  $t_{\text{fault}}$ ), ERRN goes back to high impedance and, once its voltage is above  $V_{\text{ERRN(fault)}}$ , finally the output stages are activated again.

Examples of open load or short to GND diagnosis with D-pin open or connected to GND are shown in the timing diagrams of **Figure 20** and **Figure 21**.



**Figure 20** Open load condition timing diagram example (D-pin connected to GND,  $V_{\text{F}}$  represents the forward voltage of the output load)

Load diagnosis

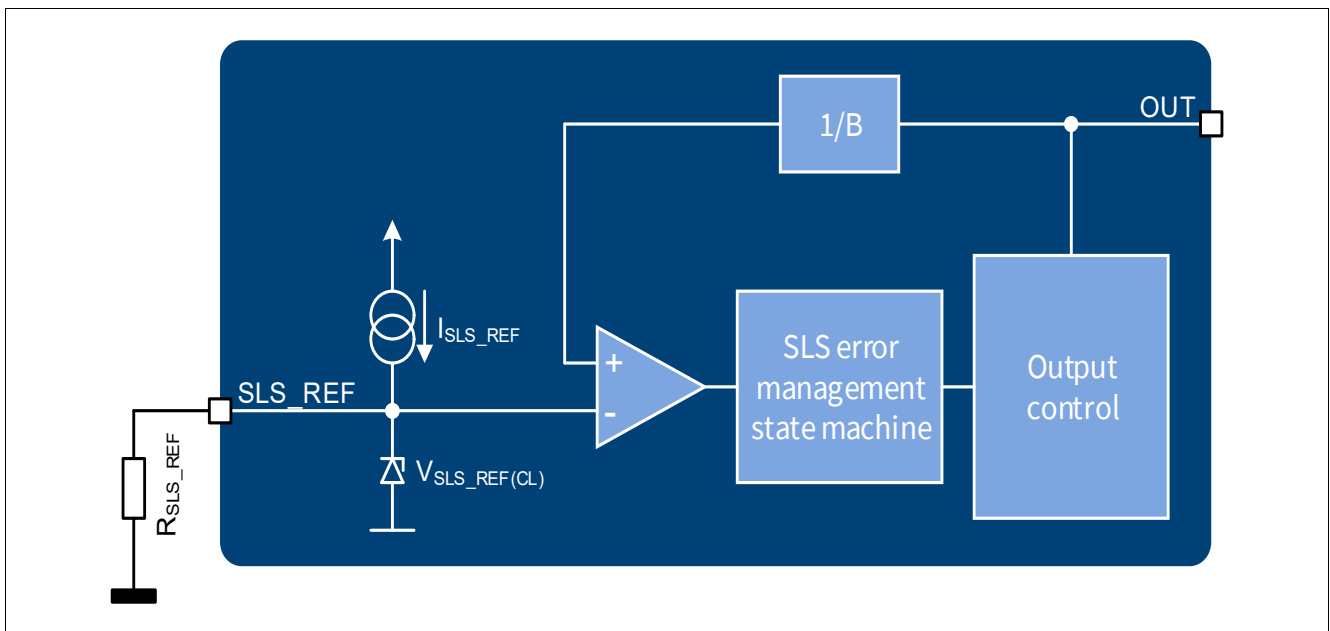


**Figure 21** Short circuit condition timing diagram example (D-pin connected to GND,  $V_F$  represents the forward voltage of the output load)

### 6.3 Single LED Short detection, SLS\_REF and DS pins

An output single LED short circuit (SLS) detection diagnosis feature is available. This allows an easy detection of loss of luminous flux in the light function due to this failure mode, which does not necessarily result in a condition similar or equivalent to an open load or short to GND condition. To make the SLS error management compliant with the majority of system requirements, the TLD2132-1EP allows the possibility to manage a low current consumption mode with a load reactivation and retry strategy (via D and DS pins connected to external capacitors), or with error detection via ERRN pin monitoring (with D-pin shorted to GND).

### 6.3.1 SLS\_REF pin



**Figure 22 SLS\_REF pin (block diagram) with resistor termination**

The SLS\_REF pin is designed to generate an accurate and tunable reference voltage to allow reliable detection of SLS failure.

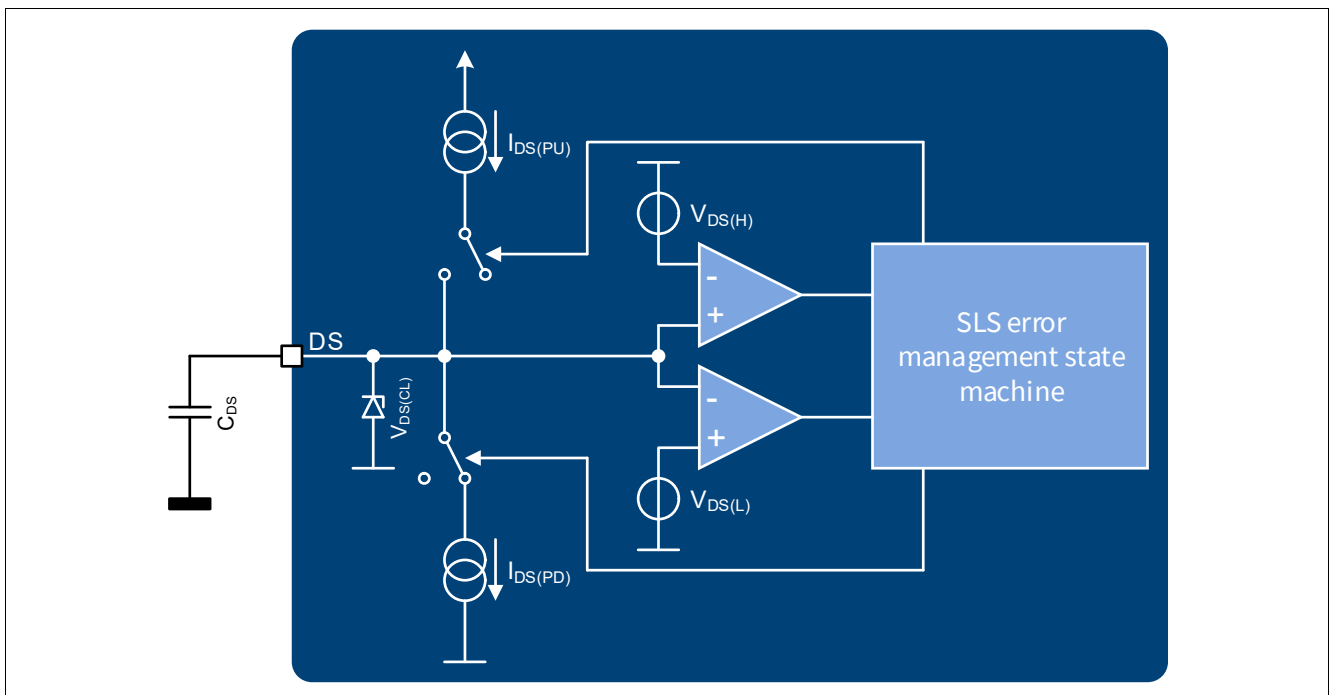
This reference can be programmed to adapt the SLS detection to the load related variables (as number of LED in series, load currents, LED forward voltages fluctuation and mismatches, etc.).

The pin provides an accurate reference current  $I_{SLS\_REF}$  (a replica of  $I_{IN\_SET}$ ) which can be used to generate the desired reference voltage with an external low cost precision resistor. The voltage  $V_{SLS\_REF}$  is then internally compared with a fraction of the OUT voltage: if the OUT voltage is below the minimum expected value, then the SLS error management starts (see [Chapter 6.3.3](#) for more detailed description and reference formulas).

[Figure 22](#) shows the basic block diagram of SLS\_REF pin.



### 6.3.2 DS pin



**Figure 23 DS pin (block diagram)**

The DS pin is used to implement a timer function which allows load reactivation retries during SLS failure. By default, when no SLS fault is detected, a pull-down current  $I_{DS(PD)}$  is sunk from the DS pin to GND. If a SLS fault condition is verified, a capacitor on DS pin allows fault management with minimal current consumption of the device for a time which depends on the capacitive load applied, according to the detailed description of [Chapter 6.3.4](#).

### 6.3.3 SLS fault detection

A single LED anode-cathode short circuit condition is detected if the OUT voltage is below a fixed multiple  $B_{SLS}$  of the voltage at SLS\_REF pin, according to [Equation \(6.3\)](#). The voltage  $V_{SLS\_REF}$  can be adjusted applying a resistor from SLS\_REF to GND, according to [Equation \(6.4\)](#) and the parameter  $K_{SLS\_REF}$  (P\_7.5.13).

$$V_{OUT} \leq B_{SLS} \cdot V_{SLS\_REF} \quad (6.3)$$

$$V_{SLS\_REF} = I_{SLS\_REF} \cdot R_{SLS\_REF} \quad (6.4)$$

### 6.3.4 SLS fault management: D and DS pins open or connected with capacitors to GND (low power consumption mode with retry strategy)

Under this pin configuration, as described in the title of this chapter, if there is an SLS condition the output is turned off when the voltage level  $V_{D(th)}$  is reached at D-pin.

Under fault condition the ERRN pin starts sinking a current  $I_{ERRN(fault)}$  to ground and the voltage level on this pin will drop below  $V_{ERRN(fault)}$  if the external pull-up resistor is properly dimensioned. After  $t_{D(set)}$ , the voltage  $V_{D(th)}$  is reached at D-pin and the IN\_SET pin goes into a weak pull-down state with a current consumption  $I_{IN\_SET(fault)}$ , after an additional latency time  $t_{IN\_SET(del)}$ .

**Load diagnosis**

Then (differently from the management of OL and SC detection) the voltage at DS pin also starts rising with a pull-up current  $I_{DS(PU)}$ , until it reaches the threshold  $V_{DS(H)}$ , when it starts discharging with the current  $I_{DS(PD)}$ . Now the DS voltage can cross the lower voltage threshold  $V_{DS(L)}$ : at this time a full wait time cycle  $t_{SL\_WAIT}$  is completed and the device performs a load reactivation retry, turning the output current back on. If the SLS fault condition persists, a new  $t_{SL\_WAIT}$  cycle is started. If at the end of one wait cycle the fault is not detected anymore, the device goes back to normal operation. The dimensioning of typical  $t_{SL\_WAIT}$  is ruled by the following equations.

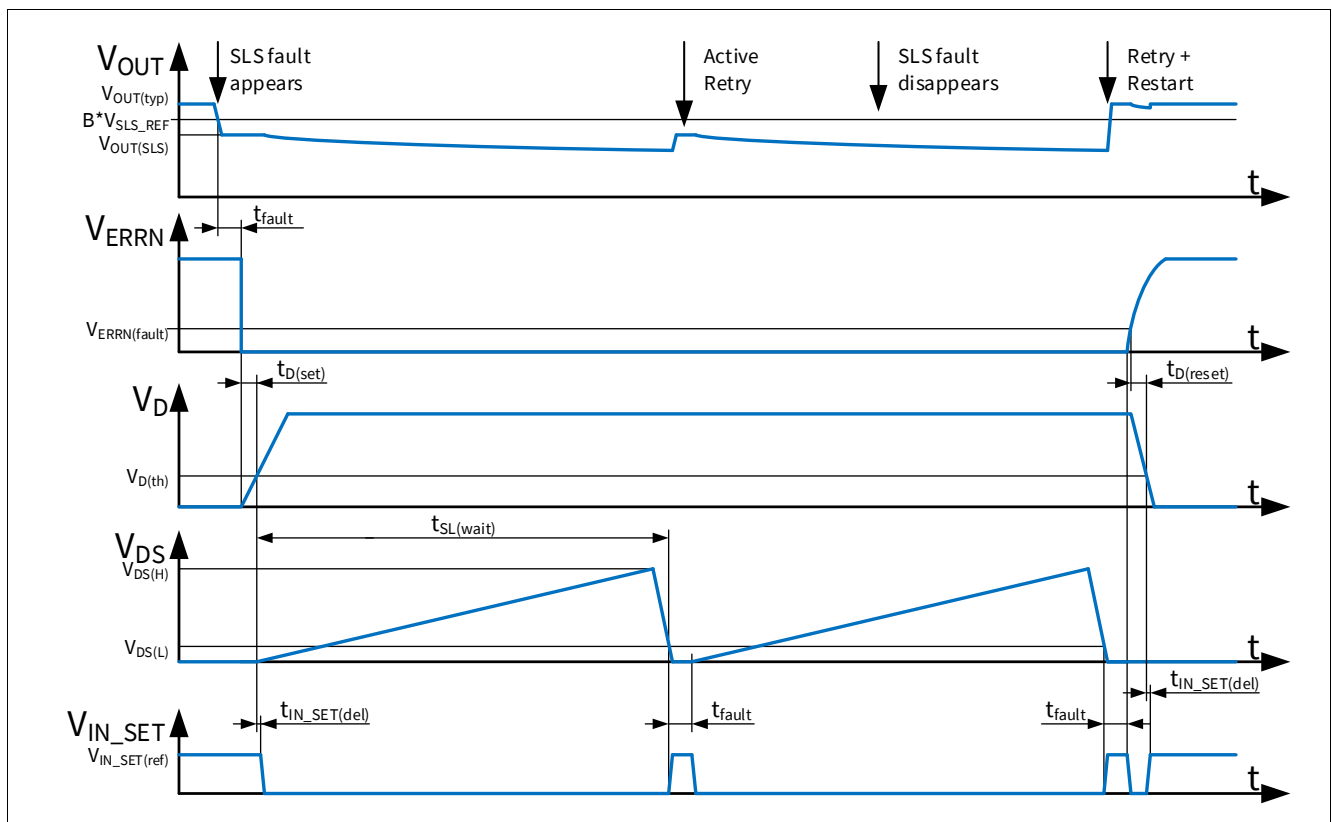
$$t_{DS(rise)} = \frac{C_{DS} \cdot V_{DS(H)}}{I_{DS(PU)}} \tag{6.5}$$

$$t_{DS(fall)} = \frac{C_{DS} \cdot (V_{DS(H)} - V_{DS(L)})}{I_{DS(PD)}} \approx \frac{C_{DS} \cdot V_{DS(H)}}{I_{DS(PD)}} \tag{6.6}$$

$$t_{SL(wait)} = t_{DS(rise)} + t_{DS(fall)} + t_{IN\_SET(del)} \approx t_{DS(rise)} \tag{6.7}$$

A graphical description is shown in the timing diagram example of **Figure 24**.

With this error management algorithm, it is possible to detect the SLS fault monitoring the device consumption from the VS line, which remains as low as  $I_{S(fault)}$  during the whole wait cycle.



**Figure 24 Single LED short condition timing diagram example (D pin not connected or connected to external capacitor to GND) output load)**

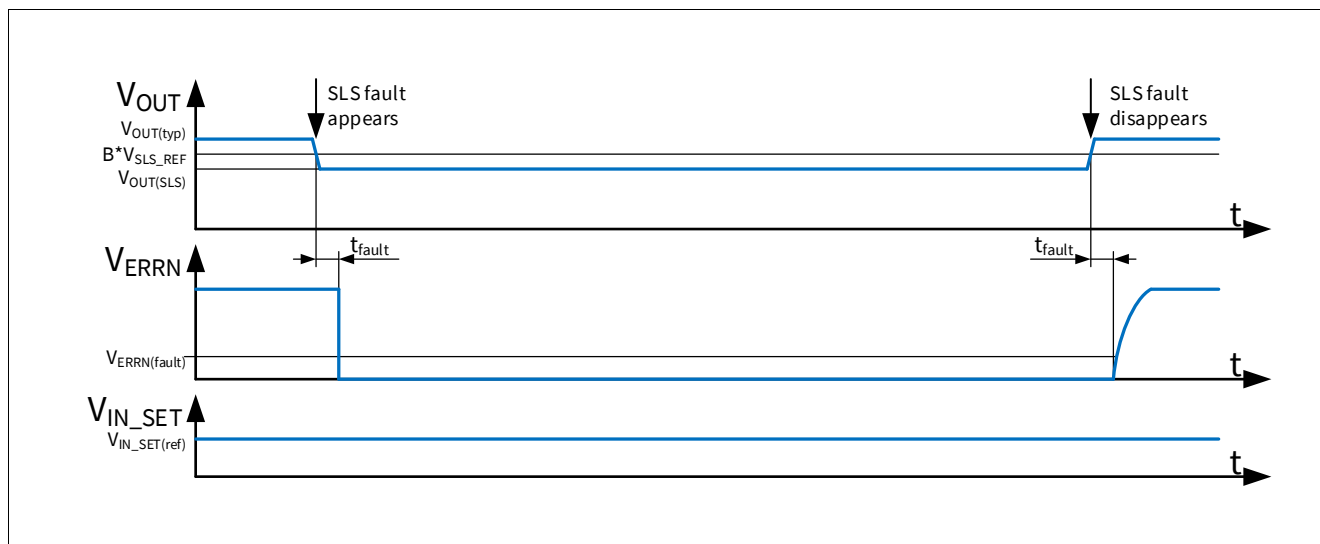
**6.3.5 SLS fault management: D-pin shorted to GND**

Under D-pin shorted to GND configuration, the output affected by a single LED short fault is not turned off, different from an open load or short circuit to GND fault condition. The potential on the IN\_SET pin remains

## Load diagnosis

$V_{IN\_SET(ref)}$ , the ERRN pin starts sinking a current  $I_{ERRN(fault)}$  toward GND. Again, the resulting ERRN low voltage can be used as input signal for a microcontroller to perform the desired diagnosis policy. Also the SLS status is not latched: as soon as the fault condition is no longer present (at least for a filter time  $t_{fault}$ ) ERRN goes back to high impedance.

An examples of this SLS diagnosis condition is shown in the timing diagrams of **Figure 25**.



**Figure 25** Single LED short condition timing diagram example (D pin shorted to GND)

## 6.4 Electrical characteristics: Load diagnosis and Overload management

**Table 8** Electrical Characteristics: Fault management

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET fault current	$I_{IN\_SET(fault)}$	–	–	10	$\mu\text{A}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{OUT} = 3.6\text{ V}$ $V_{ERRN} = 0\text{ V}$ $V_{IN\_SET} = 1\text{ V}$ D open $V_{EN} > V_{DEN(th,max)}$	P_7.5.1
ERRN fault current	$I_{ERRN(fault)}$	2	–	–	mA	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{ERRN} = 0.8\text{ V}$ Fault condition $V_{EN} > V_{DEN(th,max)}$	P_7.5.2
ERRN input threshold	$V_{ERRN(th)}$	0.8	–	2.0	V	<sup>1)</sup> $V_S > 8\text{ V}$	P_7.5.3
OL detection threshold	$V_{PS(OL)}$	0.2	–	0.4	V	$V_S > 8\text{ V}$ $V_{EN} > V_{DEN(th,max)}$	P_7.5.5
SC detection threshold	$V_{OUT(SC)}$	0.8	–	1.35	V	$V_S > 8\text{ V}$ $V_{EN} > V_{DEN(th,max)}$	P_7.5.6

**Load diagnosis**

**Table 8 Electrical Characteristics: Fault management (cont'd)**

$T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{IN\_SET} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fault detection current	$I_{OUT(fault)}$	50	–	180	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{OUT} = 0\text{ V}$ $V_{EN} > V_{DEN(th, max)}$	P_7.5.7

**D-pin**

Threshold voltage for function de-activation	$V_{D(th)}$	1.4	1.7	2	V	$V_S > 8\text{ V}$ $V_{EN} = 5.5\text{ V}$	P_7.5.8
Threshold hysteresis	$V_{D(hys)}$	–	100	–	mV	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{OUT} = V_{OUT(OL)}$	P_7.5.9
Fault pull-up current	$I_{D(fault)}$	20	35	50	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{OUT} = V_{OUT(OL)}$ $V_D = 2\text{ V}$	P_7.5.10
Pull-down current	$I_{D(PD)}$	40	60	95	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_D = 1.4\text{ V}$ $V_{ERRN} = 2\text{ V}$ $V_{PS} = 3\text{ V}$ No fault conditions	P_7.5.11
Internal clamp voltage	$V_{D(CL)}$	4	–	6	V	$V_S > 8\text{ V}$ $V_{OUT} = V_{OUT(OL)}$ D-pin open	P_7.5.12

**SLS\_REF pin**

Relative pull-up current, related to IN_SET $I_{SLS\_REF} / I_{INSET}$	$K_{SLS\_REF}$	0.972	1	1.028	–	$V_S > 8\text{ V}$ $V_{SLS\_REF} = 0.75 \dots 3.25\text{ V}$ $I_{IN\_SET} = 50 \dots 270\ \mu\text{A}$	P_7.5.13
Output attenuation factor for internal reference comparison	$B_{SLS}$	3.77	3.93	4.09	–	$V_S > 14.65\text{ V}$ $V_{OUT} = 13\text{ V}$	P_7.5.21
Output attenuation factor for internal reference comparison	$B_{SLS}$	3.76	3.93	4.10	–	$V_S > 8\text{ V}$ $V_{OUT} = 7\text{ V}$	P_7.5.22
Output attenuation factor for internal reference comparison	$B_{SLS}$	3.75	3.93	4.11	–	$V_S > 8\text{ V}$ $V_{OUT} = 5\text{ V}$	P_7.5.23
Output attenuation factor for internal reference comparison	$B_{SLS}$	3.73	3.93	4.13	–	$V_S > 8\text{ V}$ $V_{OUT} = 3\text{ V}$	P_7.5.24

**Load diagnosis**

**Table 8 Electrical Characteristics: Fault management (cont'd)**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ;  $V_S = 5.5\text{ V}$  to  $18\text{ V}$ ;  $R_{\text{IN\_SET}} = 10\text{ k}\Omega$ ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SLS saturation voltage threshold	$V_{\text{SLS\_REF(CL)}}$	3.5	–	6	V	$V_S > 8\text{ V}$ $V_{\text{EN}} = 5.5\text{ V}$ $V_{\text{PWMI}} = 0\text{ V}$ SLS_REF open	P_7.5.14

**DS pin**

High threshold voltage (to trigger from pull up to pull-down current)	$V_{\text{DS(H)}}$	2.3	2.5	2.7	V	$V_S > 8\text{ V}$ $V_{\text{SLS\_REF}} = 1.5\text{ V}$ $V_{\text{OUT}} = V_{\text{OUT}} = 7\text{ V}$ $V_{\text{OUT}} = 5\text{ V}$	P_7.5.15
Low threshold voltage for retri activation	$V_{\text{DS(L)}}$	0.2	0.3	0.4	V	$V_S > 8\text{ V}$ $V_{\text{SLS\_REF}} = 1.5\text{ V}$ $V_{\text{OUT}} = V_{\text{OUT}} = 7\text{ V}$ $V_{\text{OUT}} = 5\text{ V}$	P_7.5.16
Pull-up current	$I_{\text{DS(PU)}}$	25	35	50	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{\text{SLS\_REF}} = 1.5\text{ V}$ $V_{\text{OUT}} = V_{\text{OUT}} = 7\text{ V}$ $V_{\text{OUT}} = 5\text{ V}$	P_7.5.17
Pull-down current	$I_{\text{DS(PD)}}$	300	500	750	$\mu\text{A}$	$V_S > 8\text{ V}$ $V_{\text{EN}} = 5.5\text{ V}$ $V_{\text{DS}} = 0.4\text{ V}$ $V_{\text{ERRN}} = 2\text{ V}$ $V_{\text{PS}} = 3\text{ V}$ No fault conditions	P_7.5.18

**Timing**

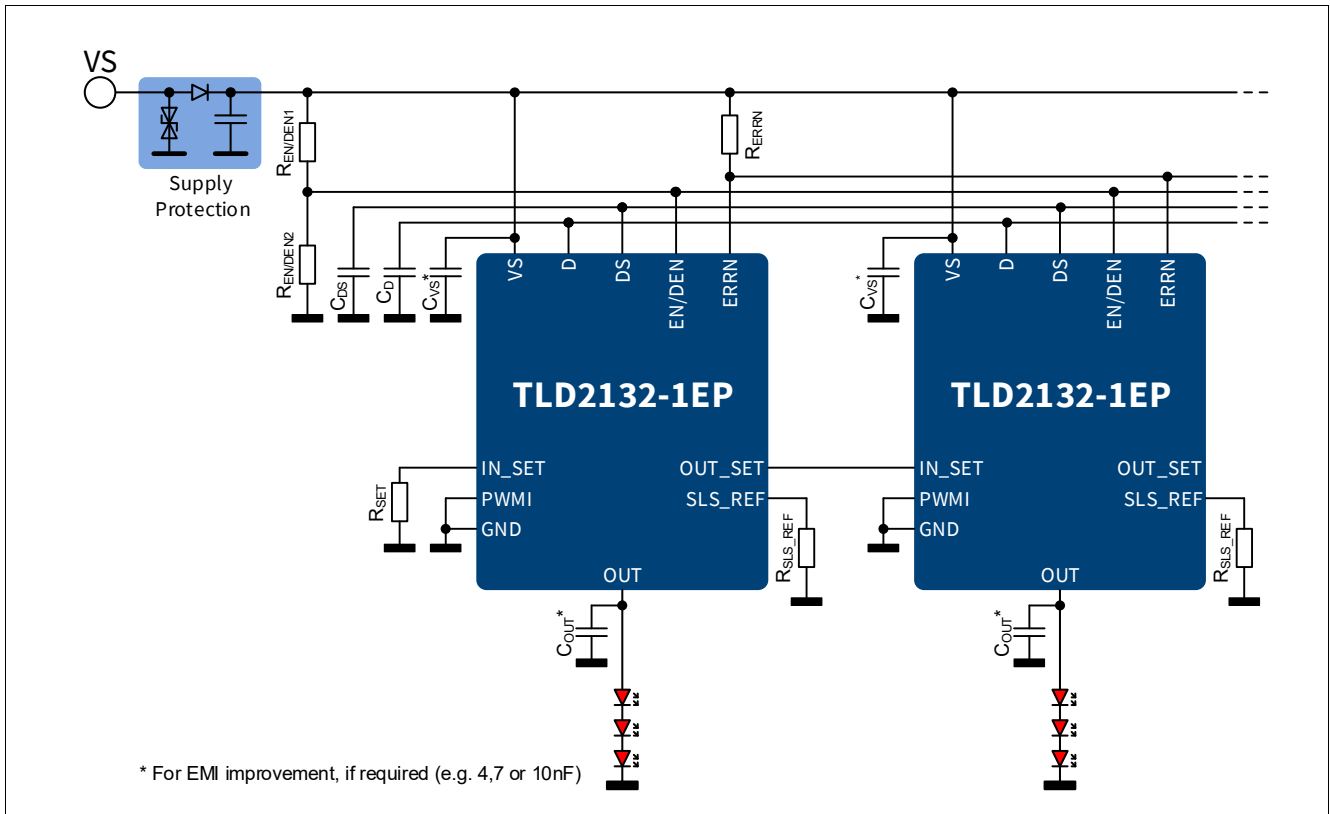
Fault to ERRN activation delay	$t_{\text{fault}}$	40	–	150	$\mu\text{s}$	<sup>1)</sup> $V_S > 8\text{ V}$ $V_{\text{OUT}}$ rising from $5\text{ V}$ to $V_S$ $V_{\text{EN}} > V_{\text{DEN(th, max)}}$	P_7.5.19
Fault appearance/removal to IN_SET deactivation/activation delay	$t_{\text{IN\_SET(del)}}$	–	–	10	$\mu\text{s}$	<sup>1)</sup> $V_S > 8\text{ V}$ OUT open D rising from $0\text{ V}$ to $5\text{ V}$ $V_{\text{EN}} > V_{\text{DEN(th, max)}}$	P_7.5.20

1) Not subjected to production test: specified by design.

**Application information**

**7 Application information**

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 26 Application diagram example**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

Package outline

8 Package outline

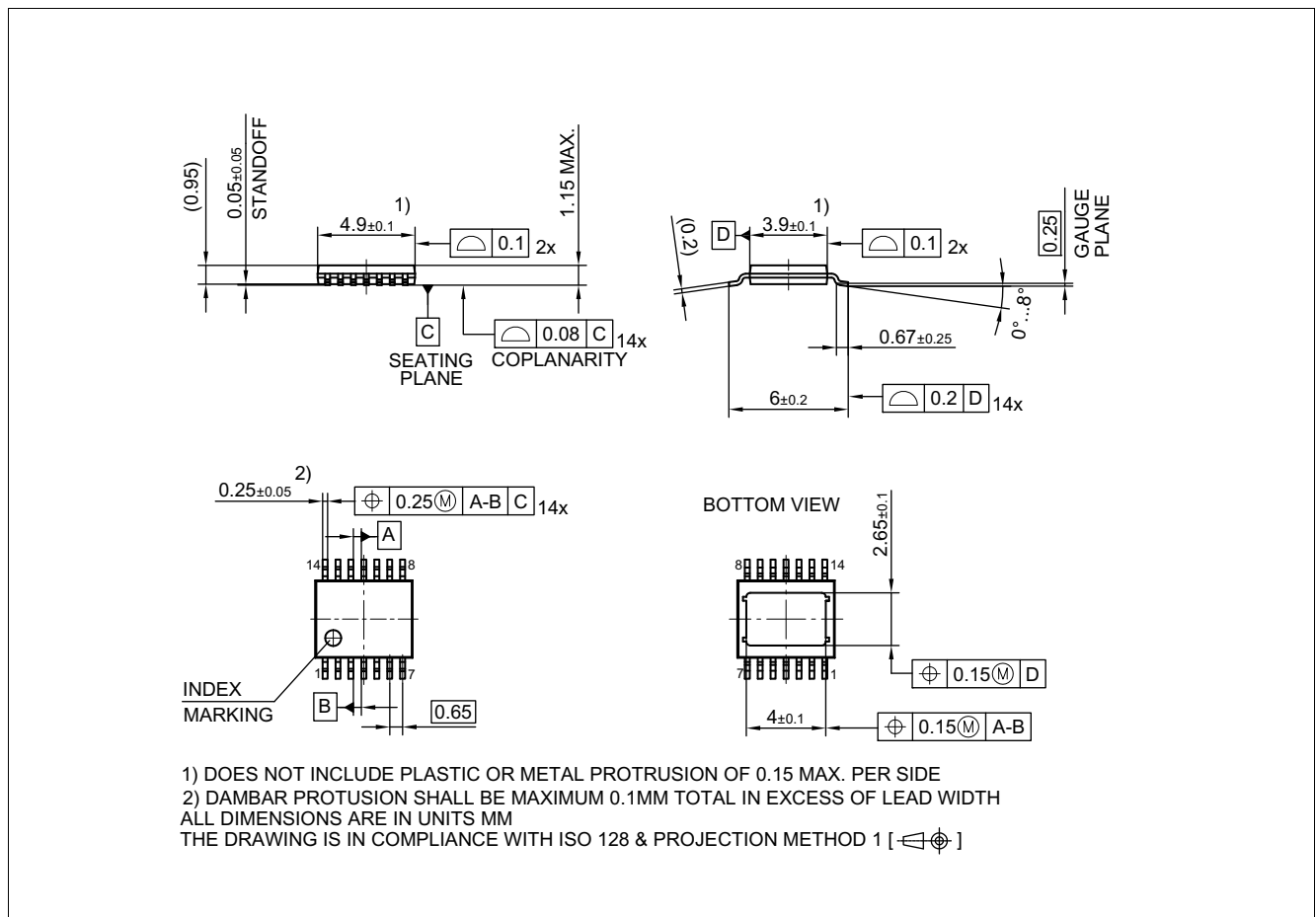


Figure 27 PG-TSDSO-14

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

Revision History

## 9 Revision History

Revision	Date	Changes
1.10	2019-09-26	Corrected copper dimensions in footnote <sup>4)</sup> in <b>Table 4</b>
1.10	2019-09-26	Updated <b>Equation (6.1)</b> and <b>Equation (6.2)</b>
1.10	2019-09-26	Specified typical value for $V_{D(th)}$ . See P_7.5.8
1.00	2018-10-09	Initial datasheet created



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