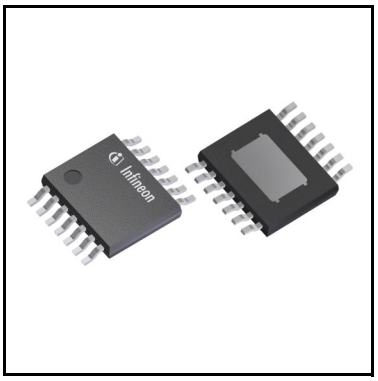
LITIX™ Power

TLD5097EP - Multitopology LITIX™ Power DC/DC Controller IC

AEC Qualified

RoHS



1 Overview

Description

The TLD5097EP is a flexibly usable DC/DC boost controller with built in diagnosis and protection features especially designed to drive LEDs.

It is designed to support fixed current and fixed voltage configurations in multiple topologies such as Boost, Buck, Buck-Boost, SEPIC and Flyback by simply adjusting the external components. The TLD5097EP drives a low side n-channel power MOSFET from an internal 5 V linear regulator.

The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can also be synchronized to an external clock source.

The TLD5097EP can be flexibly dimmed by means of analog and PWM dimming; an enable function reduces the shut-down current consumption to I_{Q_OFF} < 10 µA.

The current mode control scheme of this device provides a stable regulation loop maintained by small external compensation components. Additionally an integrated soft start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments.

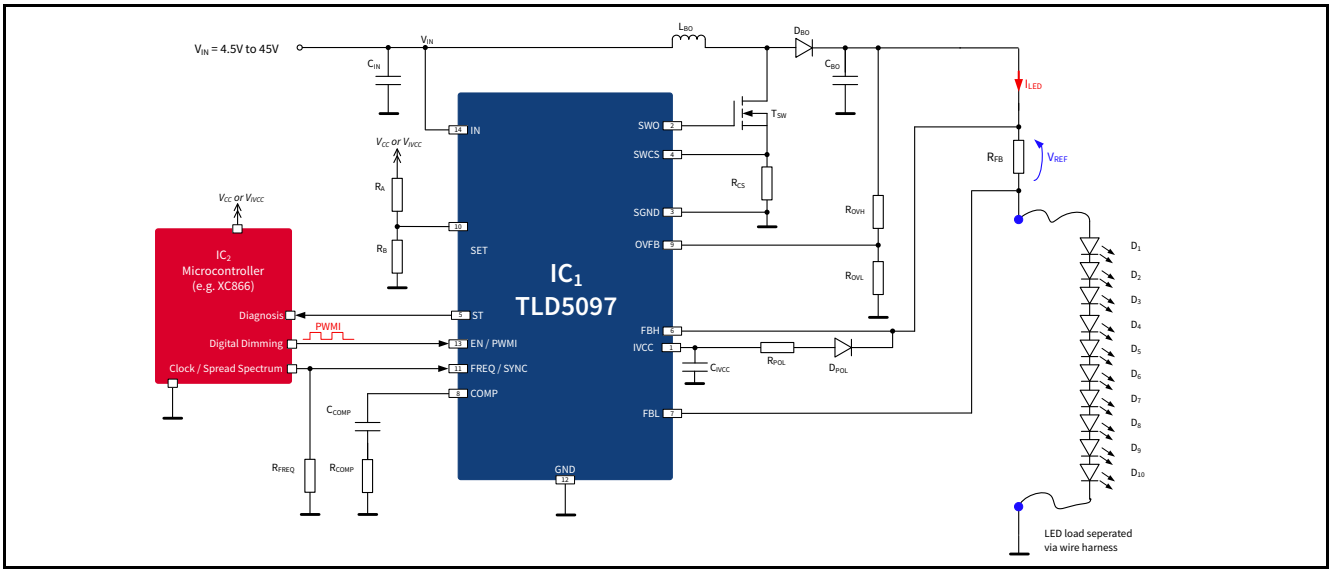


Figure 1 Typical application: Boost LED driver

Type	Package	Marking
TLD5097EP	PG-TSDSO-14	TLD5097

Potential applications

- Automotive exterior and interior lighting
- General illumination
- General purpose current/voltage controlled DC/DC driver

Features

- Fixed current or fixed voltage configuration in Boost, Buck, Buck-Boost, SEPIC and Flyback Topology
- Drives low side external n-channel switching MOSFET from internal 5 V voltage regulator
- Flexible switching frequency range from 100 kHz to 500 kHz, synchronization with external clock source
- Wide input voltage range from 4.5 V to 45 V
- Enable & PWM function with very low shutdown current: I_{Q_OFF} < 10 µA
- Analog dimming and PWM dimming feature to adjust average LED current
- Low active status output for fault communication
- Integrated protection and diagnostic functions
- Internal soft start
- 300 mV high-side current sense
- Available in a small thermally enhanced 14-pin PG-TSDSO-14 package, green product (RoHS) compliant

Table 1 Product summary

Feature	Symbol	Range
Nominal supply voltage range	V_{IN}	8 V ... 34 V
Extended supply voltage range	V_{IN}	4.5 V ... 45 V $V_{IVCC} > V_{IVCC,RTH,d}$; parameter deviations possible
Switching frequency range	f_{FREQ}	100 kHz ... 500 kHz oscillator frequency adjustment range 250 kHz ... 500 kHz synchronization frequency capture range
Maximum duty cycle	$D_{max,fixed}$	91% ...95% fixed frequency mode
	$D_{max,synced}$	88% synchronization mode
Typical gate driver peak sourcing current	$I_{SWO,SRC}$	380 mA
Typical gate driver peak sinking current	$I_{SWO,SNK}$	550 mA

Protection and diagnostic functions

- Open circuit detection
- Output overvoltage protection
- Overtemperature shutdown
- Electrostatic discharge (ESD) protection

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

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2 Block diagram

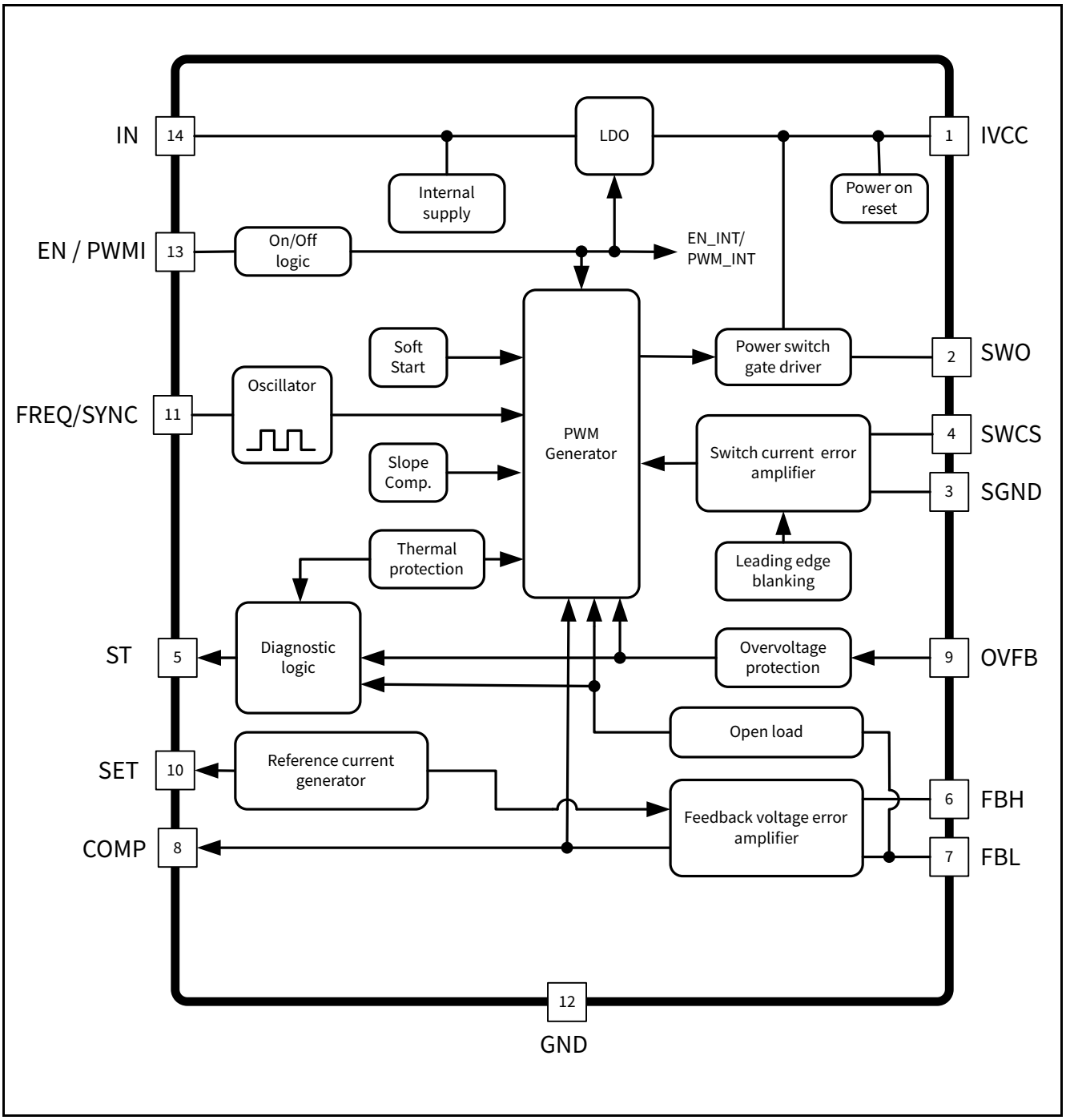

Figure 2 Block diagram TLD5097EP

3 Pin configuration

3.1 Pin assignment

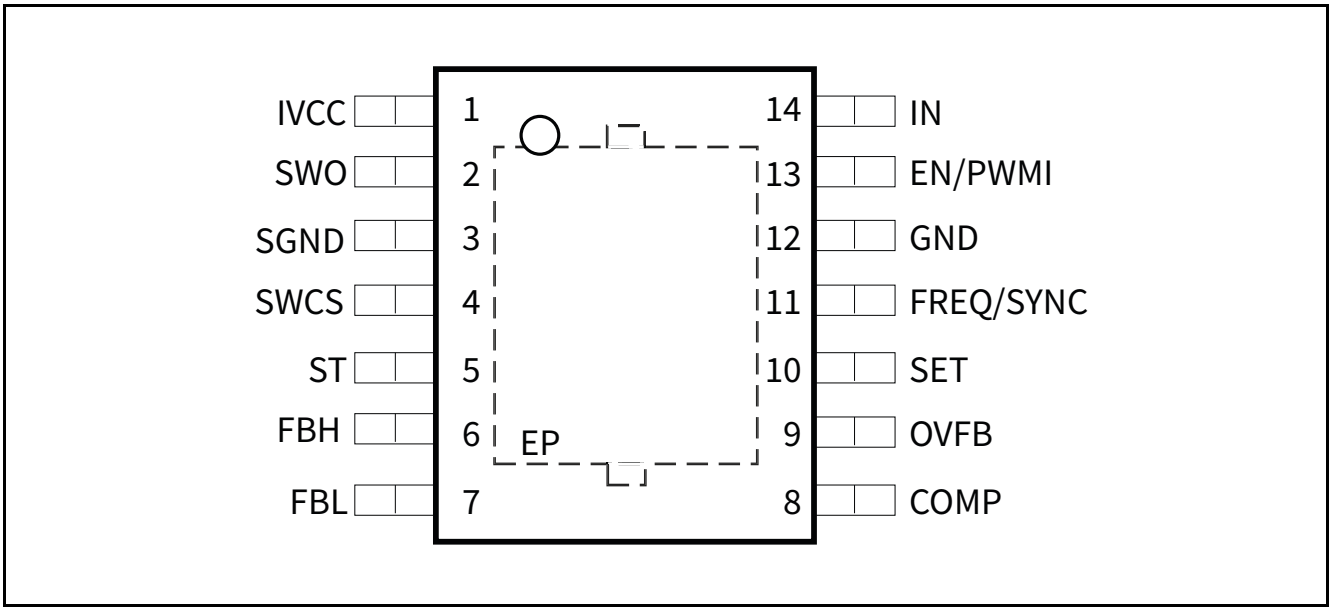

Figure 3 Pin configuration TLD5097EP

3.2 Pin definitions and functions

Table 2 Pin definition and function

#	Symbol	Direction	Function
1	IVCC	Output	**Internal LDO** Used for internal biasing and gate drive. Bypass with external capacitor. Pin must not be left open
2	SWO	Output	**Switch gate driver** Connect to gate of external switching MOSFET
3	SGND	–	**Current Sense Ground** Ground return for switch current sense
4	SWCS	Input	**Current Sense** Detects the peak current through switch
5	ST	Output	**Status** to indicate fault conditions
6	FBH	Input	**Voltage Feedback Positive** Non inverting Input (+)
7	FBL	Input	**Voltage Feedback Negative** Inverting Input (-)
8	COMP	Input	**Compensation** Connect R and C network to pin for stability

Pin configuration

Table 2 Pin definition and function

#	Symbol	Direction	Function
9	OVFB	Input	**Overvoltage Protection Feedback** Connect to resistive voltage divider to set overvoltage threshold
10	SET	Input	**Analog dimming** Load current adjustment Pin. Pin must not be left open. If analog dimming feature is not used connect to IVCC pin
11	FREQ / SYNC	Input	**Frequency Select or Synchronization** Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range
12	GND	–	**Ground** Connect to system ground
13	EN / PWMI	Input	**Enable or PWM** Apply logic HIGH signal to enable device or PWM signal for dimming LED
14	IN	Input	**Supply Input** Supply for internal biasing
	EP	–	**Exposed Pad** Connect to external heat spreading GND Cu area (e.g. inner GND layer of multilayer PCB with thermal vias)

4 General product characteristics

4.1 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 3 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
IN Supply input	V_{IN}	-0.3	–	45	V	–	P_4.1.1
EN / PWMI Enable or PWM Input	V_{EN}	-40	–	45	V	–	P_4.1.2
FBH-FBL; Feedback error amplifier differential	V_{FBH}- V_{FBL}	-40	–	61	V	The maximum delta must not exceed 61 V Differential signal (not referred to GND)	P_4.1.3
FBH; Feedback error amplifier positive input	V_{FBH}	-40	–	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61 V, refer to P_4.1.3	P_4.1.4
FBL Feedback error amplifier negative input	V_{FBL}	-40	–	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61 V, refer to P_4.1.3	P_4.1.5
FBH and FBL current	I_{FBH}, I_{FBL}		1		mA	t < 100 ms; V_{FBH} - V_{FBL} = 0.3 V	P_4.1.6
OVFB Overvoltage feedback input	V_{OVP}	-0.3	–	5.5	V	–	P_4.1.7
OVFB Overvoltage feedback input	V_{OVP}	-0.3	–	6.2	V	t < 10 s	P_4.1.8
SWCS Switch current sense input	V_{SWCS}	-0.3	–	5.5	V	–	P_4.1.9
SWCS Switch current sense input	V_{SWCS}	-0.3	–	6.2	V	t < 10 s	P_4.1.10
SWO Switch gate drive output	V_{SWO}	-0.3	–	5.5	V	–	P_4.1.11

Table 3 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SWO Switch gate drive output	V_{SWO}	-0.3	–	6.2	V	t < 10 s	P_4.1.12
SGND Current sense switch GND	V_{SGND}	-0.3	–	0.3	V	–	P_4.1.13
COMP Compensation input	V_{COMP}	-0.3	–	5.5	V	–	P_4.1.14
COMP Compensation input	V_{COMP}	-0.3	–	6.2	V	t < 10 s	P_4.1.15
FREQ / SYNC; Frequency and synchronization input	$V_{FREQ/SYNC}$	-0.3	–	5.5	V	–	P_4.1.16
FREQ / SYNC; Frequency and synchronization input	$V_{FREQ/SYNC}$	-0.3	–	6.2	V	t < 10 s	P_4.1.17
ST Status output	V_{ST}	-0.3	–	5.5	V	–	P_4.1.18
ST Status output	V_{ST}	-0.3	–	6.2	V	t < 10 s	P_4.1.19
ST Status output	I_{ST}	-2	–	2	mA	–	P_4.1.20
SET Analog dimming input	V_{SET}	-0.3	–	45	V	–	P_4.1.21
IVCC Internal linear voltage regulator output	V_{IVCC}	-0.3	–	5.5	V	–	P_4.1.22
IVCC Internal linear voltage regulator output	V_{IVCC}	-0.3	–	6.2	V	t < 10 s	P_4.1.23
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.24
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.25
ESD Susceptibility							
ESD resistivity of all pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2)]	P_4.1.26
ESD resistivity of IN, EN/PWMI, FBH, FBL and SET pin to GND	$V_{ESD,HBM}$	-4	–	4	kV	HBM[2)]	P_4.1.27
ESD resistivity	V_{ESD_CDM}	-500	–	500	V	CDM[3)]	P_4.1.28
ESD resistivity corner pins	V_{ESD_CDM}	-750	–	750	V	CDM[3)]	P_4.1.29

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002
3) ESD susceptibility, Charged Device Mode “CDM” according to AECQ100-011

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Extended supply voltage range	V_{IN}	4.5	–	45	V	[1] $V_{IVCC} > V_{IVCCT,RTH,d}$; parameter deviations possible	P_4.2.1
Nominal supply voltage range	V_{IN}	8	–	34	V	–	P_4.2.2
Feedback voltage input	V_{FBH}, V_{FBL}	3	–	60	V	–	P_4.2.3
Junction temperature	T_J	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For further information visit ***https://www.jedec.org***

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	16	–	K/W	1)2)	P_4.3.1
Junction to Ambient	R_{thJA}	–	53	–	K/W	1)3) 2s2p	P_4.3.2
Junction to Ambient	R_{thJA}	–	71	–	K/W	1)3) 1s0p + 600mm^2	P_4.3.3
Junction to Ambient	R_{thJA}	–	83	–	K/W	1)3) 1s0p + 300mm^2	P_4.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). T_A = 25°C dissipates 1 W

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board;The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu), A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. T_A=25°C, IC dissipates 1 W

5 Switching regulator

5.1 Description

The TLD5097EP regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The switching regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a PWM signal to an internal gate driver which then outputs to an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over t_{SS} (P_5.2.9) to minimize potential overvoltage at the output.

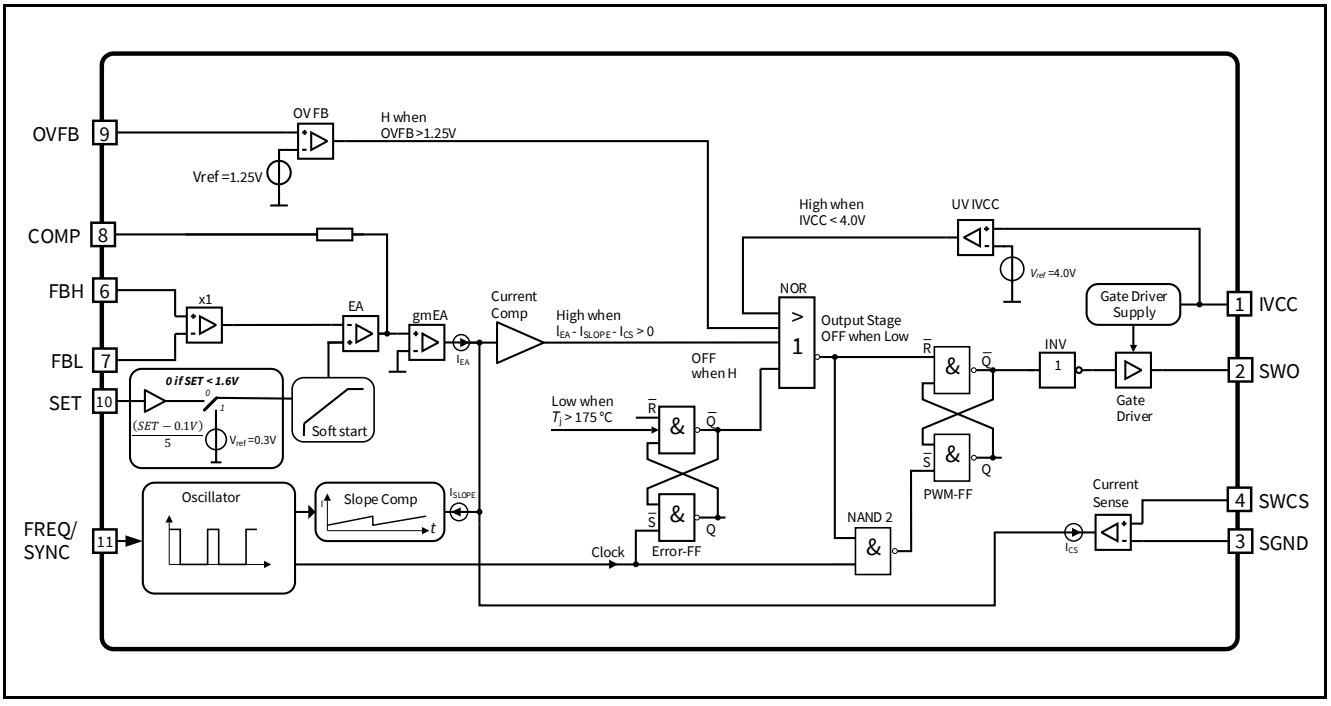

Figure 4 Switching regulator block diagram

5.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 6 Electrical characteristics: Switching regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator							
Feedback reference voltage	V_{REF}	0.29	0.30	0.31	V	refer to **Figure 29** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 5 V I_{LED} =350 mA	P_5.2.1
Feedback reference voltage	V_{REF}	0.057	0.06	0.063	V	refer to **Figure 29** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 0.4 V I_{LED}=70 mA	P_5.2.2
Feedback reference voltage offset	V_{REF_offset}	–	–	5	mV	refer to **Figure 17** and **Figure 29** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 0.1 V $V_{OUT} > V_{IN}$	P_5.2.3
Voltage line regulation	$(\Delta V_{REF} / V_{REF}) / \Delta V_{IN}$	–	–	0.15	%/V	refer to **Figure 29** V_{IN} = 8 V to 19 V; V_{SET} = 5 V; I_{LED} = 350 mA	P_5.2.4
Voltage load regulation	$(\Delta V_{REF} / V_{REF}) / \Delta I_{BO}$	–	–	5	%/A	refer to **Figure 29** V_{SET} = 5 V; I_{LED} = 100 to 500 mA	P_5.2.5
Switch peak overcurrent threshold	V_{SWCS}	130	150	170	mV	$V_{FBH} = V_{FBL}$ = 5 V V_{COMP} = 3.5 V	P_5.2.6
Maximum duty cycle	$D_{MAX,fixed}$	91	93	95	%	Fixed frequency mode	P_5.2.7
Maximum duty cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode	P_5.2.8
Soft start ramp	t_{SS}	350	1000	1500	µs	V_{FB} rising from 5% to 95% of V_{FB}, typ.	P_5.2.9
IFBH Feedback high input current	I_{FBH}	38	46	54	µA	$V_{FBH} - V_{FBL}$ = 0.3 V	P_5.2.10
IFBL Feedback low input current	I_{FBL}	15	21	27	µA	$V_{FBH} - V_{FBL}$ = 0.3 V	P_5.2.11
Switch current sense input current	I_{SWCS}	10	50	100	µA	V_{SWCS} = 150 mV	P_5.2.12

Table 6 Electrical characteristics: Switching regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input undervoltage shutdown	$V_{IN,off}$	3.5	–	4.5	V	V_{IN} decreasing	P_5.2.13
Input voltage startup	$V_{IN,on}$	–	–	4.85	V	V_{IN} increasing	P_5.2.14
Gate driver for external switch							
Gate driver peak sourcing current	$I_{SWO,SRC}$	–	380	–	mA	1) V_{SWO} = 1 V to 4 V	P_5.2.15
Gate driver peak sinking current	$I_{SWO,SNK}$	–	550	–	mA	1) V_{SWO} = 4 V to 1 V	P_5.2.16
Gate driver output rise time	$t_{R,SWO}$	–	30	60	ns	1) $C_{L,SWO}$ = 3.3 nF; V_{SWO} = 1 V to 4 V	P_5.2.17
Gate driver output fall time	$t_{F,SWO}$	–	20	40	ns	1) $C_{L,SWO}$ = 3.3 nF; V_{SWO} = 4 V to 1 V	P_5.2.18
Gate driver output voltage	V_{SWO}	4.5	–	5.5	V	1) $C_{L,SWO}$ = 3.3 nF	P_5.2.19

1) Not subject to production test, specified by design

6 Oscillator and synchronization

6.1 Description

R_{freq} vs. switching frequency

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

(6.1)

$$R_{FREQ} = \frac{1}{(141 \cdot 10^{-12}\left[\frac{s}{\Omega}\right]) \cdot \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - (3.5 \cdot 10^{3}\,[\Omega])[\Omega]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

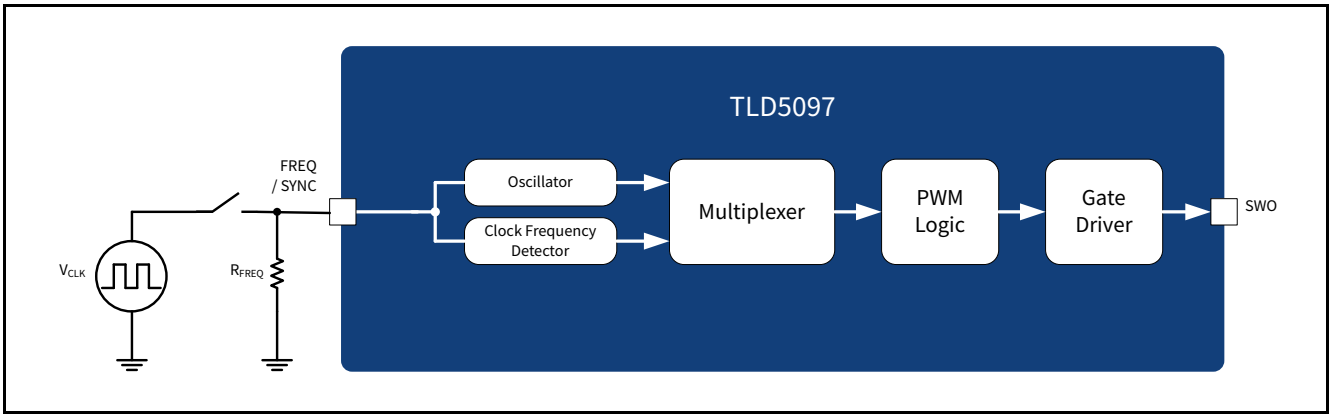

Figure 5 Oscillator and synchronization block diagram and simplified application circuit

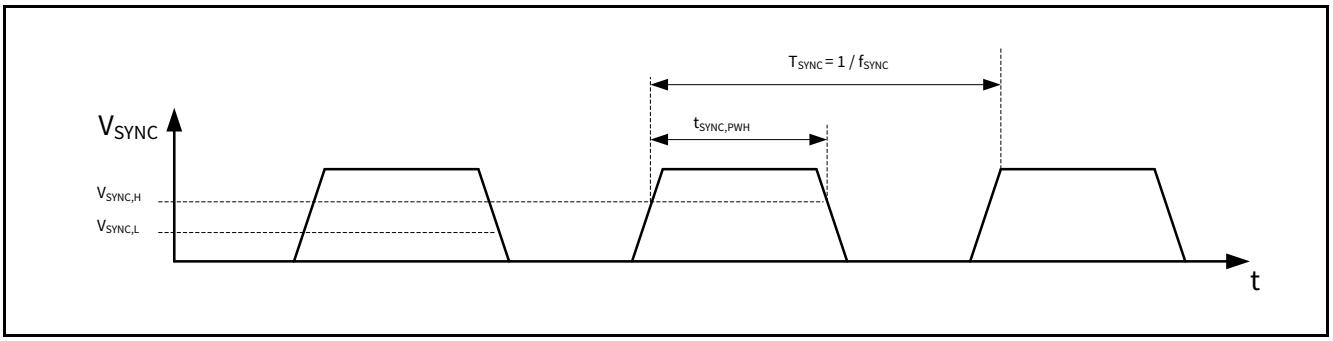

Figure 6 Synchronization timing diagram

6.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 7 Electrical characteristics: Oscillator and synchronization

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Oscillator							
Oscillator frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20 kΩ	P_6.2.1
Oscillator frequency adjustment range	f_{FREQ}	100	–	500	kHz	–	P_6.2.2
FREQ / SYNC supply current	I_{FREQ}	–	–	-700	µA	V_{FREQ} = 0 V	P_6.2.3
Frequency voltage	V_{FREQ}	1.16	1.24	1.32	V	f_{FREQ} = 100 kHz	P_6.2.4
Synchronization							
Synchronization frequency capture range	f_{SYNC}	250	–	500	kHz	–	P_6.2.5
Synchronization signal high logic level valid	$V_{SYNC,H}$	3.0	–	–	V	1)2)	P_6.2.6
Synchronization signal low logic level valid	$V_{SYNC,L}$	–	–	0.8	V	1)2)	P_6.2.7
Synchronization signal logic high pulse width	$t_{SYNC,PWH}$	200	–	–	ns	1)2)	P_6.2.8

1) Synchronization of external PWM ON signal to falling edge
2) Not subject to production test, specified by design

6.3 Typical performance characteristics of oscillator

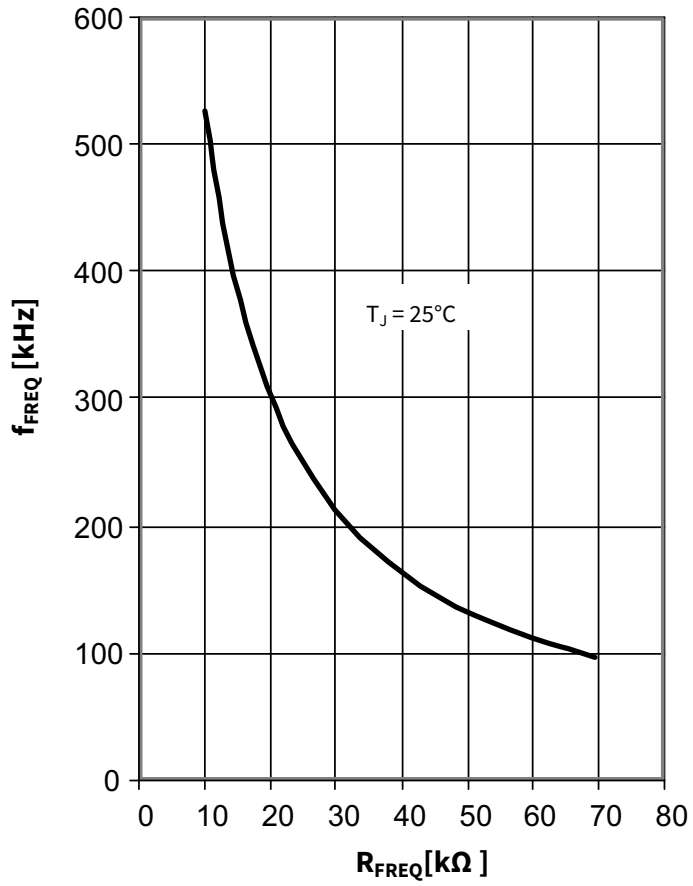

Figure 7 Switching frequency f_{SW} versus frequency select resistor to GND R_{FREQ}

7 Enable and dimming function

7.1 Description

The enable function powers the device on or off. A valid logic “low”signal on enable pin EN/PWMI powers “off” the device and current consumption is less than I_{Q_OFF} (P_7.1.8). A valid logic “high” enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is off in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to the internal gate driver. The EN/PWMI enables and disables the gate driver for the main switch during PWM operation. PWM dimming an LED is a commonly practiced dimming method and can prevent color shift in an LED light source.

The enable and PWM input function share the same pin. Therefore a valid logic “low” signal at the EN/PWMI pin needs to differentiate between an enable power “off” or a PWM dimming “low” signal. The device differentiates between enable off and PWM dimming signal by requiring the enable off at the EN/PWMI pin to stay “low” for the “**Enable turn off delay time**” ($t_{EN,OFF,DEL}$ P_7.1.6).

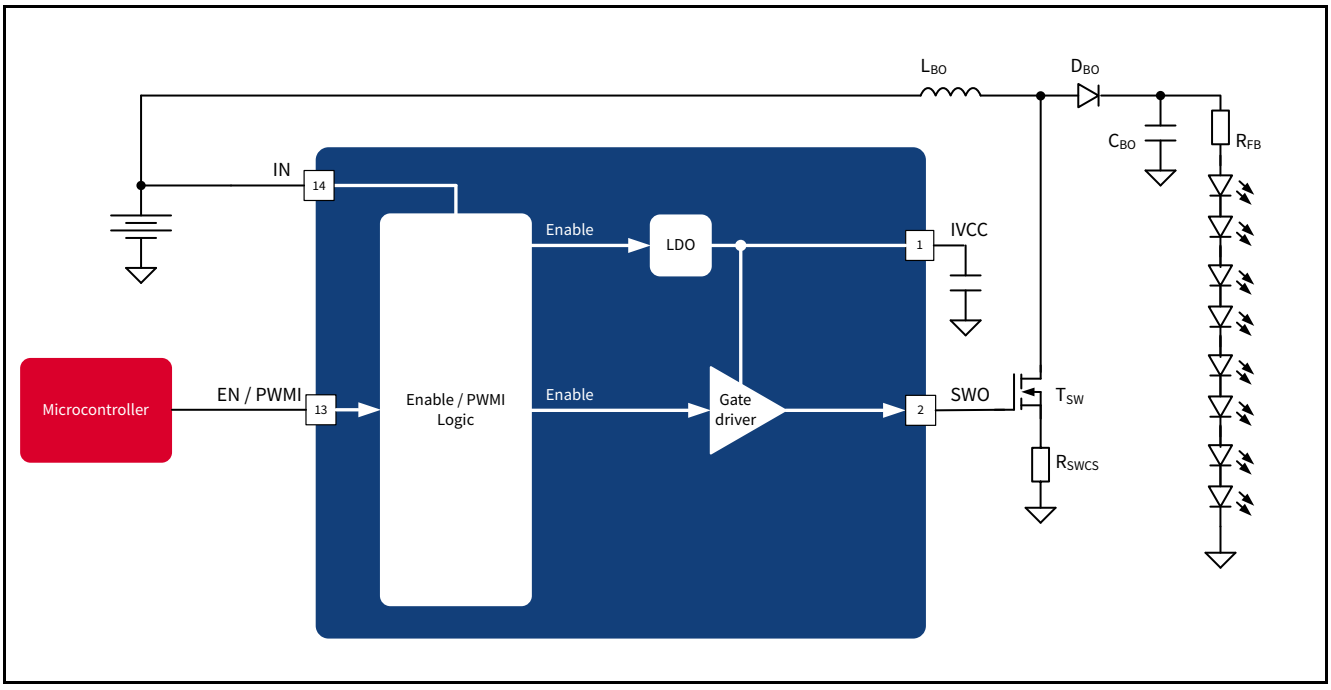

Figure 8 Block diagram and simplified application circuit enable and LED dimming

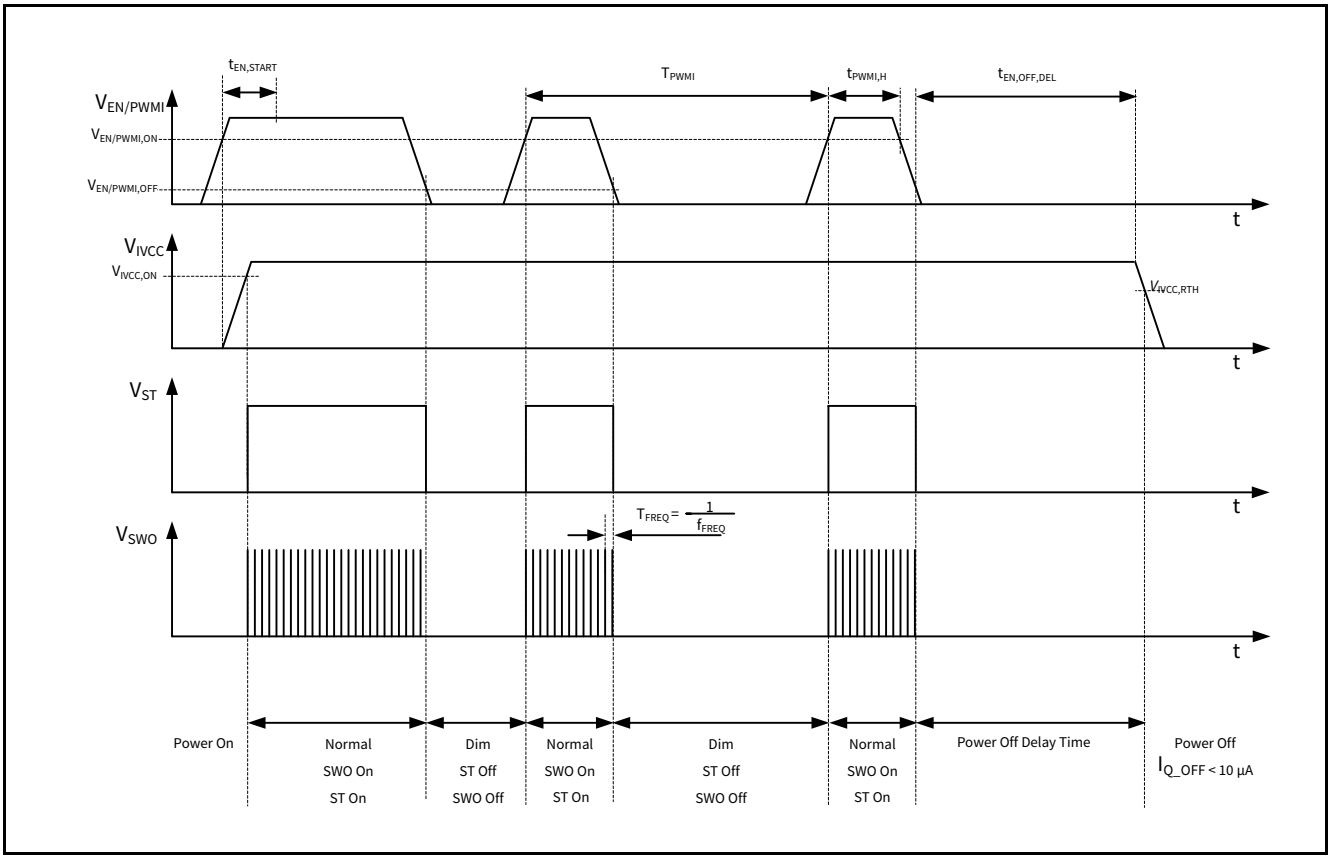

Figure 9 Timing diagram enable and LED dimming

Note: The ST signal is “low” during soft-start.

7.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 8 Electrical characteristics: Enable and dimming

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable / PWM Input							
Enable/PWMI turn on threshold	$V_{EN/PWMI,ON}$	3.0	–		V	–	P_7.1.1
Enable/PWMI turn off threshold	$V_{EN/PWMI,OFF}$	–	–	0.8	V	–	P_7.1.2
Enable/PWMI hysteresis	$V_{EN/PWMI,HYS}$	50	200	400	mV	1)	P_7.1.3
Enable/PWMI high input current	$I_{EN/PWMI,H}$	–	–	30	µA	$V_{EN/PWMI}$ = 16.0 V	P_7.1.4
Enable/PWMI low input current	$I_{EN/PWMI,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5 V	P_7.1.5
Enable turn off delay time	$t_{EN,OFF,DEL}$	8	10	12	ms	–	P_7.1.6
Enable startup time	$t_{EN,START}$	100	–	–	µs	1)	P_7.1.7
Current consumption							
Current consumption, shutdown mode	I_{Q_OFF}	–	–	10	µA	$V_{EN/PWMI}$ = 0.8 V; $T_J \leq$ 105°C; V_{IN} = 16V	P_7.1.8
Current consumption, active mode	I_{Q_ON}	–	–	7	mA	2) $V_{EN/PWMI} \geq$ 4.75 V; I_{BO} = 0 mA; V_{SWO} = 0% duty cycle	P_7.1.9

1) Not subject to production test, specified by design
2) Dependency on switching frequency and gate charge of external switches

8 Linear regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to $I_{LIM,min}$ (P_8.1.2). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (P_8.1.5) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated undervoltage protection for the external switching MOSFET

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the IVCC undervoltage reset switch OFF threshold ($V_{IVCC,RTH,d}$). The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

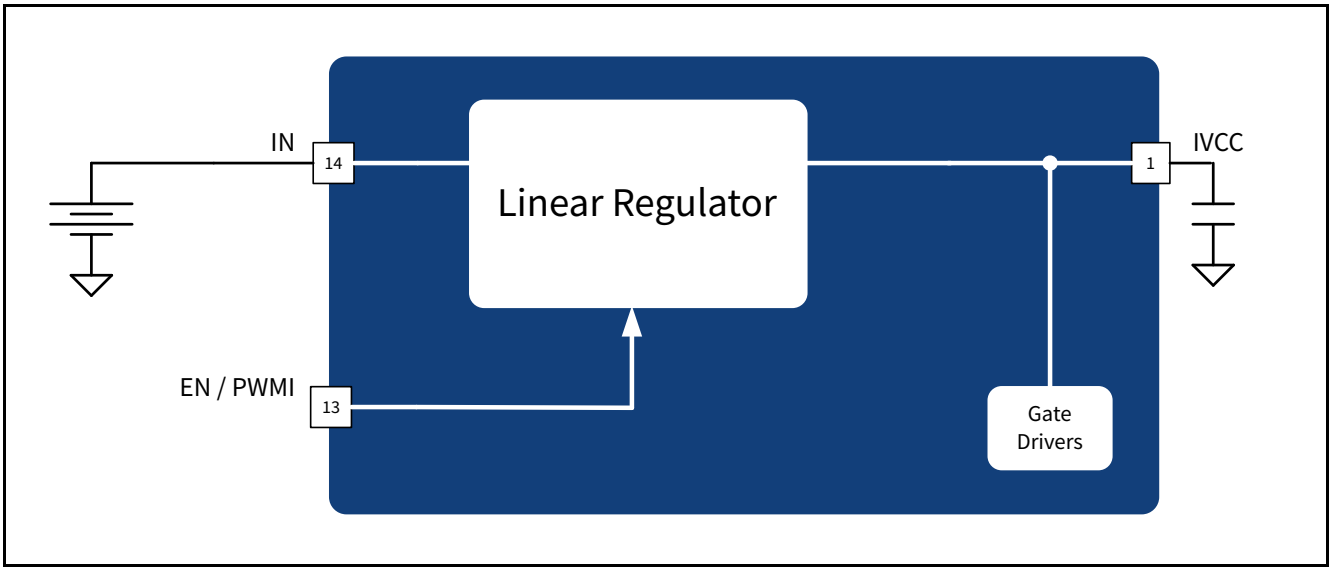

Figure 10 Voltage regulator block diagram and simplified application circuit

8.2 Electrical characteristics

V_{IN} = 8 V to 34 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 9 Electrical characteristics: Line regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_{IVCC}	4.85	5	5.15	V	6 V ≤ V_{IN} ≤ 45 V 0.1 mA ≤ I_{IVCC} ≤ 40 mA	P_8.1.1
Output current limitation	I_{LIM}	51	–	90	mA	V_{IN} = 13.5 V V_{IVCC} = 4.5 V Current flows out of pin	P_8.1.2
Drop out voltage	V_{DR}	–		0.5	V	V_{IN} = 4.5 V I_{IVCC} = 25 mA	P_8.1.3
IVCC buffer capacitor	C_{IVCC}	0.47	1	100	µF	1)2)	P_8.1.4
IVCC buffer capacitor ESR	$R_{IVCC, ESR}$	–	–	0.5	Ω	1)	P_8.1.5
Undervoltage reset headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$	P_8.1.6
IVCC undervoltage reset switch-off threshold	$V_{IVCC,RTH,d}$	3.6	–	4.0	V	3) V_{IVCC} decreasing	P_8.1.7
IVCC undervoltage reset switch-on threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing	P_8.1.8

1) Not subject to production test, specified by design
2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.
3) Selection of external switching MOSFET is crucial and the $V_{IVCC,RTH,d\ min.}$ as worst case the threshold voltage of the. MOSFET must be considered.

9 Protection and diagnostic functions

9.1 Description

The TLD5097EP has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. In case of a fault condition, the SWO signal stops operation. The ST signal will change to an active logic “low” signal to communicate that a fault has occurred (detailed overview in **Figure 11** and **Table 10** below). **Figure 12** illustrates the various open load and open feedback conditions. In case of an overtemperature condition the integrated thermal shutdown function turns off the gate driver and internal linear voltage regulator. The typical junction shutdown temperature is 175°C ($T_{J,SD}$ P_9.2.3). After cooling down the IC will automatically restart. Thermal shutdown is an integrated protection function designed to prevent IC destruction and is not intended for continuous use in normal operation (**Figure 14**). To calculate the proper overvoltage protection resistor values an example is given in **Figure 15**.

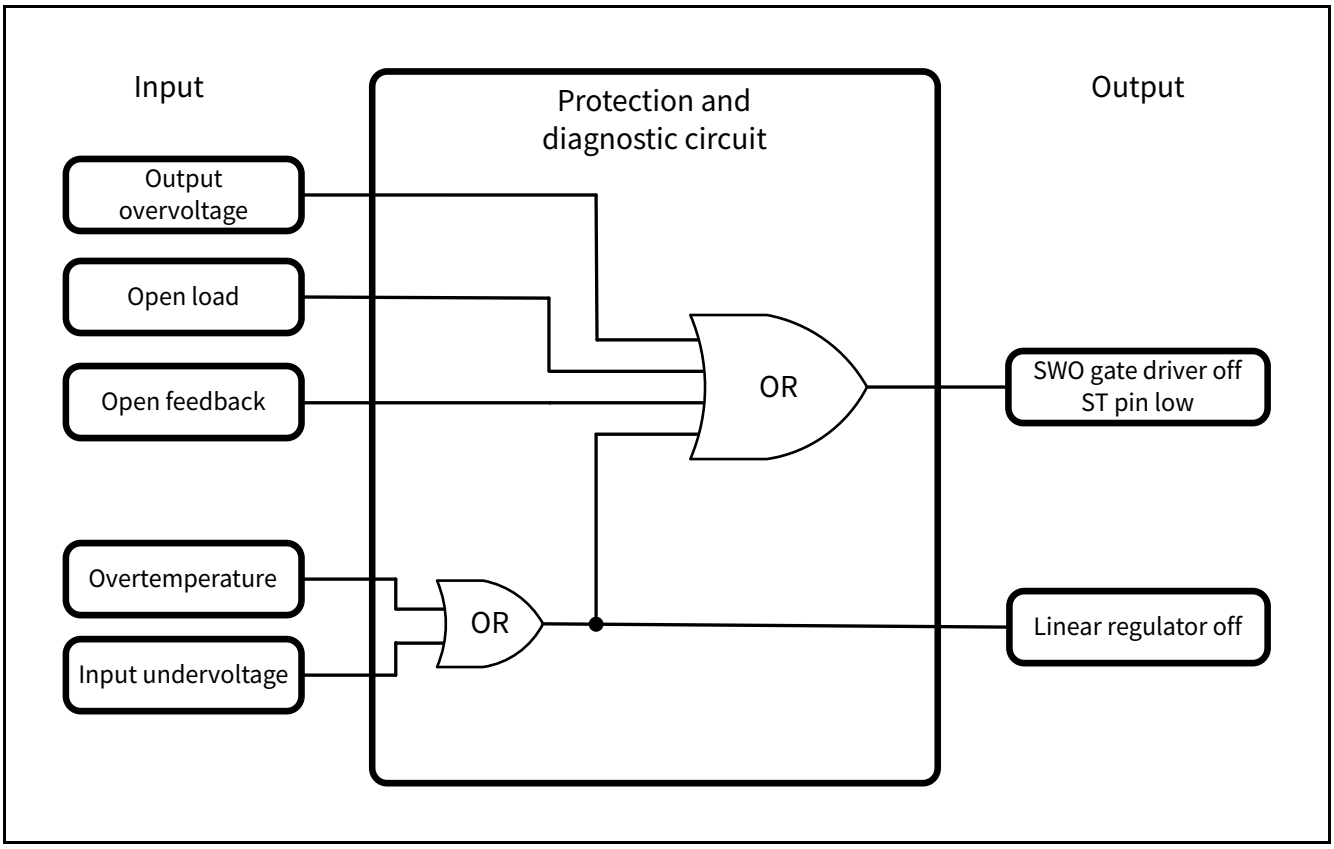

Figure 11 Protection and diagnostic function block diagram

Table 10 Diagnosis truth table[1)]

Input		Output		
Condition	**Level**	**ST**	**SWO**	**IVCC**
Overvoltage at output	False	High or Sw	Sw	Active
	True	Low	Low	Active
Open load	False	High or Sw	Sw	Active
	True	Low	Low	Active
Open feedback	False	High or Sw	Sw	Active
	True	Low	Low	Active
Overtemperature	False	High or Sw	Sw	Active
	True	Low	Low	Shutdown
Undervoltage at input	False	High or Sw	Sw	Active
	True	Low	Low	Shutdown

1) Sw = Switching; False = Condition does NOT exist; True = Condition does exist

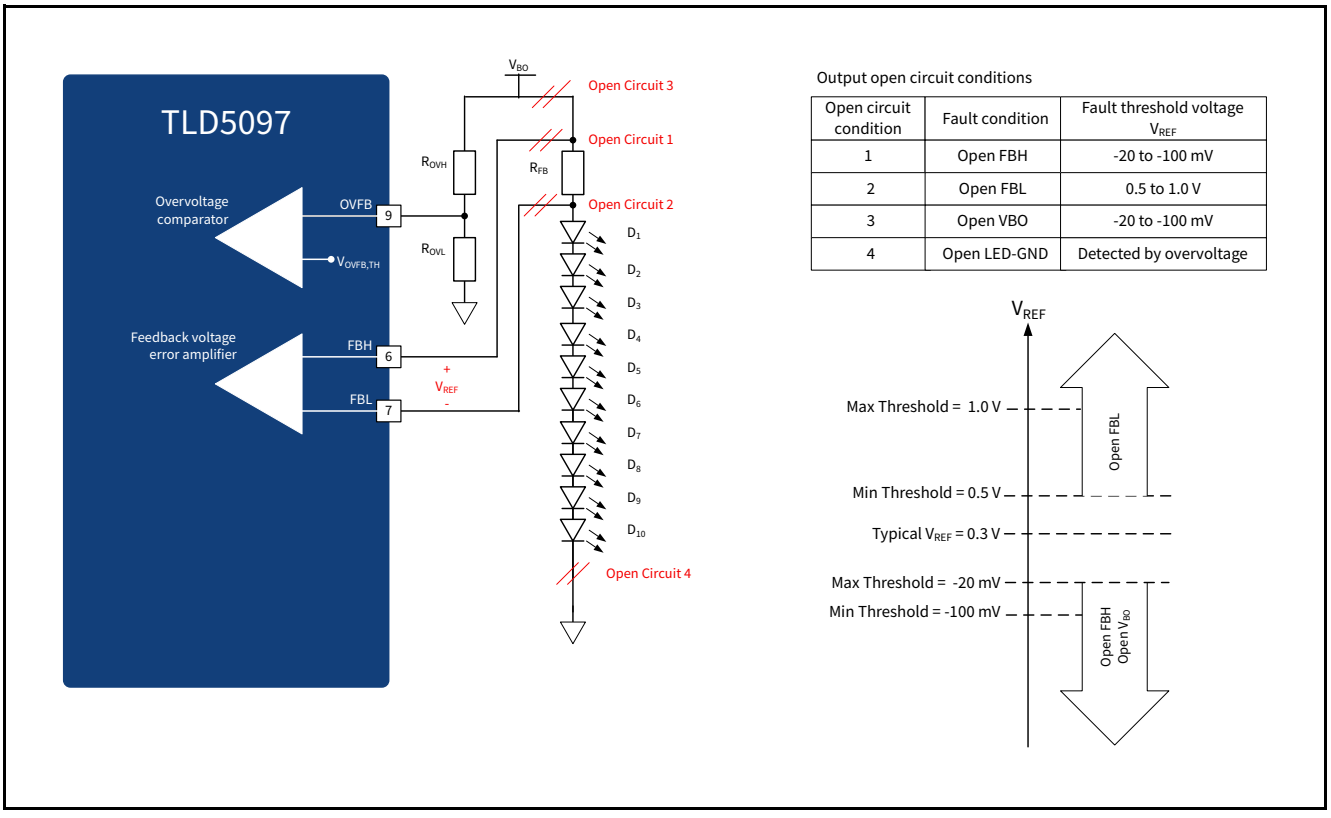

Figure 12 Open load and open feedback conditions

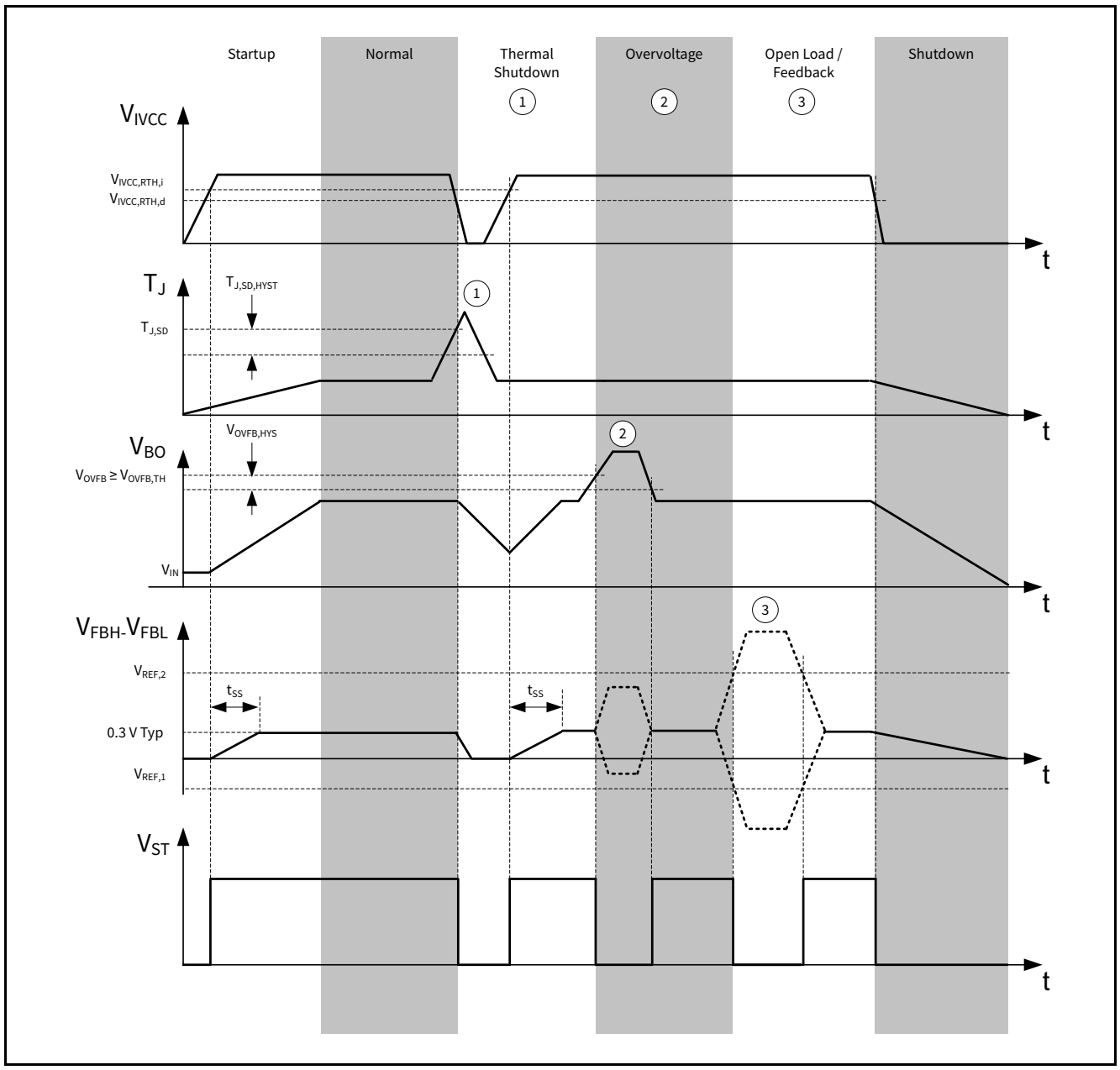

Figure 13 Open load, overvoltage and overtemperature timing diagram

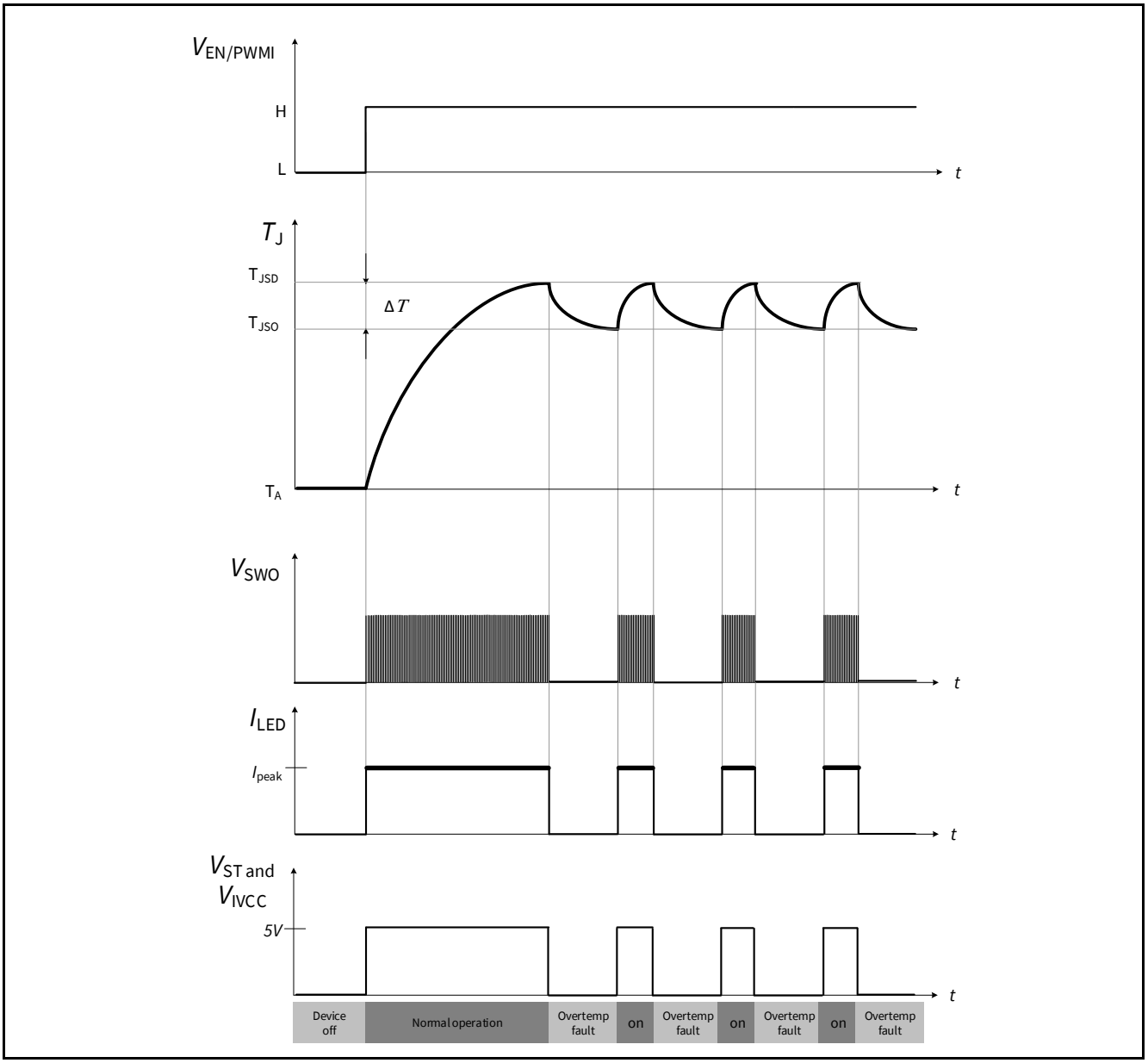

Figure 14 Device overtemperature protection behavior

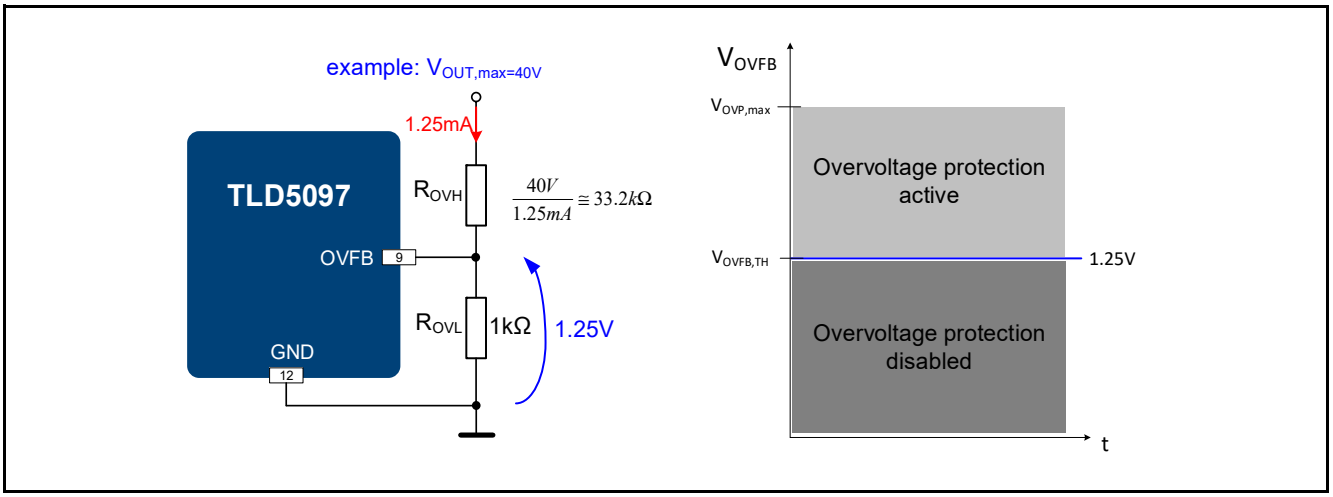

Figure 15 Overvoltage protection description

9.2 Electrical characteristics

V_{IN} = 8 V to 34 V; T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 11 Electrical characteristics: Protection and diagnosis

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Status output							
Status output voltage low	$V_{ST,LOW}$	–	–	0.4	V	1) I_{ST}= 1mA	P_9.2.1
Status output voltage high	$V_{ST,HIGH}$	V_{IVCC} -0.4	–	V_{IVCC}	V	1) I_{ST} = -1mA	P_9.2.2
Temperature protection							
Overtemperature shutdown	$T_{J,SD}$	160	175	190	°C	1) refer to **Figure 14**	P_9.2.3
Overtemperature shutdown hystereses	$T_{J,SD,HYST}$	–	15	–	°C	1)	P_9.2.4
Overvoltage protection							
Output overvoltage feedback threshold increasing	$V_{OVFB,TH}$	1.21	1.25	1.29	V	refer to **Figure 15**	P_9.2.5
Output overvoltage feedback hysteresis	$V_{OVFB,HYS}$	50	–	150	mV	1)Output voltage decreasing	P_9.2.6
Overvoltage reaction time	t_{OVPRR}	2	–	10	µs	1)Output voltage decreasing	P_9.2.7
Overvoltage feedback input current	I_{OVFB}	-1	0.1	1	µA	V_{OVFB} = 1.25 V	P_9.2.8
Open load and open feedback diagnostics							
Open load/feedback Threshold	$V_{REF,1,3}$	-100	–	-20	mV	refer to **Figure 12** $V_{REF} = V_{FBH} - V_{FBL}$ Open circuit 1 or 3	P_9.2.9
Open feedback threshold	$V_{REF,2}$	0.5	–	1	V	refer to **Figure 12** $V_{REF} = V_{FBH} - V_{FBL}$ Open circuit 2	P_9.2.10

1) Specified by design; not subject to production test.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

10 Analog dimming

This pin influences the “feedback voltage error amplifier” by generating an internal current accordingly to an external reference voltage (V_{SET}). If the analog dimming feature is not needed this pin must be connected to IVCC or external > 1.6 V supply. Different application scenarios are described in **Figure 18**. This pin can also go outside of the ECU for instance if a thermistor is connected on a separated LED module and the “Analog dimming input” is used to thermally protect the LEDs. For reverse battery protection of this pin an external series resistor should be placed to limit the current.

10.1 Purpose of analog dimming

1. It is difficult for LED manufacturers to deliver LEDs which have the same brightness, colorpoint and forward voltage class. Due to this relatively wide spread of the crucial LED parameters automotive customers order LEDs from one or maximum two different colorpoint classes. The LED manufacturer must preselect the LEDs to deliver the requested colorpoint class. These preselected LEDs are matched in terms of the colorpoint but a variation of the brightness remains. To correct the brightness deviation an analog dimming feature is needed. The mean LED current can be adjusted by applying an external voltage V_{SET} at the SET pin.
2. If the DC/DC application is separated from the LED loads the ECU manufacturers aim is to develop one hardware which should be able to handle different load current conditions (e.g. 80 mA to 400 mA) to cover different applications. To achieve this average LED current adjustment the analog dimming is a crucial feature.

10.2 Description

Application example

Desired LED current = 400 mA. For the calculation of the correct feedback resistor R_{FB} the following equation can be used: This formula is valid if the analog dimming feature is disabled and V_{SET} > 1.6 V.

(10.1)

$$I_{LED} = \frac{V_{REF}}{R_{FB}} \rightarrow R_{FB} = \frac{V_{REF}}{I_{LED}} \rightarrow R_{FB} = \frac{0.3V}{400mA} = 750m\Omega$$

Related electrical parameter is guaranteed with V_{SET} = 5 V (P_5.2.1) A decrease of the average LED current can be achieved by controlling the voltage at the SET pin (V_{SET}) between 0.1 V and 1.6 V. The mathematical relation is given in the formula below:

(10.2)

$$I_{LED} = \frac{V_{SET} - 0.1V}{5 \cdot R_{FB}}$$

Refer to the concept drawing in **Figure 17**.

If V_{SET} is equal to or smaller than 50 mV, the switching activity is stopped and I_{LED} = 0 A.

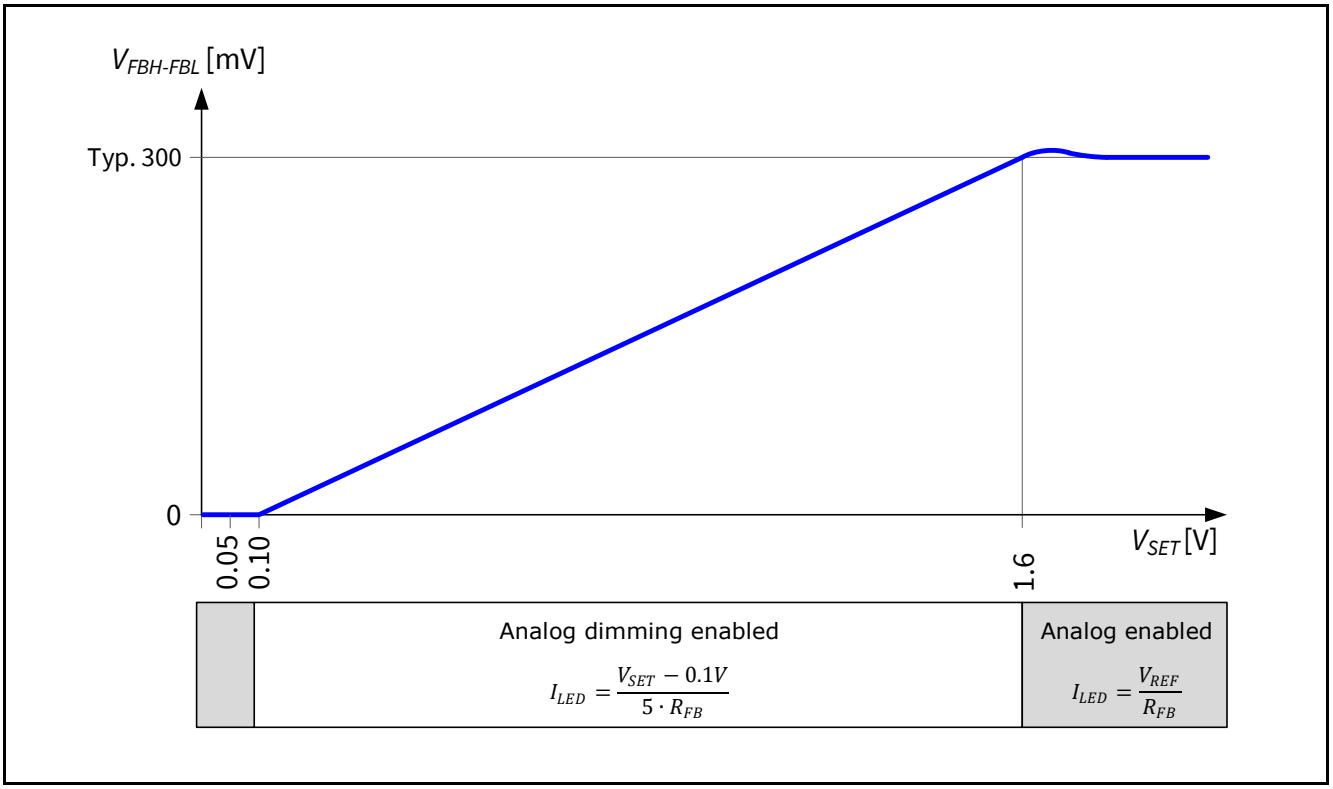

Figure 16 Basic relationship between V_{REF} and V_{SET} voltage

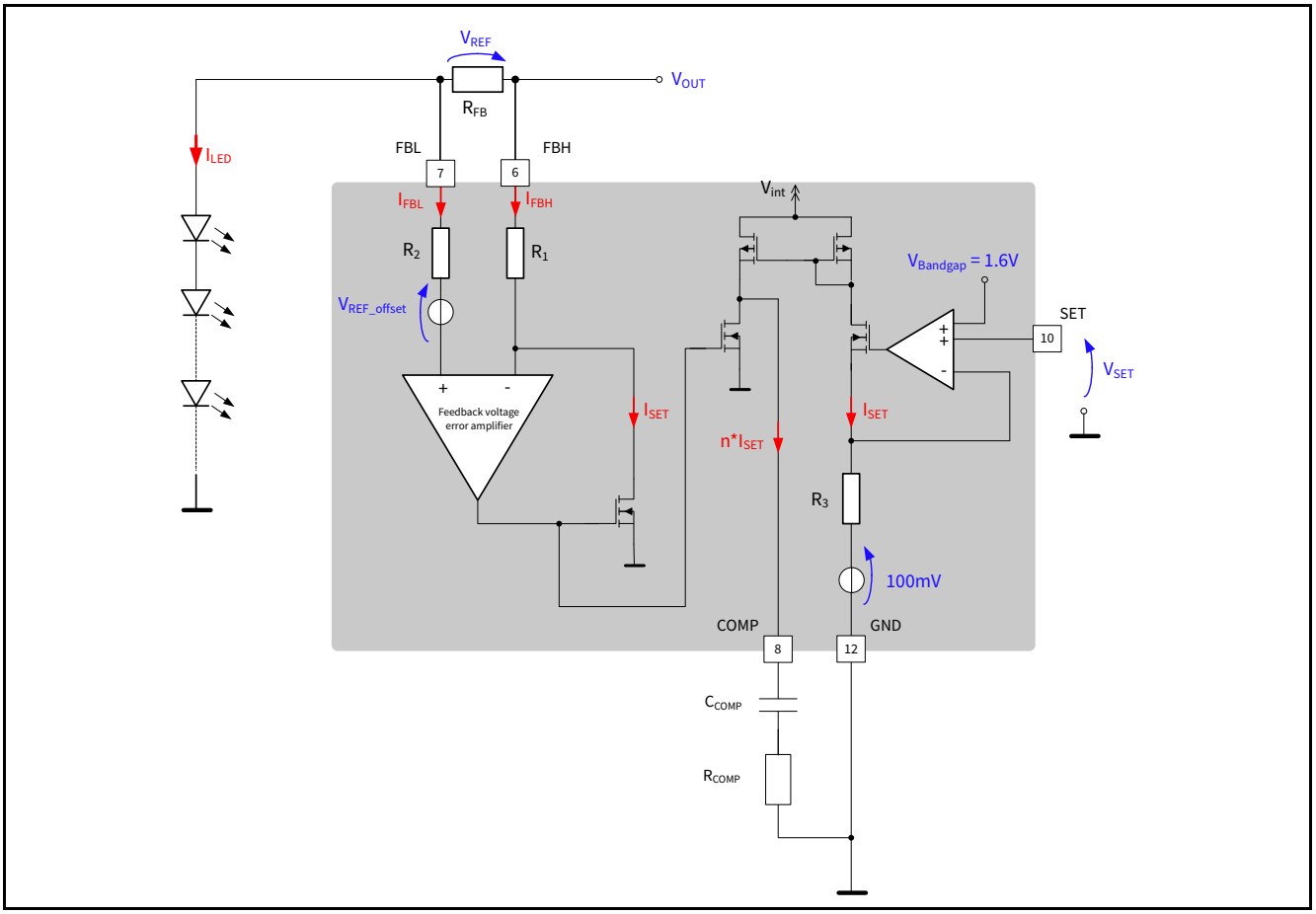

Figure 17 Concept drawing analog dimming

Analog dimming

Multi-purpose usage of the analog dimming feature

1. A µC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the TLD5097EP. The integrated voltage regulator (V_{IVCC}) can be used to supply the µC or external components if the current consumption does not exceed 20 mA.
2. The analog dimming feature is directly connected to the input voltage of the system. In this configuration the LED current is reduced if the input voltage V_{IN} is decreasing. The DC/DC boost converter is changing (increasing) the switching duty cycle if V_{IN} drops to a lower potential. This causes an increase of the input current consumption. If applications require a decrease of the LED current in respect to V_{IN} variations this setup can be chosen.
3. The usage of an external resistor divider connected between I_{VCC} (integrated 5 V regulator output and gate buffer pin) SET and GND can be chosen for systems without µC on board. The concept allows to control the LED current via placing cheap low power resistors. Furthermore a temperature sensitive resistor (Thermistor) to protect the LED loads from thermal destruction can be connected additionally.
4. If the analog dimming feature is not needed the SET pin must be connected directly to > 1.6 V potential (e.g. IVCC potential)
5. Instead of a DAC the µC can provide a PWM signal and an external R-C filter produces a constant voltage for the analog dimming. The voltage level depends on the PWM frequency (f_{PWM}) and duty cycle (DC) which can be controlled by the µc software after reading the coding resistor placed at the LED module.

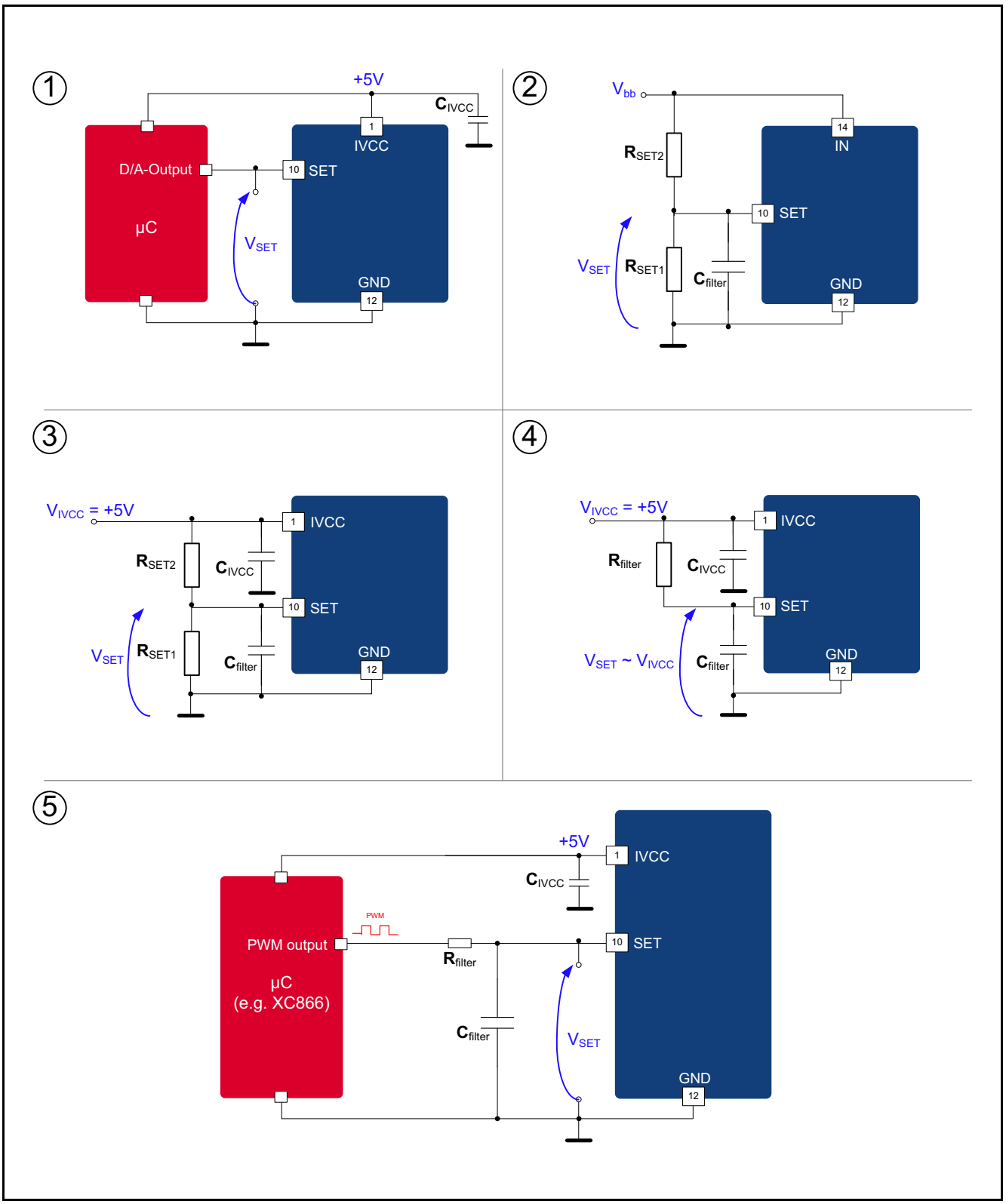

Figure 18 Analog dimming in various applications

10.3 Electrical characteristics

V_{IN} = 8 V to 34 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 12 Electrical characteristics: Protection and diagnosis

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SET programming range	V_{SET}	0	–	1.6	V	[1] refer to **Figure 16**	P_10.3.1

1) Specified by design; not subject to production test.

11 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

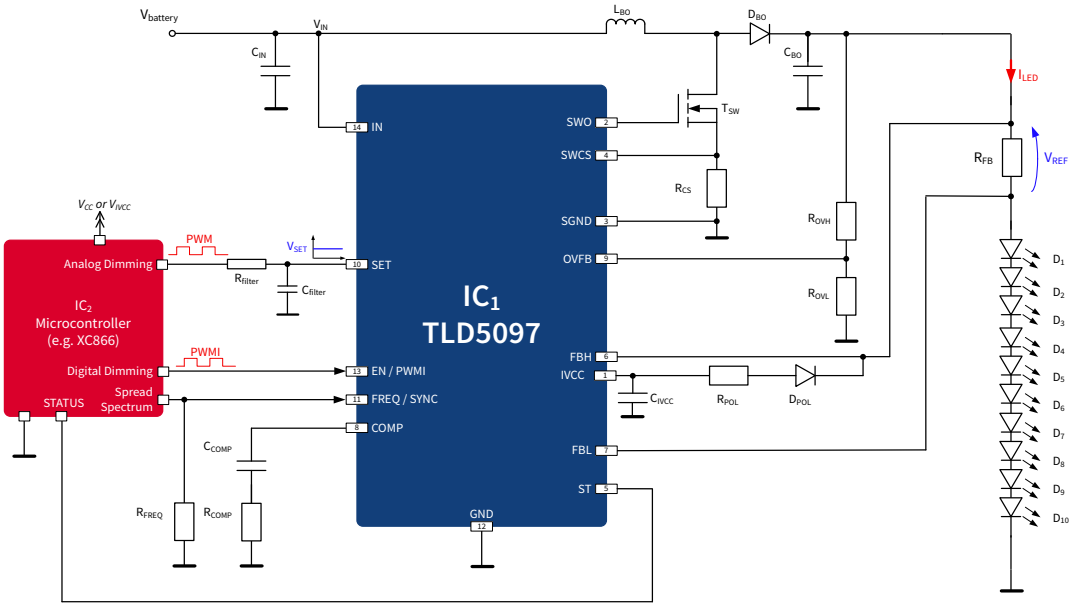

Figure 19 Boost to Ground application circuit - B2G (Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-10}	White	Osram	LUW H9GP	LED	10
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{BO}	10 uF, 50V	Panasonic	Electrolytic or Ceramic Bank	Capacitor	1
C_{COMP}	100 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1uF , 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML	Inductor	1
R_{COMP}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 20 Bill of Materials for B2G application circuit

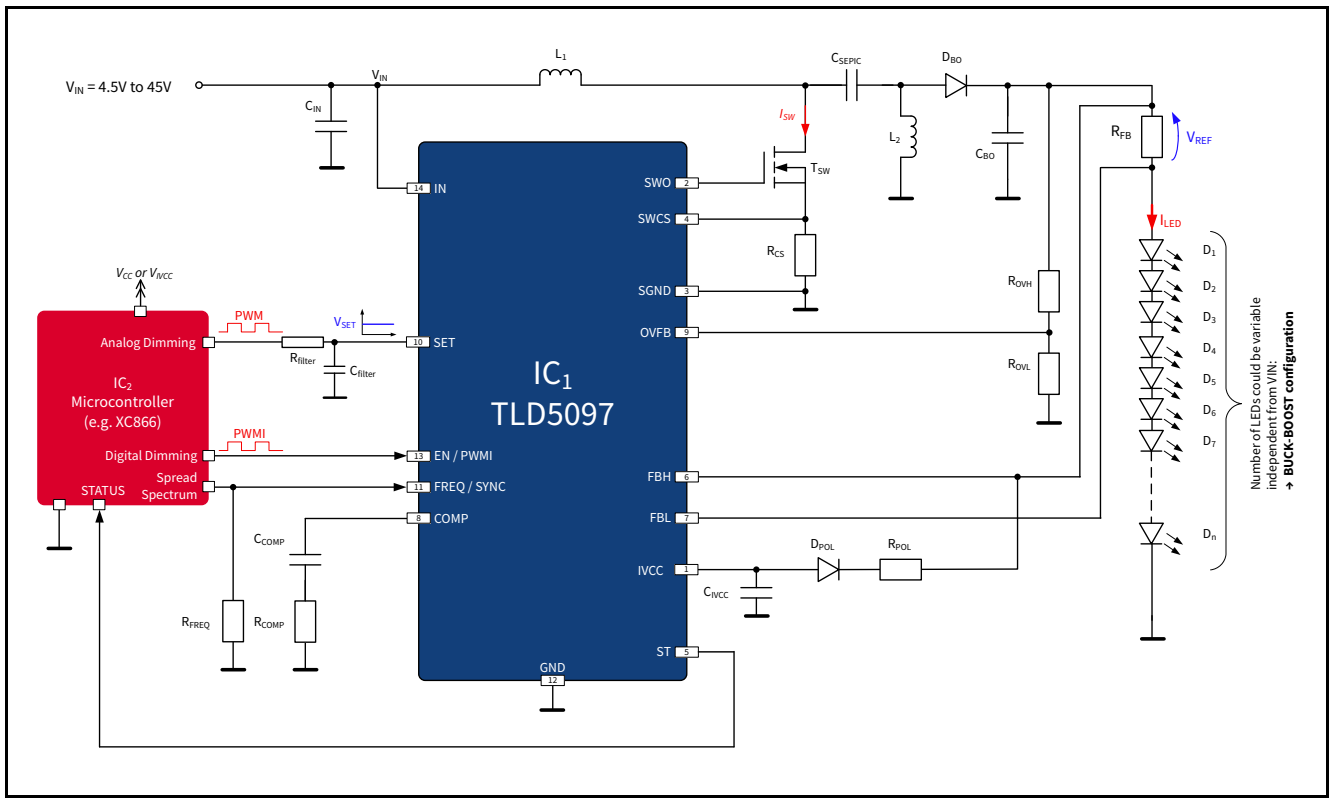

Figure 21 SEPIC application circuit (Buck - Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
D_{POL}	80V Diode	Infineon	BAS1603W	Diode	1
C_{SEPIC}	3.3 uF, 20V	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{BO}	10 uF, 50V	Panasonic	EEEFK1H100P	Capacitor	1
C_{COMP}	100 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	47 uH	Coilcraft	MSS1278T-473ML	Inductor	2
	alternativ: 22uH coupled inductor	Coilcraft	MSD1278-223MLD	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPD35N10S3L-26	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 22 Bill of Materials for SEPIC application circuit

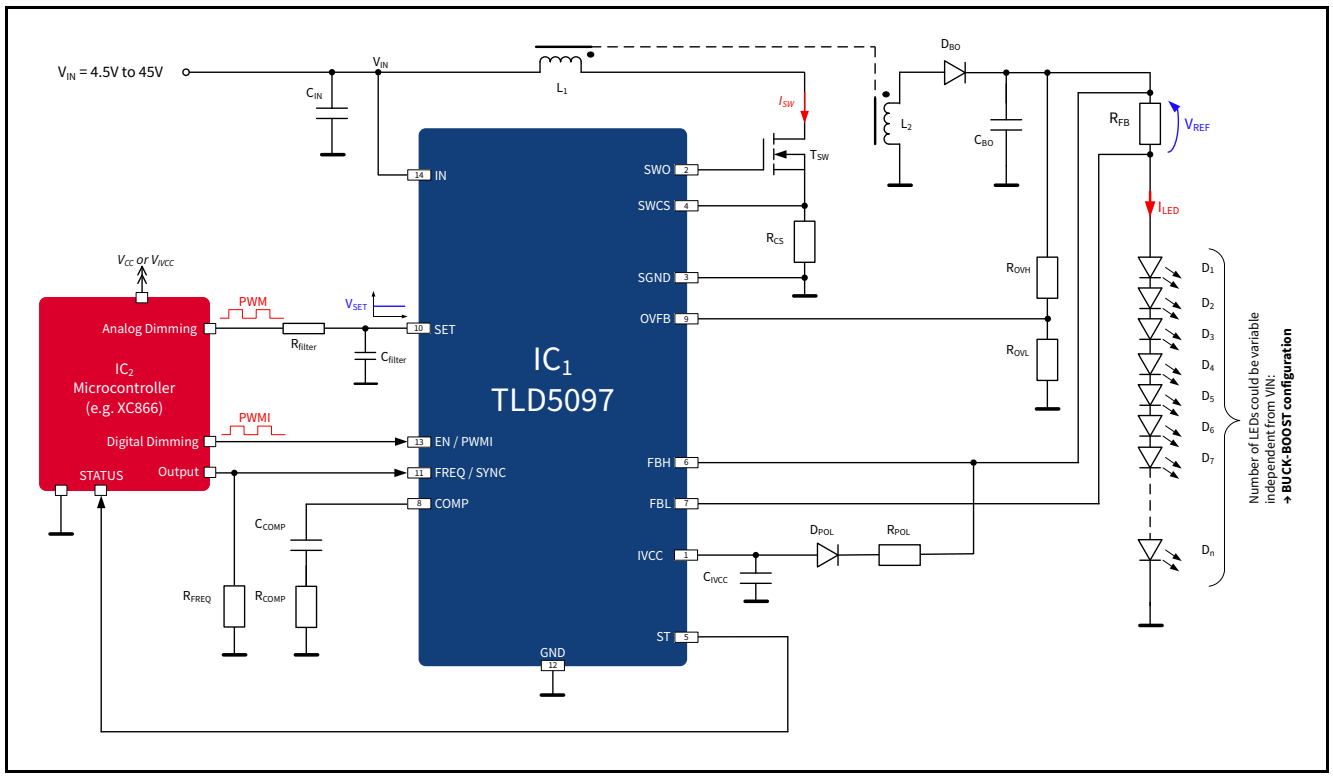

Figure 23 Flyback application circuit (Buck - Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	3.3 uF, 50V (100V)	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	1 µH / 9 uH	EPCOS	Transformer EHP 16	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
D_{POL}	80 V Diode	Infineon	BAS1603W	Diode	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{OVH}	56.2 kΩ, 1%	Panasonic	ERJ3EKF5622V	Resistor	1
R_{OVL}	1.24 kΩ, 1%	Panasonic	ERJ3EKF1241V	Resistor	1
R_{CS}	5 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 24 Bill of Materials for Flyback application circuit

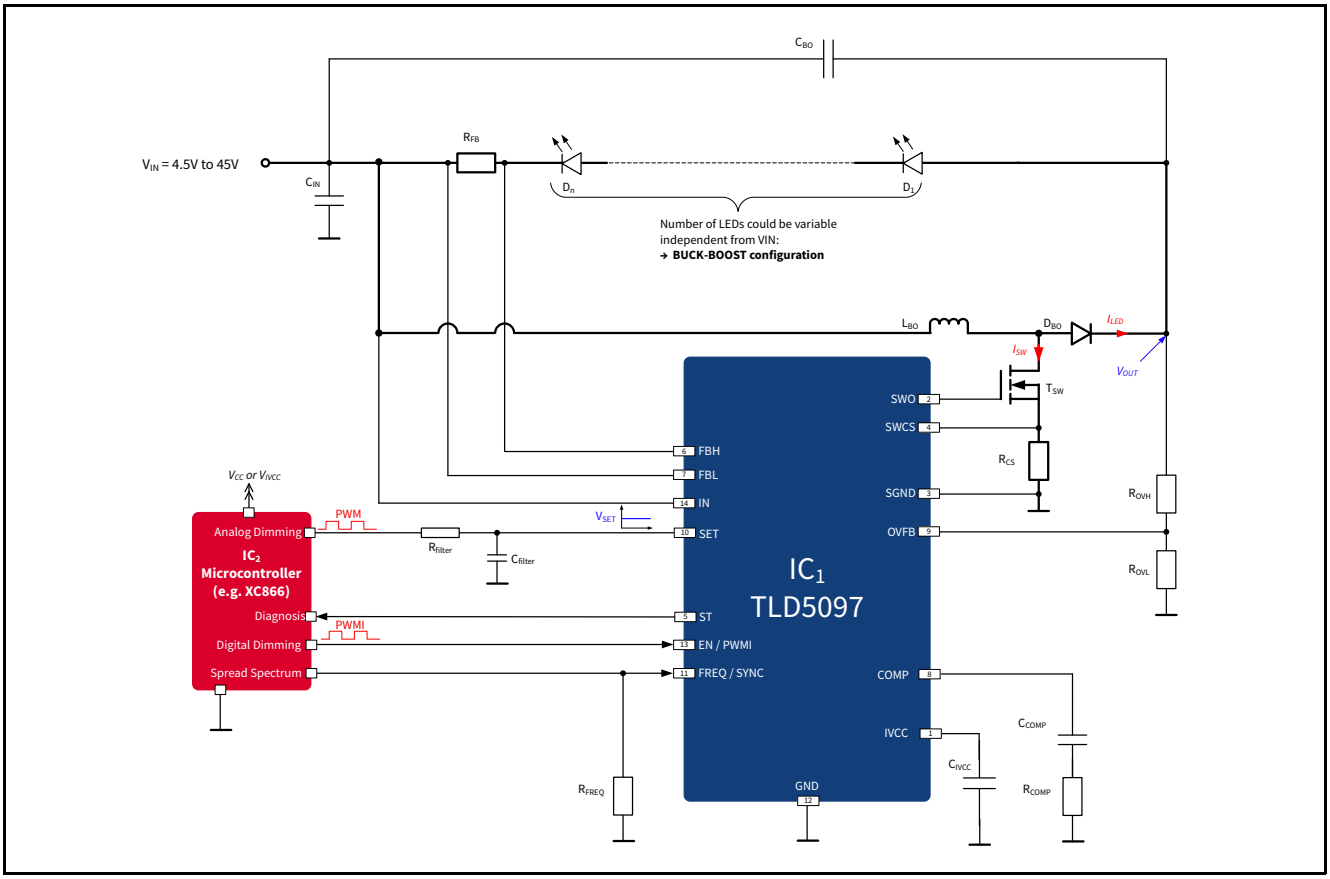

Figure 25 Boost to Battery application circuit - B2B (Buck - Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	3.3 uF, 50V (100V)	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	1 µH / 9 uH	EPCOS	Transformer EHP 16	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
D_{POL}	80 V Diode	Infineon	BAS1603W	Diode	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{OVH}	56.2 kΩ, 1%	Panasonic	ERJ3EKF5622V	Resistor	1
R_{OVL}	1.24 kΩ, 1%	Panasonic	ERJ3EKF1241V	Resistor	1
R_{CS}	5 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 26 Bill of Materials for B2B application circuit

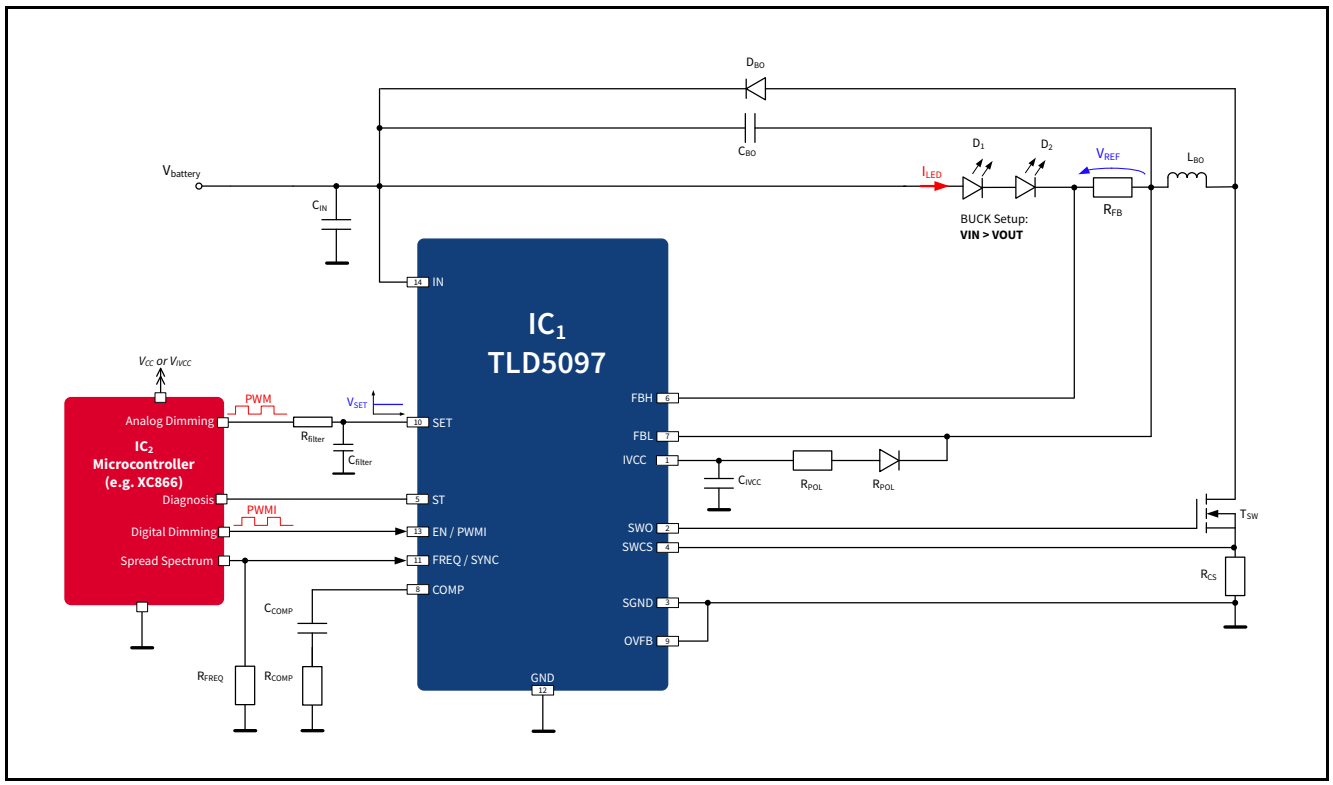

Figure 27 Buck application circuit

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-2}	White	Osram	LE UW Q9WP	LED	2
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
D_{POL}	80V Diode	Infineon	BAS1603W	Diode	1
C_{BO}	4.7 uF, 50V	EPCOS	X7R	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1	22 µH	Coilcraft	MSS1278T	Inductor	1
R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{CS}	50 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 28 Bill of Materials for Buck application circuit

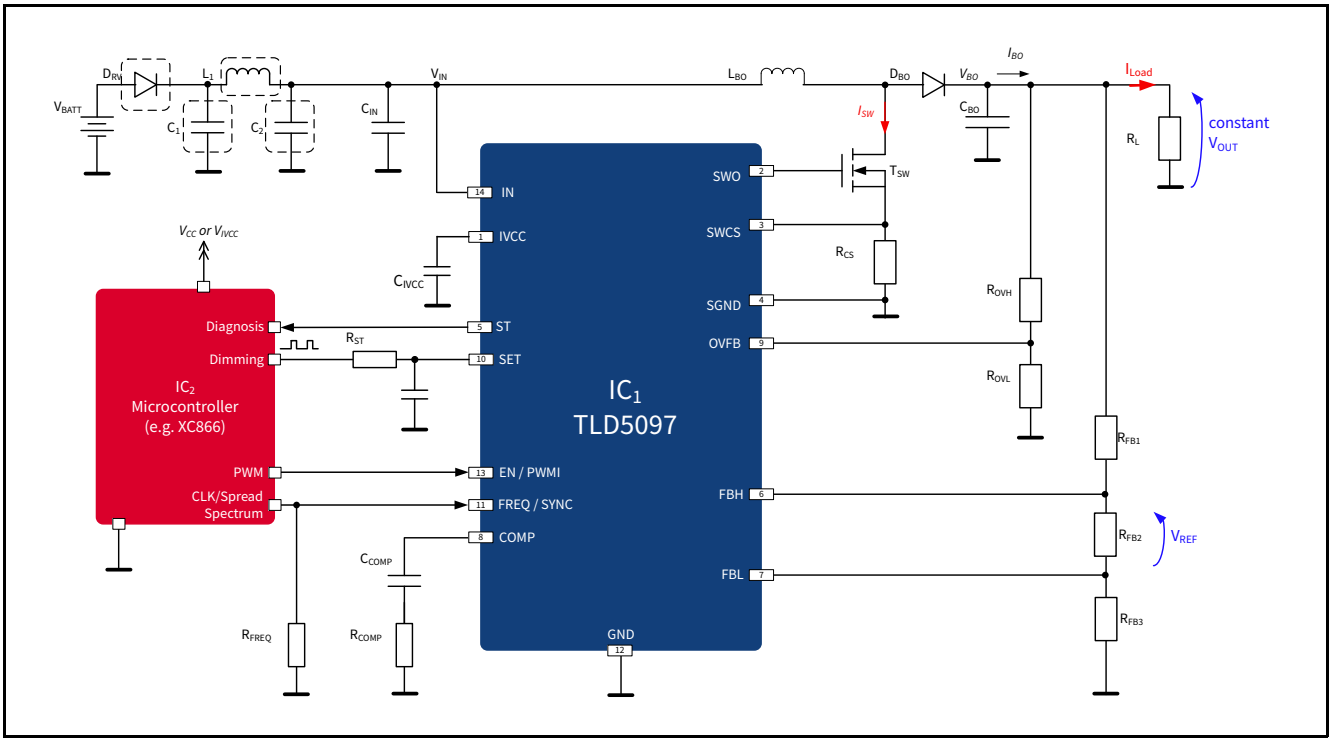

Figure 29 Boost voltage application circuit

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	100 uF, 80V	Panasonic	EEVFK1K101Q	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	10 nF, 16V	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF, 6.3V	Panasonic	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML_	Inductor	1
R_{COMP}	10 kohms, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB1},R_{FB3}	51 kohms, 1%	Panasonic	ERJ3EKF5102V	Resistor	1
R_{FB2}	1 kohms, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{FREQ}	20 kohms, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kohms, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kohms, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mohms, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	N-ch, OptiMOS-T2 100V	Infineon	IPG20N10S4L-22	Transistor	1

Figure 30 Bill of Materials for Boost voltage application circuit

Note: The application drawings and corresponding bill of materials are simplified examples. Optimization of the external components must be done accordingly to specific application requirements.

11.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**
- Application Note: TLD509x DC-DC Multitopology Controller IC “Dimensioning and Stability Guideline - Theory and Practice”

12 Package outlines

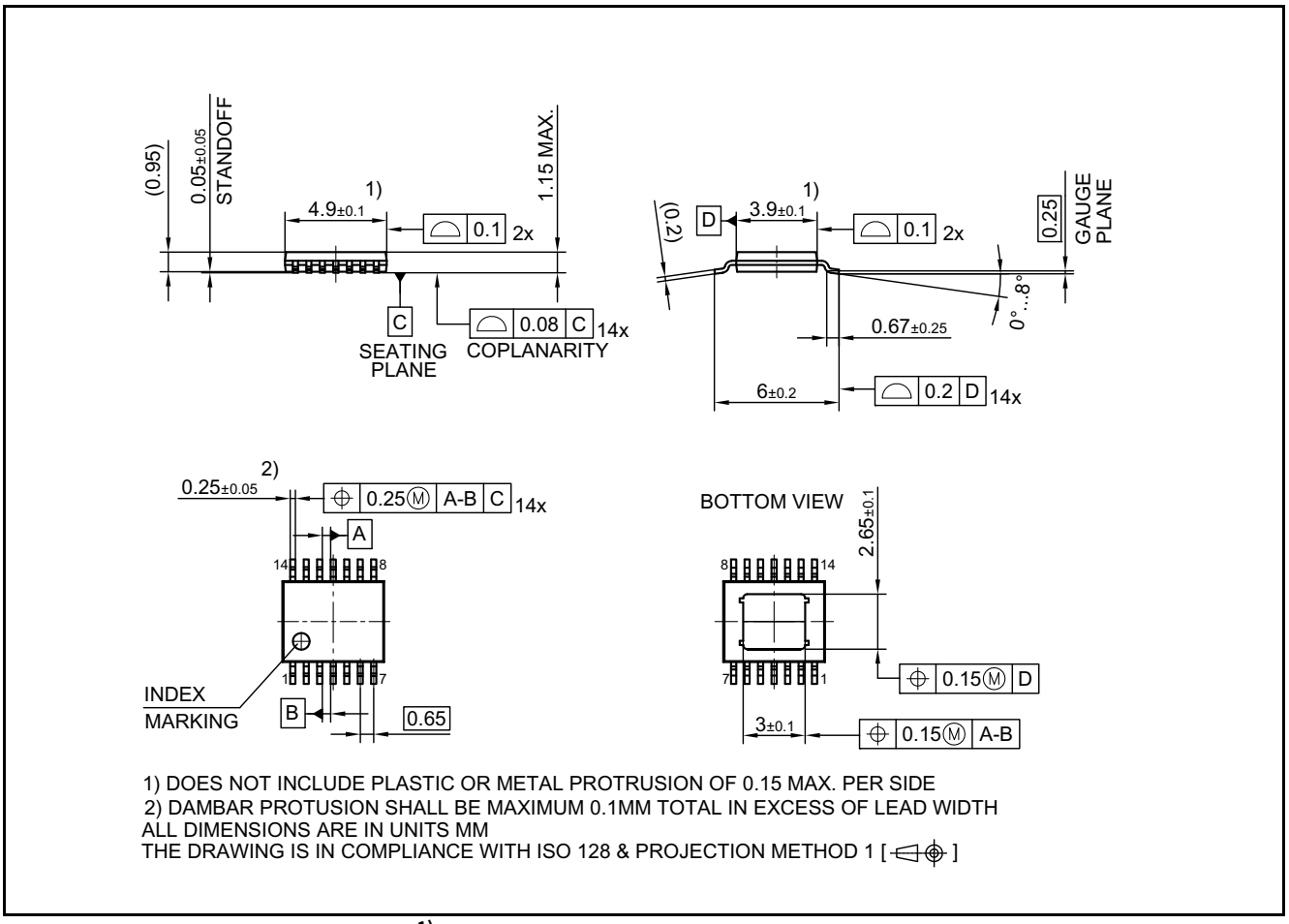

Figure 31 Outline PG-TSDSO-14[1)]

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

13 Revision history

Revision	Date	Changes
1.00	2018-12-13	Initial datasheet

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